

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
16 August 2007 (16.08.2007)

PCT

(10) International Publication Number
WO 2007/092014 A2

(51) International Patent Classification: **Not classified**

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(21) International Application Number:
PCT/US2006/004669

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(22) International Filing Date: 9 February 2006 (09.02.2006)

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(25) Filing Language: English

(26) Publication Language: English

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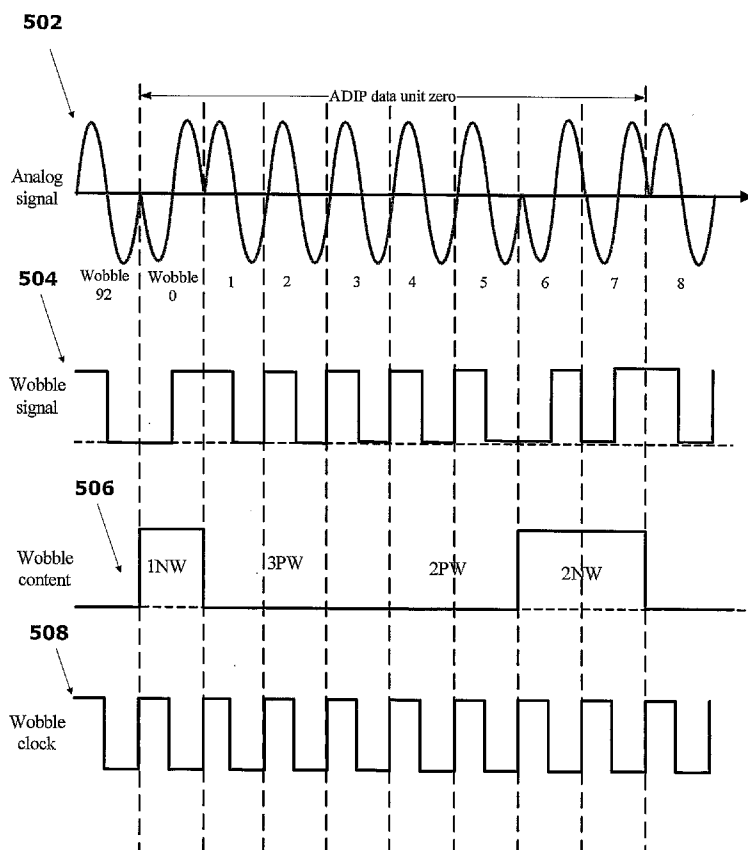
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(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,

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(54) Title: SYSTEM AND METHOD FOR IDENTIFYING ADIP INFORMATION



(57) Abstract: Methods, apparatus, and systems are provided for decoding Address in Pre-groove (ADIP) information encoded on an optical disk. One method includes receiving a wobble signal and a wobble clock, evaluating consecutive bits of the wobble signal using the wobble clock, and triggering an identification of ADIP information in the wobble signal based on the evaluation.

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FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT,
RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA,
GN, GQ, GW, ML, MR, NE, SN, TD, TG).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Published:

- *without international search report and to be republished upon receipt of that report*

System and Method For Identifying ADIP Information

TECHNICAL FIELD

[0001] The present invention relates to a system and method for processing of identifying ADIP information.

BACKGROUND

[0002] Over the past few years there has been a growing demand for storage media having increased storage capacity. Storage media have rapidly increased in storage capacity due to demand for storing a tremendous amount of information. Of all the various kinds of storage media, optical discs are the most promising due to its low-cost, small-size, low-error-rate, long-storage-time, and high-density storage capacity.

[0003] Optical disc drives are used to read information stored on an optical disc. Examples of optical disc drives include compact disc drives (CD-ROM drives) and digital versatile disc drives (DVD-ROM drives). Some optical disc drives have the additional capability of being able to write and record data onto an optical disc, i.e., CD-R/RW, DVD+R/RW and DVD-R/RW disc drives. Optical disc drives can be used in music and video playback, and implemented in recording devices and other electronic devices.

[0004] Conventional optical disks include a pre-groove or track that can store data, which is provided in advance of the recording regions of an optical disc. A wobble is typically provided to this track in order to record various additional information as a wobble signal. The pre-groove information includes address information (called Address In Pre-groove "ADIP") indicating a track position on the optical disc. The address information is necessary for accurately controlling the position of an optical pickup when recording or reproducing is performed. By using this structure, an address can be read from the wobbling information, and the data can be recorded accurately at a specific recording region of the optical disc.

[0005] The optical disc drive has to identify the correct ADIP information before the writing process can be initiated. If the ADIP information cannot be accurately detected and identified, a recording error can occur. Specifically, there exists specific spots on the optical disc where writing can both start and stop. If writing starts too early it can destroy the previously recorded data. Similarly, if writing starts too late, the recorded data can extend too far and possibly destroy subsequent data. In addition

to the need for accuracy for the start of a writing session, it is important to keep the writing tightly controlled to ensure the length over which the current recording occurs stops at the correct and intended location.

SUMMARY

[0006] In one aspect, a method is provided for decoding Address in Pre-groove (ADIP) information encoded on an optical disk. The method includes receiving a wobble signal and a wobble clock, evaluating consecutive bits of the wobble signal using the wobble clock, and triggering an identification of ADIP information in the wobble signal based on the evaluation.

[0007] Aspects of the method can include one or more of the following features. The step of receiving can further include deriving a wobble clock from a received wobble signal. The wobble clock can be substantially double a frequency of the wobble signal. The step of receiving can further include determining the wobble signal from a received analog signal. Evaluating consecutive bits can include evaluating two bits to detect a predetermined pattern. The predetermined pattern can be 00 or 11. The method can further include storing ADIP content information in a reduced size buffer. Triggering can include triggering a sampling of the content stored in the reduced size buffer. The method can further include comparing the sampled content with a predetermined pattern to identify ADIP information. The step of evaluating can include detecting a predetermined pattern in the consecutive bits. The method can further include determining if the predetermined pattern is detected, and if so, the triggering step can further include triggering a signal to guide sampling of the ADIP information.

[0008] In another aspect, a method of decoding Address in Pre-groove (ADIP) information encoded on an optical disk is provided. The method includes generating logic data, a non-phase modulated clock and logic content associated with the logic data; detecting whether a first data pattern exists in the logic data; and if the first data pattern is detected 1) adjusting a sample step of a step adjust signal, 2) enabling a guide signal in accordance with the adjusted sample step, 3) sampling the logic content, 4) comparing the sampled logic content with a second data pattern, and 5) identifying ADIP information based on the comparison.

[0009] Aspects of the invention can include one or more of the following features. The method can include enabling the guide signal periodically, and changing

transition states of the guide signal every cycle when the guide signal is disabled. The method can further include adjusting a step of the guide signal using the step adjust signal. The first data pattern can include a bit stream of "00" or "11". The logic content can be sampled in a shift register. The second data pattern can include one of a group consisting of an ADIP sync unit having a bit stream of "11110000", an ADIP data unit having a logic level of "0" defined as having a bit stream of "10000011" and an ADIP data unit having a logic level of "1" defined as having a bit stream of "10001100". Detecting whether a first data pattern exists in the logic data can include sampling the logic data and comparing the sampled logic data with the first data to generate the step adjust signal. The clock can be generated based on a phase-modulated input, and can include a period of 16 channel bits. The logic content can be sampled in a shift register using the clock.

[0010] In another aspect an optical disc apparatus capable of decoding ADIP information from an optical disc is provide. The apparatus includes a wobble signal generator to generate a wobble signal, a wobble clock and wobble content associated with the wobble signal; a pattern detector coupled to the wobble signal generator and configured to detect a first data pattern in the wobble signal and to generate a step adjust signal; a guide signal generator coupled to the pattern detector and configured to initiate a guide signal in response to the received step adjust signal; and a wobble data sample logic circuit coupled to the wobble signal generator and the guide signal generator and configured to sample the wobble content based on the guide signal and the wobble clock.

[0011] Aspects of the invention can include one or more of the following features. The pattern detector can include a n-bit shift register configured to detect the first data pattern in the wobble signal. The wobble data sample logic circuit can include an m-bit shift register configured to sample the wobble content and compare the sampled wobble content with a second data pattern. The first data pattern can be a data pattern of "00" or "11". The second data pattern can include one of a group consisting of an ADIP sync unit having a bit stream of "11110000", an ADIP data unit having a logic level of "0" defined as having a bit stream of "10000011" and an ADIP data unit having a logic level of "1" defined as having a bit stream of "10001100".

[0012] Systems and methods are proposed for generating a step adjust signal periodically. Based on the periodicity of the step adjust signal, the error tolerance of the ADIP detection circuit can be increased and the error will not be introduced to the next ADIP word. When the ADIP analog waveform has some deviation from the ideal waveform, the detected ADIP word can be an error. A step adjust signal is proposed that can re-initialize the ADIP detection to the right step and produce the right guide signal (for use in determining when to sample the ADIP content in a content register). Based on the right guide signal, wobble data sample logic can accurately determine the correct ADIP word.

[0013] In one implementation, a shift register in the wobble data sample logic is reduced from a conventional size (e.g., 16 bits) to a reduced size (e.g., 8 bits). Systems that do not produce a guide signal as described herein require a large register to find the ADIP information. Using a guide signal, the proposed wobble data sample logic can detect the ADIP information in a reduced size buffer (e.g., an 8-bit shift register). Furthermore, the error probability of a larger shift register (e.g., 16-bit shift register) is higher than the reduced size shift register (e.g., 8-bit shift register). Accordingly, the overall error tolerance of the system is increased by using the reduced sized shift register.

[0014] Using the described guide signal and a double frequency clock, the wobble data sample logic can advantageously detect a unique and precise ADIP Sync, ADIP zero and ADIP one data pattern and determine a unique and precise writing start point.

[0015] The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, aspects, and advantages of the invention will become apparent from the description, the drawings, and the claims.

BRIEF DESCRIPTION OF DRAWINGS

[0016] Fig. 1 illustrates an exemplary optical disc drive system.

[0017] Fig. 2 illustrates an exemplary ADIP sample circuit.

[0018] Figs. 3-4 illustrate are timing diagrams of waveforms associated with an ADIP sync unit.

[0019] Figs. 5-6 illustrate are timing diagrams of waveforms associated with an ADIP data unit having a logic level of "0".

[0020] Figs. 7-8 illustrate timing diagrams of waveforms associated with an ADIP data unit having a logic level of "1".

[0021] Fig. 9 is a flow diagram of an exemplary process for identifying ADIP information.

[0022] Fig. 10 illustrates an exemplary data structure for information stored in an ADIP.

DETAILED DESCRIPTION

[0023] Fig. 1 shows an exemplary optical disc drive system 100. The optical disc drive system 100 generally includes an optical disc 102 having a reflecting surface and an optical disc drive 104. The optical disc drive 104 includes, without limitation, an optical pickup 105 (OPU), a wobble signal generator 106 and an ADIP sample circuit 108. The optical disc drive 104 can be utilized to read or write data from or to the optical disc 102. The optical pickup 105 can emit a laser beam onto the optical disc 102 to record data therein and to reproduce data therefrom.

[0024] As discussed in the Background, the ADIP information is necessary for accurately controlling the position of an optical pickup when recording or reproducing is performed so that data can be recorded accurately at a specific recording region of the optical disc 102. In some implementations, from the ADIP information, the optical disc drive system 100 can detect the media type of the optical disc 102 (e.g., single layer or dual layer), and the recordable layer(s) embedded therein on which data can be recorded. Once the media type and the recordable layer(s) are determined, the optical pickup 105 can move its range of focus up, down and across the optical disc 102 to access any data embedded on the recordable layers. The optical pickup 105 can focus on a selected recordable layer to determine, for example, whether the optical disc 102 is completely blank, partially recorded in multi-session format, or finalized (completed), or whether a recording session should be initiated on the selected recordable layer.

[0025] In some implementations, the optical disc 102 can be a magnetic-optical disc. Generally magnetic-optical discs include a recordable layer having lands and grooves formed thereon. The grooves can be spirally or concentrically formed on the optical disc in a circumferential direction, and contain a data track to record data, and a wobble track to record related addressing information. Data can be recorded in these grooves via the data track, and address information of each groove can be

retained at the boundaries of the wobble track (or wobbled edges on both sides of the groove) (i.e., each groove is wobbled corresponding to the address information).

[0026] Generally, wobble tracks have a continuous sinusoidal deviation from their average centerline, and the surface of the wobble tracks protrude beyond the reflecting surface of the optical disc 102. Data tracks are positioned inside the grooves formed by the raised wobble tracks. Consequently, data is recorded in the data tracks and the address of the recorded data is read from the wobble tracks to assist the process of reading or writing data by the optical pickup 105. Thereby, the optical pickup 105 is able to extract the tracking information carried by the wobble tracks of the optical disc 102 to generate a wobble signal. The address information is then extracted from the wobble signal, for example, to determine where data has been recorded on the optical disc 102 or to ensure that the optical pickup 105 focuses at the appropriate spot on the optical disc 102.

[0027] For example, in a data recording or reproduction mode, when an access is performed on the optical disc 102 by the optical disc drive 104, the optical pickup 105 emits an incident laser beam onto the grooves of the optical disc 102, and in response, receives a reflected laser beam. Through the received laser beam, the shape of the wobbled edges is detected by the optical disc drive 104 and the address information of the wobble edges can be read out.

[0028] The data to be recorded onto the optical disc 102 can be aligned with the ADIP information modulated in the wobble signal. Fig. 10 shows an exemplary structure of the ADIP information. Referring to Fig. 10, each wobble signal generally includes 93 wobble cycles (or 2 Sync Frames). Of each 93 wobble cycles, 8 wobble cycles are phase-modulated with ADIP information to record an ADIP sync unit or an ADIP data unit, and the remaining 85 wobbles are monotone wobble cycles. Depending upon the frequency of a wobble clock being used, each wobble cycle can correspond to 8 to 32 channel bits. The address information read from the optical disc 102 can be incorporated with the wobble signal by using a phase modulation technique (i.e., the address information can be recorded according to the phase shift of a carrier).

[0029] Referring back to Fig. 1, the intensity of the reflected laser beam can be detected by the optical pickup 105 and converted into an electrical signal proportional to the intensity of the reflected laser beam by a wobble signal generator 106. In some

implementations, if the intensity is too weak to be detected, the converted electrical signal can be filtered (e.g., using a band-pass, low-pass or high-pass filter) so that the noise component of the signal is removed/reduced. The filtered signal can then be amplified to strengthen its intensity prior to being forwarded to the wobble signal generator 106. On the basis of the electrical signal, the wobble signal generator 106 can correspondingly generate a wobble signal used for timing and addressing information, and to keep a laser spot irradiated by the optical pickup 105 properly positioned, for example, at the centerline of a groove.

[0030] As shown in Fig. 1, in one implementation, the wobble signal generator 106 includes various components including a voltage control oscillator (VCO) 124, and a divider 126. A phase detector 116 (e.g., Hogge-type phase detector) compares, for example, the phases of both the input from the optical pickup 105 and the input from an ADIP demodulator 128, and outputs a phase signal. A charge-pump 120 and filter 118 (e.g., resistor-capacitor type) compensates the phase of the phase signal output by the phase detector 116, and outputs a compensated signal to the VCO 124. In response, the VCO 124 generates a clock signal having a phase corresponding to that of the compensated signal, and outputs the clock to the divider 126. This clock can be a non-phase-modulated clock having a high frequency, where the high-frequency clock is then processed by the divider 126 to generate a clock signal. In one implementation, the clock signal is produced at a frequency that is greater than the frequency of the wobble signal so as to allow for the reading of the wobble data contained therein within the time available but also to allow for various attending signal processing to occur in the system (e.g., the production of the step and guide signals). In at least one implementation, a 2* (i.e., double frequency) wobble clock is generated and will be referred to below merely as the wobble clock or 2* wobble clock.

[0031] The divider 126 divides the clock signal from the VCO 124 by a predetermined value (e.g., / 16), and outputs the divided result VCO_DIV to the phase detector 116, frequency detector 112 and the ADIP demodulator 128. The divided result VCO_DIV can be fed back to the phase detector 116 to enhance the phase detection process (e.g., because of the potentially limited frequency acquisition range of the phase detector). Other auxiliary frequency acquisition loops can be provided to enhance the frequency acquisition range.

[0032] The wobble signal generator 106 further includes a differentiator 110, a frequency detector 112 (e.g., stroboscopic-type) and a charge pump 114 to sweep away differentiated wobble edges of the input received from the optical pickup 105. As a result of the foregoing processes, the divided result VCO_DIV is frequency-equalized and can be demodulated to generate a wobble signal.

[0033] The generated wobble signal, which includes the data and addressing information of the optical disc 102, can be used to derive the current position of the laser spot irradiated on the optical disc 102. During reading, erasing, or writing, as will be discussed in greater details later, the ADIP sample circuit 108 compares the data pattern of the wobble data with a predetermined data pattern to identify the ADIP information modulated with the wobble signal.

[0034] As discussed above, the optical disc system 104 records data onto or reproduces data from the optical disc 102 using the optical pickup 105, and performs other operations including: irradiating a laser beam onto the optical disc 102; receiving the reflection of the laser beam to allow read out of the data and address information recorded on the optical disc 102; outputting the data thus read to the optical disc system 104; subsequently generating, from the received reflection of the laser beam, a wobble signal which includes the ADIP information; and, outputting the wobble signal to an ADIP sample circuit 108 for comparison with a predetermined data pattern.

[0035] In some implementations, if the wobble signal matches the predetermined data pattern, the ADIP sample circuit 108 outputs the predetermined data pattern to the optical pickup 105, and in response to the predetermined data pattern supplied from the ADIP sample circuit 108, generates a control signal to re-position the optical pickup 105 on the "correct" track, and to record or reproduce data to/from the optical disc 102.

[0036] In some implementations, the predetermined data pattern can be used to adjust the focus and the tracking of the laser beam irradiated on the optical disc 102. In other implementations, the optical disc system 104 controls a spindle motor, and the predetermined data pattern contains rotation information such that the optical disc 102 can rotate at a predetermined velocity in accordance with rotation information obtained from the predetermined data pattern.

[0037] The wobble signal generator 106 produces the wobble signal and the wobble content. The wobble content is the logic content of the wobble information contained in the wobble signal and is generated on the corresponding wobble signal. NW is the negative wobble, which starts moving towards the outside of the disc. PW is the positive wobble, which starts moving towards the inside of the disc. Based on the NW and PW definition and the corresponding wobble signal, the wobble signal generator 106 produces wobble content.

[0038] By performing the foregoing processes using the electrical signals received from the optical pickup 105, a wobble signal, wobble content and a wobble clock (e.g., 2 * wobble clock) can be generated. The wobble signal, wobble content and the wobble clock (e.g., 2* wobble clock) are then forwarded to the ADIP sample circuit 108, where the ADIP sample circuit 108 samples the wobble signal to determine whether a bit stream representative of an ADIP sync, ADIP one or ADIP zero is detected. Fig. 2 illustrates an exemplary ADIP sample circuit for sampling a wobble signal.

[0039] Referring to Fig. 2, the ADIP sample circuit 108 receives the wobble signal and the wobble clock (e.g., the 2 * wobble clock). A pattern detector 130 samples the wobble signal using, for example, an n-bit shift register 131 (e.g., 2-bit) to determine if the wobble signal contains a predetermined data pattern. While reference is made to a shift register, other sampling means can be used as is known in the art. In some implementations, the predetermined data pattern received includes a bit stream of "00" or "11". In one or more implementation, these particular predetermined data patterns are used to trigger the generation of a step signal as will be discussed in greater detail below. The wobble clock (e.g., 2 * wobble clock) can govern the periodicity in which the wobble signal is sampled at the n-bit shift register 131. The frequency of the wobble clock (e.g., 2 * wobble clock) may vary depending on a particular design application, and can be flexibly controlled. Because of the inherent delay caused by the analog components in the wobble signal generator 106, in some implementations, the negative edge of the wobble clock (e.g., 2 * wobble clock) is used to sample the wobble signal at the n-bit shift register 131.

[0040] If the predetermined data pattern (e.g., "00" or "11") is detected in the wobble signal, a step adjust signal is established and provided to a guide signal generator 132. The step adjust signal can be used to adjust the periods (steps) or

transition states of a guide signal, which is utilized for sampling the wobble content in, for example, an m-bit shift register (e.g., 8-bit), as will be discussed in greater detail below. In response to the step adjust signal, the guide signal generator 132 generates a guide signal having a waveform consistent with that defined by the step adjust signal.

[0041] When the guide signal is enabled, wobble data sample logic 134 samples the wobble content received from the wobble signal generator 106. In one implementation, the sampled data can be stored in an m-bit shift register (e.g., an 8-bit shift register 136). Other sampling and storage means can be used. The m bit (e.g., 8-bit) shift register 136 then compares the wobble content with a predetermined data pattern. Such process is repeated until a match is found, in which the predetermined data pattern is output to, for example, a separate logic circuit to retrieve other additional information associated with the optical disc 102. In some implementations, the predetermined data pattern that is used for matching in the wobble data sample logic 134 includes a bit stream of "11110000" representative of an ADIP sync unit, a bit stream of "10000011" representative of an ADIP data unit having a logic level of "0", or a bit stream of "10001100" representative of an ADIP data unit having a logic level of "1". Fig. 3 illustrates signal traces of ideal waveforms associated with an ADIP sync unit as used in one or more implementations. An analog signal 302 as shown includes 8 wobble cycles; namely, wobble 0, wobble 1, wobble 2, wobble 3, wobble 4, wobble 5, wobble 6 and wobble 7. The wobble cycles shown are utilized to record ADIP information using a phase modulation technique. Other data storage techniques are possible.

[0042] As is shown in Fig. 3, a phase shift of 180° occurs at the beginning of the first phase-modulated cycle wobble 0 of the analog signal 302. In addition, a phase shift of 180° also occurs between wobble 3 and wobble 4 of the analog signal 302. After demodulating the analog signal 302, a wobble signal 304 is generated. The wobble signal 304 includes a successive "0" between wobble 0 and wobble 1, and successive "1" between wobble 3 and wobble 4. Using the wobble signal 304, a non-phase-modulated signal wobble clock 306 can be derived for use in the system for sampling data.

[0043] The wobble signal generator 106 generates a wobble clock 508 that is non-phase-modulated. Thus, the ADIP information recorded in the wobble signal 504 can

be extracted with the aid of the wobble clock 308. Based on each cycle of the wobble clock 308, the cycle of the wobble signal 304 that is in phase with the cycle of the wobble clock 308 corresponds to a bit of 1, and the cycle of the wobble signal 304 which is in opposite phase with the cycle of the wobble clock 308 corresponds to a bit of 0.

[0044] The wobble signal 304 is sampled to develop the corresponding wobble content 306 which can be identified as an ADIP sync unit. Specifically in the example shown in Figs. 3 and 4, using a wobble clock 308, the ADIP sync unit data pattern is detected after the 8th wobble cycle (e.g., a bit stream of “11110000” is detected). Wobbles 0–3 are negative wobbles (NW) indicating that the optical disc rotates toward the center of the disc, and wobbles 4-7 are positive wobbles (PW) indicating that the optical disc rotates away from the center of the disc.

[0045] More specifically one implementation for timing and relative signal relationships is shown in the timing diagram of Fig. 4. Wobble signal generator 106 generates the wobble clock (e.g., 2*wobble clock), wobble signal and wobble content. Sample logic (e.g., in the pattern detector 130) samples the wobble signal in the n-bit (e.g., 2 bit) shift register under 2*wobble clock falling edge. After falling edge 0, the 2 bit shift register includes the pattern “10.” Table 1 shows the 2 bit shift register’s value after every falling edge. In one implementation, the 2 bit shift register has a setup time. Sample logic samples data in the register at falling edge, and the register will be changed after falling edge.

Table 1

After falling edge number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
The value of the 2 bit shift register	10	00	01	10	01	10	01	10	01	11	10	01	10	01	10	01	10	01	10

[0046] After falling edge 1, the value of the 2 bit shift register is “00” and the step adjust signal will be initialed. As will be discussed below, similarly the guide signal will be enabled after falling edge 1. After falling edge 2, the value of the 2 bit shift register is “01” and the step adjust signal will be disabled. Similarly, after falling

edge 9, the value of the 2 bit shift register is “11” and the step adjust signal will be initialed (e.g., enabled after falling edge 9). After falling edge 10, the value of the 2 bit shift register is “10” and the step adjust signal will be disabled producing the step adjust signal shown in Fig. 4.

[0047] Based on the step adjust signal, the guide signal will be enabled after falling edge 1 and will be disabled after falling edge 2 producing the guide signal waveform as shown in Fig. 4. Under the 2*wobble clock falling edge, if the guide signal is enabled, the sample logic will sample the wobble content in the m-bit (e.g., 8 bit shift register). Table 2 shows the status of the guide signal at every falling edge.

Table 2

At falling edge number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
The status of the guide signal	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

[0048] Wobble content is generated by wobble signal generator 106 as discussed above. The sample logic (e.g., wobble data sample logic 134) under a rising edge or falling edge doesn't have any effect to this signal's timing. Based on the guide signal, the sample logic will sample the wobble content in the 8 bit shift register under the 2*wobble clock's falling edge. At falling edge 0, the guide signal is enabled. The sample logic will sample the wobble content in the 8 bit shift register. So, after falling edge 0, the value is 00000000. At falling edge 1, the guide signal is disabled and the shift register will keep the value. At falling edge 2, the guide signal is enabled. The sample logic will sample the wobble content in the 8 bit shift register. So, after falling edge 2, the value is 00000001. Table 3 shows the value of the 8 bit shift register after every falling edge.

Table 3

After falling edge number	The value of the 8 bit shift register
0	00000000
1	00000000
2	00000001
3	00000001
4	00000011
5	00000011
6	00000111
7	00000111
8	00001111
9	00001111
10	00011110
11	00011110
12	00111100
13	00111100
14	01111000
15	01111000
16	11110000
17	11110000
18	11100000

[0049] In one implementation, the ADIP Sync Pattern is 11110000. After falling edge 16 and 17, the 8 bit shift register is 11110000. After falling edge 18, the 8 bit shift register is 11100000. So, the pattern is matched after falling edge 16 and 17. After falling edge 18, the pattern isn't matched. But the guide signal is disabled after falling edge 16 and is enabled after falling edge 17. So, the ADIP Sync signal will be enabled after falling edge 17. After falling edge 18, the ADIP Sync will be disabled. In this example, the sample logic samples data under falling edge. If the sample logic were to sample under rising edges, the waveforms of the 2 bit shift register, guide signal initial, guide signal, wobble data (8 bit shift register) and ADIP Sync will vary accordingly. For recording data in the same point under falling edge or rising edge, the recording start point will have some small adjusting. The adjusting is completed by other logic not shown.

[0050] Fig. 5 illustrates signal traces of ideal waveforms associated with an ADIP data unit having a logic level of "0" as used in one or more implementations. Similar to that shown in Fig. 3, the analog signal 502 includes 8 wobble cycles; namely, wobble 0, wobble 1, wobble 2, wobble 3, wobble 4, wobble 5, wobble 6 and wobble 7. The eight wobble cycles can be utilized to record ADIP information using, for example, phase modulation.

[0051] As is shown in Fig. 5, a phase shift of 180° occurs at the beginning of the first phase-modulated cycle wobble 0 of the analog signal 502. In addition, a phase shift of 180° also occurs between wobble 0 and wobble 1 and wobble 5 and wobble 6 of the analog signal 502. After demodulating the analog signal 502, a wobble signal 504 is generated. The wobble signal 504 includes a successive “0” between wobble 92 and wobble 0 and between wobble 5 and wobble 6, and successive “1” between wobble 0 and wobble 1 and between wobble 7 and wobble 8. Based on the wobble signal 504, a non-phase-modulated signal wobble clock 506 can be developed.

[0052] After a sampling process, the wobble signal 504 is sampled as corresponding to wobble content 506. Particularly, wobbles 0 and 6-7 are negative wobbles (NW) indicating that the optical disc rotates toward the center of the disc, and wobbles 1-5 are positive wobbles (PW) indicating that the optical disc rotates away from the center of the disc. In one implementation shown in relationship to Figs. 5 and 6, this particular pattern can be identified as an ADIP data unit having a logic level of 0. Specifically, using the wobble clock 508, the ADIP sync unit data pattern is detected to contain a bit stream of “10000011”.

[0053] More specifically one implementation for timing and relative signal relationships for the ADIP zero signal is shown in the timing diagram of Fig. 6. Wobble signal generator 106 generates the wobble clock (e.g., 2*wobble clock), wobble signal and wobble content. Sample logic (e.g., in the pattern detector 130) samples the wobble signal in the n-bit (e.g., 2 bit) shift register under 2*wobble clock falling edge. 2. In the implementation shown, sample logic samples the wobble signal in the 2 bit shift register under 2*wobble clock falling edge. Table 4 is the 2 bit shift register’s value after every falling edge for this detection pattern.

Table 4

After falling edge number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
The value of the 2 bit shift register	10	00	01	11	10	01	10	01	10	01	10	01	10	00	01	10	01	11	10

[0054] Based on the value of the 2 bit shift register, the step adjust signal can be produced as shown in Fig. 6. Based on the step adjust signal, the guide signal will be enabled after falling edge 1 and will be disabled after falling edge 2 producing the guide signal waveform as shown in Fig. 6. Under the 2*wobble clock falling edge, if the guide signal is enabled, the sample logic will sample the wobble content in the 8 bit shift register. Table 5 shows the guide signal's status at every falling edge.

Table 5

At falling edge number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
The status of the guide signal	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

[0055] Wobble content is generated by wobble signal generator 106. The sample logic (e.g., wobble data sample logic 134) under rising edge or falling edge doesn't have any effect to this signal's timing. Based on the guide signal, the sample logic will sample the wobble content in the 8 bit shift register under the 2*wobble clock's falling edge. At falling edge 0, the guide signal is enabled. The sample logic will sample the wobble content in the 8 bit shift register. So, after falling edge 0, the value is 00000000. At falling edge 1, the guide signal is disabled and the shift register will keep the value. At falling edge 2, the guide signal is enabled. The sample logic will sample the wobble content in the 8 bit shift register. So, after falling edge 2, the value is 00000001. Table 6 shows the contents of the 8 bit shift register after every falling edge.

Table 6

After falling edge number	The value of the 8 bit shift register
0	00000000
1	00000000
2	00000001
3	00000001
4	00000010
5	00000010
6	00000100
7	00000100
8	00001000
9	00001000
10	00010000
11	00010000
12	00100000
13	00100000
14	01000001
15	01000001
16	10000011
17	10000011
18	00000110

[0056] In one implementation, the ADIP Zero Pattern is 10000011. After falling edge 16 and 17, the 8 bit shift register value is 10000011. After falling edge 18, the 8 bit shift register value is 00000110. So, the pattern is matched after falling edge 16 and 17. After falling edge 18, the pattern isn't matched. However, the guide signal is disabled after falling edge 16 and is enabled after falling edge 17. Accordingly, the ADIP Zero will be enabled after falling edge 17. After falling edge 18, the ADIP Zero will be disabled. As with the previous example, the sample logic samples data under a falling edge. If sampled under a rising edge, the waveforms of the 2 bit shift register, guide signal initial, guide signal, wobble data (8 bit shift register) and ADIP Zero will vary accordingly.

[0057] Fig. 7 illustrates signal traces of ideal waveforms of an ADIP data unit having a logic level of "1" as used in one or more implementations. The analog signal 702 includes 8 wobble cycles; namely, wobble 0, wobble 1, wobble 2, wobble 3, wobble 4, wobble 5, wobble 6 and wobble 7, which are utilized to record ADIP information using, for example, phase modulation.

[0058] As is shown in Fig. 7, a phase shift of 180° occurs at the beginning of the first phase-modulated cycle wobble 0 of the analog signal 702. In addition, a phase shift of 180° also occurs between wobble 0 and wobble 1, and between wobble 3 and the wobble cycle 4 of the analog signal 702. After demodulating the analog signal

702, a wobble signal 704 is generated. The wobble signal 704 includes a successive “0” between wobble 92 and wobble 0 and between wobble 3 and wobble 4, and successive “1” between wobble 0 and wobble 1 and between wobble 5 and wobble 6. Based on the wobble signal 704, a non-phase-modulated signal wobble clock 708 can be developed.

[0059] As is shown in Figs. 7 and 8, using the wobble clock 708, the ADIP one data pattern is detected as contain a bit stream of “10001100”. Particularly, wobbles 0 and 4-5 are negative wobbles (NW) indicating that the optical disc rotates toward the center of the disc, and wobbles 1-3 and 6-7 are positive wobbles (PW) indicating that the optical disc rotates away from the center of the disc. The analog signal 702 corresponds to an ADIP data unit having a corresponding logic level of 1.

[0060] More specifically one implementation for timing and relative signal relationships for the ADIP one signal is shown in the timing diagram of Fig. 8. Wobble signal generator 106 generates the wobble clock (e.g., 2*wobble clock), wobble signal and wobble content. Sample logic (e.g., in the pattern detector 130) samples the wobble signal in the n-bit (e.g., 2 bit) shift register under 2*wobble clock falling edge. 2. In the implementation shown, sample logic samples the wobble signal in the 2 bit shift register under 2*wobble clock falling edge. Table 7 is the 2 bit shift register’s value after every falling edge for this detection pattern.

Table 7

After falling edge number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
The value of the 2 bit shift register	10	00	01	11	10	01	10	01	10	00	01	10	01	11	10	01	10	01	10

[0061] Based on the value of the 2 bit shift register, the step adjust signal can be produced as shown in Fig. 8. Based on the step adjust signal, the guide signal will be enabled after falling edge 1 and will be disabled after falling edge 2 producing the guide signal waveform as shown in Fig. 8. Under the 2*wobble clock falling edge, if the guide signal is enabled, the sample logic (e.g., wobble data sample logic 134) will sample the wobble content in the m-bit (e.g., 8 bit) shift register. Table 8 shows the guide signal’s status at every falling edge.

Table 8

At falling edge number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
The status of the guide signal	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

[0062] Wobble content is generated by wobble signal generator 106. Based on the guide signal, the sample logic will sample the wobble content in the 8 bit shift register under the 2*wobble clock's falling edge. At falling edge 0, the guide signal is enabled. The sample logic will sample the wobble content in the 8 bit shift register. So, after falling edge 0, the value is 00000000. At falling edge 1, the guide signal is disabled and the shift register will keep the value. At falling edge 2, the guide signal is enabled. The sample logic will sample the wobble content in the 8 bit shift register. So, after falling edge 2, the value is 00000001. Table 9 shows the 8 bit shift register after every falling edge.

Table 9

After falling edge number	The value of the 8 bit shift register
0	00000000
1	00000000
2	00000001
3	00000001
4	00000010
5	00000010
6	00000100
7	00000100
8	00001000
9	00001000
10	00010001
11	00010001
12	00100011
13	00100011
14	01000110
15	01000110
16	10001100
17	10001100
18	00011000

[0063] In one implementation, the ADIP One Pattern is 1001100. After falling edge 16 and 17, the 8 bit shift register is 10001100. After falling edge 18, the 8 bit shift

register is 00000110. So, the pattern is matched after falling edge 16 and 17. After falling edge 18, the pattern isn't matched, but the guide signal is disabled after falling edge 16 and is enabled after falling edge 17. Accordingly, the ADIP One signal will be enabled after falling edge 17. After falling edge 18, the ADIP One signal will be disabled.

[0064] Fig. 9 is a flow diagram of an exemplary process 900 for identifying ADIP information. A wobble signal, a wobble clock and a wobble content associated with the wobble signal are generated (step 902). For example, the wobble signal and the wobble clock can be generated by modulating/demodulating an electrical signal received after scanning data on an optical disc. If the electrical signal is weak, a filtering process and an amplification process can be employed to strengthen the intensity of the electrical signal.

[0065] The received wobble signal and wobble clock are then consistently checked based on a frequency (or period) defined by the wobble clock to determine if the wobble signal contains a predetermined data pattern (step 904). In some implementations, the data pattern can be a "00" or "11" data pattern. In other implementations, other data patterns may be used. The frequency of the wobble clock may vary depending on a particular design application, and can be flexibly controlled.

[0066] If the predetermined data pattern is not found in the wobble signal (the "No" branch of step 906), the process of detecting the predetermined data pattern is repeated until such data pattern is found. Once the predetermined data pattern is found (the "Yes" branch of step 906), the sample step of a step adjust signal is configured (step 908). The step adjust signal is used to enable a guide signal (step 910).

[0067] If the guide signal is not enabled (e.g., logic "0") (the "No" branch of step 912 where no pattern has been detected in step 906 and accordingly no step adjust signal provided in step 908), then step 910 is repeated until the guide signal is enabled in accordance with the sample step. Once the guide signal is enabled (the "Yes" branch of step 912), the wobble content associated with the wobble signal and received at step 902 is sampled using the wobble clock to detect and identify ADIP information contained in the wobble signal (step 914). Each time the wobble content is sampled, the resulting sampled data can be stored in a reduced size buffer (e.g., an 8-bit shift register 136). The stored value is then compared with a predetermined data

pattern (step 916). In some implementations, the predetermined data pattern can be an ADIP sync unit having a bit pattern of “11110000”, an ADIP data unit one having a bit pattern of “10000011” or an ADIP data unit zero having a bit pattern of “10001100”. If a match is not found (“No” branch of step 918), then the wobble content is sampled again at each enabled guide signal until the sampled data matches the bit stream of the predetermined data pattern. If a match is detected (the “Yes” branch of step 918), the predetermined data pattern is output. The detected ADIP data can be used to accurately control the position of the optical pickup when recording or reproducing is performed so that data can be recorded accurately at a specific recording region of the optical disc.

[0068] In some implementations, operations 902-920 may be performed in the order listed, in parallel (e.g., by the same or a different process, substantially or otherwise non-serially), or in another order to achieve the same result.

[0069] Although the above described implementations utilizes a cycle of the wobble clock that corresponds to 16 periods (e.g., wobble clocks 0-15), a wobble cycle having a frequency half of that can be generated. In one implementation, the cycle of the wobble clock corresponds to 32 periods, and the identifying process for each wobble signal can complete within a period of 32.

[0070] In some implementations, if a guide signal generator 132 or guide signal is not implemented, the shift register of the wobble data sample logic 134 can be increased from 8 bits to 16 bits to accommodate the detection of the ADIP information. For example, using a 16-bit shift register, the ADIP sync changes from a bit stream of “11110000” to a bit stream of “1111111100000000”, the ADIP data unit zero changes from a bit stream of “10000011” to a bit stream of “1100000000001111”, and the ADIP data unit one changes from a bit stream of “10001100” to a bit stream of “1100000011110000”. In these implementations, the 16-bit shift register may introduce a higher error probability and less error tolerance than the 8-bit shift register 136. Nonetheless, the 16-bit shift register can obtain the precise ADIP information for locating the write start point of the optical pickup.

[0071] Furthermore, though eight wobble cycles have been utilized to identify ADIP information contained in the wobble signal, in some implementations, to reduce error, cycles before and after the eight wobble cycles also can be taken into consideration when sampling the wobble signal. That is, the identification of the

ADIP information can be based on more than eight wobble cycles to improve the accuracy of the identifying process. For instance, wobble cycle 92 and wobble cycle 9 before and after wobble cycles 1-8 also can be incorporated into the identification process.

The sample logic can use the negative edge of the 2*wobble clock or positive edge of the 2*wobble clock to update the 2 bit register. The different sample edges have different timing diagrams. In negative edge of the 2*wobble clock, the guide signal in Fig. 4, 6 and 8 will be delayed one wobble clock. In other word, the guide signal will be enabled on 2*wobble clock 1, 3, 5, 7. For the other logic, it will be delayed one 2*wobble clock also. For recording data in the same point under negative edge of the 2*wobble clock and positive edge of the 2*wobble clock, the recording start point under negative edge will be advanced one 2*wobble clock.

[0072] A number of implementations of the present invention have been described, and it should be understood that various modifications may be made without departing from the spirit and scope of the invention. For example, the steps performed in Figs 5-7 are descriptive of the operations performed by either the renumber tool or a user, and are arbitrary. In practice, the order in which these steps are taken is random depending on a particular application. Each of the described steps may be performed separately, in combination with, or in any order, with respect to any of the other steps.

[0073] In the previous description, various implementations of the present invention have been described. However, it will be apparent to those skilled in the art that the implementations may be practiced with only some or all aspects of the invention. For purposes of explanation, specific numbers and configurations have been set forth in order to provide a thorough understanding of the implementations. However, it will also be apparent to one skilled in the art that the implementations may be practiced without the specific details.

What is claimed is:

CLAIMS

1. A method of decoding Address in Pre-groove (ADIP) information encoded on an optical disk, the method comprising:
 - receiving a wobble signal and a wobble clock;
 - evaluating consecutive bits of the wobble signal using the wobble clock; and
 - triggering an identification of ADIP information in the wobble signal based on the evaluation.
2. The method of claim 1 where the step of receiving further includes deriving a wobble clock from a received wobble signal.
3. The method of claim 2 where the wobble clock is substantially double a frequency of the wobble signal.
4. The method of claim 2 where the step of receiving further includes determining the wobble signal from a received analog signal.
5. The method of claim 1 where evaluating consecutive bits includes evaluating two bits to detect a predetermined pattern.
6. The method of claim 5 where the predetermined pattern is 00 or 11.
7. The method of claim 1 further comprising storing ADIP content information in a reduced size buffer.
8. The method of claim 7 where triggering includes triggering a sampling of the content stored in the reduced size buffer.
9. The method of claim 8 further comprising comparing the sampled content with a predetermined pattern to identify ADIP information.
10. The method of claim 1 where the step of evaluating includes detecting a predetermined pattern in the consecutive bits, the method further including
 - if the predetermined pattern is detected, the triggering step further including triggering a signal to guide sampling of the ADIP information.
11. A method of decoding Address in Pre-groove (ADIP) information encoded on an optical disk, the method comprising:
 - generating logic data, a non-phase modulated clock and logic content associated with the logic data;
 - detecting whether a first data pattern exists in the logic data; and
 - if the first data pattern is detected:
 - adjusting a sample step of a step adjust signal;

enabling a guide signal in accordance with the adjusted sample step;
sampling the logic content;
comparing the sampled logic content with a second data pattern; and
identifying ADIP information based on the comparison.

12. The method of claim 11, further comprising enabling the guide signal periodically, and changing transition states of the guide signal every cycle when the guide signal is disabled.

13. The method of claim 11, further comprising adjusting a step of the guide signal using the step adjust signal.

14. The method of claim 11, wherein the first data pattern includes a bit stream of "00" or "11".

15. The method of claim 11, wherein the logic content is sampled in a shift register.

16. The method of claim 11, wherein the second data pattern includes one of a group consisting of an ADIP sync unit having a bit stream of "11110000", an ADIP data unit having a logic level of "0" defined as having a bit stream of "10000011" and an ADIP data unit having a logic level of "1" defined as having a bit stream of "10001100".

17. The method of claim 11, where detecting whether a first data pattern exists in the logic data includes sampling the logic data and comparing the sampled logic data with the first data to generate the step adjust signal.

18. The method of claim 17, wherein the clock is generated based on a phase-modulated input, and includes a period of 16 channel bits.

19. The method of claim 18, where the logic content is sampled in a shift register using the clock.

20. An optical disc apparatus capable of decoding ADIP information from an optical disc, the apparatus comprising:

a wobble signal generator to generate a wobble signal, a wobble clock and wobble content associated with the wobble signal;

a pattern detector coupled to the wobble signal generator and configured to detect a first data pattern in the wobble signal and to generate a step adjust signal;

a guide signal generator coupled to the pattern detector and configured to initiate a guide signal in response to the received step adjust signal; and

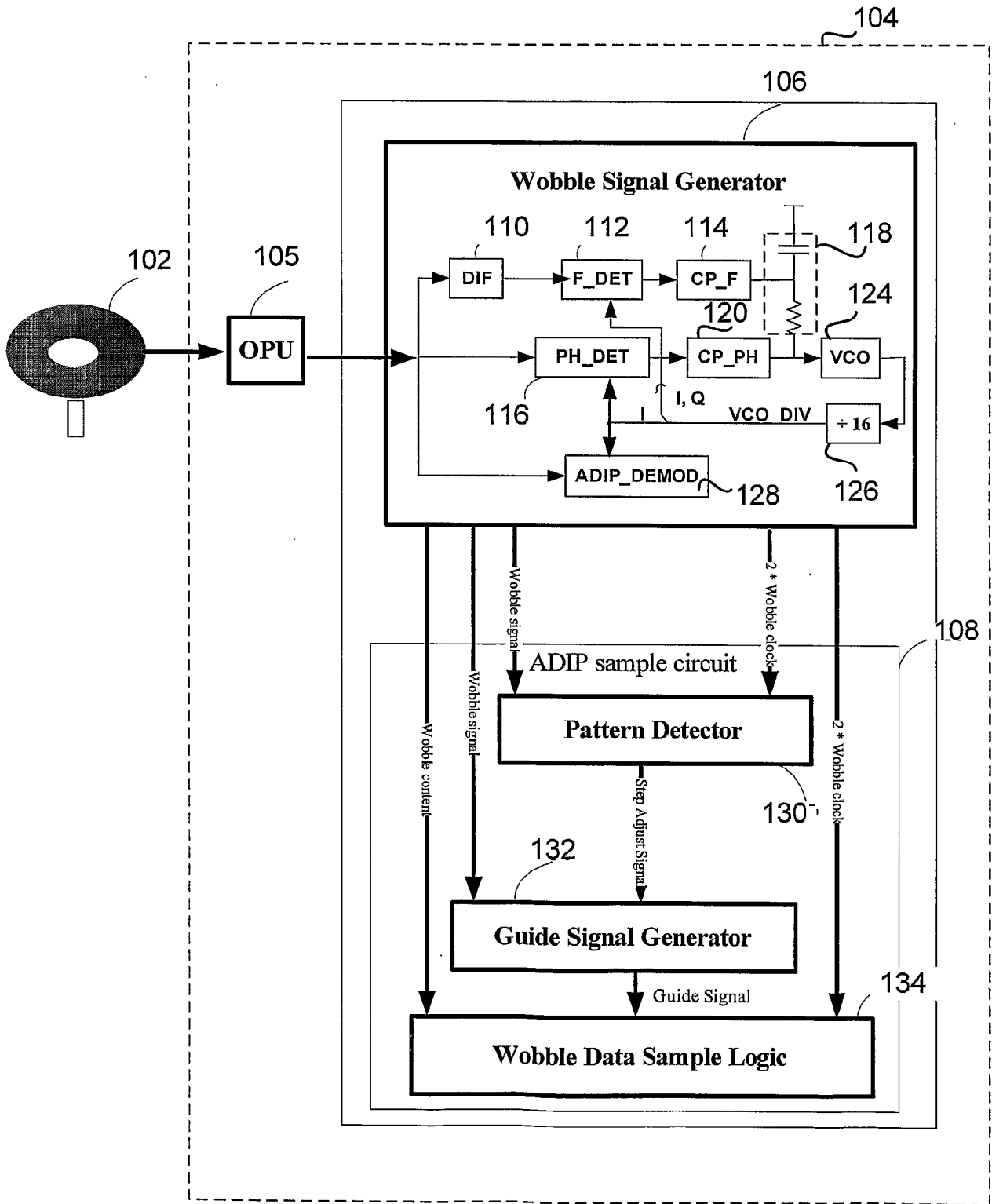
a wobble data sample logic circuit coupled to the wobble signal generator and the guide signal generator and configured to sample the wobble content based on the guide signal and the wobble clock.

21. The apparatus of claim 20, wherein the pattern detector includes a n-bit shift register configured to detect the first data pattern in the wobble signal.

22. The apparatus of claim 20, wherein the wobble data sample logic circuit includes an m-bit shift register configured to sample the wobble content and compare the sampled wobble content with a second data pattern.

23. The apparatus of claim 21, wherein the first data pattern is a data pattern of "00" or "11".

24. The apparatus of claim 22, wherein the second data pattern includes one of a group consisting of an ADIP sync unit having a bit stream of "11110000", an ADIP data unit having a logic level of "0" defined as having a bit stream of "10000011" and an ADIP data unit having a logic level of "1" defined as having a bit stream of "10001100".



100

Fig. 1

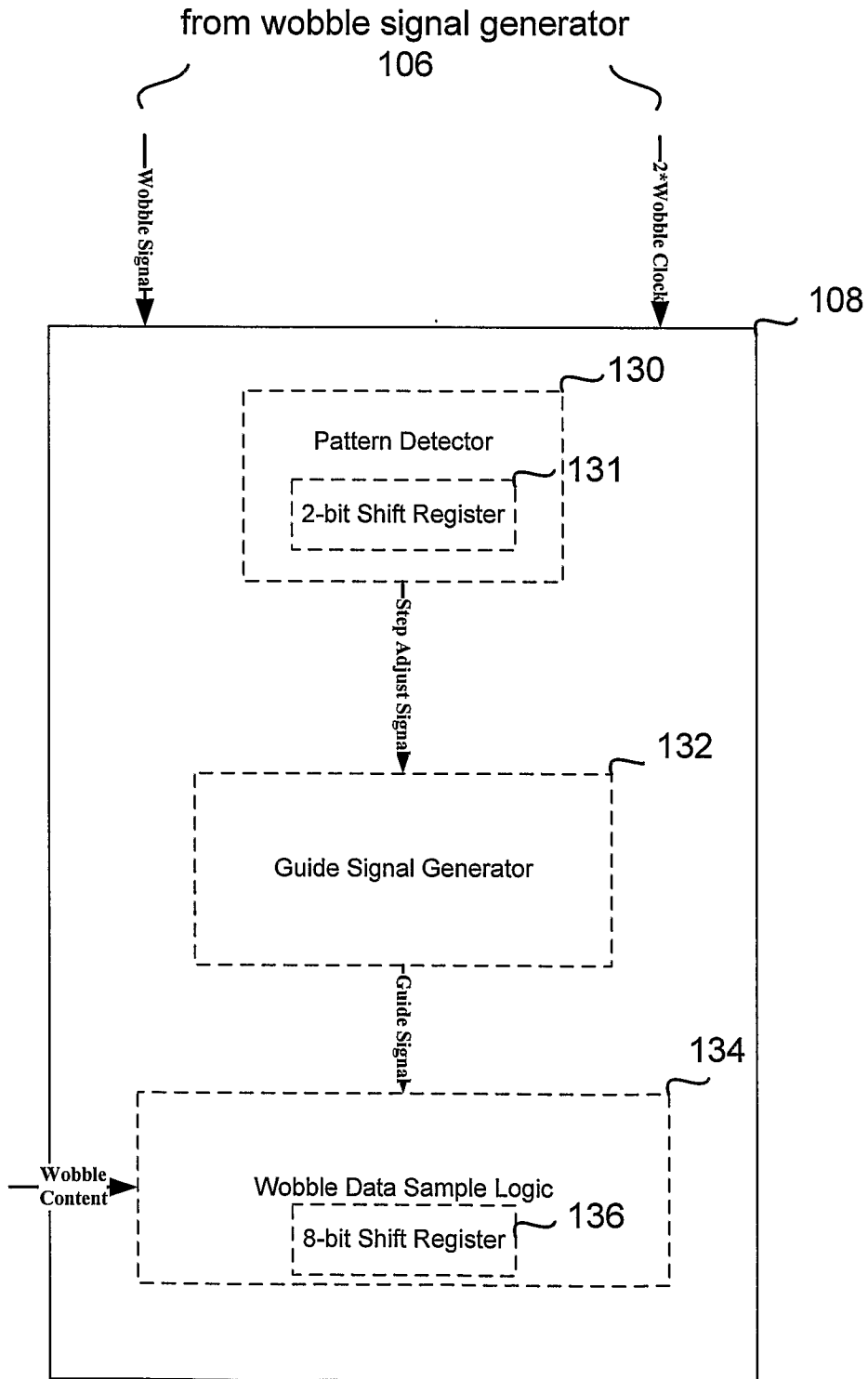


Fig. 2

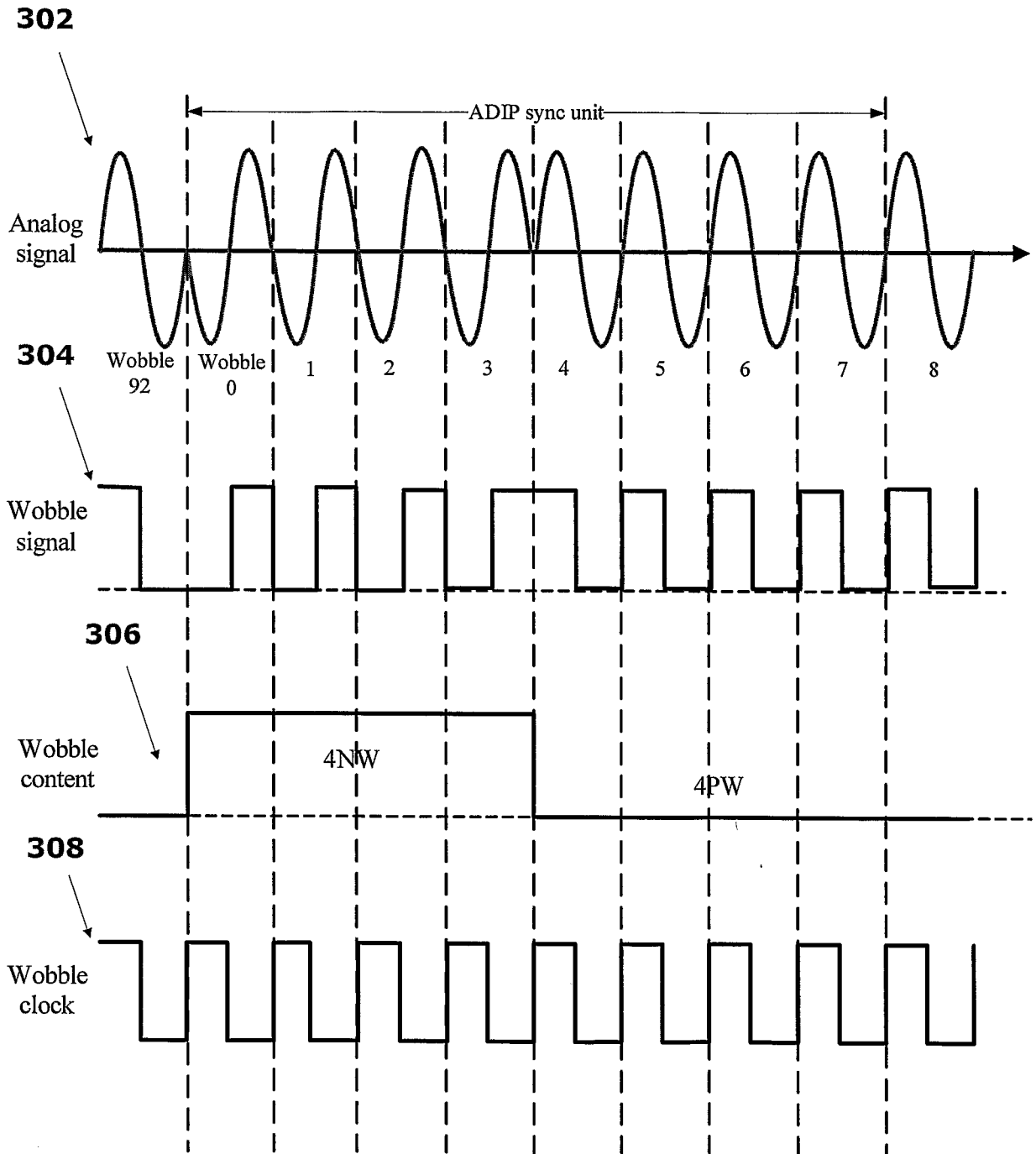


Fig. 3

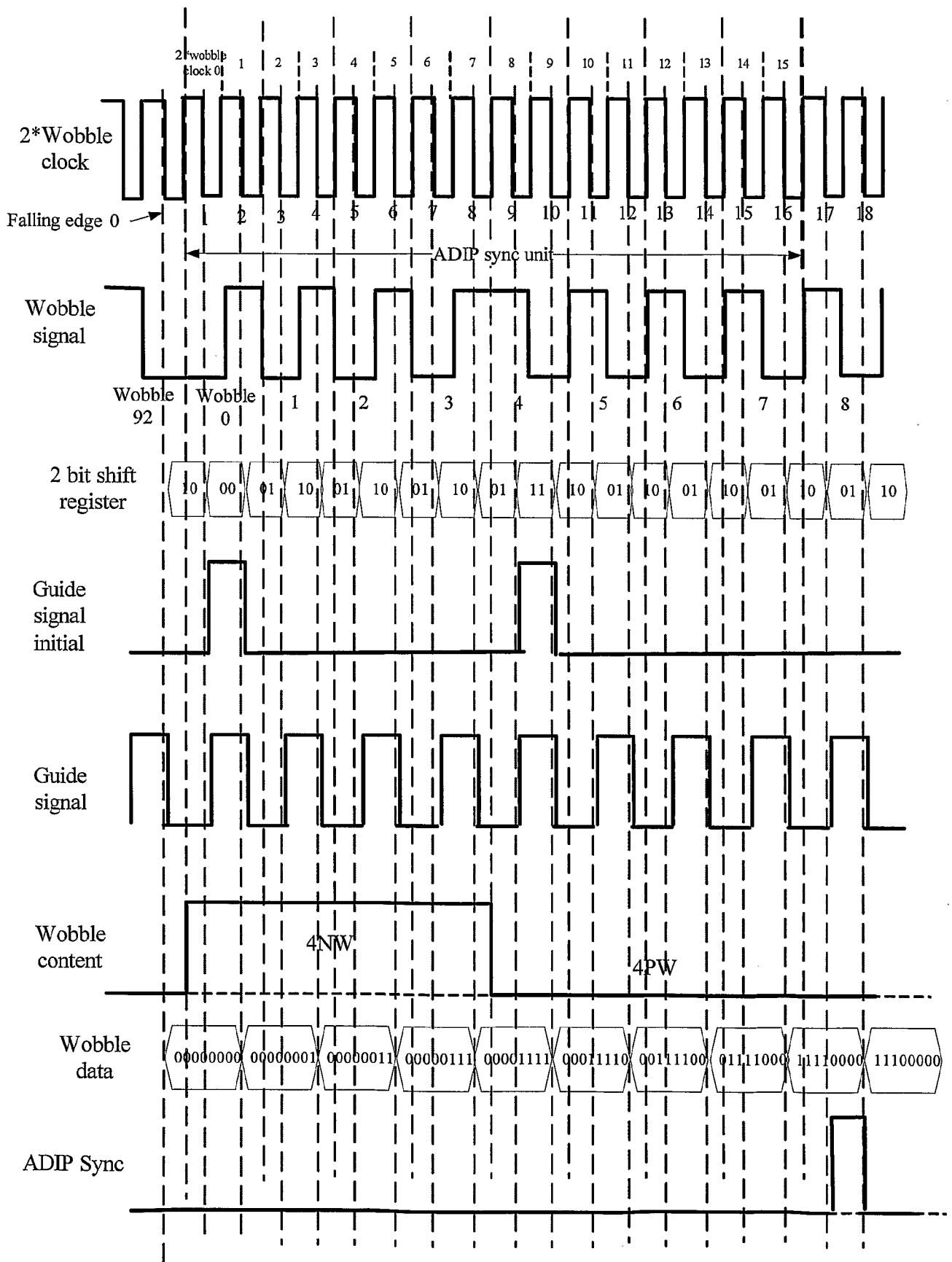


Fig. 4

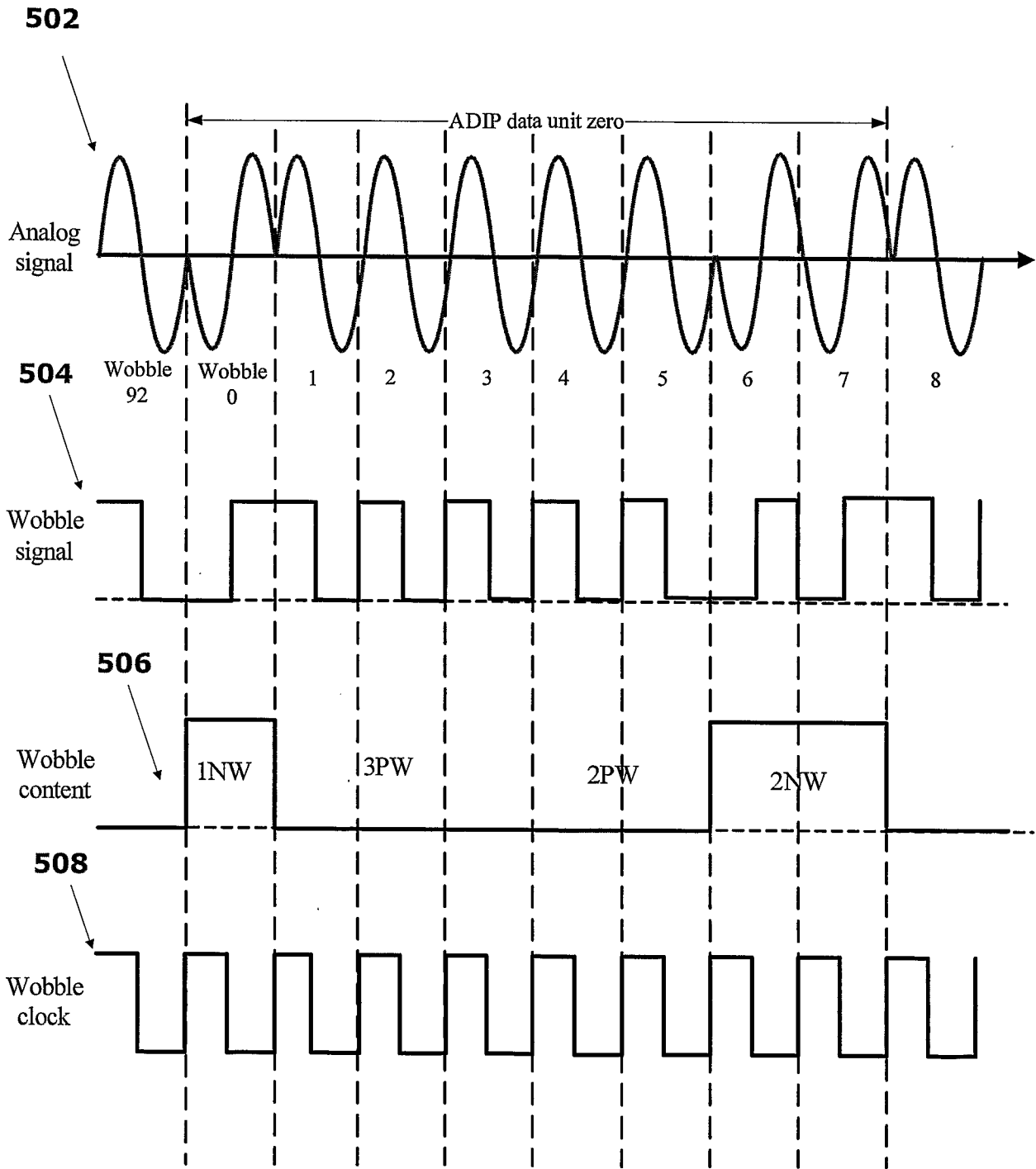


Fig. 5

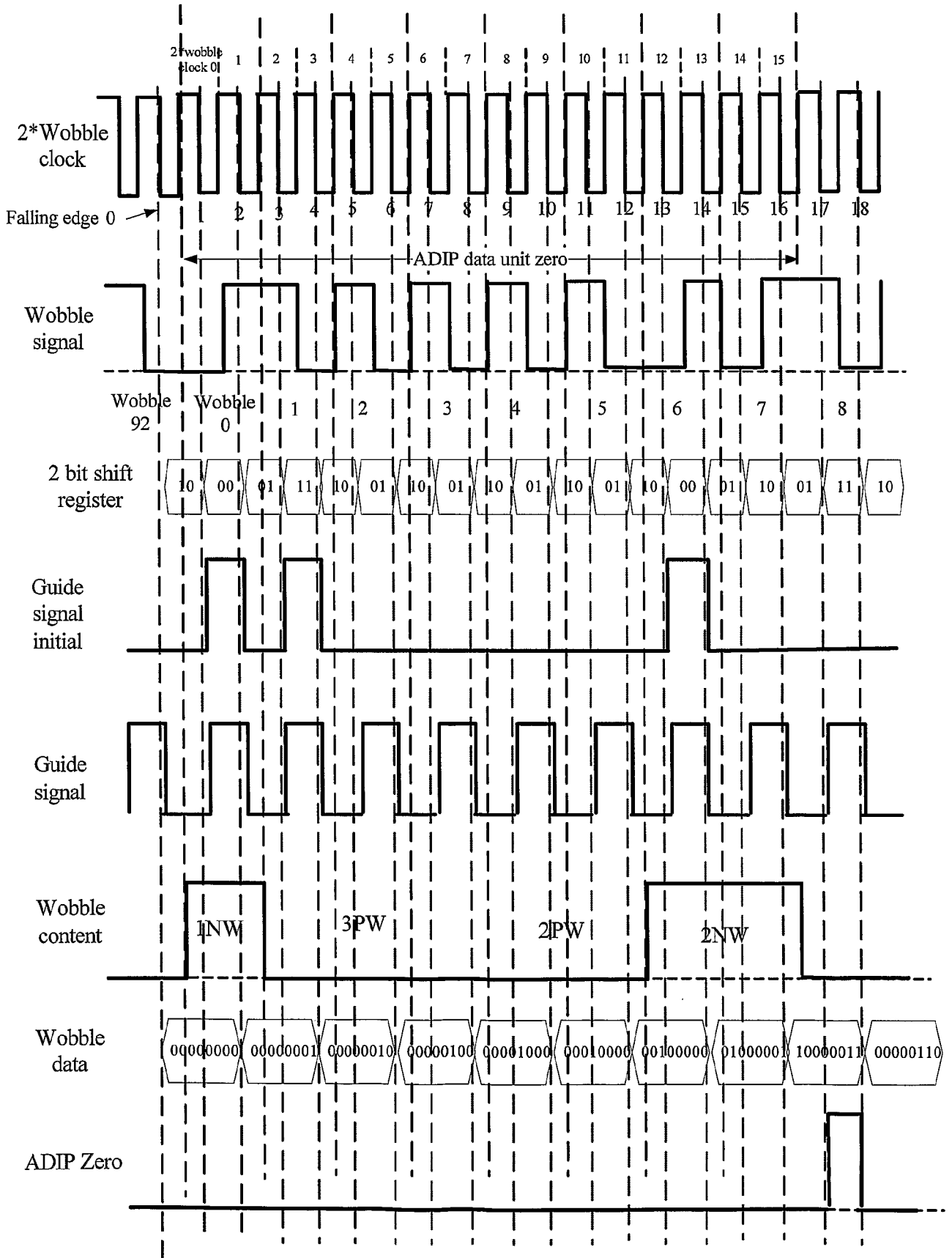


Fig. 6

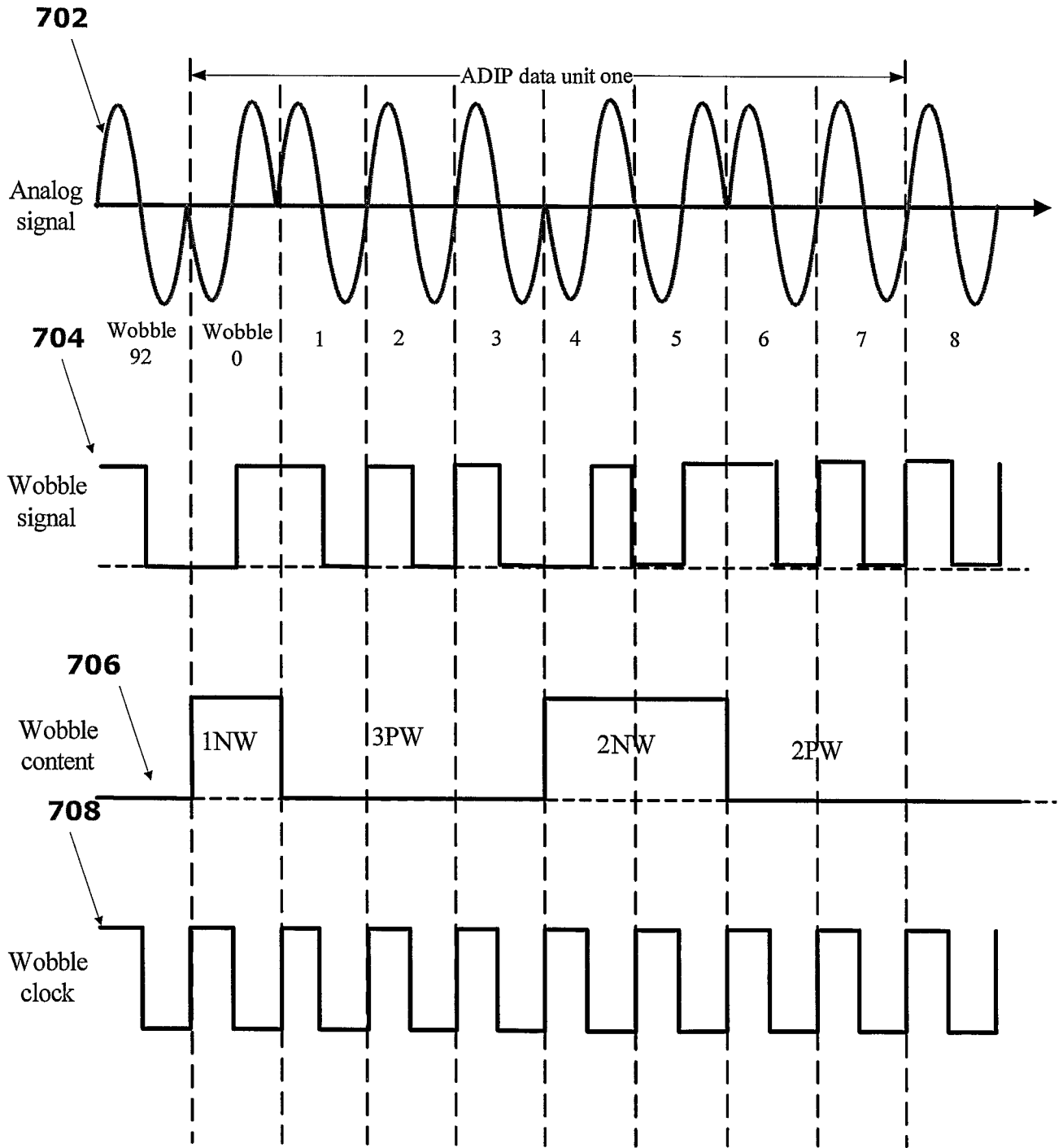


Fig. 7

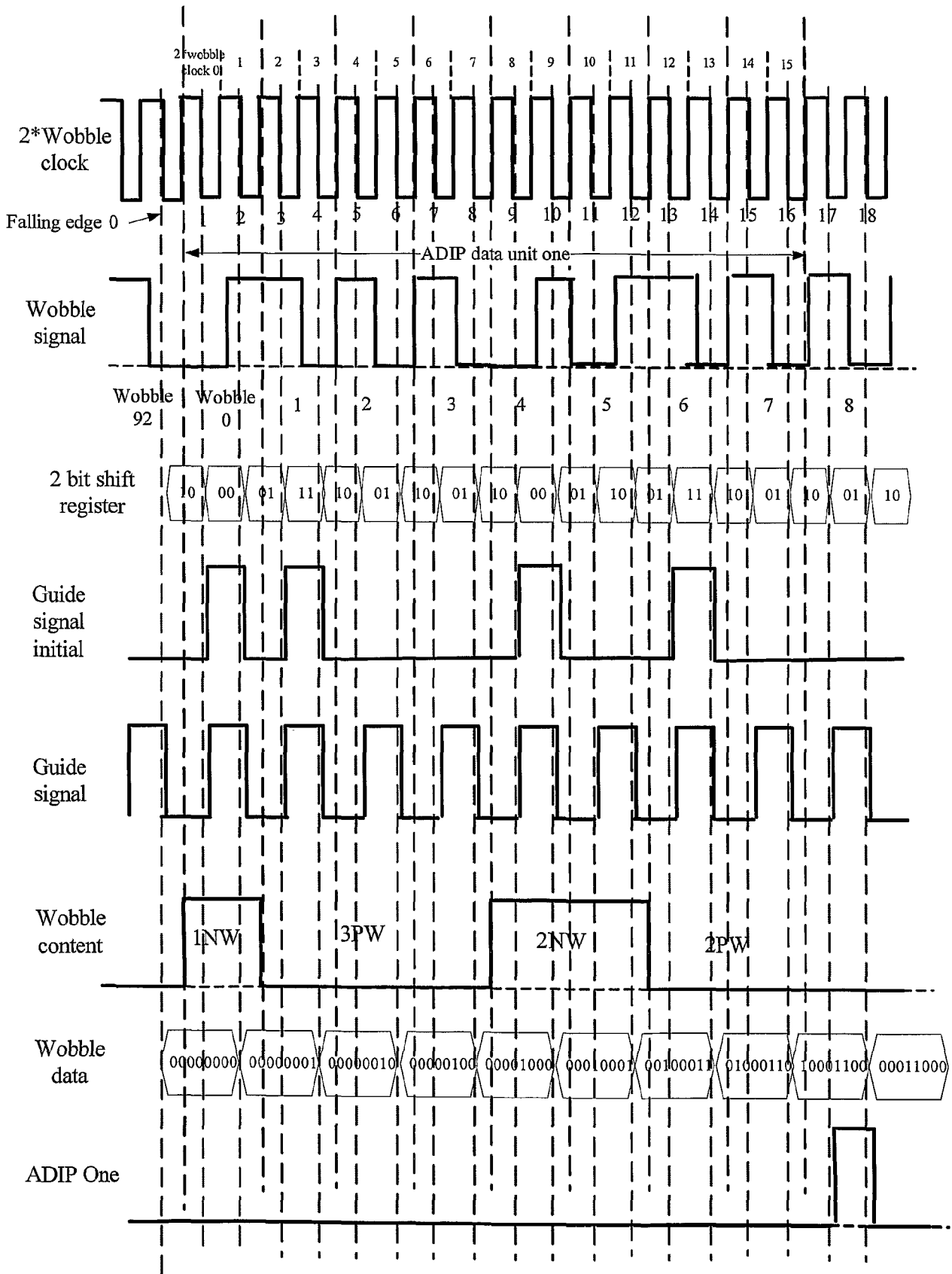


Fig. 8

900

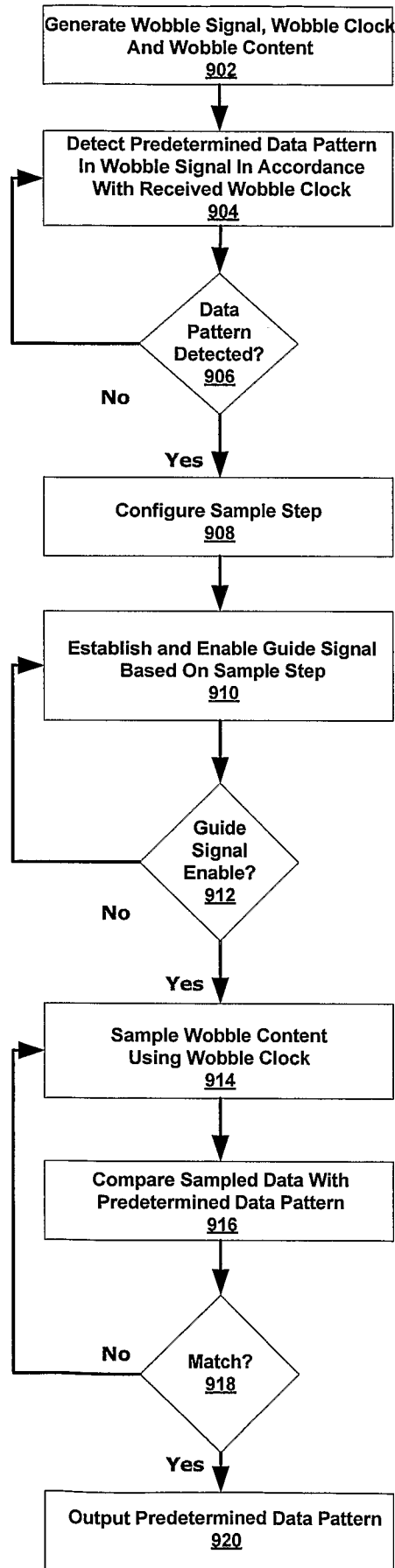


Fig. 9

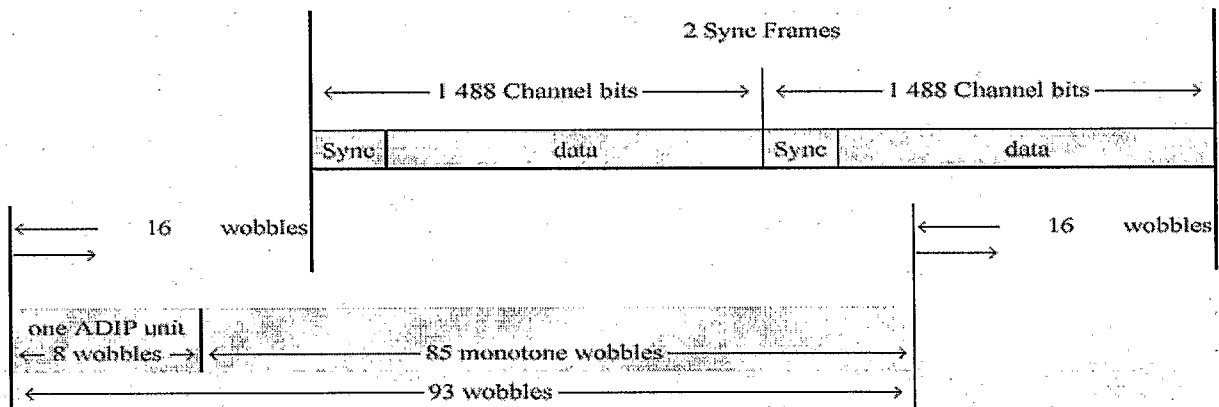


Fig. 10