(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
22 October 2015 (22.10.2015)

WIPO | PCT

(10) International Publication Number
WO 2015/160465 A1

(51) International Patent Classification:
H03K 5/151 (2006.01) *H03K 17/16* (2006.01)
H02M 1/38 (2007.01) *H03K 19/003* (2006.01)

(21) International Application Number:
PCT/US2015/021170

(22) International Filing Date:
18 March 2015 (18.03.2015)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
14/254,875 16 April 2014 (16.04.2014) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) Title: ANALOG BREAK BEFORE MAKE SYSTEM, METHOD AND APPARATUS

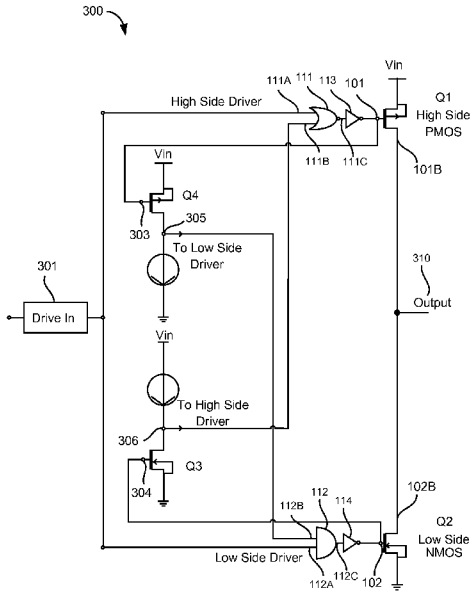

FIG. 3

(57) Abstract: A system and method of providing an analog make before break circuit includes a first transistor Q1 coupled in series with a second transistor Q2, the first transistor being configured for conducting a high portion of an input signal, the second transistor being configured for conducting a low portion of the input signal. A third transistor Q3 is configured to interrupt a connection between the input signal and a first transistor input node, the third transistor having a third transistor threshold voltage of between about 90 and about 110 percent of a second transistor threshold voltage. A fourth transistor Q4 is configured to interrupt a connection between the input signal and a second transistor input node, the fourth transistor having a fourth transistor threshold voltage of between about 90 and about 110 percent of a first transistor threshold voltage.

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ANALOG BREAK BEFORE MAKE SYSTEM, METHOD AND APPARATUS

By Inventors:

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BACKGROUND

[1] The present invention relates generally to driving circuits and methods, and more particularly, to systems, methods and apparatus for timing the conductance of driver circuits.

[2] Fig. 1A is a typical driver circuit 100. A PMOS high side transistor Q1 is connected in series with an NMOS low side transistor Q2. The respective input nodes 101 and 102 of the high side transistor Q1 and the low side transistor Q2 are cross coupled through respective driver/gates 111, 113 and 112, 114, so that as high side transistor begins to shut off (i.e., stop conducting), the low side transistor is gated to on (i.e., begin conducting). Transistor Q1 is a PMOS transistor and transistor Q2 is a NMOS transistor in the present example, however, the types of transistors can vary.

[3] However, due to various circuit dynamics, such as parasitic capacitance, slow gate turn off ramp and other issues, one high side transistor does not turn off and stop conducting instantaneously and before one low side transistor turns on and begins conducting. Figs. 1B and 1C are graphical representations of gate voltages applied to the typical driver circuit 100. In an initial state, transistor Q1 is non-conducting (state 0) and transistor Q2 is conducting (state 1).

[4] A Q2 gate voltage 122 has an initial value for fully conducting state 1 at time T0. The Q2 gate voltage 122 has a downward slope as the Q2 gate voltage gradually decreases between time T0 and time T4. At time T0, the Q2 gate voltage 122 is enabled. However, the Q2 gate voltage 122 does not drop to minimum level Vmin, instantaneously as discussed above. At a time T3, the Q2 gate voltage 122 drops below a threshold voltage V_{TN} for transistor Q2 and Q2 stops conducting. The Q2 gate voltage 122 continues to decrease to the minimum voltage Vmin at time T4.

[5] Similarly, a Q1 gate voltage 121 has an initial value for fully non-conducting state 0. Q1 gate voltage 121 has a downward slope as the gate voltage gradually decreases between time T1 and time T5. At time T1, the Q1 gate voltage 121 is disabled or removed. However, the Q1 gate voltage 121 does not drop to minimum level Vmin

instantaneously, as discussed above. At a time T2, the Q1 gate voltage 121 drops below a threshold voltage V_{TP} for transistor Q1 and Q1 begins conducting. The Q1 gate voltage 121 continues to drop to minimum level Vmin at time T5 and Q1 continue to conduct between time T2 and beyond time T5.

[6] As shown above, transistor Q2 is still conducting between time T2 and time T3 and therefore, when transistor Q1 begins conducting at time T2, then a current spike can occur through the series transistors Q1, Q2 until time T3, when Q2 stops conducting. The current spike consumes excess power and can cause component damage.

[7] Fig. 1C illustrates the inverse of the switching sequence shown in Fig. 1B. The inverse switching sequence can result in a second current spike when transistor Q2 begins conducting at time T8 before the transistor Q1 stops conducting and time T9.

[8] What is needed is a system and method to confirm the presently conducting transistor is actually in a fully non-conducting state 0 before the presently non-conducting transistor actually begins conducting and thus prevent the series current spikes described above between times T2 and T3 and between times T8 and T9.

SUMMARY

[9] Broadly speaking, the present invention fills these needs by providing a driver circuit that does not suffer series current spikes. It should be appreciated that the present invention can be implemented in numerous ways, including as a process, an apparatus, a system, computer readable media, or a device. Several inventive embodiments of the present invention are described below.

[10] One embodiment provides an analog make before break circuit including a first transistor coupled in series with a second transistor, the first transistor being configured for conducting a high portion of an input signal, the second transistor being configured for conducting a low portion of the input signal. A third transistor is configured to interrupt a connection between the input signal and a first transistor input node, the third transistor having a third transistor threshold voltage between of about 90 and about 110 percent of a second transistor threshold voltage. A fourth transistor is configured to interrupt a connection between the input signal and a second transistor input node, the fourth transistor having a fourth transistor threshold voltage of between about 90 and about 110 percent of a first transistor threshold voltage.

[11] The third transistor configured to interrupt the connection between the input signal and the first transistor input node can include coupling a third transistor input node to the second transistor input node, coupling the input signal to a first NOR gate input node, coupling a third transistor output node to a second NOR gate input node and coupling a NOR gate output node to the first transistor input node.

[12] The fourth transistor configured to interrupt the connection between the input signal and the second transistor input node can include coupling a fourth transistor input node to the first transistor input node, coupling the input signal to a first AND gate input node, coupling a fourth transistor output node to a second AND gate input node and coupling an AND gate output node to the second transistor input node.

[13] The first transistor threshold voltage can be substantially equal to the fourth transistor threshold voltage. The second transistor threshold voltage can be substantially equal to the third transistor threshold voltage. The first transistor threshold voltage can be substantially equal to the second transistor threshold voltage. The first transistor threshold voltage may not equal to the second transistor threshold voltage in at least one embodiment.

[14] The first transistor can be coupled in series with the second transistor between a supply voltage source and a ground. The circuit can also includes an analog make before break circuit output node coupled between a first transistor output node and a second transistor output node.

[15] Another embodiment provides a method of providing an analog make before break including coupling an input signal from an analog make before break circuit input node an to a first transistor input node. A first transistor is coupled in series with a second transistor, the first transistor being configured for conducting a high portion of an input signal, the second transistor being configured for conducting a low portion of the input signal. The coupling of the input signal to the first transistor input node is interrupted before coupling the input signal to a second transistor input node. The input signal is then coupled to the second transistor input node. The coupling of the input signal to the second transistor input node is interrupted before coupling the input signal to the first transistor input node.

[16] Coupling the input signal to the first transistor input node can be interrupted by a third transistor having a third transistor threshold voltage between of about 90 and about 110 percent of a second transistor threshold voltage. Coupling the input signal to the second transistor input node can be interrupted by a fourth transistor having a fourth transistor threshold voltage between of about 90 and about 110 percent of a first transistor threshold voltage.

[17] The input signal can be coupled to the first transistor input node through a first logic gate and wherein the first logic gate is disabled until the second transistor is in a non-conducting state. The input signal can be coupled to the second transistor input node through a second logic gate and wherein the second logic gate is disabled until the first transistor is in a non-conducting state.

[18] Yet another embodiment provides an analog make before break system including a first transistor coupled in series with a second transistor, the first transistor being configured for conducting a high portion of an input signal, the second transistor being configured for conducting a low portion of the input signal. A first interrupt device is coupled between the input signal and a first transistor input node. The first interrupt device configured interrupt coupling the input signal to the first transistor input node when the second transistor is in a conducting state. A second interrupt device is coupled between the input signal and a second transistor input node. The second interrupt device configured interrupt coupling the input signal to the second transistor input node when the first transistor is in a conducting state.

[19] Other aspects and advantages of the invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[20] The present invention will be readily understood by the following detailed description in conjunction with the accompanying drawings.

[21] Fig. 1A is a typical driver circuit.

[22] Figs. 1B and 1C are graphical representations of gate voltages applied to the typical driver circuit.

[23] Figs. 2A is graphical representation of ideal gate voltages applied to an improved driver circuit as the low side driver Q1 stops conducting and the high side driver Q2 begins conducting, for implementing embodiments of the present disclosure.

[24] Figs. 2B is a graphical representation of ideal gate voltages applied to the improved driver circuit as the high side driver Q2 stops conducting and the low side driver Q1 begins conducting, for implementing embodiments of the present disclosure.

[25] Fig. 3 is a schematic diagram of the analog make before break circuit, for implementing embodiments of the present disclosure.

[26] Figs. 4A is graphical representation of gate voltages applied to an improved driver circuit as the low side driver Q1 stops conducting and the high side driver Q2 begins conducting, for implementing embodiments of the present disclosure.

[27] Figs. 4B is a graphical representation of gate voltages applied to the improved driver circuit as the high side driver Q2 stops conducting and the low side driver Q1 begins conducting, for implementing embodiments of the present disclosure.

[28] Fig. 5 is a flowchart diagram that illustrates the method operations performed in preventing the series current spikes, for implementing embodiments of the present disclosure.

DETAILED DESCRIPTION

[29] Several exemplary embodiments for systems and methods or operating a driver circuit that does not suffer series current spikes will now be described. It will be apparent to those skilled in the art that the present invention may be practiced without some or all of the specific details set forth herein.

[30] One approach to prevent series current spikes is to place a coupling transistor in each of the respective input nodes of the high side transistor and the low side transistor. Each of the coupling transistors closely matches the gate voltage point of the respective driver transistor providing the input to the coupling transistor. As a result, the coupling transistor cannot gate the cycling on transistor until after the cycling off transistor is in a fully non-conducting state, thereby preventing a series current spike.

[31] Figs. 2A is graphical representation of ideal gate voltages 221, 222 applied to an improved driver circuit 300 as the low side driver Q1 stops conducting and the high side

driver Q2 begins conducting, for implementing embodiments of the present disclosure. As shown an ideal gate voltage 222 for a Q2 low side NMOS driver is initially a high value V1 such that Q2 is in a fully conducting state (state 1). At a time T3 the gate voltage 222 drops immediately to a minimum voltage Vmin and Q2 immediately stops conducting such that Q2 is in a fully non-conducting state (state 0) at time T3. Similarly, an ideal gate voltage 221 for a Q1 high side PMOS driver is initially a high value V1 such that Q1 is in a fully non-conducting state (state 0). At a time T2 the gate voltage 221 drops immediately to a minimum voltage Vmin and Q1 immediately switches to a fully conducting state (state 1) at time T2. Because time T2 occurs after time T3, the series current spike is avoided because Q2 is in a fully non-conducting state before Q1 begins conducting.

[32] Figs. 2B is a graphical representation of ideal gate voltages 221, 222 applied to the improved driver circuit 300 as the high side driver Q2 stops conducting and the low side driver Q1 begins conducting, for implementing embodiments of the present disclosure. Continuing from Fig 2A, the gate voltage 221 for a Q1 high side PMOS driver is a minimum voltage (Vmin) such that Q1 is in a fully conducting state (state 1). At a time T9 the gate voltage 221 rises immediately to a high value voltage V1 and Q1 immediately stops conducting such that Q1 is in a fully non-conducting state (state 0) at time T9. Similarly, the ideal gate voltage 222 for a Q2 low side NMOS driver is at a minimum voltage Vmin such that Q2 is in a fully non-conducting state (state 0). At a time T8 the gate voltage 222 rises immediately to a high state voltage V1 and Q2 immediately switches to a fully conducting state (state 1) at time T8. Because time T8 occurs after time T9, the series current spike is avoided because Q1 is in a fully non-conducting state before Q2 begins conducting.

[33] As stated above, the ideal gate voltages 221, 222 are able to switch from a high state (V1) to a low state (Vmin) instantaneously (i.e., with a vertical slope). Unfortunately, actual electrical circuits do not switch instantaneously. The timing of the conducting states (state 1) of transistors Q1 and Q2 can be selected to prevent the conducting states (state 1) of transistors Q1 and Q2 from overlapping and the series current spike.

[34] Fig. 3 is a schematic diagram of the analog make before break circuit 300, for implementing embodiments of the present disclosure. PMOS high side transistor Q1 is connected in series with an NMOS low side transistor Q2 between a supplied voltage source Vin and a ground potential. The improved driver circuit 300 includes a transistor

Q3 coupled to a first input node 111B of logic NOR gate 111. An output 111C of the NOR gate 111 is coupled to the input node 101 of transistor Q1 through inverter 113. The input signal 301 is coupled to a second input node 111A of NOR gate 111. The transistor Q4 input 303 is coupled to the input node 101 of transistor Q1.

[35] The circuit 300 also includes a transistor Q4 coupled to a first input 112B of logic AND gate 112. An output 112C of the AND gate 112 is coupled to the input node 102 of the low side transistor Q2 through inverter 114. The input signal 301 is also coupled to a second input node 112A of AND gate 112. The transistor Q3 input 304 is coupled to the input node 102 of transistor Q2. An output 310 of the analog make before break circuit 300 is coupled to the output nodes 101B and 102B of transistors Q1 and Q2, respectively.

[36] The transistor Q4 delays the low side transistor Q2 conducting (state 1) and can have a threshold voltage between about 90 and 110 percent of the threshold voltage of the high side transistor Q1. In one implementation, the Q4 threshold voltage is substantially equal to the Q1 threshold voltage. The source current value can be optimized (lower current increases the delay time), in order to delay signal 305 to ensure the high side transistor Q1 will fully non-conducting (state 0) before low side transistor Q2 begins to conduct (state 1), thereby avoiding the series current spikes described in Figs. 1A-C above.

[37] Similarly, transistor Q3 delays the high side transistor Q1 conducting (state 1) and can have a threshold voltage between about 90 and 110 percent of the threshold voltage of the low side transistor Q2. In one implementation, the Q3 threshold voltage can be substantially equal to the Q2 threshold voltage. The sink current value can be optimized (lower current increase the delay time) in order to delay signal 306 to ensure the low side transistor Q2 will fully non-conducting (state 0) before high side transistor Q1 begins to conduct (state 1) , thereby avoiding the series current spikes described in Figs. 1A-C above.

[38] Figs. 4A is graphical representation of gate voltages 421, 422 applied to an improved driver circuit 300 as the low side driver Q1 stops conducting and the high side driver Q2 begins conducting, for implementing embodiments of the present disclosure. As shown a gate voltage 422 for the Q2 low side NMOS driver is initially a high value V1 such that Q2 is in a fully conducting state (state 1). At a time T0 the gate voltage 422 is disabled or removed. However, the Q2 gate voltage 422 does not drop to minimum level

Vmin, instantaneously and thus Q2 does not stop conducting immediately. The gate voltage 422 drops between time T0 and T2 to the minimum voltage Vmin. As the bias voltage 422 drops to lower than Q2's threshold voltage Vtn, Q2 stops conducting such that Q2 is in a fully non-conducting state (state 0) at time T3.

[39] The gate voltage 421 for the Q1 high side PMOS driver is initially a high value V1 such that Q1 is in a fully non-conducting state (state 0). Q1 gate voltage 421 has a downward slope as the gate voltage gradually decreases between time T1 and time T5. At a time T2, the Q1 gate voltage 421 drops below a threshold voltage V_{TP} for transistor Q1 and driver transistor Q3.

[40] At time T2, transistor Q3 begins conducting. After transistor Q3 begins conducting, the input 111B of the NOR gate 111 is pulled low, thus allowing the driver input signal from the input 303 to be conducted to the input of transistor Q1 and transistor Q1 can begin conducting (state 1) some time after time T2. Because time T2 occurs after time T3, the series current spike is avoided because transistor Q2 is in a fully non-conducting state before transistor Q1 begins conducting.

[41] Figs. 4B is a graphical representation of gate voltages 421, 422 applied to the improved driver circuit 300 as the high side driver transistor Q2 stops conducting and the low side driver transistor Q1 begins conducting, for implementing embodiments of the present disclosure. Continuing from Fig 4A, the gate voltage 421 for a transistor Q1 high side PMOS driver is a minimum voltage (Vmin) such that transistor Q1 is in a fully conducting state (state 1). At a time T6 the gate voltage 421 begins to rise to a high value voltage V1 at time T8. At time T7, the gate voltage 421 rises above threshold voltage Vtn of the transistor Q3 and transistor Q3 stops conducting (state 0). After transistor Q3 stops conducting, the input 111B of the NOR gate 111 is pulled higher, thus blocking the driver input signal from the input 303 from be conducted to the input of transistor Q1 and transistor Q1 stops conducting (state 0) some time after time T7.

[42] Continuing from Fig 4A, the gate voltage 422 for a transistor Q2 low side NMOS driver is a minimum voltage (Vmin) such that transistor Q2 is in a fully non-conducting state (state 0). At time T9, the gate voltage 422 for a Q2 begins to rise to a maximum level V1 at time T11. At time T10, the gate voltage 422 rises above a threshold voltage V_{TN} for transistor Q2 and transistor Q4.

[43] At time T10, transistor Q4 begins conducting. After transistor Q4 begins conducting, the input 112B of the AND gate 112 is pulled low, thus allowing the driver input signal from the input 303 to be conducted to the input of transistor Q2 and Q2 can begin conducting (state 1) some time after time T10. Because time T10 occurs after time T7, the series current spike is avoided because Q1 is in a fully non-conducting state before Q2 begins conducting.

[44] Fig. 5 is a flowchart diagram that illustrates the method operations performed in preventing the series current spikes, for implementing embodiments of the present disclosure. The operation of the improved driver circuit 300 can be summarized as following operations. Beginning with an initial state of the low side NMOS transistor Q2 conducting (state 1) and the high side PMOS transistor Q1 is in a non-conducting (state 0). In an operation 505, the input to the low side NMOS transistor Q2 is disabled and the gate voltage is removed from transistor Q2 in an operation 510 to place Q2 in a non-conducting state (state 0).

[45] At some time after disabling the input to low side transistor Q2, the input to the high side transistor Q1 is enabled in an operation 515. The high side transistor Q1 is gated to a conducting state (state 1), in an operation 520.

[46] When the gate voltage switches to low state, in an operation 525, the input to the high side transistor Q1 is disabled and the gate is removed from Q1 in an operation 530 to place Q1 in a non-conducting state (state 0).

[47] At some time after disabling the input to high side transistor Q1, the input to the low side transistor Q2 is enabled in an operation 535. The low side transistor Q2 is gated to a conducting state (state 1), in an operation 540.

[48] As stated above, the examples of PMOS and NMOS transistors Q1, Q3 and Q2, Q4, respectively, are merely exemplary and it should be understood that different types of transistors can be used similarly.

[49] It should be understood that the above described driver circuit is merely an example for purposes of discussion of the operating principles and the circuit structure and design. Other circuits and devices can also include the improvements described above. By way of example, a switching regulator driver, an inverter and any other circuit with a high side MOS transistor in a serial connection with a low side MOS transistor.

[50] With the above embodiments in mind, it should be understood that the invention may employ various computer-implemented operations involving data stored in computer systems. These operations are those requiring physical manipulation of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. Further, the manipulations performed are often referred to in terms, such as producing, identifying, determining, or comparing.

[51] It will be further appreciated that the instructions represented by the operations in the above figures are not required to be performed in the order illustrated, and that all the processing represented by the operations may not be necessary to practice the invention. Further, the processes described in any of the above figures can also be implemented in software stored in any one of or combinations of the RAM, the ROM, or the hard disk drive of a computer.

[52] Although the foregoing invention has been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalents of the appended claims.

What is claimed is:

Claims

1. An analog make before break circuit comprising:

a first transistor coupled in series with a second transistor, the first transistor being configured for conducting a high portion of an input signal, the second transistor being configured for conducting a low portion of the input signal;

a third transistor configured to interrupt a connection between the input signal and a first transistor input node, the third transistor having a third transistor threshold voltage between 90 and 110 percent of a second transistor threshold voltage; and

a fourth transistor configured to interrupt a connection between the input signal and a second transistor input node, the fourth transistor having a fourth transistor threshold voltage of between 90 and 110 percent of a first transistor threshold voltage.

2. The circuit of claim 1, wherein the third transistor configured to interrupt the connection between the input signal and the first transistor input node includes:

coupling a third transistor input node to the second transistor input node;

coupling the input signal to a first NOR gate input node;

coupling a third transistor output node to a second NOR gate input node; and

coupling an NOR gate output node to the first transistor input node.

3. The circuit of claim 1, wherein the fourth transistor configured to interrupt the connection between the input signal and the second transistor input node includes:

coupling a fourth transistor input node to the first transistor input node;

coupling the input signal to a first AND gate input node;

coupling a fourth transistor output node to a second AND gate input node; and

coupling an AND gate output node to the second transistor input node.

4. The circuit of claim 1, wherein the first transistor threshold voltage is equal to the fourth transistor threshold voltage.

5. The circuit of claim 1, wherein the second transistor threshold voltage is equal to the third transistor threshold voltage.

6. The circuit of claim 1, wherein the first transistor threshold voltage is equal to the second transistor threshold voltage.

7. The circuit of claim 1, wherein the first transistor threshold voltage is not equal to the second transistor threshold voltage.

8. The circuit of claim 1, wherein the first transistor is coupled in series with the second transistor between a supply voltage source and a ground potential.

9. The circuit of claim 1, further comprising an analog make before break circuit output node coupled between a first transistor output node and a second transistor output node.

10. A method of providing an analog make before break comprising:

coupling an input signal from an analog make before break circuit input node an to a first transistor input node wherein a first transistor is coupled in series with a second transistor, the first transistor being configured for conducting a high portion of an input signal, the second transistor being configured for conducting a low portion of the input signal;

interrupting the coupling of the input signal to the first transistor input node before coupling the input signal to a second transistor input node;

coupling the input signal to the second transistor input node; and

interrupting the coupling of the input signal to the second transistor input node before coupling the input signal to the first transistor input node.

11. The method of claim 10, wherein coupling the input signal to the first transistor input node is interrupted by a third transistor having a third transistor threshold voltage between 90 and 110 percent of a second transistor threshold voltage.

12. The method of claim 10, wherein coupling the input signal to the second transistor input node is interrupted by a fourth transistor having a fourth transistor threshold voltage between 90 and 110 percent of a first transistor threshold voltage.

13. The method of claim 10, wherein the input signal is coupled to the first transistor input node through a first logic gate and wherein the first logic gate is disabled until the second transistor is in a non-conducting state.

14. The method of claim 10, wherein the input signal is coupled to the second transistor input node through a second logic gate and wherein the second logic gate is disabled until the first transistor is in a non-conducting state.

15. An analog make before break system comprising:

a first transistor coupled in series with a second transistor, the first transistor being configured for conducting a high portion of an input signal, the second transistor being configured for conducting a low portion of the input signal;

a first interrupt device coupled between the input signal and a first transistor input node, the first interrupt device configured interrupt coupling the input signal to the first transistor input node when the second transistor is in a conducting state; and

a second interrupt device coupled between the input signal and a second transistor input node, the second interrupt device configured interrupt coupling the input signal to the second transistor input node when the first transistor is in a conducting state.

16. The system of claim 15, wherein the first interrupt device includes a third transistor having a third transistor threshold voltage between 90 and 110 percent of a second transistor threshold voltage.

17. The system of claim 16, wherein the third transistor configured to interrupt the connection between the input signal and the first transistor input node includes:

coupling a third transistor input node to the second transistor input node;

coupling the input signal to a first NOR gate input node;

coupling a third transistor output node to a second NOR gate input node; and

coupling an NOR gate output node to the first transistor input node.

18. The system of claim 15, wherein the second interrupt device includes a fourth transistor having a fourth transistor threshold voltage of between 90 and 110 percent of a first transistor threshold voltage.

19. The system of claim 18, wherein the fourth transistor configured to interrupt the connection between the input signal and the second transistor input node includes:

coupling a fourth transistor input node to the first transistor input node;

coupling the input signal to a first AND gate input node;

coupling a fourth transistor output node to a second AND gate input node; and

coupling an AND gate output node to the second transistor input node.

20. The system of claim 18, wherein the first transistor threshold voltage is not equal to the second transistor threshold voltage.

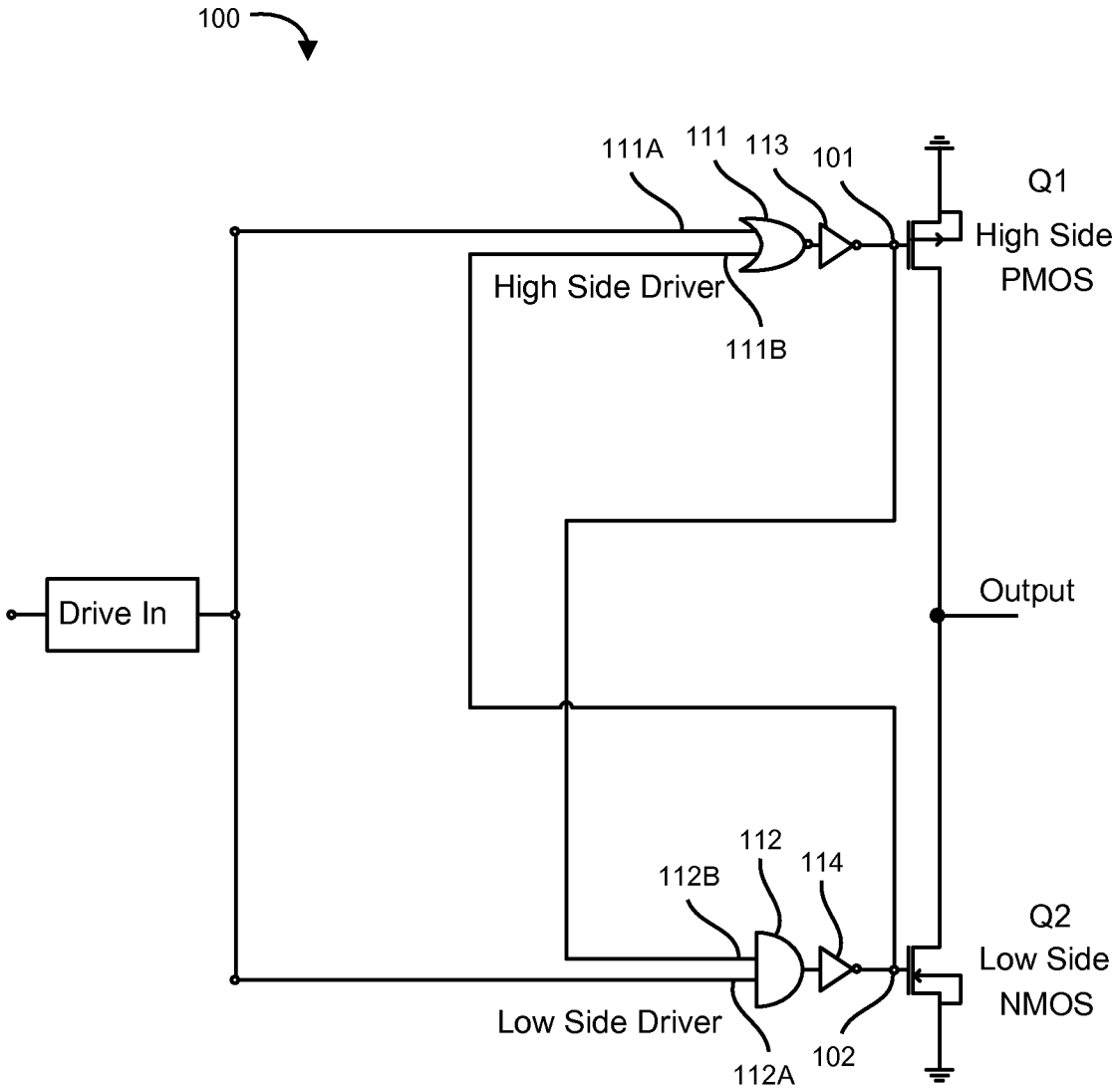

FIG. 1A
PRIOR ART

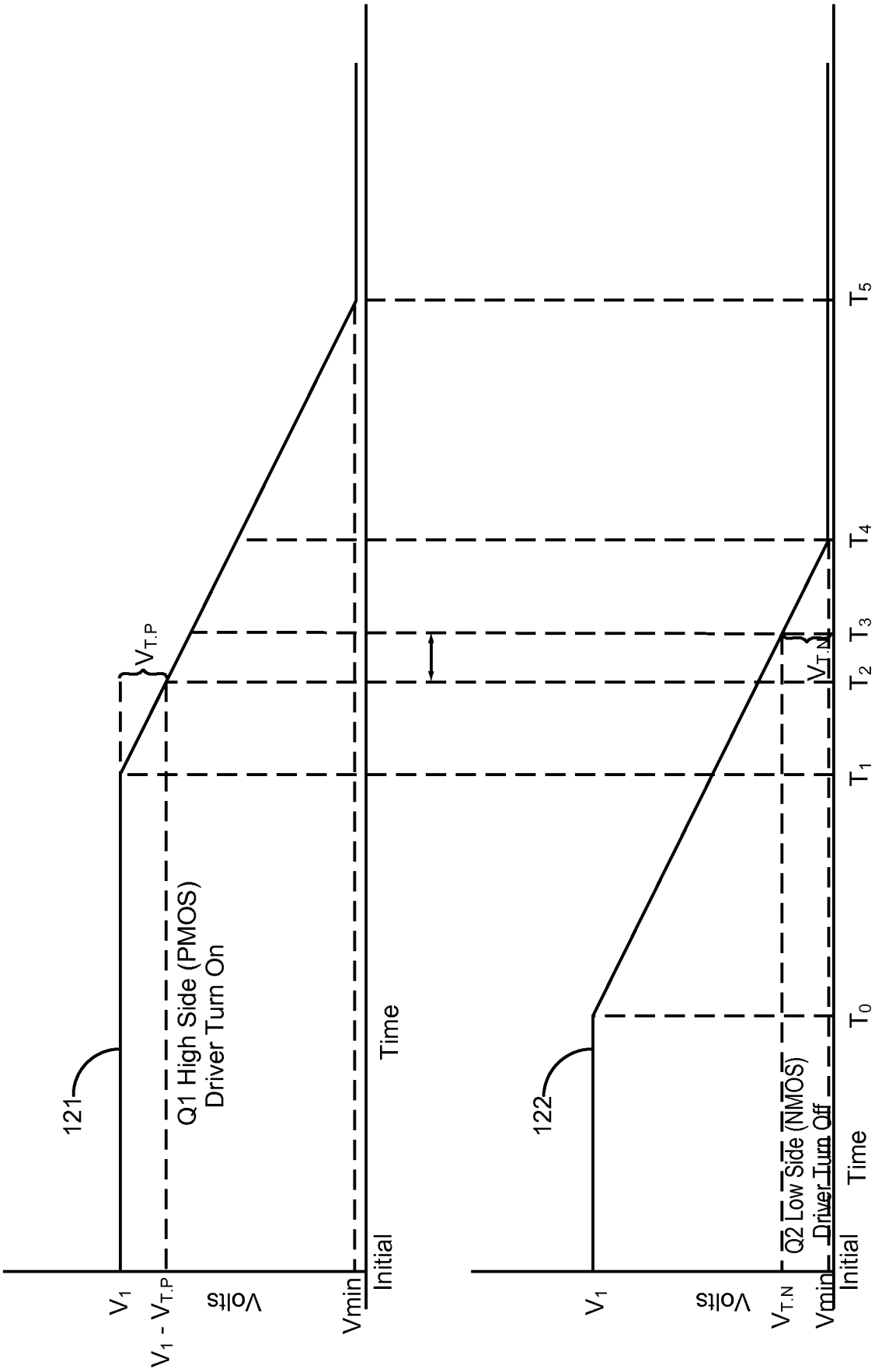

FIG. 1B
PRIOR ART

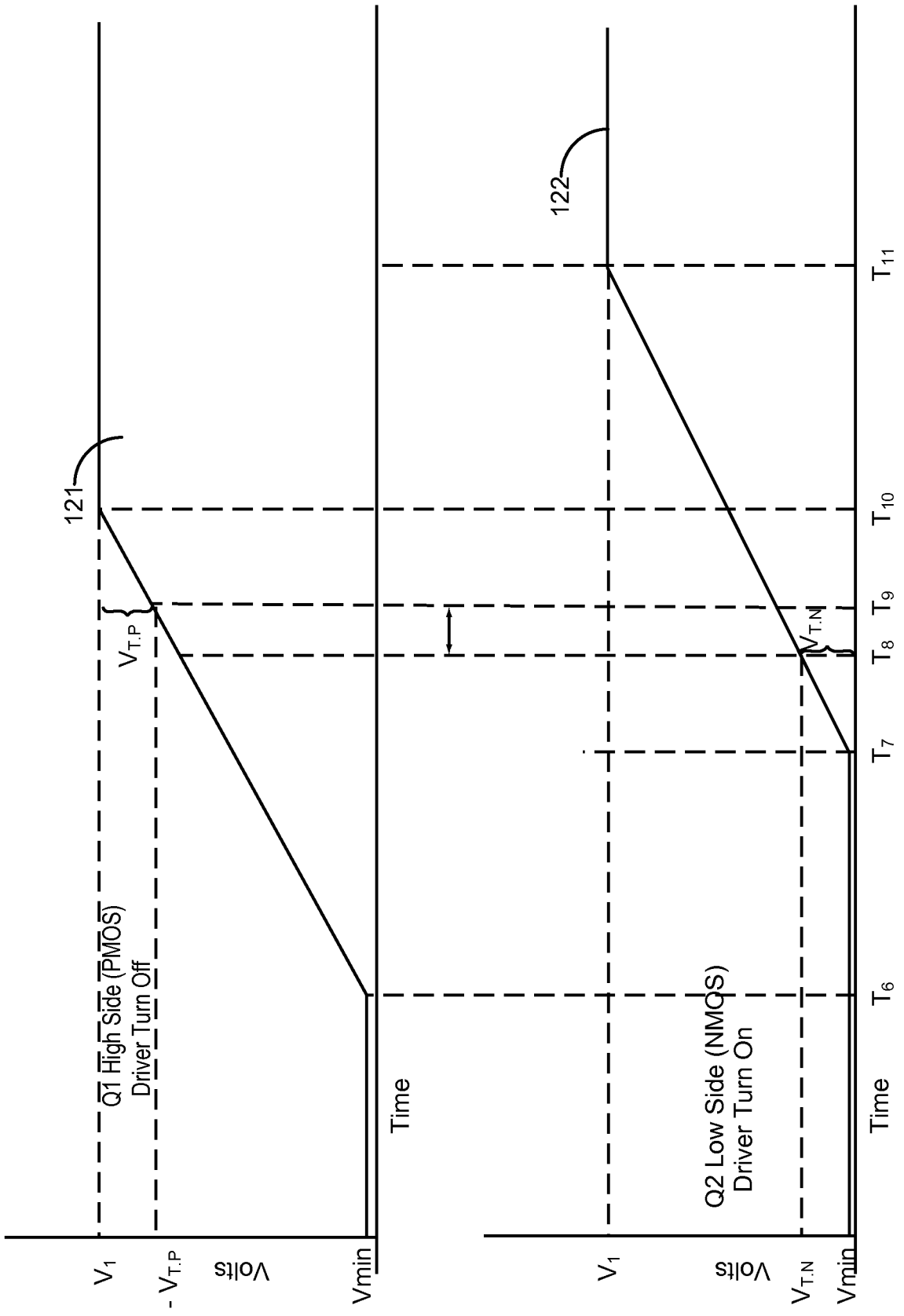

FIG. 1C
PRIOR ART

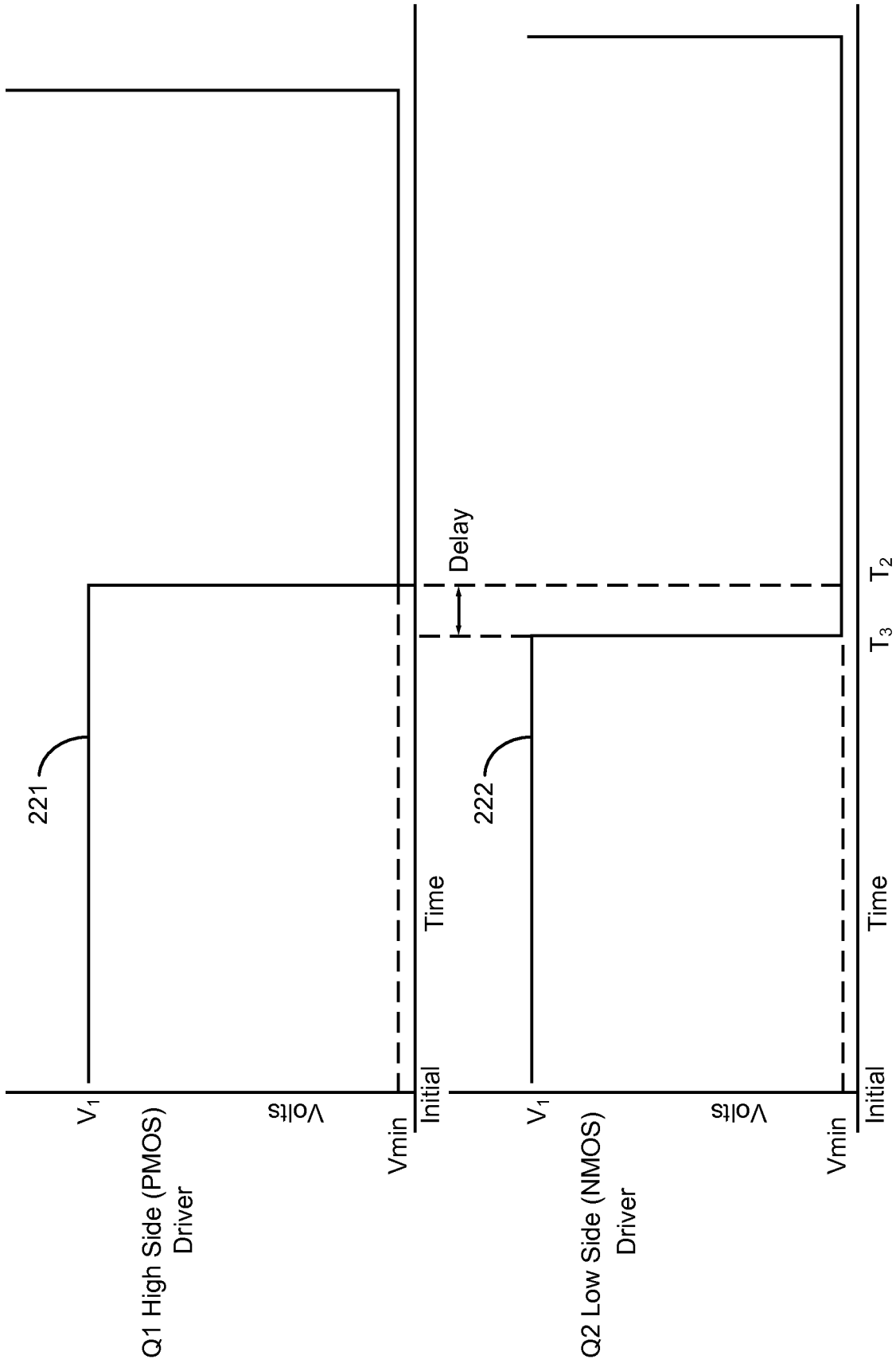
Q1 High Side (PMOS) Driver
Volts
V_1
Vmin
Initial
Time
221
Delay
Q2 Low Side (NMOS) Driver
Volts
V_1
Vmin
Initial
Time
222
T_3
T_2

FIG. 2A

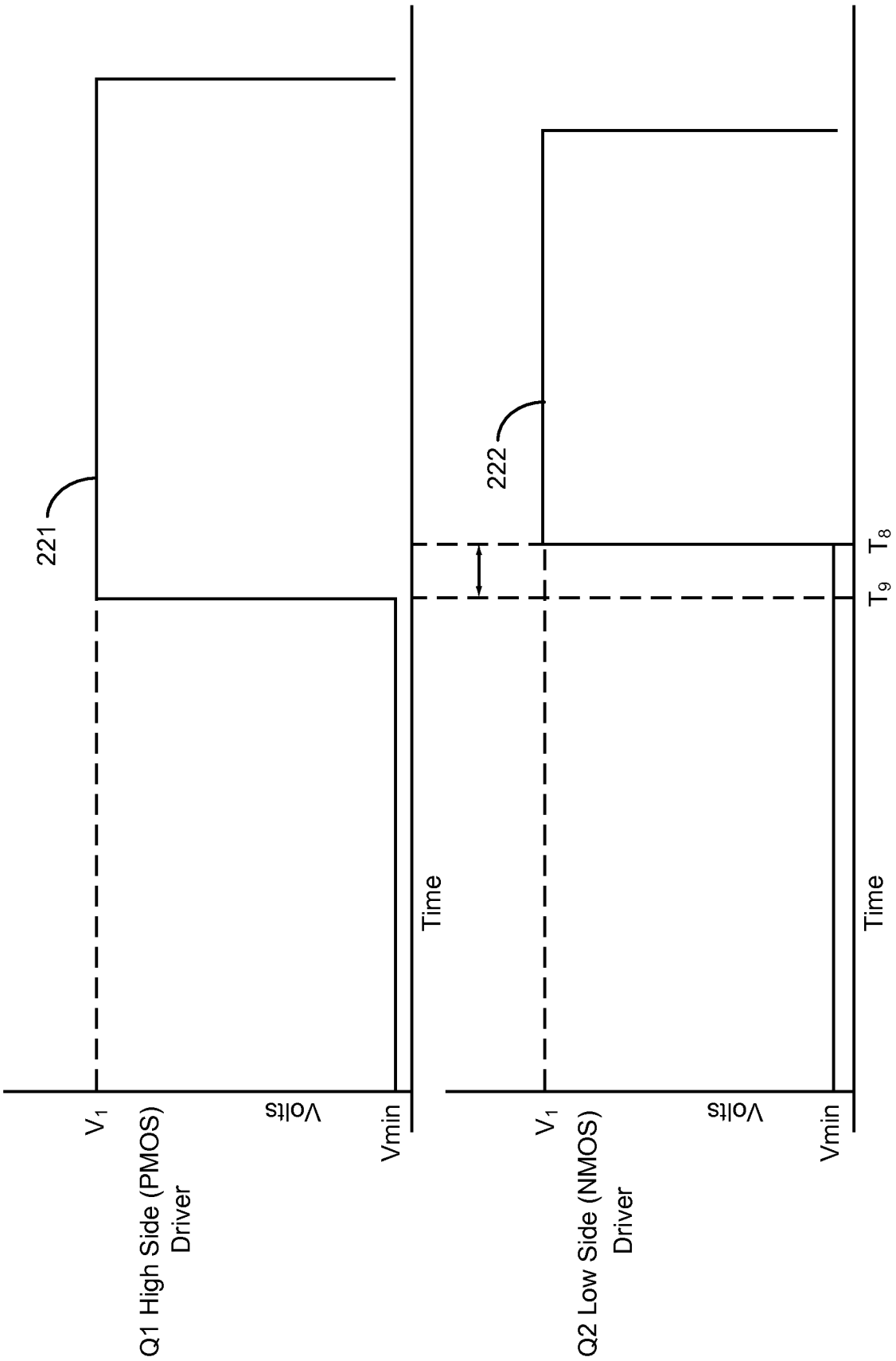
221
222
V_1
Volts
Vmin
Time
Q1 High Side (PMOS) Driver
V_1
Volts
Vmin
Time
Q2 Low Side (NMOS) Driver
T_8
T_9

FIG. 2B

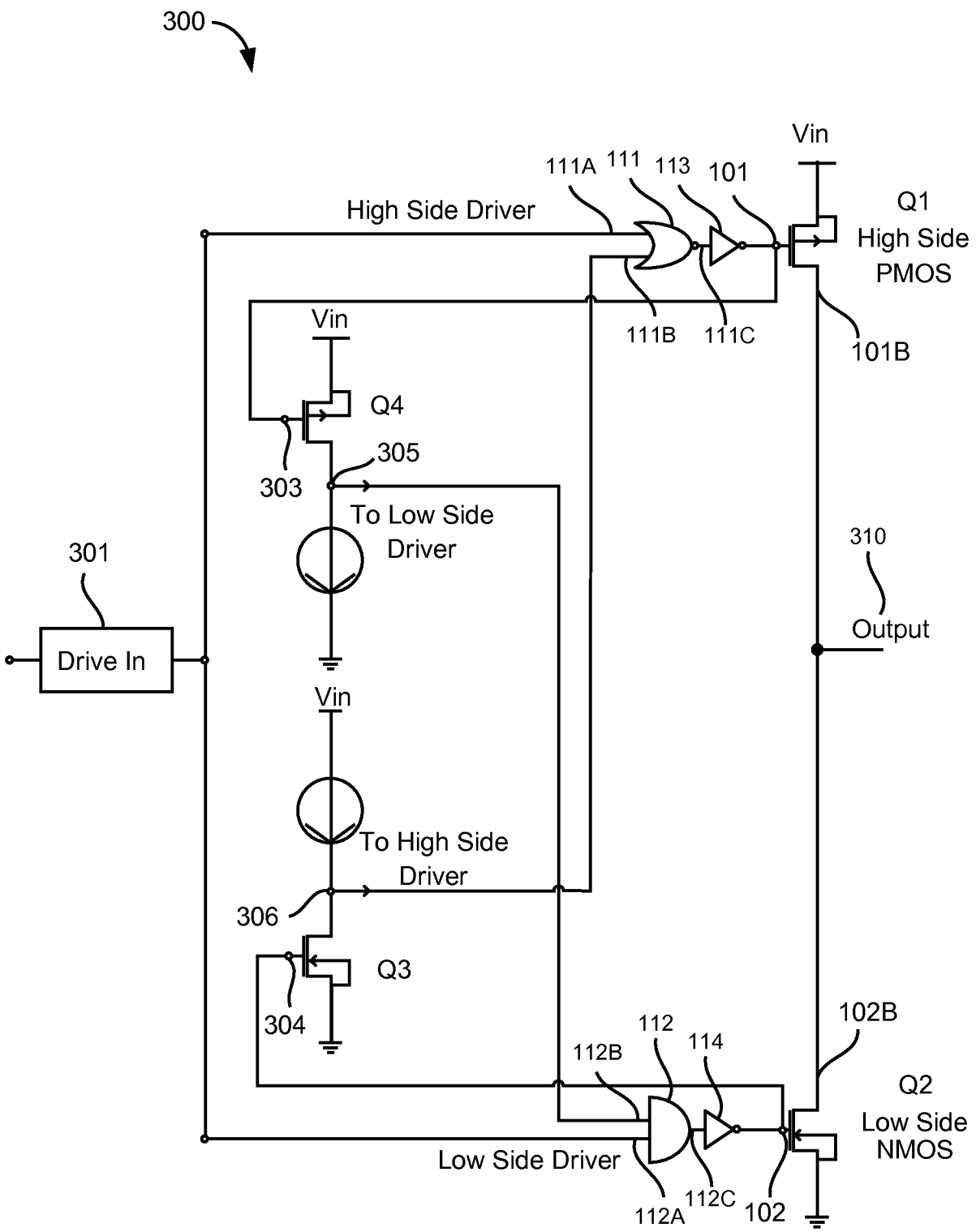
300
Vin
111A
111
113
101
High Side Driver
Q1
High Side
PMOS
Vin
111B
111C
101B
Q4
303
305
To Low Side
Driver
301
310
Drive In
Output
Vin
To High Side
Driver
306
Q3
304
102B
112
114
112B
Q2
Low Side
NMOS
Low Side Driver
112A
112C
102

FIG. 3

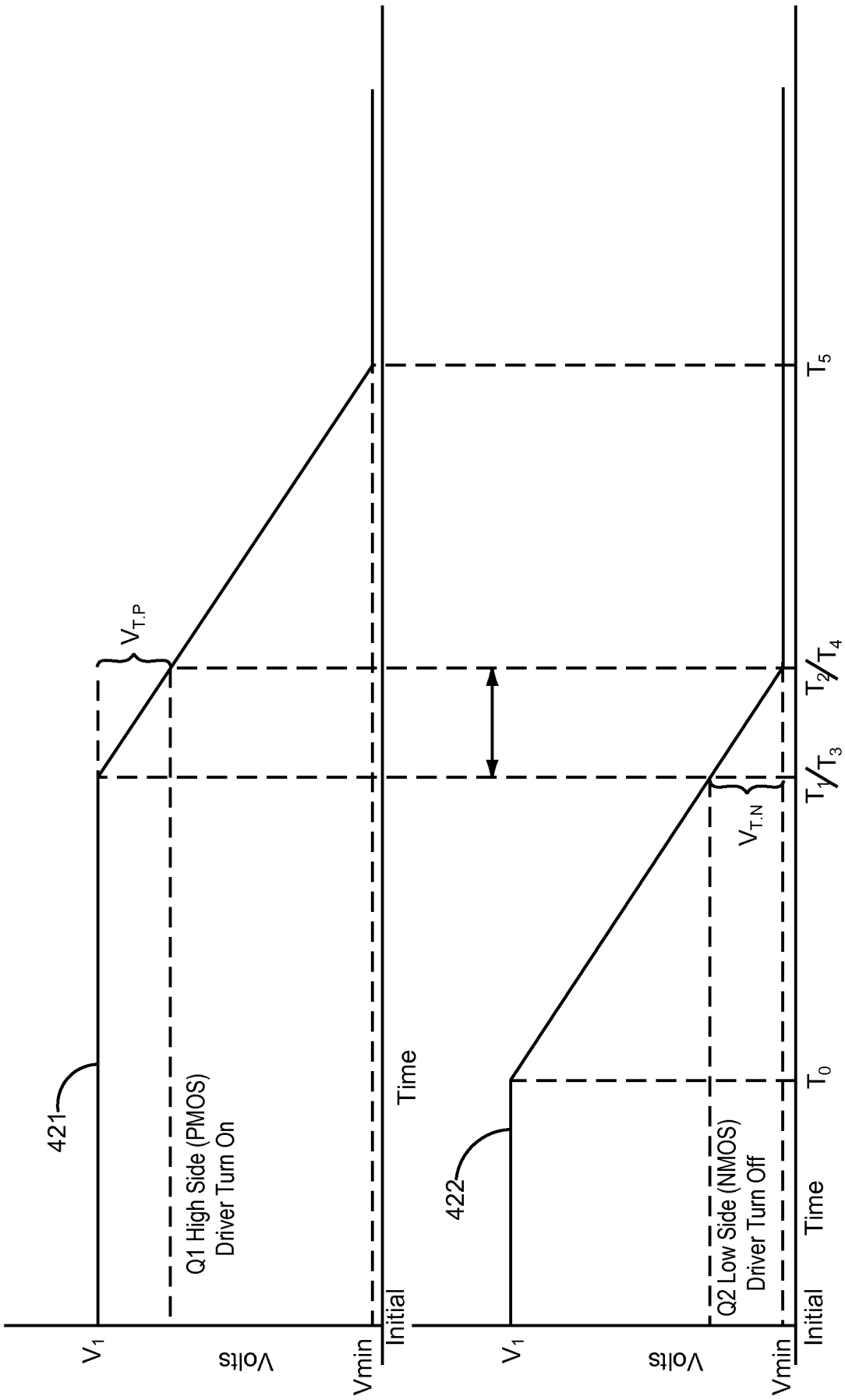
421
Q1 High Side (PMOS)
Driver Turn On
$V_{T.P}$
V_1
Volts
Vmin
Initial
Time
T_5
T_2/T_4
T_1/T_3
T_0
422
Q2 Low Side (NMOS)
Driver Turn Off
$V_{T.N}$
V_1
Volts
Vmin
Initial
Time

FIG. 4A

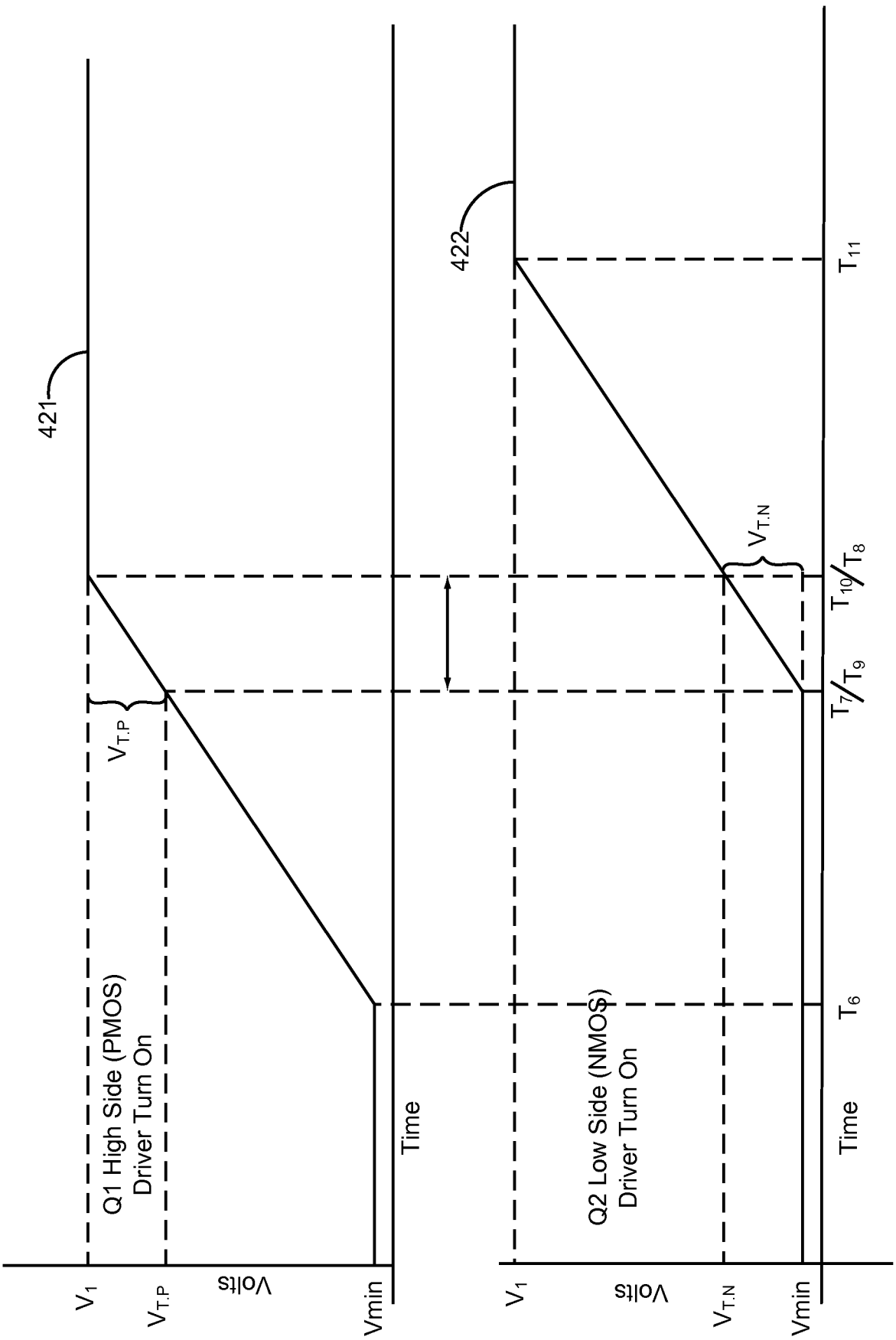
421
Q1 High Side (PMOS)
Driver Turn On
$V_{T.P}$
V_1
$V_{T.P}$
Volts
Vmin
Time
422
Q2 Low Side (NMOS)
Driver Turn On
$V_{T.N}$
V_1
$V_{T.N}$
Volts
Vmin
Time
T_6
T_7/T_9
T_{10}/T_8
T_{11}

FIG. 4B

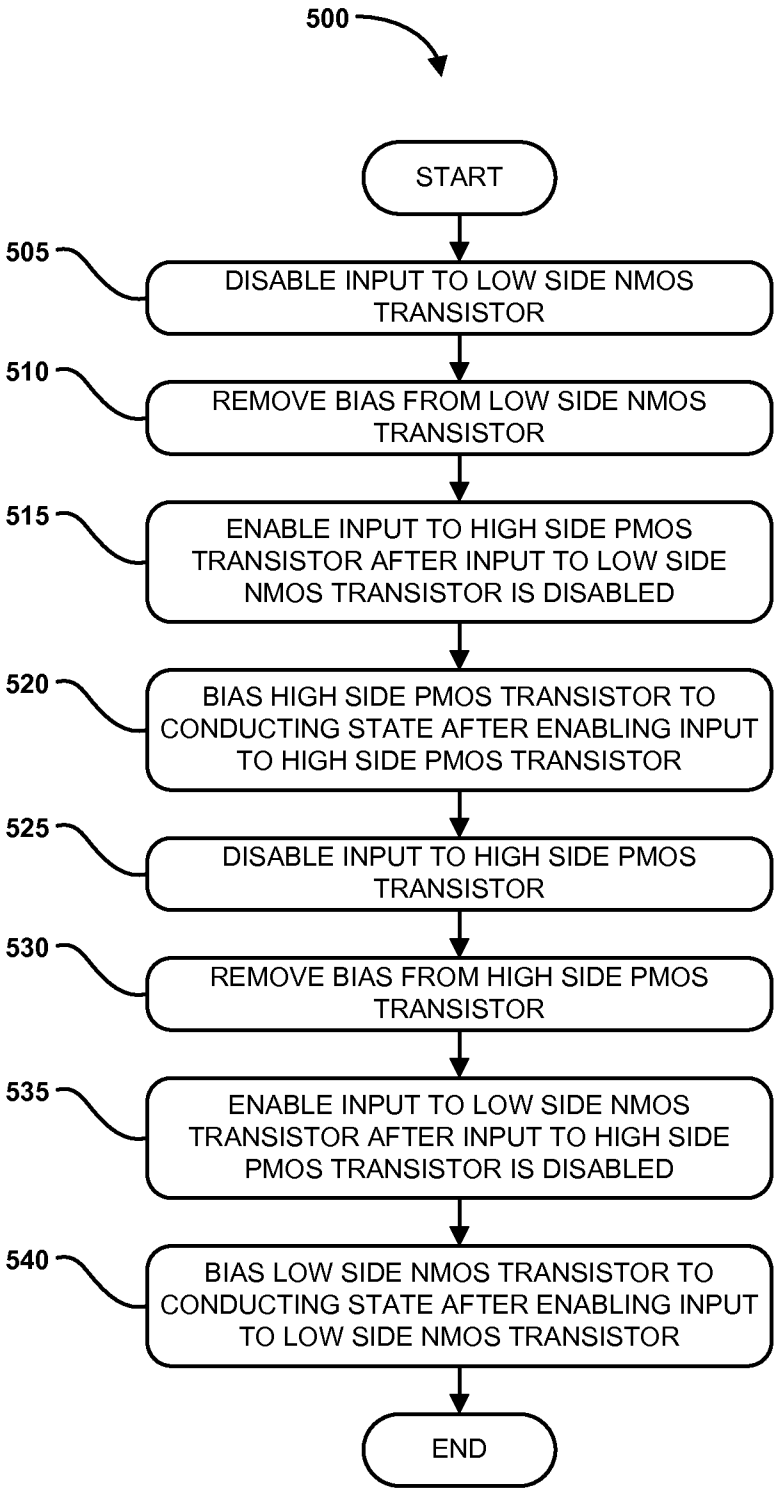
500
START
505
DISABLE INPUT TO LOW SIDE NMOS TRANSISTOR
510
REMOVE BIAS FROM LOW SIDE NMOS TRANSISTOR
515
ENABLE INPUT TO HIGH SIDE PMOS TRANSISTOR AFTER INPUT TO LOW SIDE NMOS TRANSISTOR IS DISABLED
520
BIAS HIGH SIDE PMOS TRANSISTOR TO CONDUCTING STATE AFTER ENABLING INPUT TO HIGH SIDE PMOS TRANSISTOR
525
DISABLE INPUT TO HIGH SIDE PMOS TRANSISTOR
530
REMOVE BIAS FROM HIGH SIDE PMOS TRANSISTOR
535
ENABLE INPUT TO LOW SIDE NMOS TRANSISTOR AFTER INPUT TO HIGH SIDE PMOS TRANSISTOR IS DISABLED
540
BIAS LOW SIDE NMOS TRANSISTOR TO CONDUCTING STATE AFTER ENABLING INPUT TO LOW SIDE NMOS TRANSISTOR
END

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/021170

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03K5/151 H02M1/38 H03K17/16 H03K19/003
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 930 132 A (WATANABE KAZUO [JP] ET AL) 27 July 1999 (1999-07-27) abstract; figures 1, 3, 4	1-20
X	US 2009/072864 A1 (HAGINO KOICHI [JP]) 19 March 2009 (2009-03-19) paragraphs [0051], [0052]; figures 1, 3, 4	1-20
X	US 2006/001459 A1 (AUDY JONATHAN M [US]) 5 January 2006 (2006-01-05) abstract; figures 1, 2	10,13-15
A	US 2010/085675 A1 (OKI HIROKAZU [JP]) 8 April 2010 (2010-04-08) abstract; figure 4	1-20

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 May 2015	03/06/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Loiseau, Ludovic

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/021170

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 463 854 A1 (NEC CORP [JP]) 2 January 1992 (1992-01-02) abstract; figure 1 -----	1-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2015/021170

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