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(54) **Title**: FLOATING-BODY/GATE DRAM CELL

(57) **Abstract**: Memory cell structures and biasing schemes are provided. Certain embodiments pertain to a modified floating-body gate cell, which can provide improved retention times. In one embodiment, a gated diode is used to drive the gate of a second transistor structure of a cell. In another embodiment, a body-tied-source (BTS) field effect transistor is used to drive the gate of the second transistor structure of a cell.

DESCRIPTION

FLOATING-BODY/GATE DRAM CELL

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application claims the benefit of U.S. Provisional Application Serial No. 61/144,289, filed January 13, 2009, which is hereby incorporated by reference in its entirety. The present application is also a continuation-in-part of International Application Serial No. PCT/US2008/078460, filed October 1, 2008, which claims the benefit of U.S. Provisional Application Serial No. 60/976,691, filed October 1, 2007, and U.S. Provisional Application Serial No. 61/017,941, filed December 31, 2007, which are hereby incorporated by reference in their entirety, including any figures, tables, or drawings.

BACKGROUND OF THE INVENTION

A conventional dynamic random access memory (DRAM) cell uses a stack capacitor or a deep-trench capacitor for storage, which is leading to prohibitive processing complexity as the memory technology is scaled. Accordingly, study and development of "capacitorless" one-transistor (1T) DRAM cells that utilize the floating body of a silicon-on-insulator (SOI) metal oxide semiconductor field effect transistor (MOSFET) as the storage element have intensified, mainly for complementary metal oxide semiconductor (CMOS) embedded-memory applications. In such 1T floating-body cells (FBCs), charging and discharging the MOSFET body define the memory states, and the stored data are sensed via a difference, or signal margin, in the channel current (ΔI_{DS}) corresponding to the threshold-voltage variation (ΔV_t) that results from the body charging/discharging, i.e., from the varying body-source junction voltage (V_{BS}). The widespread FBC studies, which began with partially depleted (PD) SOI MOSFETs, have recently focused on fully depleted (FD) devices, including planar FD/SOI MOSFETs and FD double-gate (DG) FinFETs to avoid body-doping issues and to render the FBC more scalable with the CMOS. The FD devices require a substrate, or back-gate bias to create an accumulation layer that emulates the PD body, and enables effective charge storage and data sensing.

While FinFET CMOS technology could enable scaling of the 1T FBC to gate lengths (L_g) less than 10 nm, there are other issues that tend to inhibit mainstream adaptation of the 1T FBC utilizing FinFET technology. In particular, the 1T FBC utilizing FinFET technology relies on current sensing of the stored data, which can be less desirable than conventional voltage sensing because of more sophisticated sense amplifiers and added power consumption. The 1T FBC utilizing FinFET technology requires the noted bias-induced accumulation, which can complicate the cell/chip design, undermine reliability, and sacrifice layout area. In addition, because the attainable ΔV_t is fundamentally limited, several paralleled fins are needed to increase the device effective width and current to get acceptable ΔI_{DS}, thus severely undermining the memory density actually achievable. For example, in the paper "Retention characteristics of zero-capacitor RAM (Z-RAM) cell based on FinFET and tri-gate devices," by Nagoda *et al.*, with the SOI substrate biased at -30 V to get the needed accumulation, 10 fins yielded a current margin of less that 10 μA from an L_g = 100 nm composite n-channel double gate (DG) FinFET.

Thus, there exists a need in the art for a scalable memory.

BRIEF SUMMARY

Embodiments of the present invention relate to memory devices. In accordance with an embodiment, a memory cell structure and biasing scheme is provided.

A memory cell structure is provided that can include a simplified two-transistor memory cell structure where the body of the first transistor is connected to the gate of the second transistor. In a specific embodiment, the first transistor is simplified as a p+-intrinsic-n+ (PIN) gated diode for ease of connection of the body of the first transistor to the gate of the second transistor, which can be a metal oxide semiconductor field effect transistor (MOSFET). In a specific embodiment, the gate of the 'first transistor' can be fabricated to include an overlap between the gate and the 'source' of the 'first transistor' (P-region of the PIN gated diode). In a further embodiment, the gate of the 'first transistor' can be fabricated to include an underlap between the gate and the 'drain' of the 'first transistor' (N-region of the PIN gated diode).

In accordance with embodiments of the present invention, a biasing scheme is provided that induces a channel between the 'source' and 'drain' of the 'first transistor.' Here, retention time of the memory cell can be resolved by effectively connecting the N-region of the gated diode to the P-region of the gated diode in order to create an interface for tunneling and charging.

According to a variety of implementations, a word line can be used to control the inversion of the channel region of the 'first transistor.'

In one embodiment, a biasing scheme is provided for the subject memory cell where a word line is connected to the gate of the 'first transistor,' a first bit line is connected to the 'drain' of the 'first transistor' (N-region of the PIN gated diode), a second bit line is connected to the drain of the second transistor, and a ground line is connected to the source of the second transistor. The first bit line can be used for writing to the memory cell, and the second bit line can be used for reading from the memory cell. According to an embodiment, a positive bias can be applied through the first bit line to charge the floating body of the 'first transistor' that is tied to the gate of the second transistor. In addition, a positive bias can be applied through the word line and a negative bias can be applied through the first bit line to discharge the floating body of the 'first transistor' that is tied to the gate of the second transistor. The read operation can be performed through the second bit line by raising the voltage of the floating body of the 'first transistor' that is tied to the gate of the second transistor without adversely disturbing the memory state of the cell.

In another embodiment, a biasing scheme is provided for the subject memory cell where a word line is connected to the gate of the 'first transistor,' a bit line is connected to the 'drain' of the 'first transistor' (N-region of the PIN gated diode) and the drain of the second transistor, and a ground line is connected to the source of the second transistor. The bit line can be used for writing to and reading from the memory cell. According to an embodiment, a positive bias can be applied through the bit line to charge the floating body of the 'first transistor' that is tied to the gate of the second transistor. In addition, a positive bias can be applied through the word line and a negative bias can be applied through the bit line to discharge the floating body of the 'first transistor' that is tied to the gate of the second transistor. The read operation can be performed by raising the voltage of the floating body of the 'first transistor' that is tied to the gate of the second transistor without adversely disturbing the memory state of the cell.

According to yet another embodiment, a memory cell structure is provided that includes a two-transistor memory cell structure where the body and the source of the first transistor are tied together and connected to the gate of the second transistor. According to one such embodiment, the first transistor having its body tied to its source charges is able to charge and discharge the gate of the second transistor for write '1' and write '0', via channel current.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a representation of a memory cell with two bit lines according to an embodiment of the present invention.

Figures 2A and 2B show plots of a transient sequential memory operation of a memory cell of the embodiment shown in Figure 1, predicted by a 2-D mixed-mode numerical simulation using SenTaurus using parameters of an FD/SOI-based structure with Lg = 28nm, tox = 2nm, tSi = 14nm, tbox = 50nm, gate-source overlap=5nm, gate-drain underlap=30nm, undoped thin bodies, and midgap work function (TiN) gates.

Figures 3A and 3B show band diagrams. Figure 3A is a band diagram of a charging operation in accordance with an embodiment of the present invention; and Figure 3B is a band diagram of a discharging operation in accordance with an embodiment of the present invention.

Figure 4 shows a representation of a memory cell with a single bit line according to an embodiment of the present invention.

Figures 5A and 5B show plots of a transient sequential memory operation of a memory cell of the embodiment shown in Figure 4, predicted by a 2-D mixed-mode numerical simulation using SenTaurus using parameters of an FD/SOI-based structure with Lg = 28nm, tox = 2nm, tSi = 14nm, tbox = 50nm, gate-source overlap=5nm, gate-drain underlap=30nm, undoped thin bodies, and midgap work function (TiN) gates.

Figure 6 shows a plot of data retention characteristics of the device of Figure 1, predicted by a 2-D mixed-mode numerical simulation using SenTaurus using parameters of an FD/SOI-based structure with Lg = 28nm, tox = 2nm, tSi = 14nm, tbox = 50nm, gate-source overlap=5nm, gate-drain underlap=30nm, undoped thin bodies, and midgap work function (TiN) gates.

Figure 7 shows a circuit diagram of a memory cell with two bit lines according to another embodiment of the present invention.

Figures 8A and 8B shows a representation of a memory cell with two bit lines according to an embodiment of the circuit of Figure 7. Figure 8A shows a plan view of a portion of the memory cell in accordance with one embodiment; and Figure 8B shows a schematic representation of the memory cell in accordance with an embodiment of the present invention.

Figures 9A and 9B show plots of a transient sequential memory operation of a memory cell of the embodiment shown in Figure 8B, predicted by a physics-based compact model UFPDB (ver. 2.5) in Spice3 using parameters of a 90nm PD/SOI nMOSFET based structure with Lg = 90nm, tox = 2nm, tSi = 120nm, n+ poly gates, Vt = 0.4V, BL2 bias = 0.2V.

DETAILED DISCLOSURE

Embodiments of the present invention relate to memory devices. In accordance with an embodiment, a memory cell structure and biasing scheme is provided.

Embodiments of the subject technology provide a modified two-transistor floating-body cell for DRAM applications. Embodiments of the present invention can be applicable to any SOI (silicon-on-insulator) technology. In addition, certain embodiments of the present invention are applicable to bulk silicon technology. The two transistors of the modified two-transistor floating-body cell can be fabricated via planar processing, or via 3-D integration with one transistor “stacked” on top of the other. Although preferred embodiments of the present invention utilize n-type transistor structures (such as nFinFET), embodiments of the present invention can also utilize p-type transistor structures but may require a larger cell area.

Figure 1 shows a schematic representation of an embodiment of a memory cell structure. Referring to Figure 1, a modified floating-body/gate cell (FBGC) is shown that can be fabricated on SOI for a DRAM array with two bit lines. Here, the first ‘transistor’ **T1** is provided as a gated diode, where the transistor source is made the same conductive type as the body of **T1** (e.g., p-type for an n-channel transistor structure). Thus, the ‘source’ of **T1** can be connected to the gate of the second transistor **T2**. A distinguishing feature of this simplified cell is the p+ region of **T1**. In accordance with implementations of the present invention, **T1** can be a p+-intrinsic-n+ (PIN) gated diode, where the intrinsic portion can be a region that is not intentionally doped. For example, the intrinsic portion can, in practice, be a p- region. The p+ “source” enables an easy, direct connection of the **T1** body to the gate of the **T2** MOSFET as indicated in Figure 1.

For the configuration shown in Figure 1, a word line **WL** can be applied to the gate of **T1**, a first bit line **BL** can be applied to the ‘drain’ of **T1**, a second bit line can be applied to the drain of **T2**, and the source of **T2** can be tied to ground.

According to an embodiment of the present invention, **T1** can be designed with underlap at its ‘drain’ and overlap at its ‘source.’ Advantageously, alignment of the gate is not as restrictive compared to the alignment required for a conventional transistor structure.

In certain embodiments, the offset created by the underlap at the 'drain' and overlap at the 'source' can provide improved performance of the cell.

A biasing scheme and memory cell operation will now be described with reference to Figures 1 and 2A. According to an embodiment, by inverting the channel of **T1** and applying a positive bias at the drain of **T1** through **BL1**, the tunneling current between the inversion layer and the "p+ source" can be utilized to charge the **B1/G2** node. That is, an n+ channel can be induced between the n+ region at the 'drain' and the p+ region at the 'source' by application of a positive bias through the word line **WL**. The induced inversion of the channel of **T1** can effectively connect the n+ region to the p+ region, thereby creating an interface for tunneling and charging. That interface provides a location for tunneling current to charge the **B1/G2** node.

To discharge **B1/G2**, a forward-biased body (**B1/G2**) – to - **BL1** PN junction is realized by applying a positive bias to the gate of **T1** through **WL** and a negative bias to **BL1**. A read operation can be performed by raising the **B1/G2** voltage without disturbing the memory state and sensing the current, or voltage, of **T2**.

As shown in Figures 2A and 2B, a predicted operation sequence illustrates the effects of the described biasing scheme. In the plots, a constant voltage of 0.2V is applied to the second bit line **BL2** to sense the current difference between a '1' state and a '0' state. Referring to Figure 2B, it can seen that the signal margin between the '1' state and the '0' state is about 70 μA/μm.

To better understand embodiments of the subject biasing scheme, the band diagram for charging is shown in Figure 3A and the band diagram for discharging is shown in Figure 3B. Referring to Figure 3A, electrons can tunnel from the valence band of "p+ source" region to the conduction band of the n+ channel/drain region. The application of particular **WL** and **BL1** voltages can modulate the tunnel width and the available density of states. Due to the very small storage capacitance with the modified FBGC, the sub-1ns write '1' time might be reached by carefully tuning the drain (using **BL1**) and gate (using **WL**) biases. Referring to Figure 3B, the discharging current is the forward-biased PN junction current.

Referring back to Figure 2A, it can be seen that the same **WL** voltage can be used for both write '1' and write '0' as is done in the conventional 1T/1C DRAM.

Figure 4 shows a schematic representation of another embodiment of a memory cell structure. Referring to Figure 4, a modified floating-body/gate cell (FBGC) is shown that can be fabricated on SOI for a DRAM array with one bit line. Here, the first 'transistor' **T1** is provided as a gated diode, where the transistor source is made the same conductive type as the body of **T1** (e.g., p-type for an n-channel transistor structure). Thus, the 'source' of **T1** can be connected to the gate of the second transistor **T2**. A distinguishing feature of this simplified cell is the p+ region of **T1**. In accordance with implementations of the present invention, **T1** can be a p+-intrinsic-n+ (PIN) gated diode where the intrinsic portion is a region that is not intentionally doped. The p+ "source" enables an easy, direct connection of the **T1** body to the gate of the **T2** MOSFET as indicated in Figure 4. Again, similarly to the embodiment shown in Figure 1, **T1** can be designed with underlap at its 'drain' and overlap at its 'source.'

For the configuration shown in Figure 4, a word line **WL** can be applied to the gate of **T1**, a single bit line **BL** can be applied to the 'drain' of **T1** and the drain of **T2**, and the source of **T2** can be tied to ground.

A biasing scheme and memory cell operation will now be described with reference to Figure 4. According to an embodiment, by inverting the channel of **T1** and applying a positive bias at the drain of **T1** through **BL**, the tunneling current between the inversion layer and the "p+ source" can be utilized to charge the **B1/G2** node. To discharge **B1/G2**, a forward-biased body (**B1/G2**) – to - **BL** PN junction is realized by applying a positive bias to the gate of **T1** through **WL** and a negative bias to **BL**. A read operation can be performed by raising the **B1/G2** voltage without disturbing the memory state and sensing the current, or voltage, of **T2**.

Figure 5A shows the SenTaurus-predicted operation sequence waveforms for one implementation of this biasing scheme with **BL1** and **BL2** tied together (i.e., single bit line). Referring to Figure 5B, it can seen that the signal margin between the '1' state and the '0' state is about 25 μA/μm. Hence, the memory cell of the modified FBGC according to embodiments of the present invention can work using one WL and one BL, which is similar to the conventional 1T/1C DRAM.

Based on the functionality verification transient simulations, the retention time with disturbs are predicted by SenTaurus. The simulations are performed with the designed **T1** gate-drain underlap. Advantageously, the gate-drain underlap can effectively reduce the unwanted GIDL current in '0' state holding under **BL** disturb. By designing with the example 30 nm gate-drain underlap at the drain side of **T1**, ultra long (~10s) retention time with enough sense margin (ΔV_{BS}=0.2V) is achieved, as shown in Figure 6. For these simulations, the operation voltages for write and read are the same as in Figure 2A. It should be noted that the simulations were conducted with the 30 nm gate-drain underlap, but embodiments of the present invention are not limited thereto.

Another embodiment of the subject technology provides a two-transistor floating-body cell for DRAM applications utilizing a body-tied-to-source (BTS) structure. Embodiments of the present invention can be applicable to any SOI (silicon-on-insulator) technology. In addition, certain embodiments of the present invention are applicable to bulk silicon technology. The two transistors of the two-transistor floating-body cell can be fabricated via planar processing, or via 3-D integration with one transistor “stacked” on top of the other. Although preferred embodiments of the present invention utilize n-type transistor structures (such as nMOSFET), embodiments of the present invention can also utilize p-type transistor structures but may require a larger cell area.

Embodiments of the can yield ultra-short (i.e., fast) write times, as well as good memory performance (i.e., large signal margin and low operating power) and very long charge-data retention times under worst-case conditions. Further, low-voltage operation is enabled, thereby providing good cell reliability.

Figure 7 shows a circuit representation and Figures 8A and 8B show a schematic representation of an embodiment of a memory cell structure. Referring to Figures 7, 8A, and 8B, a floating-body/gate cell utilizing a body-tied-to-source (BTS) structure (BTS-FBGC) is shown that can be fabricated on SOI for a DRAM array with two bit lines. Here, the first transistor **T1** is configured as a BTS MOSFET, where its body **B1** and source **S1** are tied together. The **B1/S2** of **T1** is connected to the gate **G2** of the second transistor **T2**.

For the configuration shown in Figures 7 and 8B, a word line **WL** can be applied to the gate of **T1**, a first bit line **BL** can be applied to the drain of **T1**, a second bit line can be applied to the drain of **T2**, and the source of **T2** can be tied to ground.

As shown in Figure 8A, in one embodiment, the body **B1** of **T1** can be connected to the gate **G2** of **T2** by using an extended p-type region in a portion of the source region of **T1**. That is, similarly to the modified FBGC of Figure 1, a p+ “source” region of **T1** can be connected to the gate **G2** of the second transistor **T2**. The p+ “source” enables an easy, direct connection of the **T1** body to the gate of the **T2** MOSFET as indicated in Figure 8A.

According to an embodiment of the present invention, **T1** can be designed with underlap at its source and drain, such as shown in Figures 8A and 8B. Advantageously, alignment of the gate is not as restrictive compared to the alignment required for a conventional transistor structure. In certain embodiments, the offset created by the underlap at the source and drain can provide improved performance of the cell. The gate-source/drain underlap can be used to suppress GIDL for hold '0'.

A biasing scheme and memory cell operation will now be described with reference to Figures 8B and 9A. According to an embodiment, the BTS-FBGC design enables **T1** to charge and discharge **G2**, for write '1' and write '0', via channel current. For hold '1', the **G2** charge is transferred, via fast diffusion, to **B1** for storage on the gate capacitance of **T1**, biased in accumulation. The BTS structure of **T1** enables the movement of charge from **G2** to **B1**. Therefore, it is not necessary to leave charge on **G2** for hold (emulating the conventional 1T/1C DRAM cell with the capacitor replaced by the gate of **T2**), which would not be viable for small charges. This transfer of the stored charge to **B1** for hold '1' also avoids a false read operation without having to add a read access transistor to the cell. In particular, the body/source of **T1** drives the gate of **T2** for reading data without significantly affecting the stored charge in **T1**.

As shown in Figures 9A and 9B, a predicted operation sequence illustrates the effects of the described biasing scheme. The BTS-FBGC design enables **T1** to charge and discharge **G2**, for write '1' and write '0', via channel current, which can yield ultra-fast write times (~10ps) at low **WL** and **BL1** voltages. After writing a '1', the stored charge is moved to **B1** for holding '1' by dropping the **WL** voltage negative, which removes the **T1** channel and creates an accumulation condition for storing the charge.

In the plots, a constant voltage of 0.2V is applied to the second bit line **BL2**. The fixed voltage to **BL2** causes the **BL2** current during write '1'; this current would be effectively eliminated via **BL2** pulsing in actual memory operation, thereby yielding very low overall dynamic power. Referring to Figure 9B, it can seen that the signal margin between the '1' state and the '0' state is about 30 μA/μm. Further, the inclusion of the underlap of the gate to the source and drain of T1 can provide long retention times. These long retention times can be further lengthened by using the enabled low operational voltages.

Although the simulations for the BTS-FBGC are demonstrated using PD/SOI (partially depleted) MOSFETs, FD/SOI may be used as well, including FinFETs.

Advantageously, the BTS-FBGC enables use of a MOSFET in lieu of the capacitor in conventional DRAM. Further, memory operation can be accomplished using small stored charge because the charge in the body **B1** of **T1** is used to drive **T2** for reading data without being significantly expended.

All patents, patent applications, provisional applications, and publications referred to or cited herein are incorporated by reference in their entirety, including all figures and tables, to the extent they are not inconsistent with the explicit teachings of this specification.

It should be understood that the examples and embodiments described herein are for illustrative purposes only and that various modifications or changes in light thereof will be suggested to persons skilled in the art and are to be included within the spirit and purview of this application. In addition, any elements or limitations of any invention or embodiment thereof disclosed herein can be combined with any and/or all other elements or limitations (individually or in any combination) or any other invention or embodiment thereof disclosed herein, and all such combinations are contemplated with the scope of the invention without limitation thereto.

CLAIMS

We claim:

1. A memory comprising:

a gated diode comprising a first region of a first conductive type, a second region of a second conductive type, and a first gate electrode; and

a transistor comprising a source region of the second conductive type, a drain region of the second conductive type, and a second gate electrode, wherein the first region of the gated diode is connected to the second gate electrode of the transistor, and wherein the first gate electrode of the gated diode is connected to a word line such that a channel of the second conductive type is induced below the first gate electrode during a write operation of the memory.

2. The memory according to claim 1, wherein the gated diode further comprises a third region of the first conductive type disposed between the first region and the second region.

3. The memory according to claim 2, wherein the first region of the gated diode comprises a high concentration of first conductive type dopants and the third region of the gated diode comprises a low concentration of first conductive type dopants to provide a PIN structure.

4. The memory according to claim 2, wherein the first gate electrode of the gated diode is disposed such that a portion of the first gate electrode overlaps the first region.

5. The memory according to claim 2, wherein the first gate electrode of the gated diode is disposed to underlap the third region, such that a portion of the third region adjacent the second region extends a distance from an edge of the first gate electrode to cause the second region to be spaced apart from the edge of the first gate electrode.

6. The memory according to claim 5, wherein the first gate electrode of the gated diode is further disposed such that a portion of the first gate electrode overlaps the first region.

7. The memory according to claim 1, wherein the gated diode and the transistor are formed on a silicon-on-insulator substrate.

8. The memory according to claim 1, wherein the second region of the gated diode is connected to a first bit line; and wherein the drain of the transistor is connected to a second bit line and the source of the transistor is connected to a ground line.

9. The memory according to claim 1, wherein the second region of the gated diode and the drain of the transistor are connected to a same bit line.

10. A memory comprising:

a first transistor structure having a first gate, a first drain connected to a first bit line, a first source, and a first body, wherein the first source is tied to the first body; and

a second transistor structure having a second gate coupled to the first body that is tied to the first source, a second source connected to a ground, and a second drain connected to a second bit line.

11. The memory according to claim 10, wherein the first gate is connected to a word line such that the first transistor structure charges and discharges the second gate by using channel current of the first transistor structure.

12. A memory cell, comprising:

a first gate electrode on a gate insulating layer on a p- type region of a substrate, the first gate electrode being connected to a word line;

a first n+ drain region at one side of the p-type region in the substrate, the first n+ drain region being connected to a first bit line;

a first n+ source region in the substrate at an opposite side of the p-type region from the first n+ drain region;

a p+ region extending from the p-type region at the opposite side of the p-type region adjacent the first n+ source region, the p+ region providing a contact region for electrical connection to the p-type region;

a second gate electrode on a second gate insulating layer, wherein the n+ source region and the p+ region are tied together and connected to the second gate electrode;

a second n+ drain region at a side of the gate electrode, the second n+ drain region being connected to a second bit line; and

a second n+ source region at another side of the gate electrode, the second n+ source region being connected to a ground.

13. The memory cell according to claim 12, wherein the first gate electrode is disposed having an underlap with at least one of the first n+ drain region and the first n+ source region.

14. A method of controlling a memory comprising a gated diode comprising a first region of a first conductive type, a second region of a second conductive type, and a first gate electrode, and a transistor comprising a source region of the second conductive type, a drain region of the second conductive type, and a second gate electrode, wherein the first region of the gated diode is connected to the second gate electrode of the transistor at a body-gate node, and wherein the first gate electrode of the gated diode is connected to a word line, the method comprising:

applying a first positive bias to the second region of the gated diode through a first bit line and applying a second positive bias to the word line in order to charge the body-gate node during a write operation of a '1';

applying a negative bias to the second region of the gated diode through the first bit line and applying a third positive bias to the word line in order to discharge the body gate node during a write operation of a '0'; and

using a second bit line connected to the drain of the transistor in order to perform a read operation.

15. The method according to claim 14, wherein the second positive bias is substantially the same as the third positive bias.

16. The method according to claim 14, wherein the first positive bias is smaller than the second positive bias.

17. The method according to claim 14, wherein the first bit line and the second bit line are tied together.

18. A method of controlling a memory cell comprising a gated diode and a first transistor, wherein the gated diode has a first conductive type region connected to a gate of the first transistor, wherein a gate electrode of the gated diode is connected to a word line, the method comprising:

inducing a channel below the gate electrode of the gated diode to write a '1'.

19. The method according to claim 18, wherein inducing the channel below the gate electrode to write a '1' comprises applying a first positive voltage to the word line.

20. The method according to claim 18, wherein a same positive voltage as the first positive voltage is applied to the word line to write a '0'.

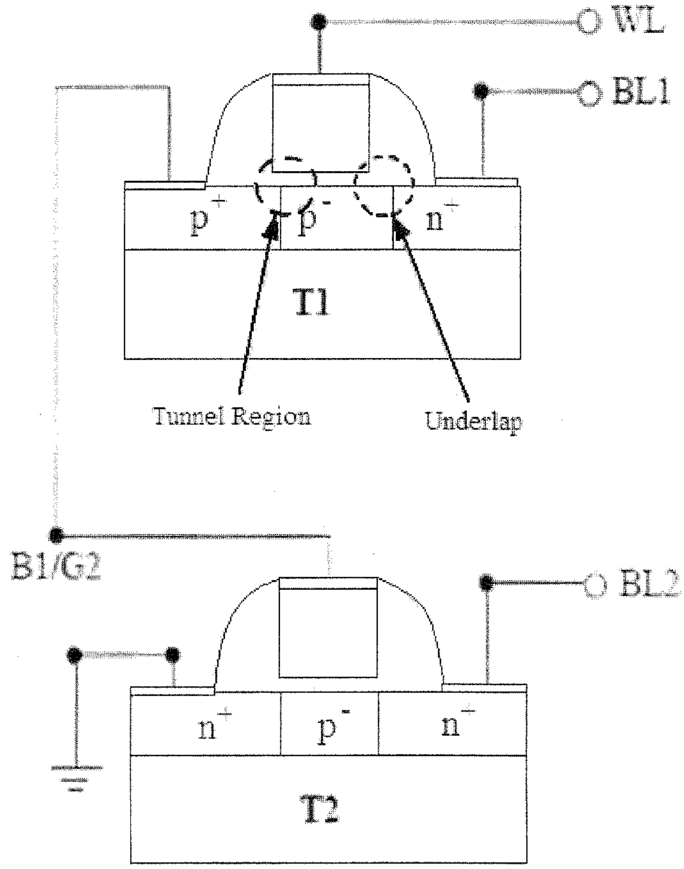

Figure 1

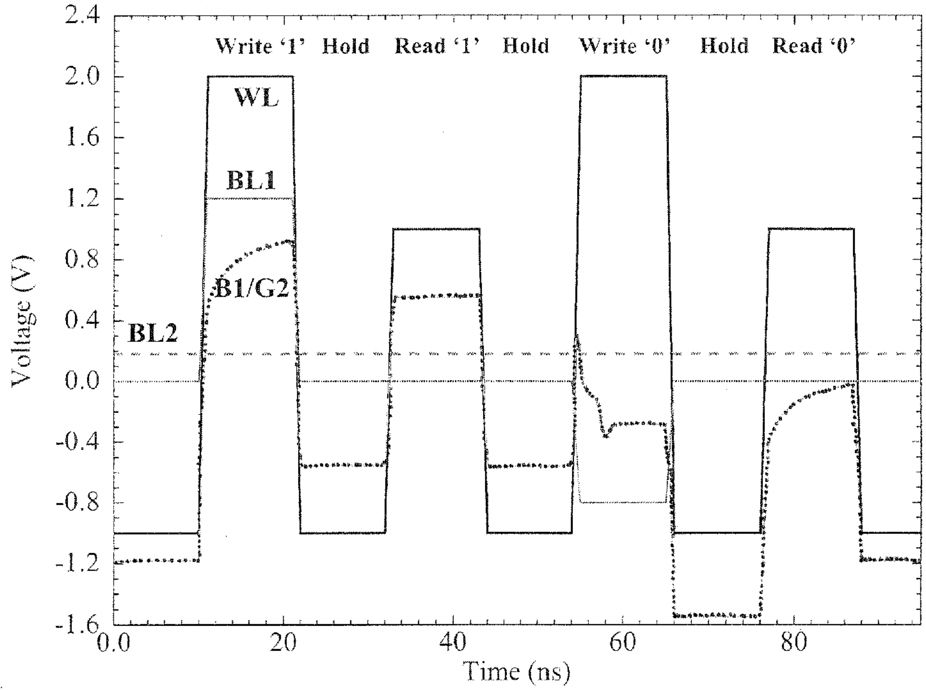

Figure 2A

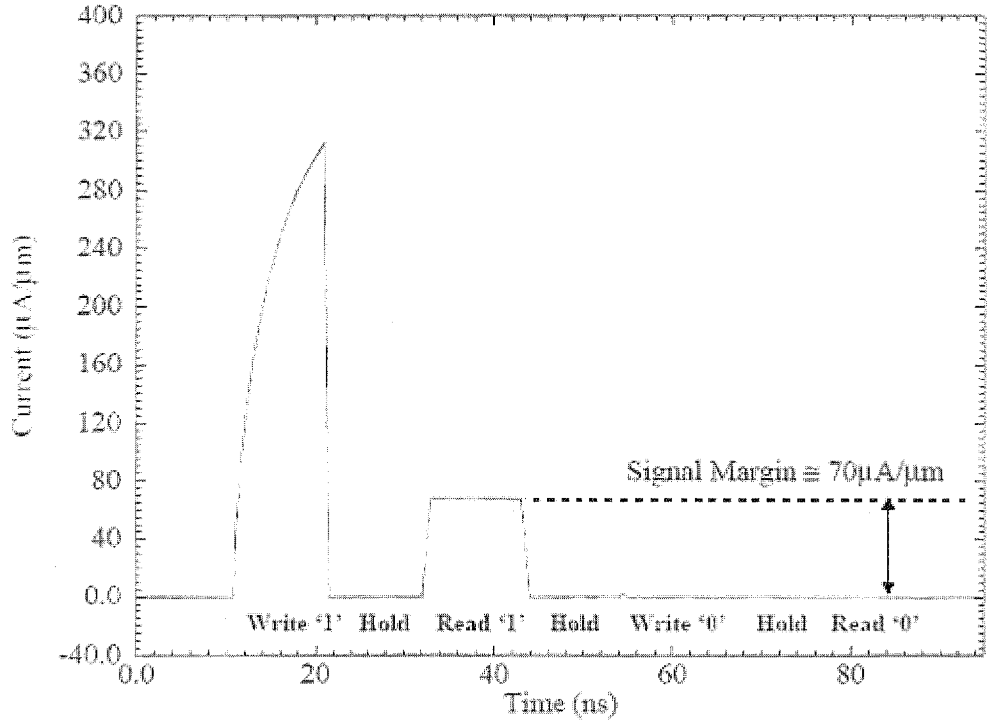

Figure 2B

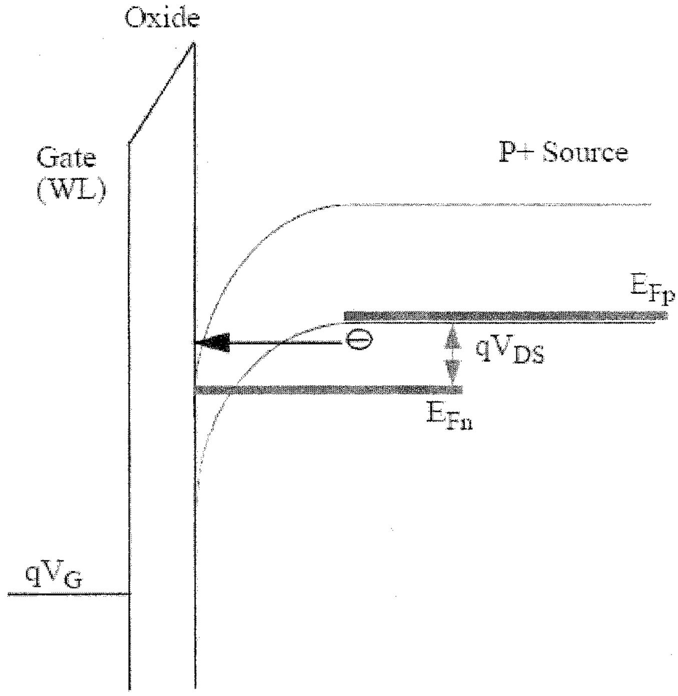

Figure 3A

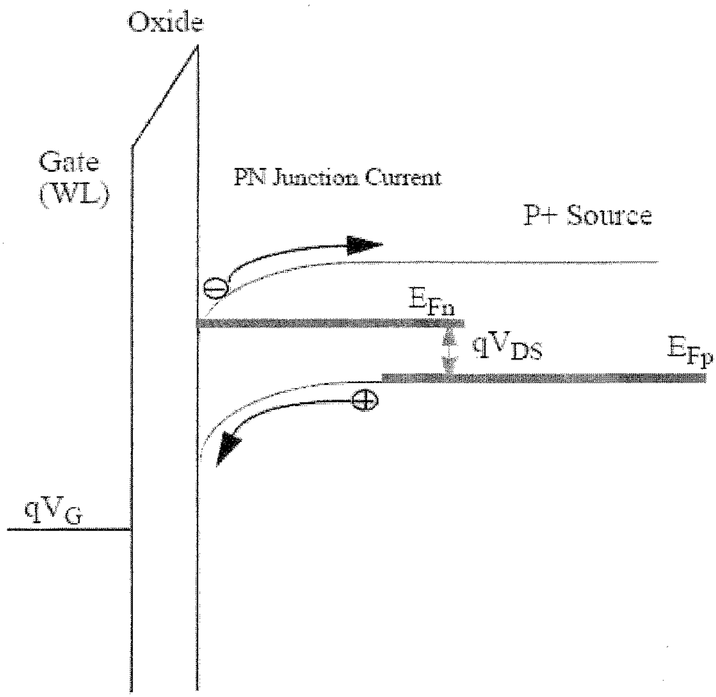

Figure 3B

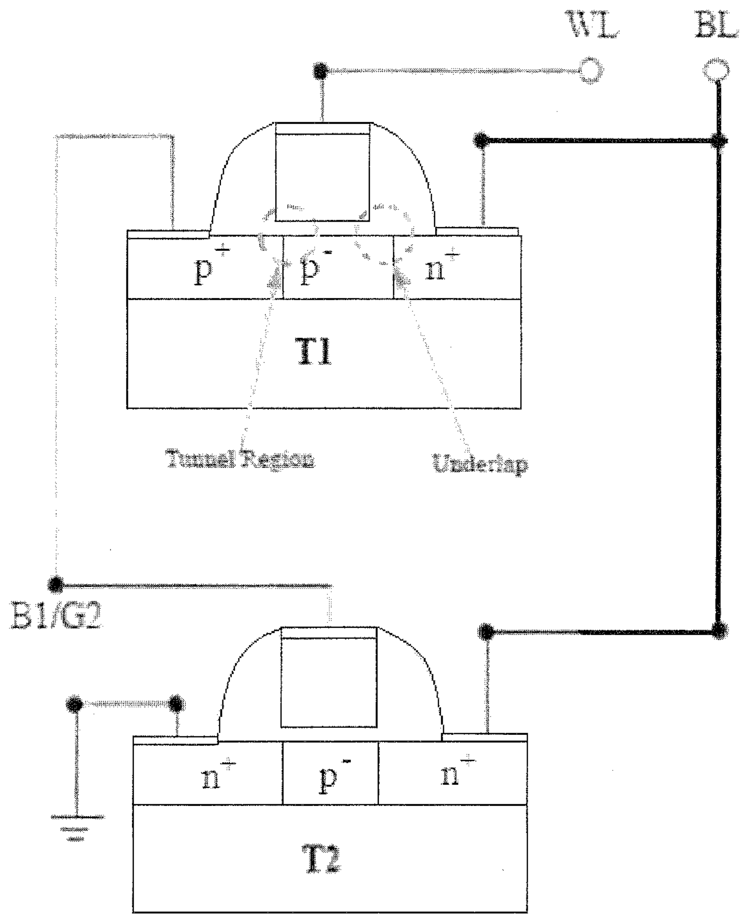

Figure 4

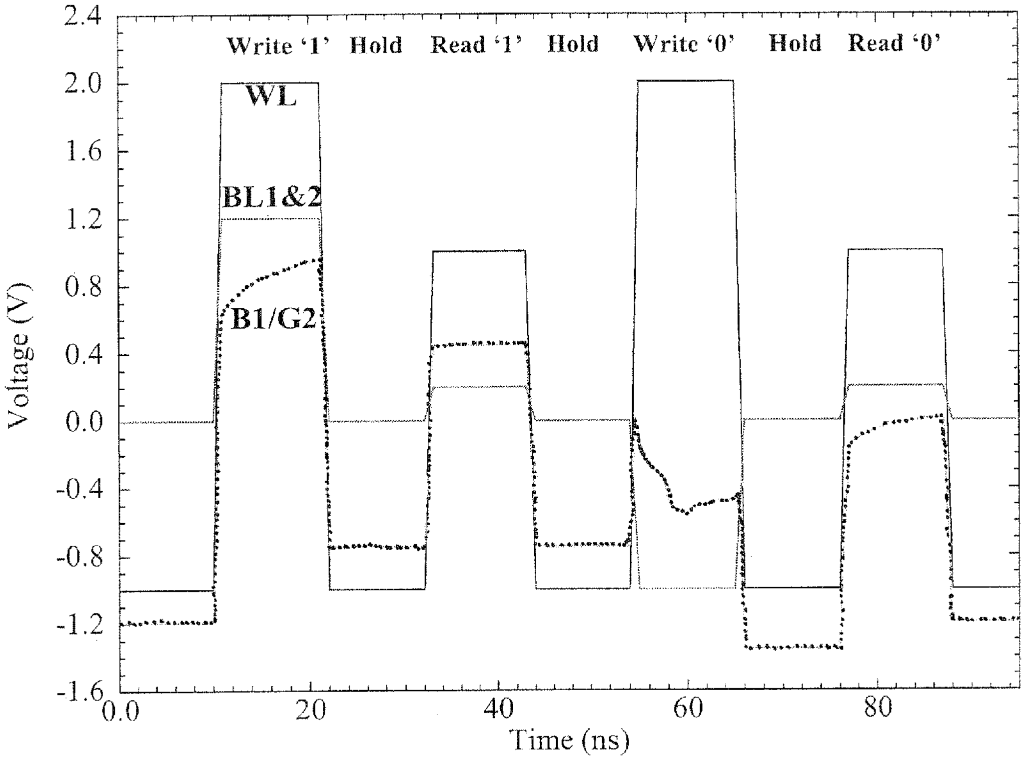

Figure 5A

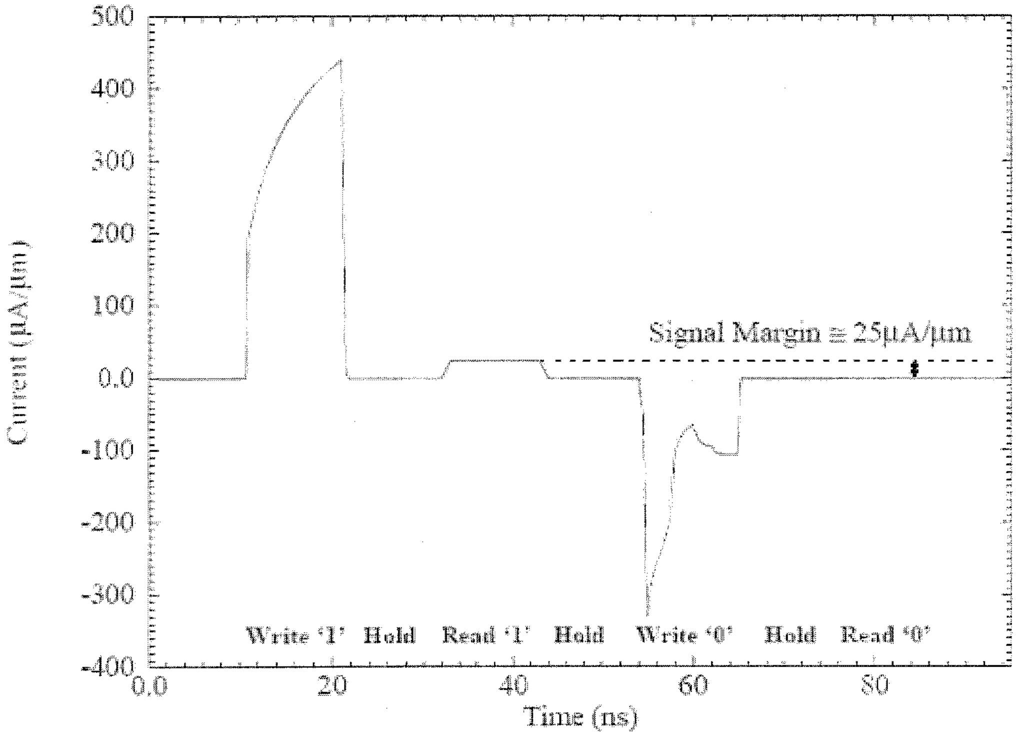

Figure 5B

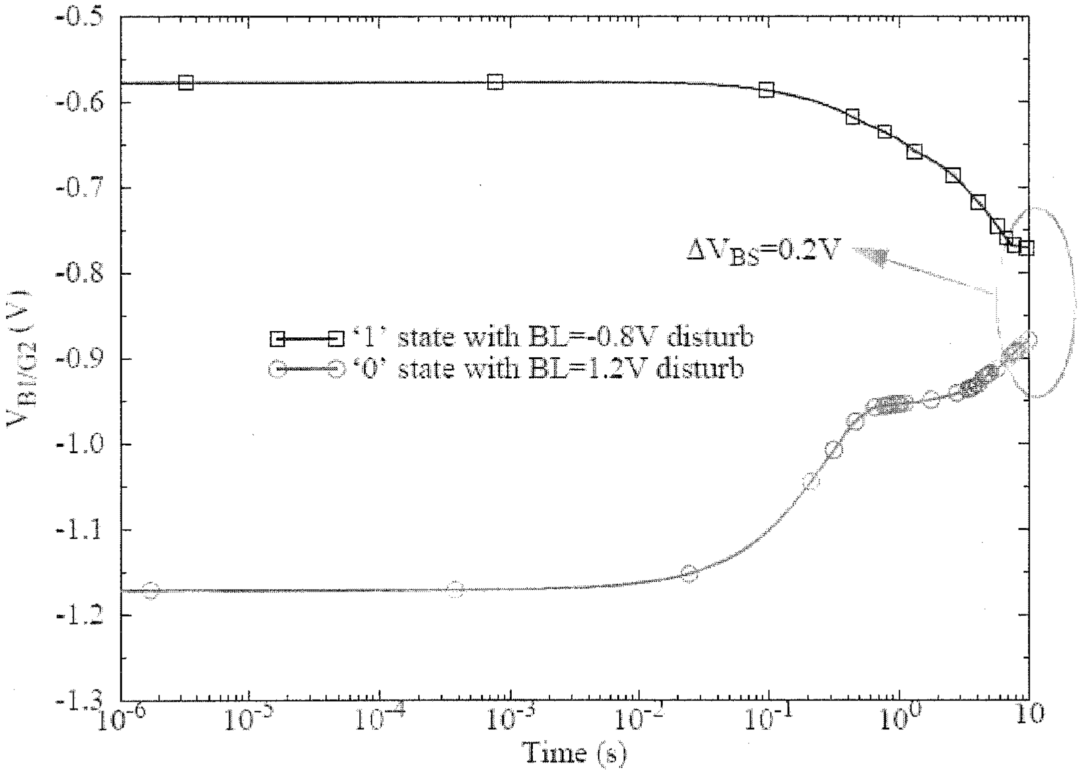
-0.5
-0.6
-0.7
-0.8
-0.9
-1.0
-1.1
-1.2
-1.3
$V_{B1/G2}$ (V)
ΔV_{BS}=0.2V
'1' state with BL=-0.8V disturb
'0' state with BL=1.2V disturb
10^{-6}
10^{-5}
10^{-4}
10^{-3}
10^{-2}
10^{-1}
10^{0}
10
Time (s)

Figure 6

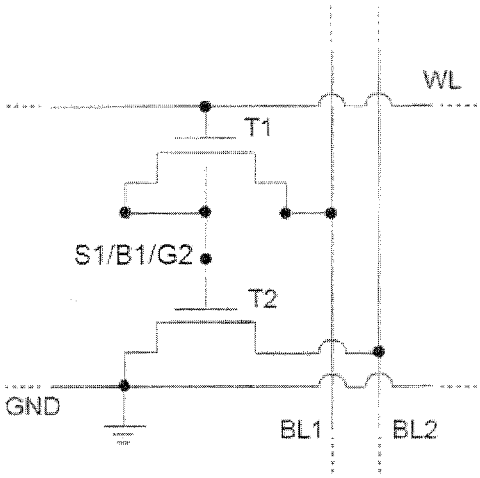

Figure 7

Figure 8A

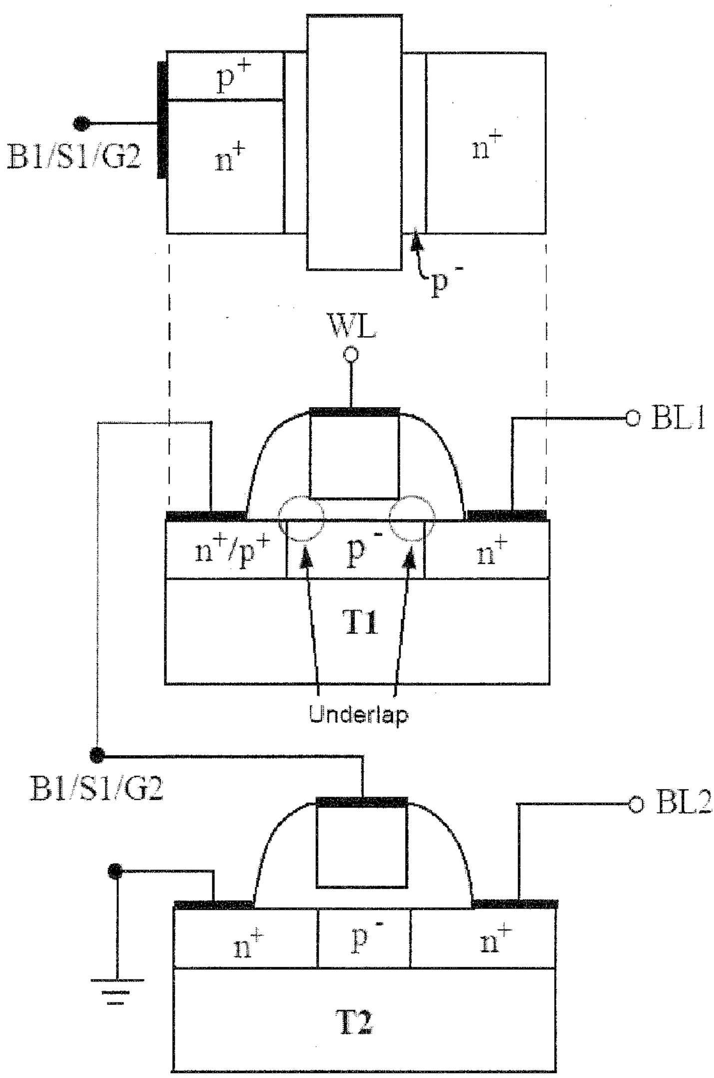

Figure 8B

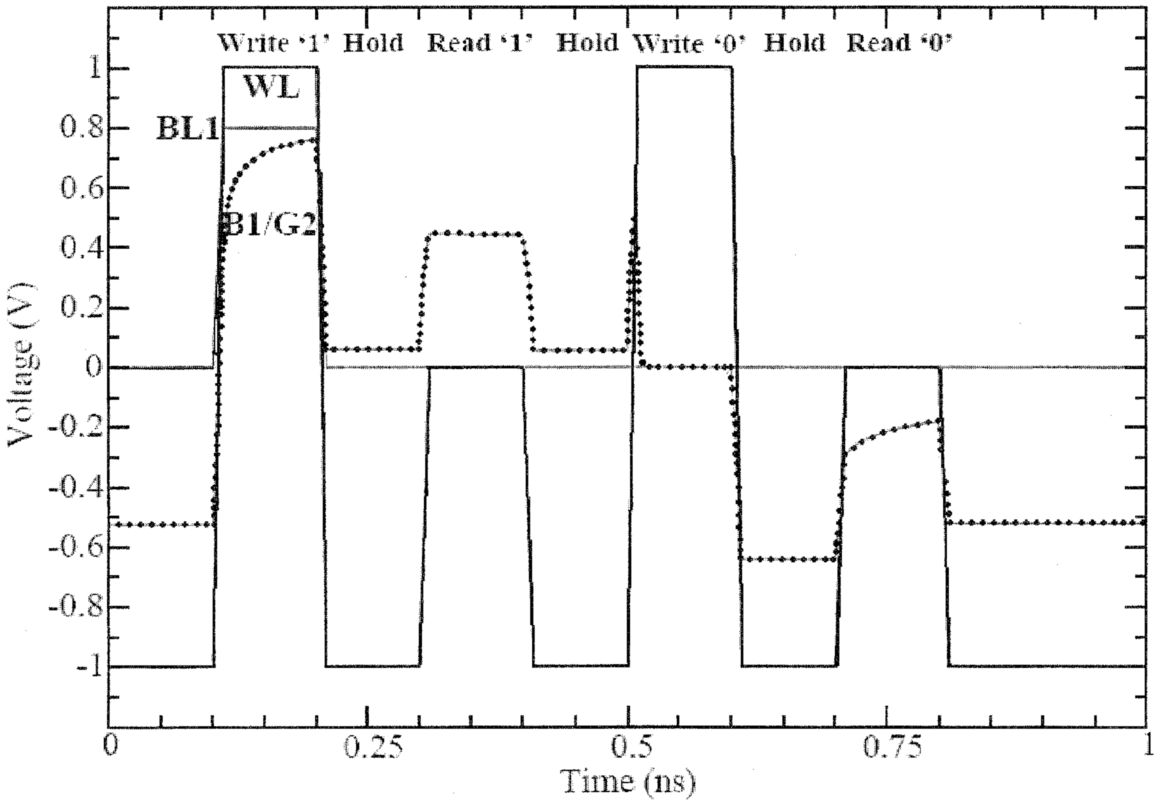

Figure 9A

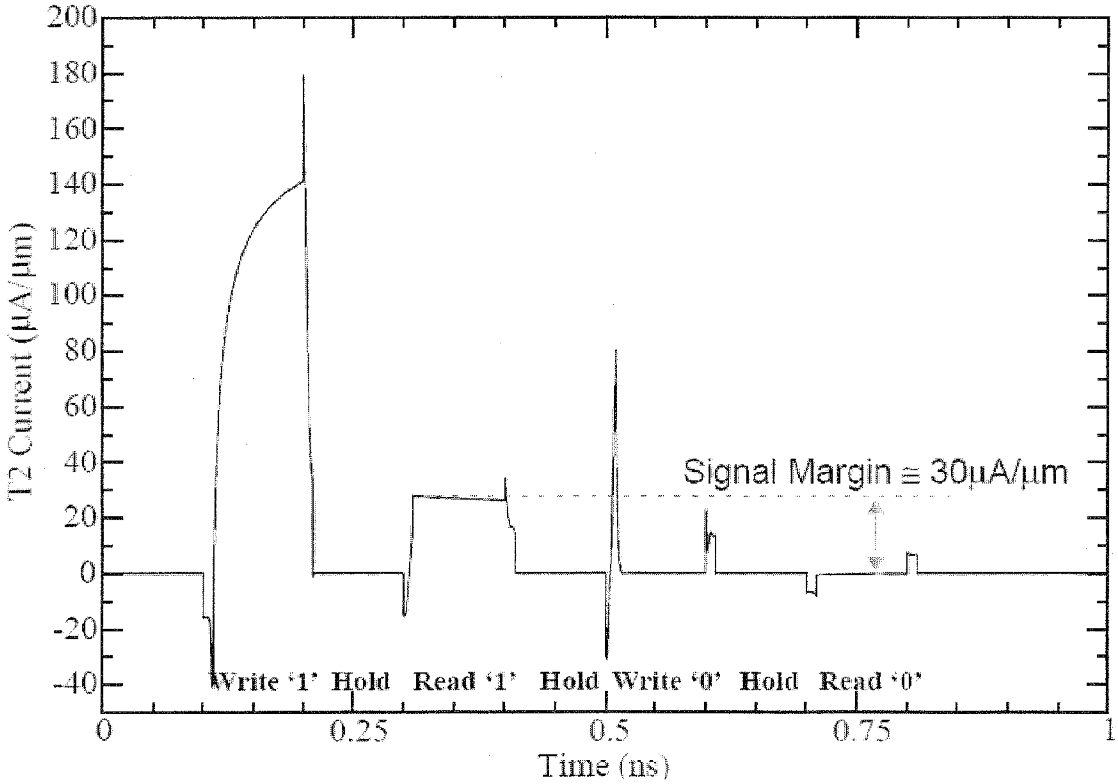

Figure 9B