(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 September 2013 (26.09.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/142076 A2

(51) International Patent Classification:
G05F 3/30 (2006.01)

(21) International Application Number:
PCT/US2013/029545

(22) International Filing Date:
7 March 2013 (07.03.2013)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
13/423,427 19 March 2012 (19.03.2012) US
13/599,776 30 August 2012 (30.08.2012) US

(71) Applicant: **SANDISK TECHNOLOGIES INC.** [US/US]; Two Legacy Town Center, 6900 North Dallas Parkway, Plano, Texas 75024 (US).

(72) Inventor: **YOUSSEFI, Behdad**; 3017 Kaiser Drive, Unit B, Santa Clara, California 95051 (US).

(74) Agents: **CLEVELAND, Michael G.** et al.; Davis Wright Tremaine LLP, 505 Montgomery Street, Suite 800, San Francisco, California 94111 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

(54) Title: CURVATURE COMPENSATED BAND-GAP DESIGN TRIMMABLE AT A SINGLE TEMPERATURE

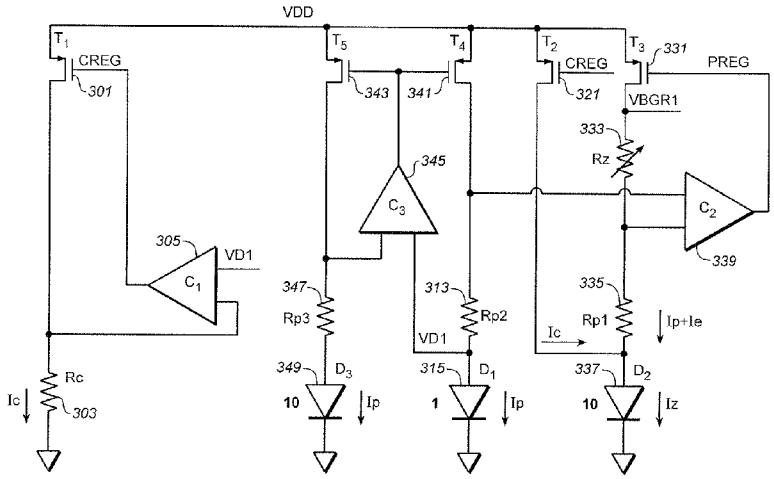

FIG. 5

(57) Abstract: A band-gap reference circuit is compensated for temperature dependent curvature in its output. A voltage across a diode with a fixed current is subtracted from a voltage across a diode with a proportional to absolute temperature (PTAT) current. The resultant voltage is then magnified and added to a PTAT voltage and a diode's voltage that has a complementary-to-absolute temperature (CTAT) characteristic, resulting in a curvature corrected band-gap voltage. This allows for the band-gap reference circuit to be trimmed at a single temperature. This allows the circuit to be made with only a single trimmable parameter, which, in the exemplary circuits, is a resistance value.

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CURVATURE COMPENSATED BAND-GAP DESIGN TRIMMABLE AT A SINGLE TEMPERATURE

FIELD OF THE INVENTION

[0001] This invention pertains generally to the field of band-gap voltage reference circuit and, more particularly, to compensating for the temperature dependence band-gap circuits.

BACKGROUND

[0002] There is often a need in integrated circuits to have a reliable source for a reference voltage. One widely used voltage reference circuit is the band-gap voltage reference. The band-gap voltage reference is generated by the combination of a Proportional to Absolute Temperature (PTAT) element and a Complementary to Absolute Temperature (CTAT) element. The voltage difference between two diodes is used to generate a PTAT current in a first resistor. The PTAT current typically is used to generate a voltage in a second resistor, which is then added to the voltage of one of the diodes. The voltage across a diode operated with the PTAT current is the CTAT element that decreases with increasing temperature. If the ratio between the first and second resistor is chosen properly, the first order effects of the temperature can be largely cancelled out, providing a more or less constant voltage of about 1.2–1.3 V, depending on the particular technology.

[0003] Since band-gap circuits are often used to provide an accurate, temperature independent reference voltage, it is important to minimize the voltage and temperature related variations over the likely temperature range over which the band-gap circuit will be operated. One usage of band-gap circuits is as a peripheral element on non-volatile memory circuits, such as flash memories, to provide the base value from which the various operating voltages used on the circuit are derived. There are various ways to make band-gap circuits less prone to temperature dependent variations; however, this is typically made more process limited, and is difficult in applications where the band-gap circuit is a peripheral element, since it will share the same substrate and power supply with the rest of the circuit and will often be allowed only a relatively small amount of the total device's area.

SUMMARY OF THE INVENTION

[0004] A circuit for providing a reference voltage is presented. The circuit includes a first diode connected between a proportional to absolute temperature current source and ground and a first resistance connected between the first diode and the proportional to absolute temperature current source. A first op-amp has a first input connected to a node between the first resistance and the first diode, an output connected to the gate of a first transistor connected between a high voltage level and ground. The first transistor is connected to ground through a second resistance and the second input of the first op-amp is connected to a node between the first transistor and the second resistance. A second diode is connected between ground and the high voltage level, where the second diode is connected to the voltage level by a first and a second leg. The first leg includes a second transistor whose gate is connected to receive the output of the first op-amp. The second leg includes a third transistor connected in series with a resistive voltage divider, where the resistive voltage divider is connected between the second diode and the third transistor. A second op-amp has an output connected to the gate of the third transistor, a first input connected to a node between the proportional to absolute temperature current source and the first resistance, and a second input connected to a node of the resistive voltage divider. The reference voltage is provided from a node between the third transistor and the resistive voltage divider.

[0005] Other aspects relate to a trimmable reference voltage circuit. The circuit includes a first diode connected between a proportional to absolute temperature current source and ground and a first resistance connected between the first diode and the proportional to absolute temperature current source. The circuit also includes a first op-amp having a first input connected to a node between the first resistance and the first diode, an output connected to the gate of a first transistor connected between a high voltage level and ground. The first transistor is connected to ground though a second resistance and the second input of the first op-amp is connected to a node between the first transistor and the second resistance. A second diode is connected between ground and the high voltage level, wherein the second diode is connected to the voltage level by a first and a second leg. The first leg includes a second transistor whose gate is connected to receive the output of the first op-amp. The second leg includes a third transistor connected in series with a resistive voltage divider, where

the resistive voltage divider is connected between the second diode and the third transistor and includes a trimmable element. The trimmable element of the resistive voltage divider is the only trimmable element of the reference voltage circuit. A second op-amp has an output connected to the gate of the third transistor, a first input connected to a node between the proportional to absolute temperature current source and the first resistance, and a second input connected to a node of the resistive voltage divider. The reference voltage is provided from a node between the third transistor and the resistive voltage divider.

[0006] In further aspects, a method is presented for providing a circuit having a temperature compensated band-gap circuit to supply a reference voltage. The method includes receiving a circuit including a temperature compensated band-gap circuit to supply a reference voltage, wherein the circuit is manufactured so that the temperature compensated band-gap circuit has only a single trimmable parameter for setting the reference voltage value. The temperature compensated band-gap circuit is trimmed by setting the trimmable parameter, wherein the trimming is performed at a single temperature. The value of the trimmable parameter is fixed as determined by the trimming process.

[0007] Various aspects, advantages, features and embodiments of the present invention are included in the following description of exemplary examples thereof, which description should be taken in conjunction with the accompanying drawings. All patents, patent applications, articles, other publications, documents and things referenced herein are hereby incorporated herein by this reference in their entirety for all purposes. To the extent of any inconsistency or conflict in the definition or use of terms between any of the incorporated publications, documents or things and the present application, those of the present application shall prevail.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The various aspects and features of the present invention may be better understood by examining the following figures, in which:

Figure 1 schematically illustrates taking the voltage difference between two diodes.

Figure 2 shows voltages for two different diodes with different curvatures in temperature.

Figure 3 schematically illustrates taking the voltage difference between a diode with a PTAT current and a diode with a constant current.

Figure 4 is a schematic of an exemplary embodiment of a band-gap reference voltage circuit.

Figure 5 is a version of Figure 4 with more detail on a PTAT current source.

Figure 6 shows a comparison between the temperature variation of a conventional band-gap reference circuit and of an implementation of output of the exemplary embodiment.

Figure 7 illustrates an exemplary flow for trimming at a single temperature.

Figures 8A and 8B schematically illustrate the cancellation of amplifier offsets.

Figures 9A-C are a schematic for an exemplary circuit corresponding to Figure 8B.

DETAILED DESCRIPTION

[0009] The techniques presented here can be employed to overcome some of the limitations of the prior art and can effectively help with the cancelation of band-gap curvature with relative process insensitivity. If a voltage across a diode with fixed current is subtracted from a voltage across a diode with current proportional to absolute temperature (PTAT), a nonlinear voltage in temperature is derived. This voltage is then divided by a resistor to generate a nonlinear current which can be used to cancel out curvature of band gap current. This current is then flown through a resistor to generate a curvature corrected band-gap voltage. In the design presented here, a voltage across a diode with fixed current is subtracted from a voltage across a diode with current proportional to absolute temperature (PTAT). The resulting voltage is then magnified and added to a PTAT voltage and a diode's voltage which has complementary-to-absolute-temperature (CTAT) characteristic which results in a curvature corrected band-gap voltage.

[0010] As addition of PTAT and CTAT voltage and curvature correction is done all at once in this arrangement, the number of op-amps and current mirrors needed in this design is considerably less than other comparable designs, which makes it simpler and less susceptible to process variations. In addition, as the band-gap current is passed through a diode, as opposed to a resistor, this design is far less susceptible to absolute value and temperature coefficient of resistors. Moreover, with the addition of an extra resistor in the PTAT chain, this design enjoys an added flexibility of choosing amplification of PTAT and nonlinear voltage independently of one another. This makes trimming the band-gap voltage at one temperature possible.

[0011] One use of a band-gap circuit is as a peripheral element on a circuit, such as on a memory chip for providing a reference voltage from which various operating voltages can be generated, such as the wordline bias voltage V_{WL} for reading a (in this case) floating gate memory cell in a NAND type architecture. This application of a band-gap circuit is described further in US patent number 7,889,575. More detail and examples related to temperature related operation, mainly in the context of memory devices, and uses where band-gap reference values can be used to generate operating voltages can be found in the following US patents and publications: 6,735,546; 6954,394; 7,057,958; 7,236,023; 7,283,414; 7,277,343; 6,560,152; 6,839,281; 6,801,454; 7,269,092; 7,391,650; 7,342,831; 2008/0031066A1; 2008/0159000A1; 2008/0158947A1; 2008/0158970A1; 2008/0158975A1; 2009/0003110A1; 2009/0003109A1; US 2008/0094908; 2008/0094930A1; 2008/0247254A1; and US 2008/0247253A1. Another example of temperature compensation for a band-gap voltage generation circuit and its use in a non-volatile memory is found in US2010/0074033A1. Along with these temperature related aspects, the generation of various operating voltages from reference values is presented in 5,532,962. The techniques presented here can be applied for the various base reference voltages described in these references as well as other applications where band-gap circuits are employed, but being particularly advantageous when used as a peripheral element on a larger circuit where the design, process, technology, and/or product limitations of the larger circuit can negatively affect the band-gap reference element. In addition to the main example of a non-volatile memory, these techniques also have application where high voltage biases are needed, such as when a band-gap voltage is used as the reference voltage for charge pump regulation and the high voltage output from the

charge pump is generated by multiplying of the band-gap voltage. Various process and device limitations require an accurate voltage level be provided without too much variation so as to prevent oxide/junction break downs or punch through effect on the devices. In this application, any temperature variation of the band-gap voltage would be multiplied in forming the high voltage biases. Consequently, the minimizing the temperature variation of the band-gap voltage is important for this type of application as well.

[0012] In a conventional band-gap reference generator, the circuit adds a Proportional-to-Absolute-Temperature (PTAT) voltage, which is linear in the temperature, to a voltage drop across a diode which has Complimentary-to-Absolute-Temperature (CTAT) characteristics (and is consequently not linear in temperature) to get a voltage with zero first-order Temperature Coefficient (TC). PTAT voltages can be generated by subtracting voltage drop across two diodes with different current densities. For example, referring to Figure 1, this shows a diode D_2 103 with a current density I_p and a diode D_1 101 with a current density mI_p, so that the ratio of these two currents is m. If the voltage drops across these two are subtracted, this gives the relationship:

$$V_{D1} - V_{D2} = V_T \ln(m),$$

providing the desired PTAT behavior. However, because of the nonlinearity of a diode's voltage with temperature, band-gap references always have some residual finite curvature with respect to temperature.

[0013] The issue of curvature is relevant for several reasons. The temperature dependent curvature of the band-gap can introduce an error in the reference voltage at mid temperatures, even with zero first order temperature coefficient (TCO). For example, in a data converter design or any other circuits requiring an accurate reference voltage, this sets a limit on their accuracy which lowers Effective-number-of-bits (ENOB), since if the variation is large enough it will be greater the change in some number of least significant bits. In the case where the band-gap circuit is used to generate control gate read voltages (V_{CGRV}), as the reference value is scaled up to provide these voltages, the error voltage could be as high as 50mV, for example, at room temperature even with perfect first order TCO.

[0014] For example, in a fairly conventional band-gap reference circuit, the error for the output of the circuit over a temperature range -40C to 100C is as much as 10mV. For use in reading a memory level with a threshold voltage of 6V, this is error is scaled up by a factor of about 6V/1.2V=5, so that the error in the read voltage error could be up to 50mV. In a multistate memory of, say, 3-bits, where 8 state distributions need to fit into a window of 6 volts, this can be non-negligible.

[0015] Another reason why curvature is important has to do with the fact that variation in curvature also varies the first order TCO. As a result, a different positive TCO is needed to compensate for diode's negative TCO. Referring to Figure 2, this shows the voltage versus temperature for two diodes with different curvatures in temperature. In Figure 2, the broken line is a linearization of the variation over the operating temperature range. This variation is a cause of variation in the band-gap reference voltage, a consequence of which is that a manufacturer cannot trim all dies at one voltage and get a zero TCO. In a fairly typical case, the variations between different dies can be ~30mV.

[0016] A number of prior art schemes have been proposed to compensate for the curvature of band-gap references, but they are either very complicated, and thus more susceptible to process variations, or inherently incapable of removing all nonlinearities. In addition, some of these schemes are dependent on the absolute value of resistors, which makes them less useful when the absolute value of resistor is not accurately known before fabrication or when resistors themselves have large temperature coefficients. The arrangement described here is both relatively simple, and if trimmed correctly, capable of removing all nonlinearities. Additionally, it is relatively insensitive to temperature coefficient and absolute value of resistors.

[0017] By way of background, the voltage across diode is given by

$$V_D = V_T \ln(\frac{I_D}{I_s})$$

where I_D is the current through the diode, V_T is the thermal voltage, and I_s is the saturation current, where $I_s = bT^{4+m}e^{\frac{-E_g}{V_T}}$, m is a process parameter, and E_g is the band gap of silicon. Combining these gives:

$$V_D = V_T \ln(I_D) - V_T \ln(b) - (4+m)V_T \ln(T) + E_g .$$

The $(4+m)V_T$ term is non-linear in temperature. Similarly to Figure 1, Figure 3 shows a pair of diodes D_{ptat} 201 with a PTAT current and D_{ztc} 203 with a current with no temperature coefficient. For the first of these, the current and voltage are:

$$I_D = I_{ptat} = \alpha T \Rightarrow V_{D_{ptat}} = V_T \ln(\alpha / b) - (3+m) V_T \ln(T) + E_g$$

For the second the relations are:

$$I_D = I_z \Rightarrow V_D = V_T \ln(I_z / b) - (4+m) V_T \ln(T) + E_g \quad .$$

If the voltage drop across the diode D_{ztc} 203 with constant current is subtracted from that of D_{ptat} 201 with a PTAT current, the nonlinear term $V_T \ln(T)$ can be achieved:

$$V_{D_{ptat}} - V_{D_{ztc}} = V_T \ln(\alpha / I_z) + V_T \ln(T) \ .$$

The last term with the non-linearity in temperature can be cancelled by choice of the correct coefficient. This can then be used to produce a band-gap reference level of:

$$BGR = V_D + \beta (V_{D_{ptat}} - V_{D_{ztc}}) = E_g \ ,$$

where β is the ratio of voltage divider where the output is taken. (For example, in the arrangement of Figures 4 and 5, this is Rz/Rp1.)

[0018] Figures 6 and 7 show exemplary embodiments for a band-gap circuit that can be used to achieve this sort of curvature compensation. One of the practical problems in implementing this arrangement is that, in practice, the difference in diode sizes cannot not be made too great within a given circuit. Consequently, by just relying upon the relative sizing on of the two diodes restricts the value of $(V_{D_{ptat}} - V_{D_{ztc}})$ to be a small value as a practical matter. This can make it more susceptible to noise and amplifier's offset and generally harder to adjust the relative values. In an aspect of the band-gap reference circuits presented here, a resistance (such as R_{p2} of Figure 4) is added to achieve a larger value for this difference. This serves to make the effective relative area of the diode more, while keeping the actual relative area small and thus overcoming the problem of having diodes of quite different sizes. The arrangement presented here also makes the output of the circuit dependent on the ratio of resistances in the circuit, rather than the absolute value of a resistance, making the circuit less sensitive to process variations and temperature dependencies in the resistances.

[0019] Figure 4 is an exemplary embodiment of a schematic for a band-gap reference circuit. The output of the circuit is at VBGR1 and the elements are connected by the high (Vdd) and low (ground) voltage levels of the chip. Starting on the left is a portion to generate a complimentary to absolute temperature (CTAT) current Ic. This has a first leg of the circuit including a transistor T1 301 connected between the high voltage level and ground through the resistor Rc 303, where the current flowing through is Ic. The gate of T1 301 is controlled by the output CREG of op-amp C1 305, whose first input is from a node between T1 301 and Rc 303. A second leg includes a PTAT current source, providing a current Ip, connected in series with the resistance Rp2 313 and the diode D1 315. The second input of the op-amp C1 305 is taken from a node between Rp2 313 and D1 315.

[0020] A second diode D2 337 is fed by the combination of two legs. The first provides has a transistor T2 321 connected between the high voltage level and D2 337, where the gate of T2 321 is controlled by the output CREG of C1 305, so that it will provide a current Ic into D2 337. A current of (Ip+Ie), where Ie represents the portion for the error (the non-linear term) current, is also supplied to D2 337 by the series combination of T3 331, Rz 333, and Rp1 335. The combined current through D2 337 is then Iz. The gate of T3 331 is controlled by the output PREG of op-amp C2 339, which has a first input connect to a node between the Iptat current source 311 and Rp2 313 and has a second input connected to a node between Rz 333 and Rp1 335. The output of the circuit VBGR1 is then taken from between Rz 333 and T3 331.

[0021] In Figure 4, the numbers 1 and 10 that are respectively next to D1 315 and D2 337 indicate the relative sizes of these diodes. As discussed above, it is desirable to have a larger value for the difference $(V_{D_{ptat}} - V_{D_{ztc}}) = (V_{D1} - V_{D2})$, which can be achieved by increasing the size differential between the diodes; however, to go much beyond this factor of 10 is generally not practically achievable. The inclusion of the resistance Rp2 313 above the diode D1 313 functionally acts as if the diode D1 where smaller, helping to increase the difference.

[0022] Figure 5 adds some detail for a specific embodiment of the PTAT current source 311 I_{PTAT} 311 of Figure 4. In addition to the elements shown in Figure 4, a transistor T4 341 is connected between Vdd and Rp2 313 to supply the PTAT current

Ip into D1 315. The gate of T4 341 is controlled by the output of op-amp C3 345. A first input of the op-amp is taken from the same node (here marked VD1) between Rp2 313 and D1 315 as used as an input for C1 305. The output of C3 345 is also connected to control a transistor T5 343 that is connected between Vdd and ground through first a resistance Rp3 347 and a diode D3 349 that is sized the same as D2 337, through which again flows Ip. The second input of C3 345 is taken from a node between T5 343 and Rp3 347.

[0023] The output of the circuit, VBGR1, can be found by looking at the currents through D1 315 and D2 337:

$$\begin{cases} I_{D1} = I_z \Rightarrow V_{D1} = V_T \ln(I_z / b) - (4+m)V_T \ln(T) + E_g \\ I_{D2} = I_p = \alpha T \Rightarrow V_{D2} = V_T \ln(\alpha / b) - (3+m)V_T \ln(T) + E_g \end{cases},$$

Taking the difference gives:

$$V_{D1} - V_{D2} = V_T \ln(\alpha / I_z) + V_T \ln(T) \ .$$

From this follows the current through R_Z:

$$I_p + I_e = \frac{V_{D2} + I_p.R_{p2} - V_{D3}}{R_{p1}} = \frac{V_T}{R_{p1}} \ln(\frac{\alpha.n}{I_z}) + \frac{V_T}{R_{p1}} \ln(T) + \frac{R_{p2}}{R_{p1}} \alpha.T \ , \quad I_z = I_c + I_p + I_e$$

and

$$V_{BGR1} = V_T . \left[\frac{R_Z}{R_{p1}} \ln(\frac{\alpha.n}{I_{ztc}}) + \frac{\alpha.R_{p2}}{K/q} (\frac{R_Z}{R_{p1}} + 1) + \ln(\alpha / b) \right] + \left[\frac{R_Z}{R_{p1}} - (3+m) \right] . V_T . \ln(T) + E_g$$

,

to give the value of VBGR1, where k is the Boltzmann constant, q is the charge unit, and n is the ratio of diode areas (n = area(D2)/area(D1), which is 10 in the example).

[0024] Figure 6 shows the temperature variation of an implementation of the output of the exemplary embodiment over the same range of -40C to 120C. This is shown at 401, where the output typical of a conventional BGR circuit is shown at 403. As shown, the variation 401 of the exemplary embodiment over this range of -40C to 120C is noticeably flatter, having a variation of ~15μV, as compared to ~2mV at 403 for the conventional design. Consequently, the band-gap reference generator described above can provide curvature compensation in a relatively simple scheme that makes it less susceptible to process variations. As the curvature of a band-gap reference circuit is process dependent, the value of the circuit's voltage varies with

process as well. Thus, when the curvature is perfectly compensated for, the value of BGR voltage will be independent of process and only a function of physical properties of silicon. This makes trimming the band-gap reference at one temperature possible.

Trimmability at a Single Temperature

[0025] This section considers this ability to trim the band-gap circuit at a single temperature. As band-gap reference (BGR) circuits of the prior art display some degree of temperature variation, the usual approach to trimming a band-gap reference circuit at multiple temperatures, where the circuit will have a corresponding set of trimmable parameters. After the device with the BGR is manufacturer, but before shipping out to customers, in order to operate accurately it would need to undergo the trimming process, but trimming at multiple temperatures is a relatively costly process. This section is based on the exemplary embodiment for a curvature compensated band-gap circuit described above with respect to Figures 4 and 5. The circuit enables trimming curvature of band-gap voltage for each die and thus eliminates the curvature. With curvature eliminated, the band-gap voltage depends only on physical properties of silicon crystal and becomes process independent. This can also be combined with an offset cancelation scheme to help make the BGR independent of the amplifiers' offsets. This makes trimming the band-gap circuit at one temperature practical as BGR voltage will be independent of temperature and process. Because of this relative simplicity and insensitivity to process variations, the BGR voltage has the ability to be trimmed at only one temperature, so that the circuit needs to have only a single trimmable parameter. In the exemplary embodiment of Figures 4 and 5, the trimmable element will be taken as part of the resistive voltage divider connected between the output node and the diode D2 337. Specifically, the value of R_Z 333 will be set in the trimming process.

[0026] Going back to the equation for V_D as discussed above,

$$V_D = V_T \ln(I_D) - V_T \ln(b) - (4+m)V_T \ln(T) + E_g \ ,$$

variations in the process parameter b affect the just the first order TCO and can be removed by trimming the band gap reference (BGR) circuit to the appropriate voltage, which can be done at a single temperature. Variations in m, however, affect both the first order TCO and the curvature of the BGR, so that it will affect the band-gap

reference even if it has zero first order TCO characteristics. This makes trimming a temperature compensated BGR at one temperature impossible in conventional BGR circuits. Due to the logarithmic function, variations in b are relatively negligible compared to variations in m. Therefore, trimming m enables trimming the BGR at only one temperature to a voltage with zero (or minimized) first order TCO, reducing the problem of trimming BGR to being able to trim the curvature of BGR.

[0027] Returning now to the expression for the output level VBGR1 in Figure 5 discussed above, setting the second term in square brackets (multiplying $V_T\ ln(T)$) to zero gives: $R_Z = (3+m).R_{p1}$.

so that $\Delta R_Z = \Delta m.R_{p1}$. Considering the first term of the expression for VBGR1, this also includes R_Z, so that varying R_Z in the second term also varies the first term. To cancel out this variation of the first term, R_{p2} is also varied. Taking the derivative of the first term of the VBGR1 equation with respect to R_Z and R_{p2} and equating this to zero gives: $\Rightarrow \Delta R_{p2} = -\frac{\Delta R_Z}{R_Z + R_{p1}}.(\frac{V_T.\ln(\alpha.n/I_Z)}{I_P} + R_{p2}) \Rightarrow \Delta R_{p2} = \frac{\Delta R_Z}{R_Z + R_{p1}}.(\frac{V_T.\ln(I_Z/\alpha.n)}{I_P} - R_{p2})$

.

Considering the first of these equations relating ΔR_{p2} and ΔR_Z, the coefficient of ΔR_Z i is not a well defines integer or even a fraction, which can make designing the circuit difficult if all these conditions are to be met. Instead, the approach used here is to set ΔR_{p2} to zero so that R_{p2} is fixed for whatever adjustment is made in Rz.

[0028] Considering the second expression for $\Delta R_{p2} = 0$, this can be achieved if the term in the parentheses is zero:

$$\frac{V_T.\ln(I_Z/\alpha.n)}{I_P} - R_{p2} = 0 \Rightarrow R_{p2} = \frac{V_T.\ln(I_Z/\alpha.n)}{I_P} = \frac{k/q.\ln(I_Z/\alpha.n)}{\alpha} \quad .$$

As before, k is the Boltzmann constant, q is the charge unit, and n is the ratio of diode areas. In the band-gap reference circuit, α, n, and I_Z are all design parameters, so that the circuit can be designed to set R_{p2} to meet this condition. As the circuit is then temperature compensated, only a single parameter needs to be left trimmable to set the circuit's reference value. In the exemplary embodiment, the trimming is done in the resistive divider between T_3 331 and D_2, specifically by having the value of R_Z

being settable. R_{p2}, along with all the other parameter value (R_{p1}, R_{p3}, ...) except R_Z, can be fixed when manufactured.

[0029] Figure 7 schematically illustrates the trimming process. At 501, the circuit having the temperature compensated band-gap is received, where the circuit is manufactured so that the temperature compensated band-gap circuit has only a single trimmable parameter for setting the reference voltage value. For example, this band-gap circuit could be that of the exemplary embodiments of Figures 4 or 5, where R_Z value is trimmable. Next, at 503, the band-gap circuit is trimmed. This could be done by the manufacturer as part of the test process before the device is sent out or could be done elsewhere, such as by a supplying who receives the circuits from the initial manufacturer and packages it as part of a system, for example. In any case, the compensated band-gap circuit is then trimmed by setting the trimmable parameter, where this process can be done at a single temperature. This can be done at a convenient temperature by just adjusting the output reference voltage to the desired value. In the exemplary flow, the fixing of the trimmable parameter is listing separately at 505, although this would be typically be done as part of the larger trimming process.

Offset Cancelation for Amplifiers

[0030] Going back to the exemplary embodiments of Figures 4 and 5, so far the discussion has not considered the characteristics of the amplifiers. As is also the case for other band-gap reference circuit designs, the amplifiers of Figures 4 and 5 (such as C_1 305, C_2 339, and C_3 345) will have offsets and temperature dependent behavior of their own.

[0031] For example, considering the offset voltages (V_{os}) for the output voltage of the BGR circuit of Figure 5 due to the op-amps, these are amplified according to the following equations:

$$V_{OS-BGR1} = \frac{R_{p2}.R_Z}{R_{p3}.R_{p1}} V_{OS-C3} + \frac{R_Z}{R_{p1}} V_{OS-C2} \quad ,$$

where the offsets are that of the output (VBGR1), op-amp C_3 345, and op-amp C_2 339. The amplifiers' offsets have their own TCO and thus in addition to adding a large offset to the nominal BGR voltage, they will add their TCOs to the nominal

value. To improve accuracy, the BGR trimming should take the effects of amplifiers' offsets into account and be able to successfully reduce or cancel them.

[0032] For a properly designed amplifier, the offset is normally dominated by the input pair transistors' threshold voltage (Vt) mismatch. In this case, the offset of the amplifier can be cancelled by continuously switching the input pair and current mirror transistors back and forth with a clock signal. The clock frequency should be set to be higher than amplifier's bandwidth, so that the switching noise is attenuated by the amplifier. This condition can typically be met by an available clock signal on the device. This can be illustrated with respect to Figures 8A and 8B.

[0033] Figure 8A is a high level representation of the situation. An op-amp 601 has the + and – inputs, where the offset Vos is shown. The inputs are then switched, as represented by the arrow, with the clock signal. Figure 8B gives some more detail, showing an implementation of the op-amp in terms of transistors. The current mirror pair 621, 623 respectively feed the transistor pair 611, 613 of the −, + inputs. Using the clock signal, the two pairs are switched back and forth, cancelling off the off-set. Taken together, a BGR circuit based on the exemplary embodiments can reduce op-amp's offset by several factors of ten.

[0034] Figures 9A-C Are a schematic for an exemplary circuit corresponding to Figure 8B in order to illustrate the how both the inputs and polarity of the op-amp can be switched according to the clock signal. As shown in Figures 9A and 9B, the + and − inputs (here as VP and VN) are switched by the clock signal CLK and its inverse CLKn to alternately provide these as VB and VA as the clock signal alternates. The VA and VB levels are then used as inputs into the op-amp respectively at transistors M13 and M12, as shown in Figure 9C.

[0035] The op-amp of Figure 9C is connected between the supply level VSUP and ground, where VA and VB are input respectively at the PFET transistors M13 and M12 and the output OUT is taken at right between M9 and M2. The input at the gate of M4 is a biasing voltage to set the current for the circuit and the transistors M9-M11 across the top form a current mirror. The clock signals CLK and CLKn are used with the central transistors M17-M20 to change the polarity of the current mirror,

switching it back and forth. The switching of both the inputs and the internal switching using the clock CLK as shown can then greatly reduce the op-amp's offset.

Conclusion

[0036] The foregoing has presented a systematic way of trimming a band-gap reference circuit at one temperature. By including a trimmable element, such as R_Z, into the exemplary embodiments of a curvature-compensated BGR circuit, the circuit can be trimmed for curvature. Being able to trim the curvature of the BGR circuit allows for its curvature to be set to a known value from simulation. Having a fixed curvature, the circuit can be trimmed at one temperature as the voltage that has the zero first order characteristic as already known from simulation. Together, these can significantly reduce the TCO variation compared to the conventional BGR circuit.

[0037] Although the invention has been described with reference to particular embodiments, the description is only an example of the invention's application and should not be taken as a limitation. Consequently, various adaptations and combinations of features of the embodiments disclosed are within the scope of the invention as encompassed by the following claims.

IT IS CLAIMED:

1. A circuit for proving a reference voltage, comprising:

a first diode connected between a proportional to absolute temperature current source and ground;

a first resistance connected between the first diode and the proportional to absolute temperature current source;

a first op-amp having a first input connected to a node between the first resistance and the first diode, an output connected to the gate of a first transistor connected between a high voltage level and ground, wherein the first transistor is connected to ground though a second resistance and the second input of the first op-amp is connected to a node between the first transistor and the second resistance;

a second diode connected between ground and the high voltage level, wherein the second diode is connected to the voltage level by a first and a second leg, wherein:

the first leg includes a second transistor whose gate is connected to receive the output of the first op-amp; and

the second leg includes a third transistor connected in series with a resistive voltage divider, where the resistive voltage divider is connected between the second diode and the third transistor; and

a second op-amp having an output connected to the gate of the third transistor, a first input connected to a node between the proportional to absolute temperature current source and the first resistance, and a second input connected to a node of the resistive voltage divider,

wherein the reference voltage is provided from a node between the third transistor and the resistive voltage divider.

2. The circuit of claim 1, wherein the resistive voltage divider includes a trimmable element, the trimmable element of the resistive voltage divider being the only trimmable element of the reference voltage circuit

3. The circuit of claim 2, wherein the value of the first resistance is set to minimize the first order temperature coefficient of the reference voltage.

4. The circuit of claim 3, wherein the value of the first resistance depends on the ratio of the area of the first diode to the area of the second diode.

5. The circuit of claim 2, wherein the resistive voltage divider includes:

a third resistance connected between the second diode and said node of the resistive voltage divider; and

a fourth resistance connected between the third transistor and said node of the resistive voltage divider, wherein the fourth resistance is the trimmable element.

6. The circuit of claim 1, wherein the second diode is sized larger than the first diode.

7. The circuit of claim 6, wherein the ratio of sizes of the second diode to the first diode is approximately ten.

8. The circuit of claim 1, wherein the proportional to absolute temperature current source includes:

a fourth transistor connected between the first resistance and the high voltage level;

a fifth transistor connected between the high voltage level and a third resistor, and a third diode connected between the third resistor and ground; and

a third op-amp having a first input connected to a node between the fifth transistor and the third resistor, and second input connected to the node between the first diode and the first resistance, and having an output connected to the gates of the fourth and fifth transistors.

9. The circuit of claim 8, wherein the third diode is sized the same as the second diode.

10. The circuit of claim 8, further comprising:

offset cancellation circuitry connected to the second and third op-amps and connected to receive a clock signal, wherein the offset cancelation circuitry alternates

the connection of the first and second inputs for the second op-amp and the first and second inputs of the third op-amp based upon the clock signal.

11. The circuit of claim 10 wherein the offset cancelation circuitry further alternates the connection of internal elements for the second and third op-amps based upon the clock signal.

12. A method of providing a circuit having a temperature compensated band-gap circuit to supply a reference voltage, comprising:

receiving a circuit including a temperature compensated band-gap circuit to supply a reference voltage, wherein the circuit is manufactured so that the temperature compensated band-gap circuit has only a single trimmable parameter for setting the reference voltage value;

trimming the temperature compensated band-gap circuit by setting the trimmable parameter, wherein the trimming is performed at a single temperature; and

fixing the value of the trimmable parameter as determined by the trimming process.

13. The method of claim 12, wherein receiving the circuit comprises manufacturing the circuit having a temperature compensated band-gap circuit to supply a reference voltage.

14. The method of claim 13, wherein manufacturing the circuit includes manufacturing a plurality of integrated circuits to the same design, wherein the circuit having a temperature compensated band-gap circuit to supply a reference voltage is one of the plurality of integrated circuits manufactured to the same design.

15. The method of claim 13, wherein said trimming and fixing are performed as part of a post-manufacturing test process.

16. The method of claim 12, wherein the trimmable parameter is a resistance value.

17. The method of claim 16, wherein the circuit includes a first resistance having a value set to minimize the first order temperature coefficient of the reference voltage.

18. The method of claim 17, wherein the value of the first resistance depends on a ratio of diode areas.

19. The method of claim 17, wherein the circuit includes

a first diode connected between a proportional to absolute temperature current source and ground;

a first resistance connected between the first diode and the proportional to absolute temperature current source;

a first op-amp having a first input connected to a node between the first resistance and the first diode, an output connected to the gate of a first transistor connected between a high voltage level and ground, wherein the first transistor is connected to ground though a second resistance and the second input of the first op-amp is connect to a node between the first transistor and the second resistance;

a second diode connected between ground and the high voltage level, wherein the second diode is connected to the voltage level by a first and a second leg, wherein:

the first leg includes a second transistor whose gate is connected to receive the output of the first op-amp; and

the second leg includes a third transistor connected in series with a resistive voltage divider, where the resistive voltage divider is connected between the second diode and the third transistor and a resistance whose value is the trimmable parameter; and

a second op-amp having an output connected to the gate of the third transistor, a first input connected to a node between the proportional to absolute temperature current source and the first resistance, and a second input connected to a node of the resistive voltage divider,

wherein the reference voltage is provided from a node between the third transistor and the resistive voltage divider.

20. The method of claim 19, wherein the resistive voltage divider of the circuit includes:

a third resistance connected between the second diode and said node of the resistive voltage divider; and

a fourth resistance connected between the third transistor and said node of the resistive voltage divider, wherein the fourth resistance is the resistance whose value is the trimmable parameter.

21. The method of claim 20, further comprising:

receiving a clock signal; and

alternating the connection of the first and second inputs for the second op-amp based upon the clock signal.

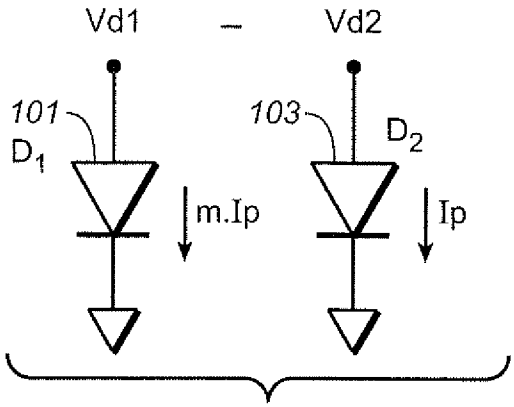


FIG. 1

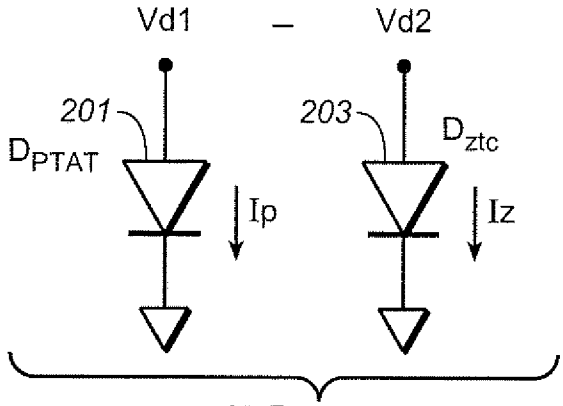


FIG. 3

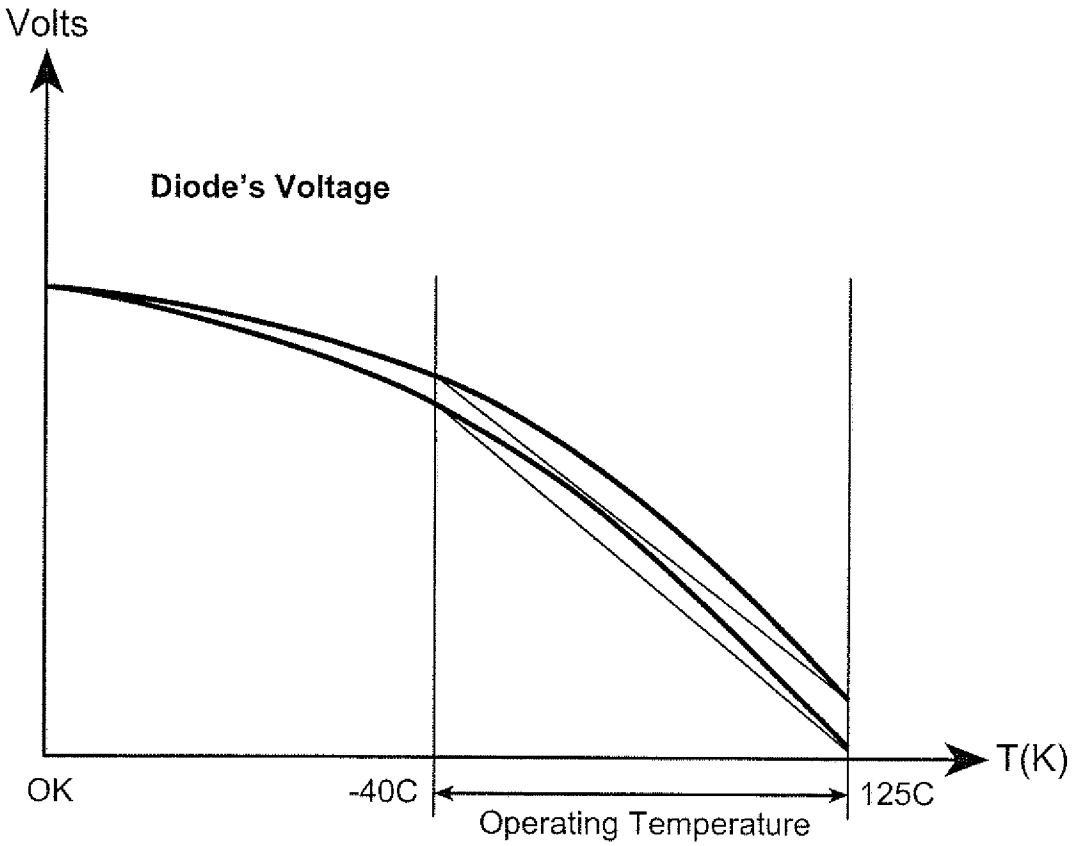
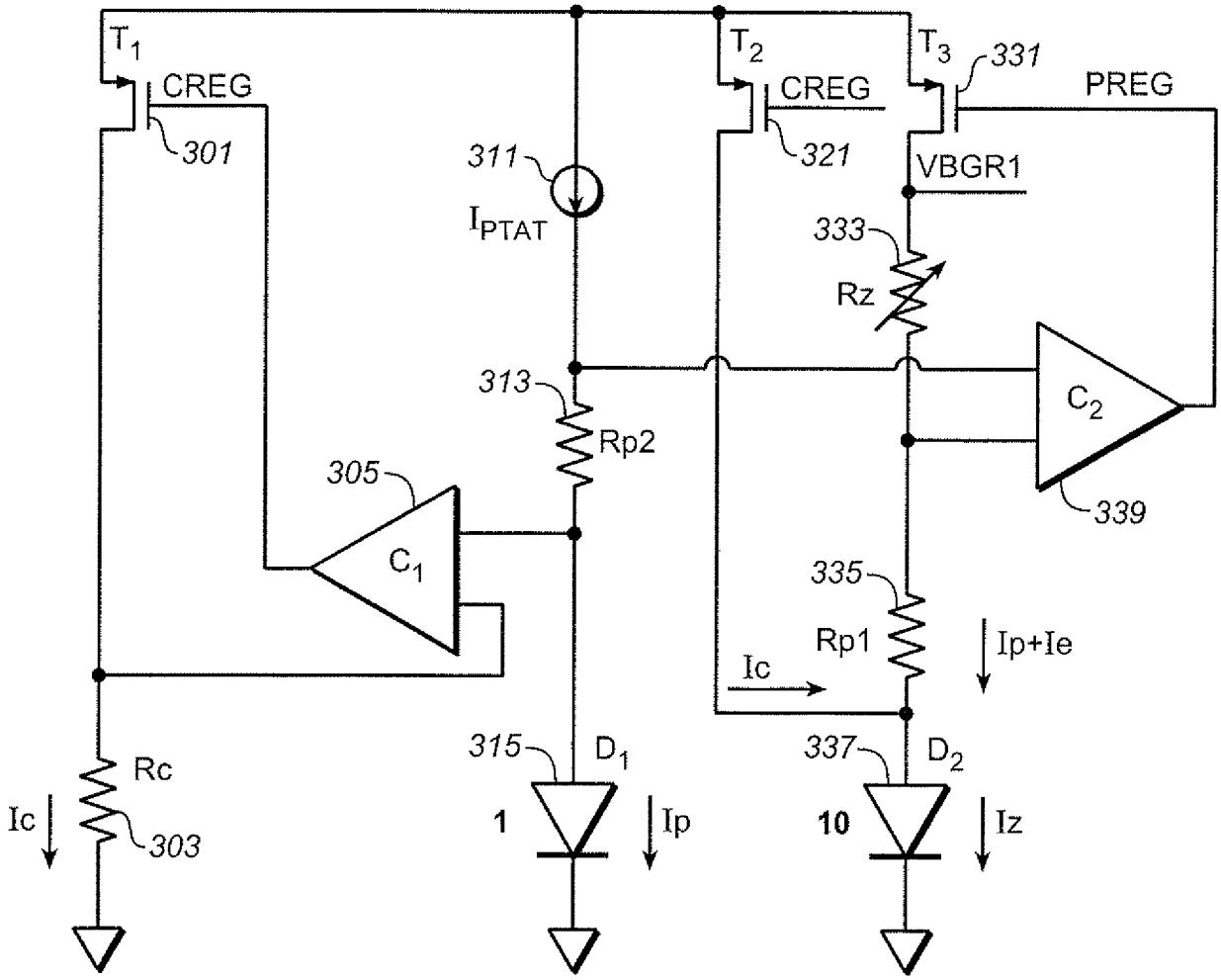


FIG. 2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339
305
C1
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Ic
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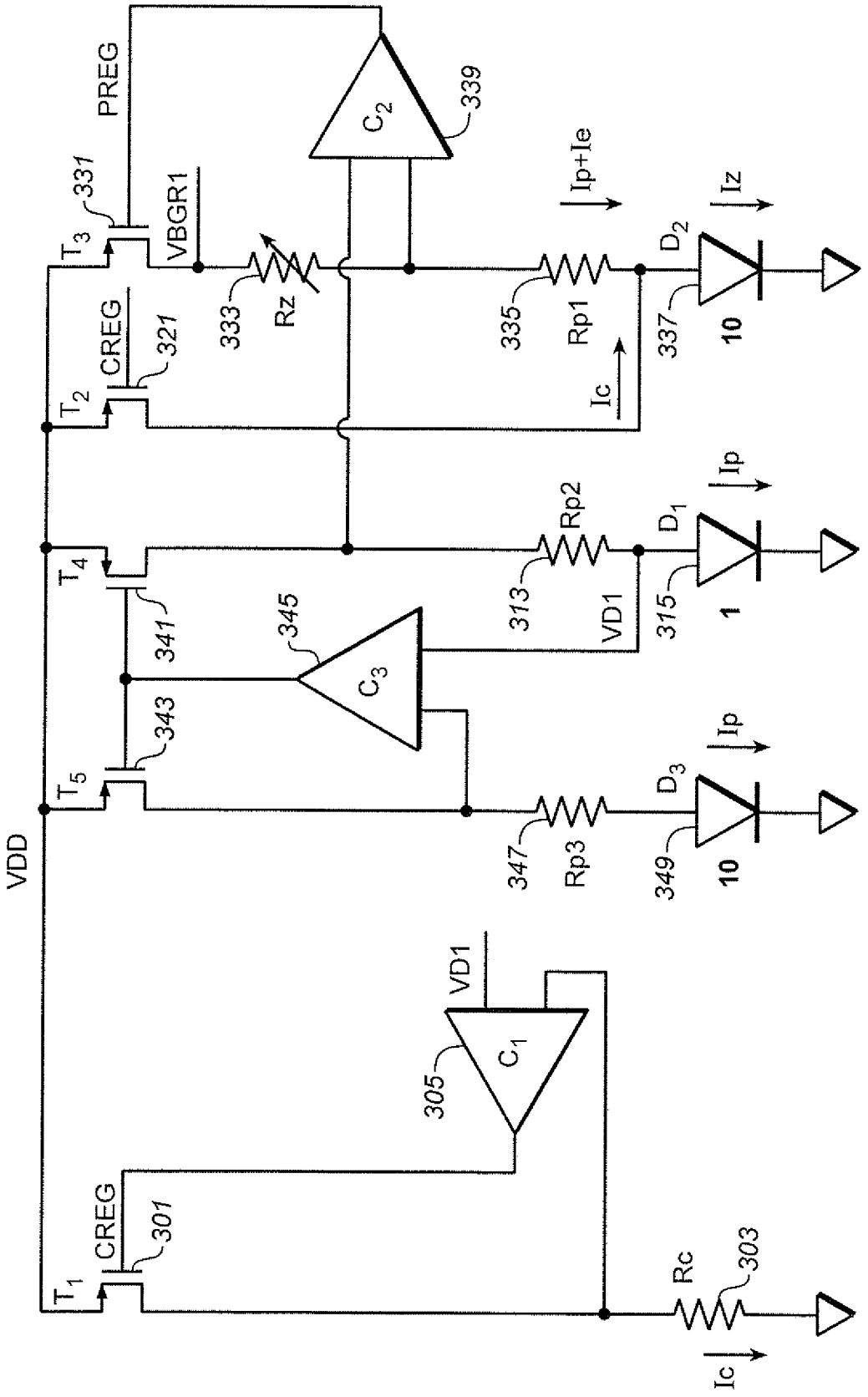
Rc
Ic
303

FIG. 4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Rp1
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Rp3
Rc
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D_2
D_3
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Iz
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FIG. 5

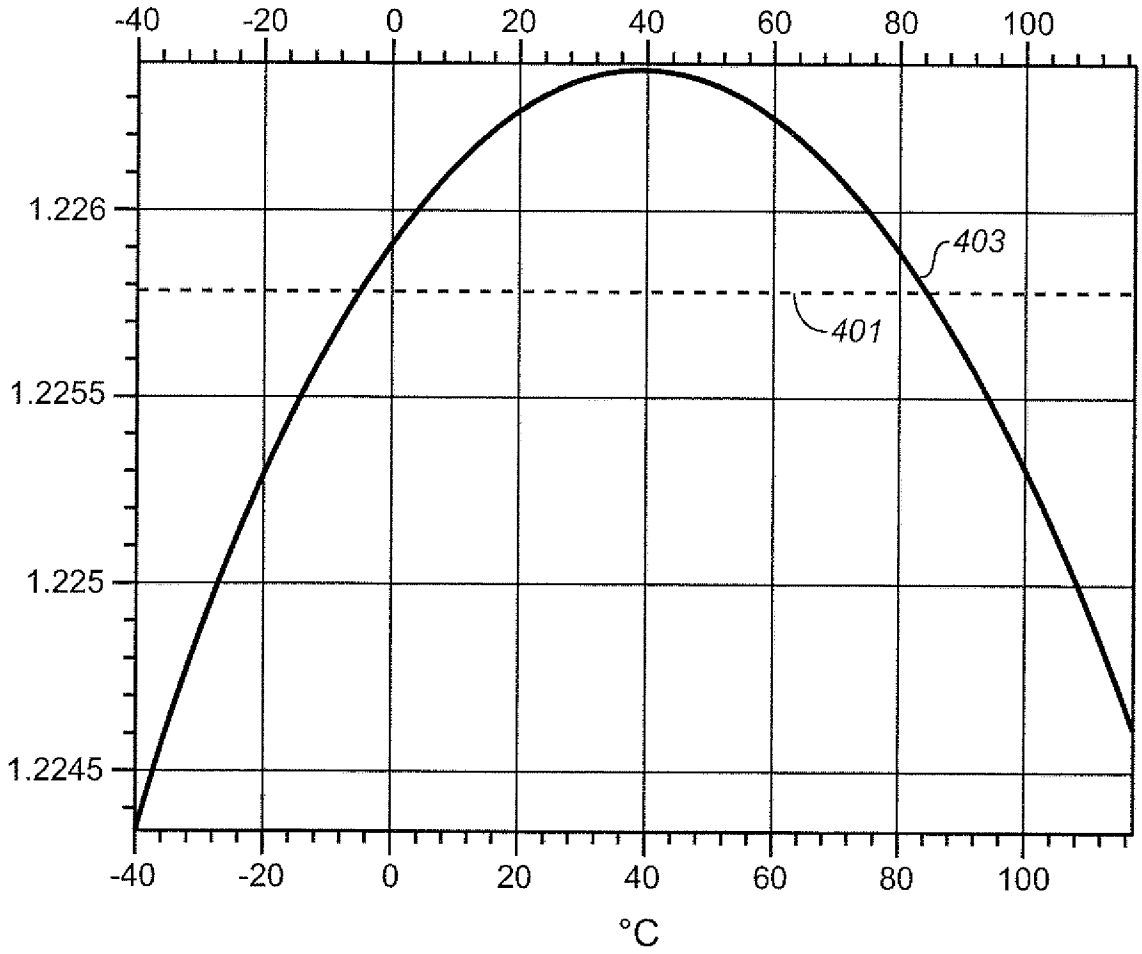
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FIG. 6

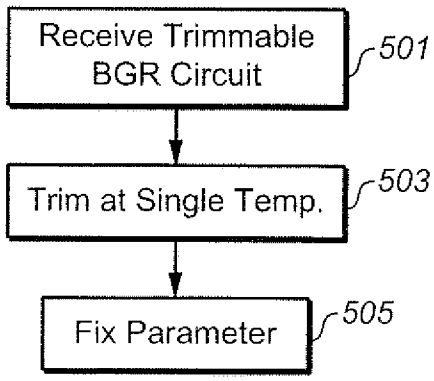

Receive Trimmable BGR Circuit
501
Trim at Single Temp.
503
Fix Parameter
505

FIG. 7

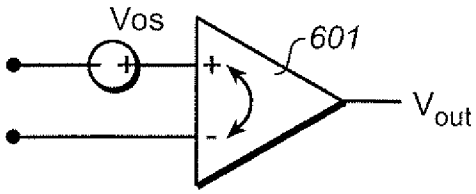


FIG. 8A

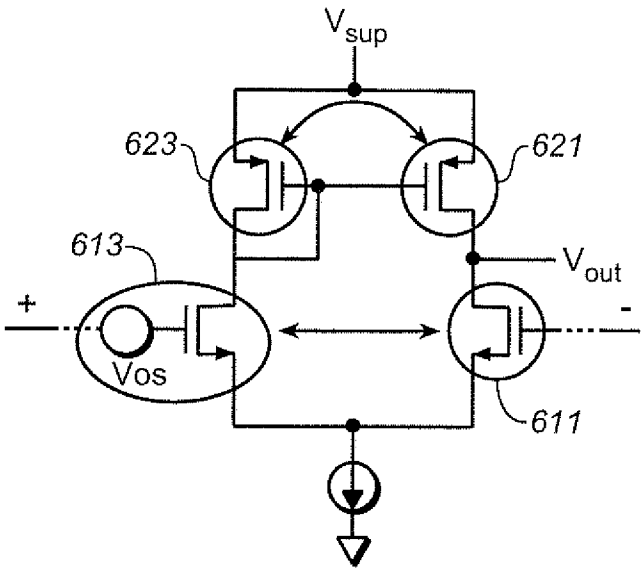


FIG. 8B

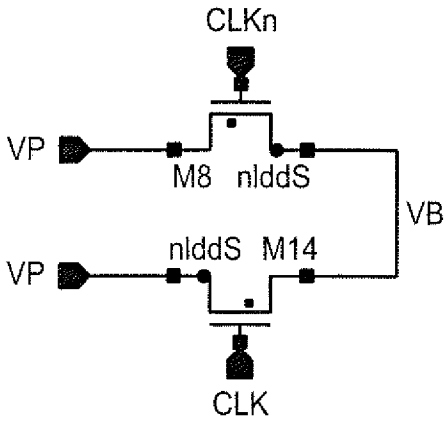


FIG. 9A

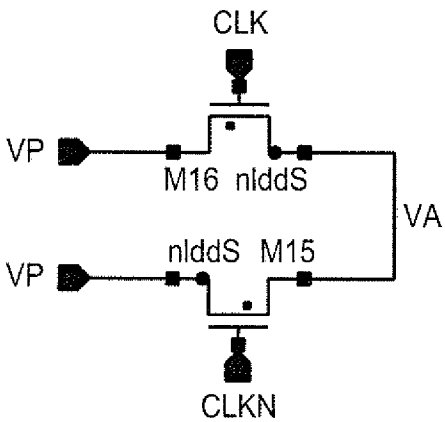
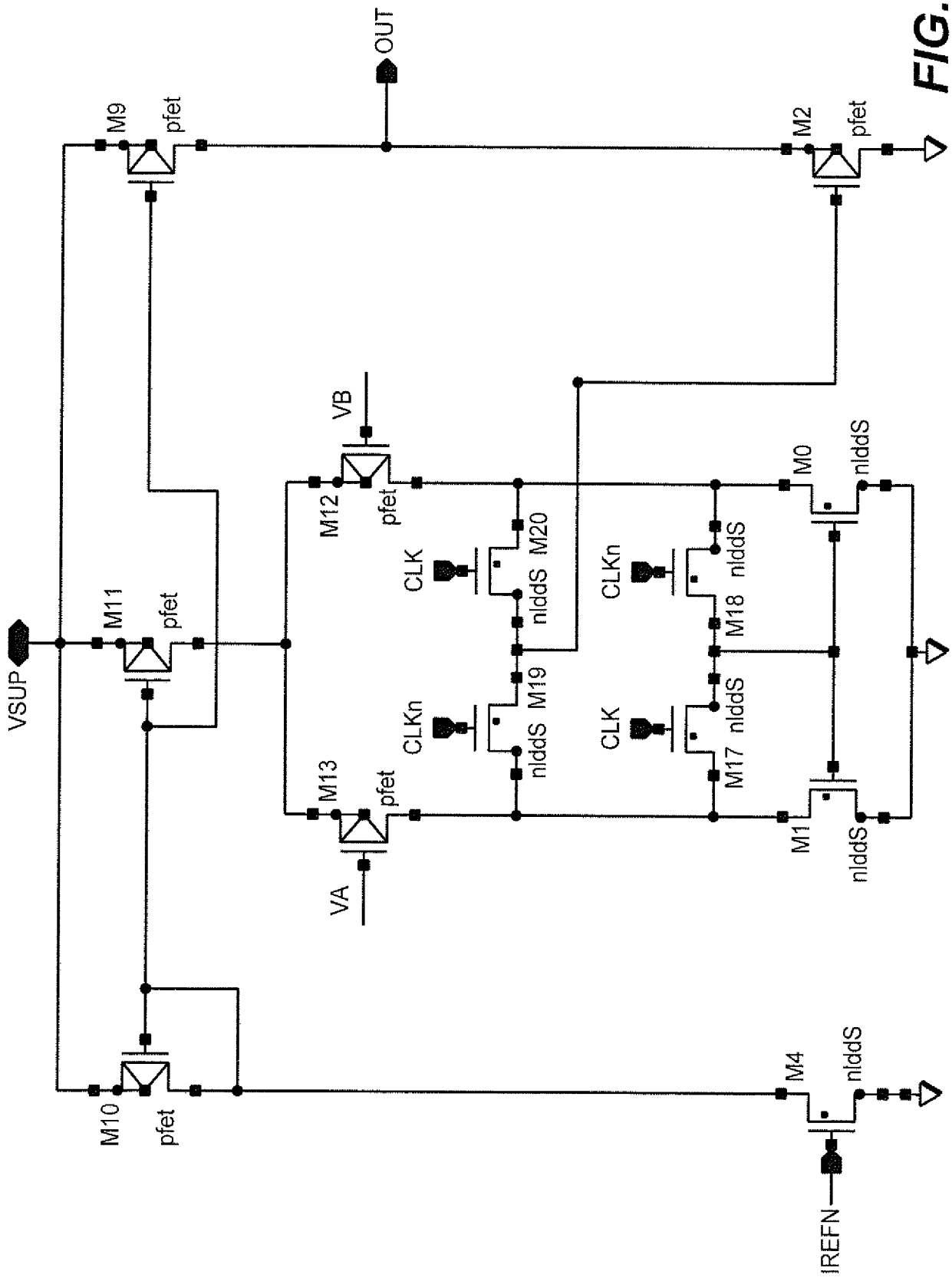


FIG. 9B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CLK
M17
nlddS
M13
pfet
VA
M1
nlddS
M10
pfet
M4
nlddS
IREFN

FIG. 9C