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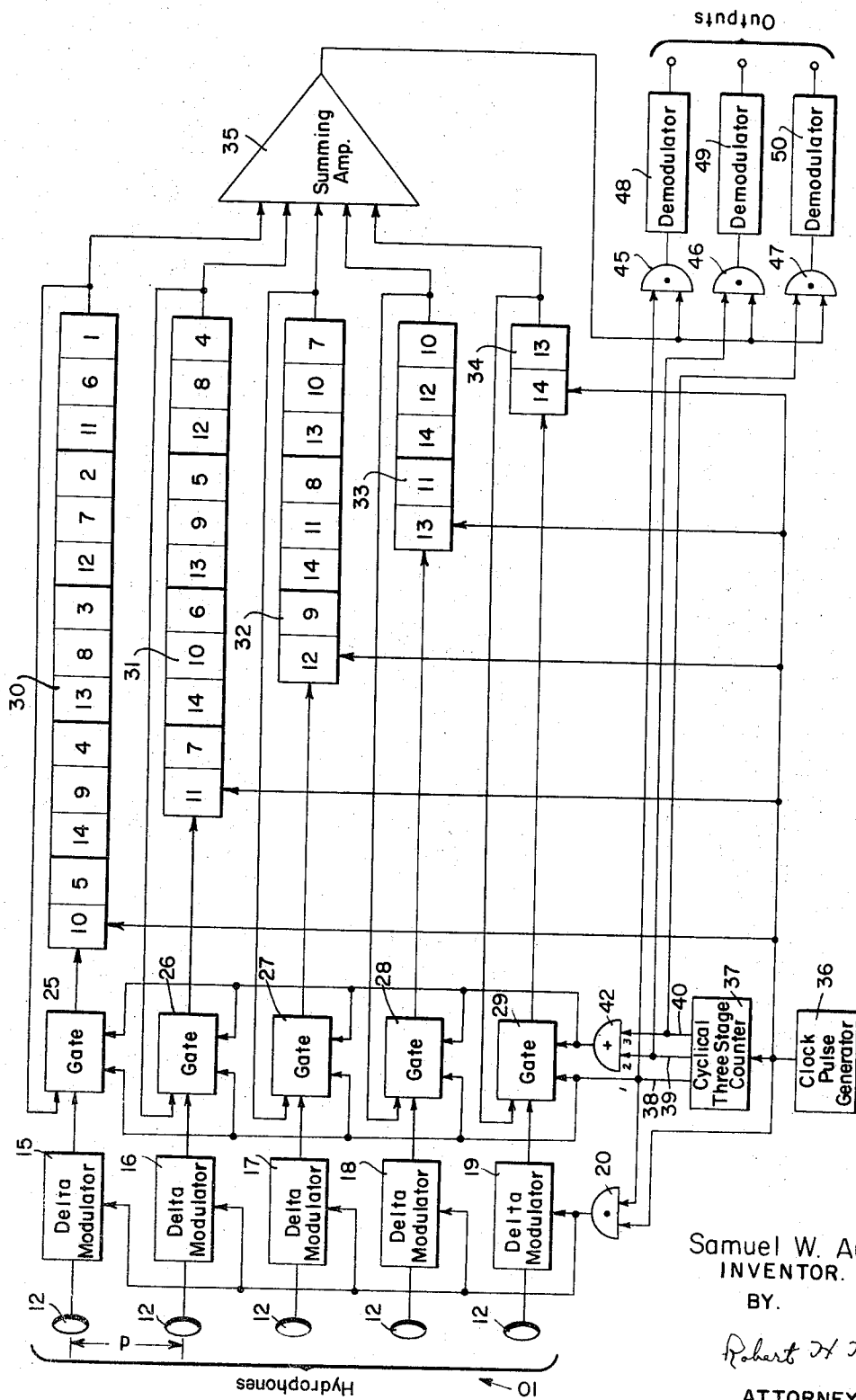
S. W. AUTREY

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ANALOG BEAM FORMING APPARATUS

Filed July 19, 1966

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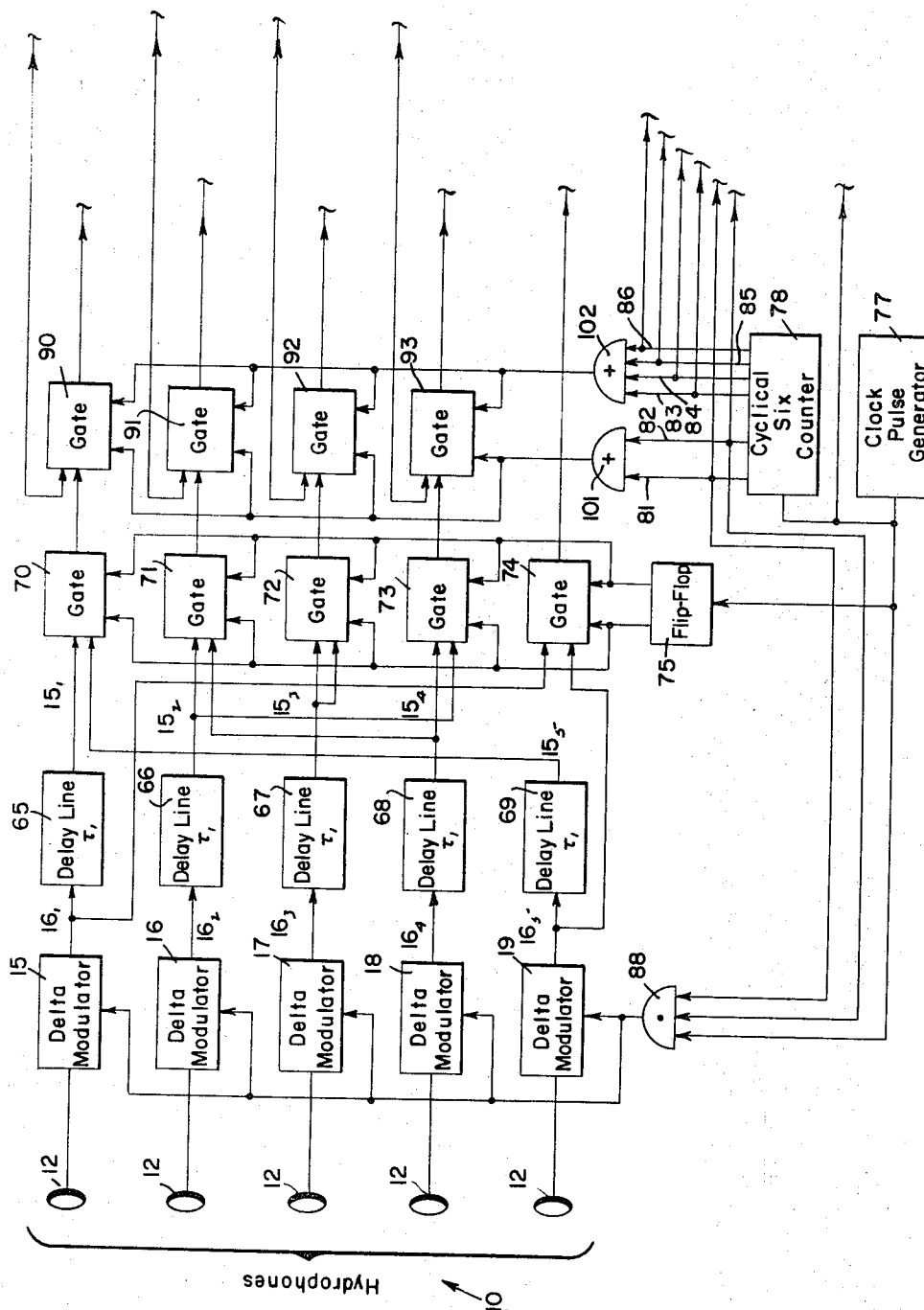


Fig. 2a.

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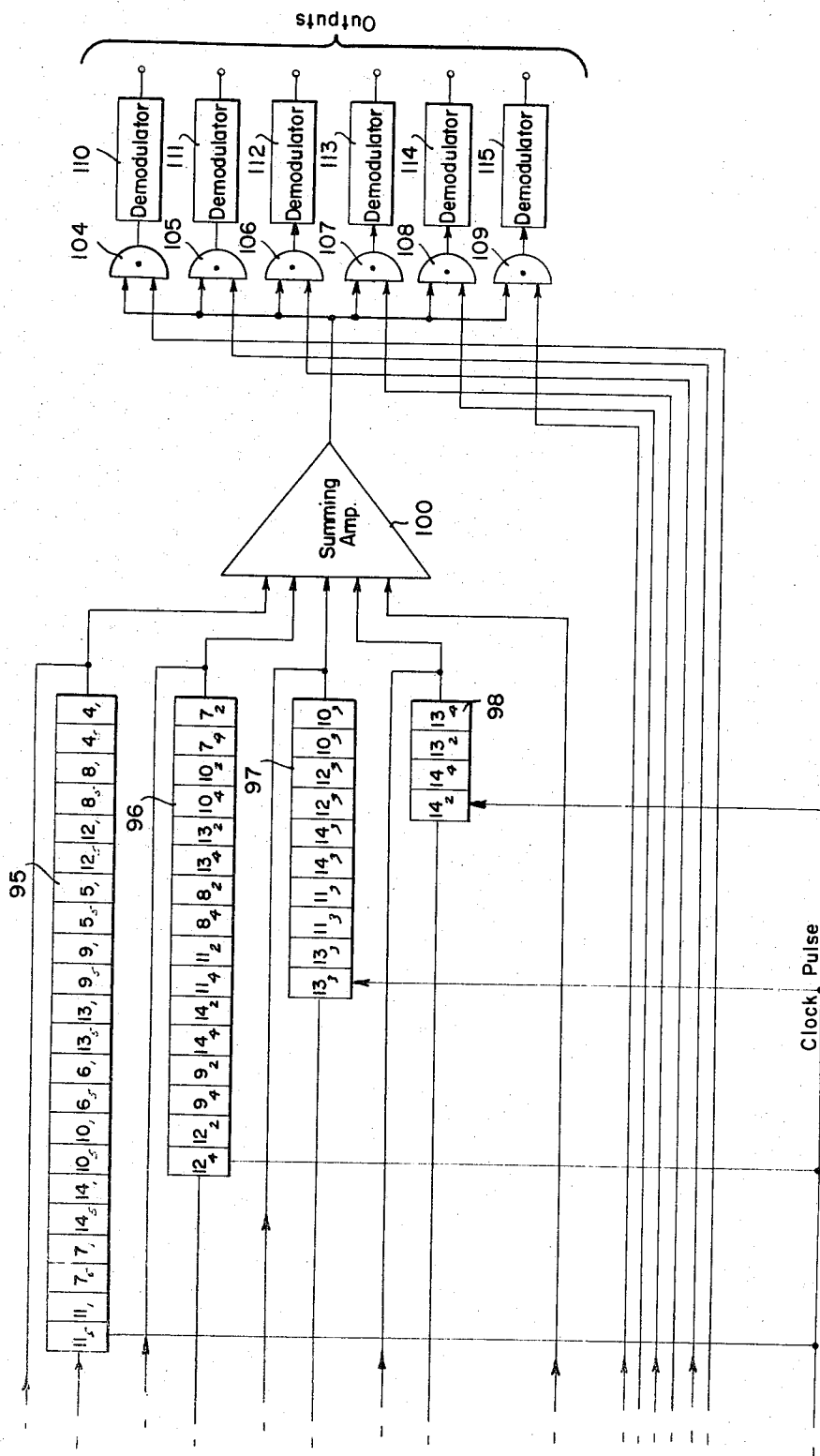


Fig. 2b.

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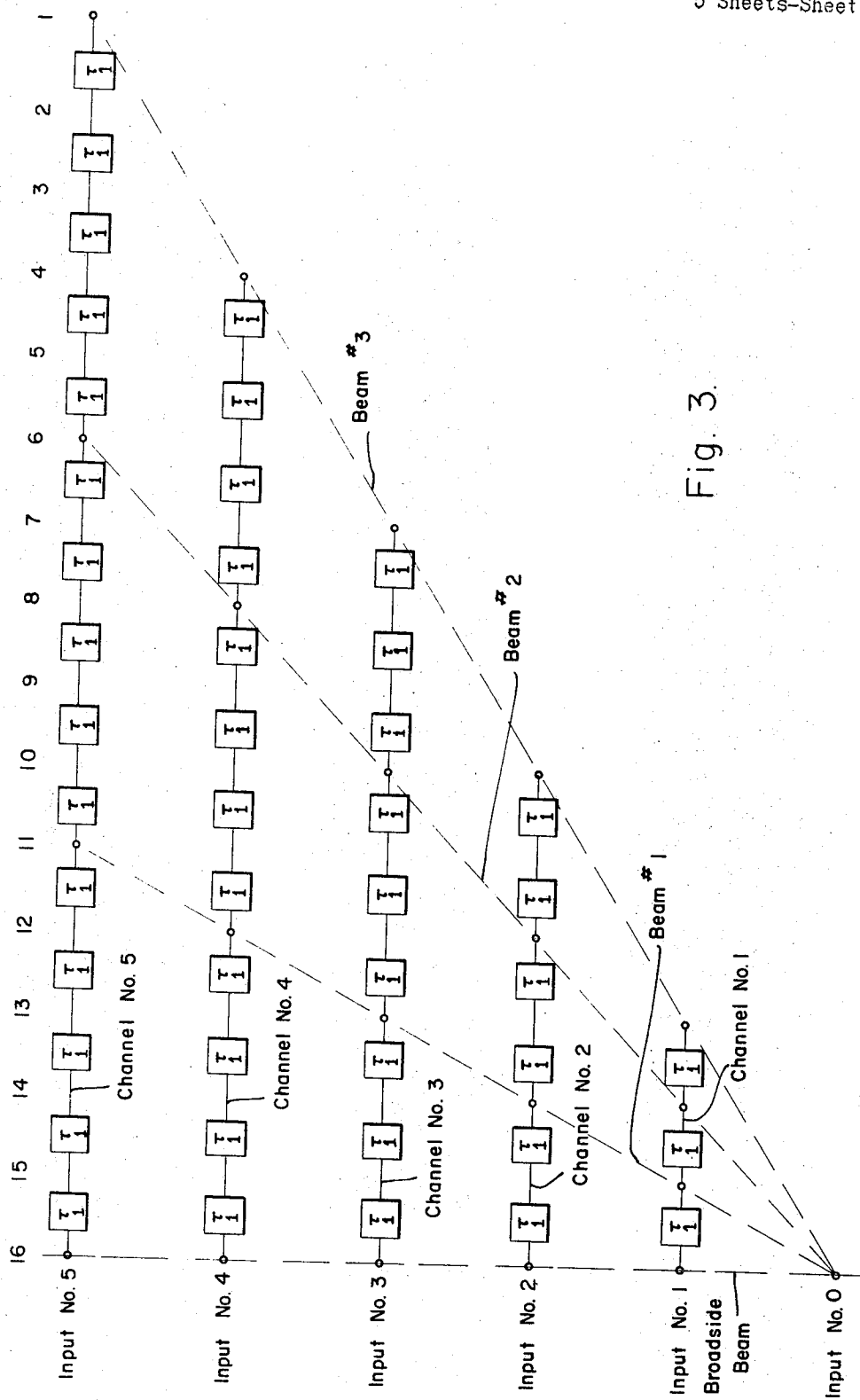


Fig. 3.

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Fig. 4.

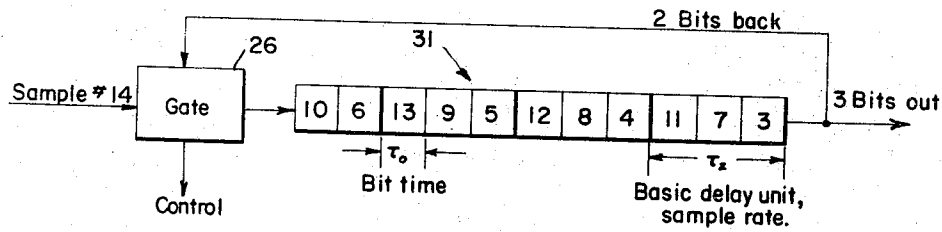


Fig. 5.

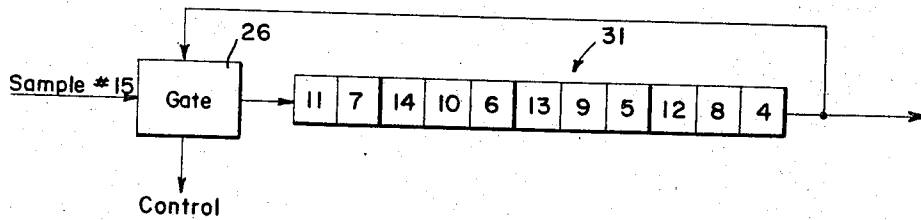


Fig. 6.

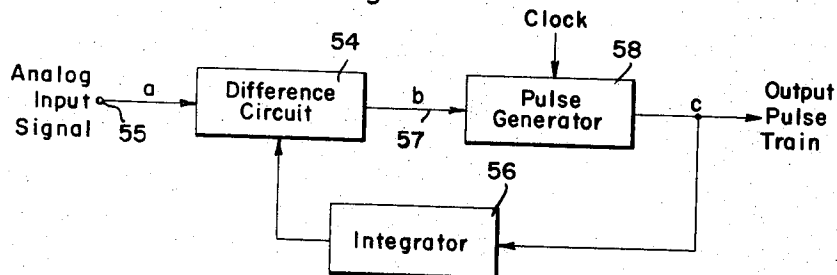
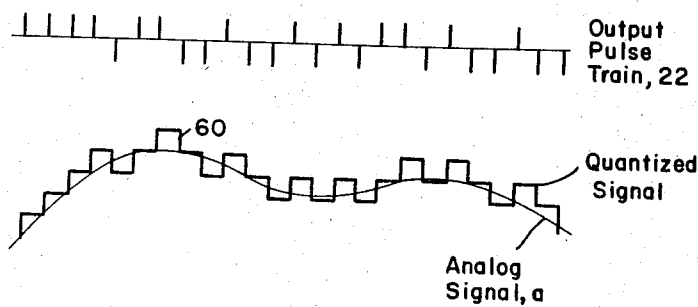


Fig. 7.



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ANALOG BEAM FORMING APPARATUS

Samuel W. Autrey, Fullerton, Calif., assignor to Hughes Aircraft Company, Culver City, Calif., a corporation of Delaware

Filed July 19, 1966, Ser. No. 567,327

8 Claims. (Cl. 340-6)

This invention relates to a broadband analog beam forming apparatus and more particularly to apparatus employing delay-line time-compressors together with digital multibeam steering to form a large number of beams simultaneously.

In contemporary digital beam forming apparatus, the inputs to the digital multibeam steering device are infinitely clipped so that only the zero crossings are preserved. Because the input signals are always quantized in time, however, some error in the determination of the zero crossings always occurs. Additional phase errors occur in contemporary digital multibeam steering devices built to date due to the overly large quantization of the delays provided in the shift registers, resulting in incorrect tap points. In addition to these implementation problems, problems inherent in the digital multibeam steering concept include a small degradation of signal-to-noise ratio, capture of digital multibeam steering signals by strong targets or own ships noise in the case of passive sonars, anomalous responses to certain frequencies at specified directions, and an intrinsic beam balance problem.

On the other hand, contemporary broadband analog beamforming apparatus will generally be found to be subject to degradation due to differential gains of the signal channels, dispersion effects, dissipation effects, and non-linear phase effects, and will often have only narrow-band capability or have low dynamic range. Additionally, it will generally be found that large numbers of summing networks or read heads are required in the implementation, leading to an intrinsic beam balance problem.

It is therefore an object of the present invention to provide an improved apparatus for forming broadband analog beams.

Another object of the invention is to provide a broadband analog beamforming apparatus for line arrays with equally spaced elements yielding beams with equal crossover levels.

Still another object of the present invention is to provide an analog beamforming apparatus having none of the aforementioned implementation problems that are characteristic of conventional systems employing broadband multibeam steering.

A further object of the invention is to provide a broadband beamformer apparatus which utilizes a sufficiently high sample frequency together with delta modulators and demodulators to convert the beamformer from a digital multibeam steering to an analog beamformer.

In accordance with the present invention, the output signals from a linear array of elements are applied to corresponding delta modulators to produce respective series of binary 1's and 0's at a clock rate substantially higher than the highest frequency component of the signals applied thereto. The delta modulators generate binary 1's at the clock rate when the signal is greater than the integrated output of the modulator and binary 0's at the clock rate when the signal is less than the integrated output of the modulator. The single bit binary numbers are applied to delay-line time-compressors of progressively increasing lengths and which provide successive samples that differ by one fundamental delay period in adjacent channels. In operation, the single bit binary numbers for each beam become concurrently

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available from the respective outputs of the delay-line time-compressors thereby enabling them to be summed sequentially during each fundamental delay unit of time and directed to demodulators corresponding to the individual beams.

The above-mentioned and other features and objects of this invention and the manner of obtaining them will become more apparent by reference to the following description taken in conjunction with the accompanying drawings, wherein:

FIG. 1 illustrates a schematic block diagram of an embodiment of the invention for five inputs and three off-broadside beams in one quadrant;

FIG. 2 (divided into FIGS. 2a and 2b) illustrates a schematic block diagram of an embodiment of the invention for five inputs and six off-broadside symmetrically disposed beams in two adjacent quadrants;

FIG. 3 illustrates the proportional delays required to generate beams having equal crossover levels;

FIGS. 4 and 5 illustrate the operation of a delay-line time-compressor for input No. 4 in the situation of FIG. 3;

FIG. 6 shows a schematic block diagram of a typical delta modulator in the apparatus of FIG. 1; and

FIG. 7 illustrates an example of an output pulse train from a delta modulator together with other waveforms in the apparatus of FIG. 6.

In describing the apparatus of the present invention, a convention is employed wherein individual "and" and "or" gates are shown as semicircular blocks with the inputs applied to the straight side and the output appearing on the semicircular side. An "and" gate is indicated by a (·) and an "or" gate by a (+) in the semicircular block. In the present case, an "and" gate produces a 1 or information level output signal when every input differs from the 0 level and an "or" gate produces a 1 or information level output signal when a single input differs from the 0 level.

Referring now to FIG. 1 of the drawings, there is shown, by way of example, embodiment of the present invention which operates in response to a linear array 10 of five hydrophones 12. The apparatus as shown is adapted for illustrative purposes to generate only 3 off-broadside beams in only one quadrant. In particular, the hydrophones 12 are uniformly spaced at a distance d apart and are immersed in a medium wherein energy has a propagation velocity c . Angles relative to the linear array 10 are measured from the normal thereto. Thus, a wavefront is said to be incident on the linear array 10 at the angle φ as measured between a normal to the linear array 10 and the direction of propagation of the wavefront.

Output signals from the five hydrophones 12 are applied to respective inputs of delta modulators 15, 16, 17, 18 and 19. In addition, each delta modulator 15-19 receives a clock pulse input from the output of an "and" gate 20. The clock pulse rate employed should be many times the highest signal frequency for which the apparatus is designed. The function of the delta modulators 15-19 is then to convert an input thereto into a series of binary 1's and binary 0's as determined approximately by whether the input signal increased or decreased, respectively, during the period since the occurrence of the prior clock pulse. A typical output pulse train 22 is shown in FIG. 7 of the drawings. In the output pulse train 22, the positive excursions are considered to be binary 1's and the negative excursions binary 0's. The binary 0's may be eliminated entirely if this is compatible with the digital circuitry employed in the remainder of the system.

Output pulse train 22 generated by the delta modulators 15-19 are applied, respectively, to one input of 2-input gates 25, 26, 27, 28 and 29. The outputs from

gates 25-29 are, in turn, connected, respectively, to the inputs of delay-line time-compressor lines 30, 31, 32, 33 and 34. The outputs of each of the delay-line time-compressor lines 30-34 are applied to the inputs of a summing amplifier 35 and, in addition, are each connected back to the remaining input of the corresponding gates 25-29. A clock pulse generator 36 develops synchronizing pulses which are applied to each of the delay-line time-compressors 30-34 and in addition, are applied to one input of the "and" gate 20 and to the input of a cyclical-three counter 37. The cyclical-three counter 37 develops information level output signals in rotation on three output leads 38, 39 and 40 in response to synchronizing pulses from clock pulse generator 36. Output leads 39, 40 from the cyclical-three counter 37 are applied to the inputs of a 2-input "or" gate 42 whereby the output therefrom is at information level for two successive counts out of every three generated by the counter 37. The output lead 38 from counter 37 is applied to the remaining input of "and" gate 20 and to a control input of each of the gates 25-29 so as to gate the output of the delta modulators 15-19 through to the respective inputs of the delay-line time-compressors 30-34 during count 1 of the cyclical counter 37. The output from the "or" gate 42 is applied to the remaining control inputs of gates 25-29 whereby the outputs of the respective delay-line time-compressors 30-34 are gated through to the respective inputs thereof during these intervals. In addition, the output leads 38, 39 and 40 of cyclical counter 37 are applied, respectively, to one input of 2-input "and" gates 45, 46 and 47, the output of summing amplifier 35 being applied to the remaining inputs thereof. The outputs of the "and" gates 45, 46 and 47 are then connected to respective inputs of demodulators 48, 49, 50, respectively, the outputs from which each constitute successive components of the three off-broadside beams. The demodulators 48, 49, 50 convert successive sums of binary 1's and 0's appearing at the output of summing amplifier 35 into respective analog signal outputs for the three off-broadside beams of the apparatus of the present invention. A broadside beam may, of course, be formed continuously by connections directly to the hydrophones 12 of the linear array 10.

An array factor, A , (beam pattern) for an unshaded linear array 10 of n equally spaced elements or hydrophones 12 is given by Equation 1 as follows:

$$A = \frac{1}{n} \frac{\sin \frac{n\psi}{2}}{\sin \frac{\psi}{2}} \quad (1)$$

where ψ is the number of electrical degrees by which the n input signals progressively differ from each other at the point of summation. In the present case:

$$\psi = \frac{2\pi d}{\lambda} \sin(\varphi) + \delta \quad (2)$$

where λ is the signal wavelength in the medium with propagation velocity c , and δ is the beamformer phase shift between adjacent inputs.

With n fixed, it is evident from Equation 1 that the array factor, A , is dependent only on ψ . The converse, however, is true only over the limited range where A approximates unity in which case the principal value of ψ is determined except for its sign. To obtain an overlapping pattern of beams for which the array factor has some specified value, A_0 , at the beam crossover points, the corresponding electrical angle, $\pm\psi_0$, must exist at the crossover points. The beam steering angles are numbered and measured from broadside with the broadside beam being number zero. The beam steering angles yielding equal crossover levels are readily determined by equating the upper crossover point of the i^{th} beam, φ_i^+ , with the

lower crossover point of the $(i+1)^{\text{st}}$ beam, $\varphi_{i+1}^- + 1$. Thus, it can be shown that the time delays for each input are:

$$\tau_i = \frac{d}{c} \cdot \frac{2}{r} \cdot i \quad (3)$$

where r is the number of off-broadside beams in both quadrants. From Equation 3 the time delay, τ_1 , between two adjacent inputs is:

$$\tau_1 = \frac{2d}{cr} \quad (4)$$

The delay τ_1 is referred to as the basic delay period. All of the required delays are multiples of this basic delay, τ_1 , as will be hereinafter explained in more detail in connection with FIG. 3. It can be shown, by way of example, that -3 db beam crossovers are obtained at the frequency for which the array element spacing is one-half wavelength if the number of off-broadside beams is $\frac{1}{2}$ the number of array elements 12, i.e., $r/n = \frac{1}{2}$.

Referring to FIG. 3, there is shown the necessary requirements for the basic delay unit τ_1 to provide $r/2 = 3$ beams per quadrant where r is the number of off-broadside beams in the half space on one side of the linear array 10. In particular, inputs Nos. 1, 2, 3, 4, 5 receive signals, respectively, from hydrophones 12 of the linear array 10, FIG. 1. Each input m , where m assumes successive values from 1 to 5 of the input Nos. 1, 2, 3, 4, 5, is connected to one extremity of progressively increasing series connected groups of basic delay units, τ_1 , constituting channels 1 to 5, respectively. That is, the number of groups of the basic delay units, τ_1 , connected to each input is equal to the number of off-broadside beams per quadrant, i.e., for three off-broadside beams per quadrant there are three groups of basic delay units, τ_1 , connected to each input. In addition, there are m series connected basic delay units τ_1 , in each group thereof where m , as before, assumes successive values from 1 to 5 for channels 1 to 5, respectively. Binary signal samples are available at the output of each group of the basic delay units, τ_1 , with that at the initial and hence maximum delay component designated as 1. The groups of basic delay units τ_1 of channel No. 5 provide signal samples, or equivalently, delays defined by 1, 6, 11 and 16, FIG. 3. Similarly, signal samples or delays defined by 4, 8, 12 and 16, FIG. 3, are provided by channel No. 4; delays defined by 7, 10, 13 and 16 are provided by channel No. 3; delays defined by 10, 12, 14 and 16 are provided by channel No. 2; and delays defined by 13, 14, 15 and 16 are provided by channel No. 1. Concurrent beams Nos. 1, 2 and 3 are formed by combining samples defined by (11, 12, 13, 14, 15), (6, 8, 10, 12, 14) and (1, 4, 7, 10, 13), respectively. As specified above, the number of off-broadside beams per quadrant available is equal to the number of groups of basic delay units τ_1 in each channel No. 1, 2, 3, 4, 5.

It is to be noted that the broadside beam combines components that are of zero time difference, and beams Nos. 1, 2 and 3 combine components that successively increase by one, two and three basic delay periods, respectively. In order to achieve this result, it is only necessary that each group of basic delay units τ_1 differ by one basic delay period from groups of basic delay units, τ_1 , in immediately adjacent channels. That is, channels corresponding to inputs Nos. 1, 2, 3, 4 and 5 can be used just as effectively as channels corresponding to inputs Nos. 0, 1, 2, 3 and 4 or inputs Nos. 2, 3, 4, 5 and 6.

Referring again to FIG. 1 of the drawings, input energy from hydrophones 12 of linear array 10 is converted to a series of binary 1's and 0's by the delta modulators 15-19 thereby enabling digital circuitry to be employed. In addition, all of the groups of basic delay units, τ_1 , in each of the channels, Nos. 1-5 shown in FIG. 3, are replaced by delay-line time-compressors 30-34.

These delay-line time-compressors 30-34 may be magnetostrictive delay lines or of the shift register type such as those employing magnetic cores or transistors. The speed of operation of the delay-line time-compressors 30-34 is set at the sample rate of the delta modulators 15-19 times the number of off-broadside beams. By way of example, the operation of delay-line time-compressor 31 of FIG. 1 is shown in FIGS. 4 and 5. In particular, the length of delay-line time-compressor 31 is one bit time less than one group of basic delay units τ_1 in channel No. 4, FIG. 3. A bit time is defined as the basic delay period provided by τ_1 divided by the number of off-broadside beams in one quadrant. In the case of the apparatus of FIG. 1, three bit intervals, τ_0 , equal one basic delay unit, τ_1 , whereby delay-line time-compressor 31 includes eleven bit time intervals, τ_0 . In operation, gate 26 cyclically inserts a new sample into the line 31 and then recirculates two bits from the output. Referring to FIG. 4, there is shown the sequence of samples in line 31 just prior to receiving sample No. 14. FIG. 5 then shows the sequence of samples in line 31 just prior to receiving sample No. 15. It is to be especially noted that the samples 4, 8, 12 available during the next basic delay period τ_1 are identical to those available at the contacts between the groups of basic delay units τ_1 in channel No. 4 at the time shown.

Referring now to FIG. 1, the lines 30-34 are each one bit time shorter than the groups of basic delay units, τ_1 in the respective channels Nos. 5, 4, 3, 2, 1, FIG. 3 and operate in the same manner as described in connection with line 31, FIGS. 4 and 5. The lines 30-34, FIG. 1 show samples just prior to sample No. 15, which samples are identical to those available at the contacts of the apparatus of FIG. 3. That is, during the next basic time period samples (1, 4, 7, 10, 13), (6, 8, 10, 12, 14) and (11, 12, 13, 14, 15) which correspond to beams 3, 2, and 1, respectively, are applied in sequence to the inputs of summing amplifier 35. The output from summing amplifier 35 is applied to each of the "and" gates 45, 46, 47 which are cyclically opened by counter 37. Thus, successive samples for only one beam appear at the output of each "and" gate 45, 46, 47.

An example of a delta modulator of the type employed as delta modulators 15-19, FIG. 1, is shown in FIG. 6. In particular, the delta modulator includes a difference circuit 54 which receives an analog input signal at an input 55 and a signal from the output of an integrator 56 and develops an output signal on a lead 57 of a polarity dependent upon the magnitude of the analog input signal relative to that of the output of integrator 56. The output lead 57 from difference circuit 54 is applied to a pulse generator 58 along with clock pulses from the output of "and" gate 20. Pulse generator 58 develops a pulse concurrently with the occurrence of every clock pulse and of a polarity that is the same as that applied thereto from the difference circuit 54. Output pulse train 22, FIG. 7, is a representative output of pulse generator 58. In addition to providing an output from the delta modulator, the output of pulse generator 58 is applied back to integrator 56. In operation, the integrator 56 provides an output waveform such as waveform 60, FIG. 7, which increases in amplitude every time a positive pulse occurs and decreases in amplitude upon the occurrence of a negative pulse in output pulse train 22. The waveform 60 thus generated is referred to as a quantized signal. The difference circuit 54 compares the amplitude of the analog input signal with that of the quantized signal 60 to determine the polarity of the successive pulses generated by clock pulse generator 58 which pulses constitute the output pulse train 22.

Referring now to FIG. 2 of the drawings, there is shown an embodiment of the invention responsive to the linear array 10 of equally spaced hydrophones 12 and the delta modulators 15-19 for generating three off-broadside symmetrically disposed beams in adjacent quadrants. In ad-

dition, delay-line time-compressors corresponding to channels Nos. 1-4, FIG. 3, are used which necessitates the use of delay lines having a basic delay period τ_1 following the delta modulators 15-19. In particular, delta modulators 15-19 receive inputs from the hydrophones 12 of linear array 10 in the same manner as in the apparatus of FIG. 1. Delta modulators 15-19 are connected to delay lines 65-69, each of which provide a basic delay period, τ_1 . Gates 70-74 alternately provide a signal component for a beam in one quadrant and then for a symmetrically disposed beam in the adjacent quadrant. To achieve this, the output of delay lines 65-68 are connected to corresponding inputs of gates 70-73, respectively. In addition, the output of delta modulator 19 is connected directly to the corresponding input of gate 74. Secondly, delay lines 69, 68, 67, 66 are connected to remaining inputs of gates 70, 71, 72 and 73, respectively. Lastly, the output of delta modulator 15 is connected directly to the remaining input of gate 74. The principal and complementary outputs of a flip-flop 75 are connected to the control inputs of the gates 70-74. Thus, when an information level signal appears at the principal output of flip-flop 75, outputs from the delay lines 65-68 and the outputs from delta modulator 19 appear at the output of gates 70-74, respectively. Alternately, when an information level signal appears at the complementary output of flip-flop 75, outputs from the delay lines 69, 68, 67, 66 and the delta modulator 15 appear at the outputs of gates 70-74, respectively.

A clock pulse generator 77 is connected to the input of flip-flop 75, thereby to cause it to change state every bit interval of operation. In addition, clock pulses from clock pulse generator 77 are applied to the input of a cyclical-6 counter 78. Cyclical-6 counter 78 provides information level signals in rotation on leads 81, 82, 83, 84, 85 and 86. Leads 81 and 82 are connected to the inputs of an "and" gate 88 along with the output of clock pulse generator 77 whereby clock pulses appear at the output thereof only during count intervals 1 and 2. The output of "and" gate 88 is connected to the delta modulators 15-19 thereby to control the sampling intervals thereof.

The outputs from gates 70-73 are connected to corresponding inputs of gates 90 and 93. The outputs of gates 90-93 are, in turn, connected to the inputs of delay lines 95, 96, 97, 98, respectively, the outputs from which are connected back to a remaining input of corresponding gates 90-93. In addition, the outputs from delay lines 95-98 along with the output of gate 74 are connected to inputs to a summing amplifier 100. The delay lines 95-98, as before, may be of the magnetostrictive or shift register type and receive synchronized pulses directly from the clock pulse generator 77. In the present case, the delay lines 95-98 are time shared between two quadrants, whereby the bit interval in the apparatus of FIG. 2 is necessarily one-half that of FIG. 1. Thus, the delay lines 95-98 have 6 bit times per each basic delay unit, τ_1 . In addition, delay line 95 is 2 bit times less than four basic delay units, τ_1 ; delay line 96 is 2 bit times less than three basic delay units, τ_1 ; delay line 97 is 2 bit times less than two basic delay units, τ_1 ; and delay line 98 is 2 bit times less than one delay unit, τ_1 . The gates 90-93 are operated in a manner to insert two new samples into the delay lines 95-98, respectively, and then circulate four samples from the respective outputs thereof. This may be achieved by connecting the outputs leads 81-82 from cyclical counter 78 through an "or" gate 101 to corresponding control inputs of the gates 90-93. In addition, outputs leads 83, 84, 85, 86 are connected through an "or" gate 102 to the remaining control inputs of the gates 90-93.

Lastly, the output from summing amplifier 100 is connected through one input of 2-input "and" gates 104, 105, 106, 107, 108, 109, to the respective inputs of demodulators 110, 111, 112, 113, 114 and 115, the outputs from which constitute the channels for the six symmetrically disposed beams of the present invention. The outputs

from the "and" gates 104-109 are gated on in rotation by connections to the remaining inputs thereto from the outputs leads 81-86 of cyclical counter 78.

The operation of the apparatus of FIG. 2 is generally the same as that of FIG. 1, with the exception that a bit time in the apparatus of FIG. 2 is $\frac{1}{2}$ that of the apparatus of FIG. 1, thereby enabling the delay lines 95-98 to be time shared. This time sharing is achieved by taking two successive samples out of every six by means of the output leads 81-82 of cyclical counter 78 being applied through "and" gate 88 to the delta modulators 15-19. The sequence of the linear array 10 is alternately reversed by the operation of the gates 70-74, whereby each pair of samples constitute components from symmetrically disposed beams in adjacent quadrants.

The samples shown in delay lines 95-98 correspond to delay lines 31-34, FIG. 1, and to channels Nos. 4, 3, 2 and 1 of FIG. 3. In order to provide the 5th sample; i.e., in order to utilize input No. 0, FIG. 3, it is necessary to generate sample No. 16, FIG. 3. This is accomplished by the basic unit delay lines 65-69. In that different components are fed into different channels, the channels are numbered 1 to 5 from top to bottom. The numbers identifying the channels are hereinafter used as subscripts to numbers designating samples. Using this notation, the beams formed during the next six bit intervals commencing from the samples shown in the delay lines 95-98 are: ($4_1, 7_2, 10_3, 13_4, 16_5$), ($4_5, 7_4, 10_3, 13_2, 16_1$), ($8_1, 10_2, 12_3, 14_4, 16_5$), ($8_5, 10_4, 12_3, 14_2, 16_1$), ($12_1, 13_2, 14_3, 15_4, 16_5$) and ($12_5, 13_4, 14_3, 15_2, 16_1$). As can be seen by comparing these samples with the illustration in FIG. 3, delay times corresponding to inputs 0, 1, 2, 3 and 4 for generating beams Nos. 1, 2 and 3, together with the mirror images thereof, are provided. As before, a broadside beam can be developed by using outputs directly from the delta modulators 15-19. The summing amplifier 100 and subsequent demodulating are the same as in the apparatus of FIG. 1.

An apparatus with only five inputs and three off-broadside beams in each quadrant has been shown and described for the purpose of illustration. In a practical embodiment, it is contemplated that a linear array having 35 elements with half wavelength spacing at 400 cycles per second would be employed to generate 66 off-broadside beams. Under these circumstances, a sample frequency of $400 \times 66 = 26,400$ cycles per second would be required together with a delay-line time-compressor clock frequency of 1.7424 megacycles. This apparatus would then require delays from 36.7 to 1287.3 microseconds.

Although the invention has been shown in connection with a certain specific embodiment, it will be readily apparent to those skilled in the art that various changes in form and arrangement of parts may be made to suit requirements to enable the invention to be used with arrays of hydrophones, geophones, microphones or other form of transducer or the length of time-compressor delay-lines modified to yield different sample sequences all without departing from the spirit and scope of the invention.

What is claimed is:

1. An apparatus for forming a predetermined number of analog beams from signals received from a plurality of transducer elements disposed in a linear array, said apparatus comprising means coupled to each of said plurality of transducer elements for converting said signals therefrom into a series of pulse trains of binary 1's and 0's as determined by whether the amplitude of said signals is increasing or decreasing, the clock rate thereof being substantially higher than the highest frequency of said signals from said transducer elements; a corresponding plurality of delay-line time-compressors of progressively changing length differing by one basic delay unit, said delay-line time-compressors corresponding to successive transducer elements of said linear array and being responsive to said pulse trains of binary 1's and 0's therefrom and said basic delay unit being directly pro-

portional to the spacing of said transducer elements and inversely proportional to said predetermined number of analog beams; means for successively summing the output from said delay-line time-compressors at a rate equal to said predetermined number of analog beams per each basic delay unit thereby to provide a resultant pulse train; means responsive to said resultant pulse train for cyclically isolating resultant pulses therefrom corresponding to individual analog beams; and means for demodulating said isolated resultant pulses thereby to produce an output signal for each of said predetermined number of analog beams.

2. The apparatus for forming a predetermined number of analog beams from signals received from a plurality of transducer elements disposed in a linear array as defined in claim 1 wherein said corresponding plurality of delay-line time-compressors of progressively changing length differing by one basic delay unit includes means for generating bit pulses at a rate equal to said clock rate times said predetermined number of analog beams; means responsive to said bit pulses for generating a first gating signal concurrent with the bit pulses that are concurrent with said binary 1's or 0's and a second gating signal concurrent with the remaining bit pulses per each basic delay interval; a number of delay lines equal to the number of delay-line time-compressors, said delay lines progressively increasing in length by one basic delay unit and being an integral number of basic delay units long less one bit interval; and means connected to the respective inputs and outputs of said delay lines controlled by said first and second gating signals and responsive to said binary 1's and 0's for cyclically entering binary 1's or 0's into said delay lines and recirculating binary 1's or 0's from the respective outputs thereof at said bit pulse rate whereby samples corresponding to each of said predetermined number of analog beams appear in sequence at the outputs of said delay lines during each basic delay interval.

3. The apparatus for forming a predetermined number of analog beams from signals received from a plurality of transducer elements disposed in a linear array as defined in claim 2 wherein said basic delay unit equals $2d/rc$ where d is separation of the array transducer elements, r is the number of off-broadside beams and c is the velocity of propagation of said signals in the medium surrounding said transducer elements.

4. An apparatus for forming a predetermined number of analog beams from signals received from a plurality of transducer elements uniformly spaced in a linear array, said apparatus comprising means coupled to each of said plurality of transducer elements for converting said signals therefrom into a series of pulse trains of binary 1's and 0's as determined by whether the amplitude of said signals is increasing or decreasing, the clock rate thereof being substantially higher than the highest frequency of said signals from said transducer elements; a delay-line time-compressor responsive to each of said pulse trains of binary 1's and 0's and adapted to operate at a bit rate equal to an integral multiple of said predetermined number times said clock rate, said delay-line time-compressor corresponding to said transducer element at one extremity of said linear array being one basic delay unit less one bit interval in length and said delay-line time-compressors increasing one basic delay unit in length commencing from said delay-line time-compressor corresponding to said one extremity of said linear array and proceeding towards the other, said basic delay unit being directly proportional to the spacing of said transducer elements and inversely proportional to said predetermined number of analog beams; means including a summing amplifier for successively summing the output from said delay-line time-compressors at a rate equal to said predetermined number of analog beams per each basic delay unit thereby to provide a resultant pulse train; means responsive to said resultant pulse train for cyli-

cally isolating resultant pulses therefrom corresponding to specific ones of said analog beams; and means for demodulating said isolated resultant pulses thereby to produce an analog output signal for each of said predetermined number of analog beams.

5. The apparatus for forming a predetermined number of analog beams from signals received from a plurality of transducer elements uniformly spaced in a linear array as defined in claim 4 wherein an additional transducer element is disposed at the extremity of said linear array nearest the transducer element corresponding to the shortest delay-line time-compressor; means for inserting a delay equal to said basic delay unit before each of said delay-line time-compressors; and means for applying the pulse train of binary 1's and 0's corresponding to said additional transducer element of said linear array directly to said summing amplifier thereby to provide an additional component for each pulse of said resultant pulse train.

6. An apparatus for forming a predetermined number of analog beams from signals received from a plurality of transducer elements uniformly spaced in a linear array, said apparatus comprising means coupled to each of said plurality of transducer elements for converting said signals therefrom into a series of pulse trains of binary 1's and 0's as determined by whether the amplitude of said signals is increasing or decreasing, the clock rate thereof being substantially higher than the highest frequency of said signals from said transducer elements; means for generating a bit rate pulse train having a repetition rate equal to said predetermined number multiplied by said clock rate; means including a corresponding plurality of gates responsive to said series of pulse trains of binary 1's and 0's corresponding to said transducer elements of said linear array and to said bit rate pulse train for reversing the sequence of transducer elements to which said pulse trains of binary 1's and 0's correspond once each basic delay period, said basic delay period being directly proportional to the spacing of said transducer elements and inversely proportional to said predetermined number of analog beams; a delay-line time-compressor connected to the output of each of said corresponding plurality of gates and adapted to operate at said bit rate, said delay-line time-compressor corresponding to a transducer element at an extremity of said linear array being one basic delay unit unless one bit interval in length and each adjacent delay-line time-compressors proceeding towards the other extremity increasing one basic delay unit in length; means including a summing amplifier for successively summing the output from said delay-line time-compressors at a rate equal to said predetermined number of analog beams per each basic delay period thereby to provide a resultant pulse train; means responsive to said resultant pulse train for cyclically isolating resultant pulses therefrom corresponding to specific ones of analog beams; and means for demodulating said isolated resultant pulses thereby to produce an analog output signal for each of said predetermined number of analog beams.

7. The apparatus for forming a predetermined number of analog beams from signals received from a plurality of transducer elements uniformly spaced in a linear array as defined in claim 6 wherein said delay-line time-compressors each include a delay-line of a length equal thereto operated at said bit rate; a gate device having an input responsive to one of said pulse trains of binary 1's and 0's, an input connected to the output of said delay line

and an output connected to the input of said delay line; and control means connected to said gate device for causing one bit per quadrant from said pulse trains of binary 1's and 0's to be entered into said delay line during each basic delay period.

8. An apparatus for forming $2, 4 \dots (m-2), m$ analog beams from signals received from $1, 2, 3 \dots (n-1), n$ transducer elements uniformly spaced in a linear array where m is an even integer no less than six and where n is an integer no less than three, said apparatus comprising means including $1, 2, 3 \dots n$ delta modulators coupled to each of said $1, 2, 3 \dots n$ transducer elements, respectively, for converting said signals therefrom into n pulse trains of binary 1's and 0's as determined by whether the amplitude of said respective signals is increasing or decreasing, the clock rate thereof being substantially higher than the highest frequency of said signals from said transducer elements; $1, 2, 3 \dots n$ delay devices, each of a delay equal to a basic delay period connected to the output of said $1, 2, 3 \dots n$ delta modulators, respectively, said basic delay period being directly proportional to the spacing of said transducer elements and inversely proportional to said m analog beams; means for generating a bit rate pulse train having a repetition rate equal to m times said clock rate; means including $1, 2, 3 \dots (n-1), n$ gates having first and second inputs, said first input of said 1st gate being connected directly to the output of said 1st delta modulator, and said first inputs of said $2, 3 \dots n$ gates being connected directly to the outputs of said $2, 3 \dots n$ delay devices, respectively, said second input of said first gate being connected directly to said n^{th} delta modulator and said said second inputs of said $2, 3 \dots n$ gates being connected to the outputs of said $(n-1) \dots 3, 2, 1$ delay devices, respectively, said $1, 2, 3 \dots n$ gates additionally being responsive to said bit rate pulse train for alternately connecting the first and second inputs thereto to the respective outputs thereof once each basic delay period; a summing amplifier having an input connected directly to the output of said 1st gate; $1, 2, 3 \dots (n-1)$ delay-line time-compressors adapted to operate at said bit rate connected from the output of each of said $2, 3 \dots n$ gates to an input of said summing amplifier, said 1st delay-line time-compressor being one basic delay unit less one bit interval in length and each successive one of said $2, 3 \dots (n-1)$ delay-line time-compressors increasing one basic delay unit in length whereby said summing amplifier successively sums the output from said first delta modulator and said $1, 2, 3 \dots (n-1)$ delay-line time-compressors m times during each basic delay period thereby to provide a resultant pulse train; means responsive to said resultant pulse train for cyclically isolating resultant pulses therefrom corresponding to specific ones of said m analog beams; and means for demodulating said isolated resultant pulses thereby to produce an analog output signal for each of said m analog beams.

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65 RICHARD A. FARLEY, *Primary Examiner.*