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(81) Designated States: US, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

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(54) Title: FLIP CHIP BONDING WITH NON-CONDUCTIVE ADHESIVE

Table 1

	Substrate 1	Substrate 2
Material	FR-4	FLEX (Espanex)
Size	2" x 2"	2" x 2"
Electrode	Cu/Ni/Au	Cu/Ni/Au
	IC	
Size	5.0 x 5.0 mm , 7.5 x 7.5 mm	
Pitch	200 µm, 300 µm	
Pad size	80 µm octagonal	
Bumps	Au stud bumps	

(57) Abstract

Suggested is a flip chip technology using non-conductive adhesives (20) and gold ball bumps (10) or connectors. The concept is to simultaneously attach and interconnect bare chips with gold ball bumps to organic substrates (30). The chip is fixed by cooling the insulative adhesive. Environmental testing has demonstrated that performance characteristics were acceptable after 1000 hours of continuous exposure to humidity, and were excellent after 1000 temperature cycles. Such stable interconnections can only be realized by the compliance of the flip chip joint. This stability can be achieved by precise control of the bonding parameters such as temperature and pressure. This bonding technique allows quality attachment of bare chips on low cost organic substrates.

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Flip chip bonding with non conductive adhesive

The invention concerns the field of microelectronics packaging technology. Various bonding methods and mediums may be used to attach the IC die. Since the development of the flip chip mounting process using solder by IBM (C4 process) in the early 1960's, the face down bonding technology has become popular and manifold and original interconnection methods have been reported. At the same time the interest in flip chip bonding is being driven by demands for substrates accepted in the consumer field. Therefore the substrates which are to be bonded by flip chip **have been changing from inorganic to organic**, such as polyimide foil and printed circuit boards (often FR-4). By using solder alloys it is possible to attain low resistance as well as a good thermal contact between the chip and the packaging substrate, including FR-4 and polyimide flex with the use of encapsulants. The result is an improvement in the thermal life cycle of flip chips mounted on high CTE packaging substrates.

The interest in flip chip assemblies using adhesives for high density, fine pitch and high performance interconnections has increased rapidly. In this context a new flip chip technology is suggested **using non-conductive adhesives** in place of the known stiffenable resin (cf. US 4,749,120). The concept is to simultaneously attach and electrically interconnect bare chips with gold stud bumps to many types of packaging substrates, the bumps having a certain shape to ease the piercing through the sheet or sheet-foil of adhesive (Claim 1). By this interconnection method, the chip is bonded face down and is electrically connected via compressed and deformed gold ball bumps with the organic substrate. The chip is fixed by the non-conductive adhesive film which fills the entire gap between the die (the bare chip) and packaging substrate. The new method obtains greater compliance or flexibility, especially advantageous for organic substrates.

Compared to US 4,749,120 (Hatada, Matsushita) the bonding by heat was extraordinarily accelerated although physical bonding parameters were improved and flexibility (compliance) of the bonded microelectronic package was obtained.

The adhesive is best to be applied in sheet foil form (claim 3).

An exemplary non-conductive adhesive film was studied with an emphasis on the properties of COF (chip on flex) and COB (chip on board) interconnections. Electrical and mechanical performance of the adhesive bonds were studied by evaluating initial contact resistance and mechanical adhesion as a function of temperature and humidity.

Both mechanical and electrical properties were measured before and after the environmental tests and compared to soldered contacts. For flip chip interconnects with a pad size of $100\mu m^2$ on the chip site and a contact area of approx. $60\mu m$ round, the resistance is less than $8m\Omega$. This low contact resistance can be attributed to the special process and materials applied according to the invention. Moreover, the bonding pressure (claim 4), bonding temperature and time (claim 1) in comparison with the contact resistance were examined.

The results of the inventive concept indicate that the control of these process parameters will yield good bonding quality. Non-conductive adhesive flip chip technique offers several important advantages over solder filling materials, however, introduce other new problems. The major disadvantages are that they do not allow rework, they have manufacturability problems such as long cure time and they need high solder bumps. The use of adhesives instead of soldering in flip chip bonding on organic substrates avoids the problems with solder. Also there are potential cost benefits in the reduction of processing steps if adhesive flip chip bonding is used.

The invention is based on stud bumps and non-conductive adhesives. This technique allows quality attachment of IC's on low cost organic substrates and offers numerous advantages in the assembly of electronic circuits. These include low processing temperatures, fluxless bonding, high density interconnections, replaceability and high reliability, speeding up of the attachment process and allowing for elastic movement of the bonded microelectronic package.

The shape of the bumps is contained in claim 5; they may be of gold, to yield best results (claim 6). To improve and ease the deformation during bonding, the protruding front section is softer than the base part of the bumps (claim 2).

Examples and test results will demonstrate the invention in greater detail.

Figure 1 is a schematic flow chart of the non-conductive adhesive flip chip process.

Table 1 is a summarized example organic board spec. (FR-4; FLEX).

Figure 2a
Figure 2b
Figure 3 show the ball bump geometry. The bump shape showing a basic slightly flattened body with a protruding top or peak. The thinner top part being softer than the bottom almost ball shaped part, to more easily be deformed. Between the peak top part and the ball shaped bottom part a conical section is established, being also softer than the bottom ball shaped part. Figure 3 demonstrates the dimensions of the bumps, here a gold bump of Au 98 Pd. Figure 2b is an area configuration.

Figure 4
Figure 5 is a basic example of the inventive method with temperature/pressure parameters for bonding.

Figure 6a
Figure 6b are representations of bonded IC to FR-4 substrate with deformed gold bumps, showing the gold, nickel and copper interface.

Table 2 is a summarized specification of the adhesive.

Figure 7 shows adhesive temperature vs. thermode temperature at bonding site.

Figure 8 is a representation of a temperature test cycle.

Figure 9a
Figure 9b show temperature test cycle results (FR-4; FLEX).

Figure 10a
5 **Figure 10b** show humidity test results (FR-4; FLEX).

Figure 11 shows temperature dependant resistance.

Figure 12 shows the influence of humidity and temperature on
10 bonding strength.

Testchip and testsubstrate:
The continuity test devices for most of this work have a size of 5 and 7.5mm², pitches of 200 and 300μm and pad sizes of 80μm
15 octagonal (see **Table 1**). The metallization is 1μm AlSi 1% with a PSG-passivation. The substrates used for this flip chip bonding were 1mm thick printed circuit boards (FR-4) and 25μm flexprint (Espanex). The overall dimension of the substrates was 2inch² (see **Table 1**). The conductor patterns were gold/nickel coated
20 copper in both cases. The printed circuit board, which was also used for flip chip attachment using solder, carries a solder mask as a finishing layer. The mask has no influence on the non-conductive adhesive process. Both test vehicles carry interconnection tracks which allow monitoring of the electrical
25 integrity by measuring the contact resistance (four-point-probe) and transit resistance (daisy chain).

Bump processing:
The gold ball bumps are fabricated with a flexible low cost
30 bumping technique based on the conventional wire bonding procedure (cf. 1994, ITAP & Flip Chip Proceedings, pages 74 to 79, by J. Eldring et al.). Established wire bonding machines can be used, therefore, expensive bumping process equipment for sputtering photolithography and plating is not necessary. The
35 sizes and geometry of ball bumps are principally dependent on the wire diameter, the geometry of the capillary as well as on the bumping parameters.

Non-conductive adhesive:
The adhesive film suggested, consists of insulative thermosetting/thermoplastic blend adhesive without conducting particles and fillers. The adhesive was fabricated in a dry film format with different film thicknesses of 25μm and 50μm. For repairing the interconnection, the whole flip chip joint is heated to a temperature of approximately 125°C to 130°C in order to debond the IC. Their detailed specifications as well as the bonding parameters are summarized in **Table 2**.

Bonding Process:
The fundamental process flow for the non-conductive adhesive flip chip attachment is shown **in Figure 4**.

This process is made up of three basic steps:

Step 1: Non-conductive adhesive is applied to the substrate for the purpose of fixing the chip.
Step 2: The gold ball bumps on the chip and the electrodes on the substrate are aligned.
Step 3: Bonding the chip on the substrate with an appropriate load (min. 20kg/cm2) and with a temperature up to 180°C for 15 to 20sec (see **Figure 5**).

Thus the IC is electrically connected to the substrate via compressed and deformed gold ball bumps (see **Figures 6a, b**).

The pressure is maintained on the bond site, until the chip is fixed by cooling the thermode. The bonding process was performed with the semi-automatic flip chip bonder FC 950 from Carl Süß (France). This piece of equipment utilizes two stage heating in the thermocompression mode and allows cooling while pressure is being maintained. Because of the accuracy needed, the bonder consists of a split-field optic to locate the chip and the substrate. The recommended temperature should be maintained throughout the total bond cycle. Therefore, the actual adhesive temperature was measured by embedding a thermocouple in the adhesive during the bonding process.

Figure 7 shows the measured temperature difference between the thermode set point and the real bond temperature in the adhesive. The significant difference depends on the
5 thermoconductivity of each material. The cold chuck, where the substrate is fixed by vacuum, acts as a heat sink for the flip chip joint. The combined thickness of the adhesive and substrate plays an additional role for the heat exchange.

10 **Reliability tests:**
In order to clearly distinguish the failure mode and degradation mechanism of non-conductive adhesive joints, both the mechanical adhesion by pull test and the electrical performance were evaluated. To obtain these data, test samples were assembled and
15 subjected to accelerated life testing. The test method includes thermal cycling and storage at high temperature and humidity. The applied acceleration test method for thermal cycling involved 1000 cycles between -55 and +125°C, with a cycle duration of 30 minutes. Samples were measured after 50, 100,
20 250, 500 and 1000 cycles. The cycle regime was taken from a modification of the MIL standard 883 thermal shock test. A schematic drawing of the actual thermal cycle profile is shown **in Figure** 8. The constant humidity test was performed at a constant temperature of 85°C and at a relative humidity of 85%.
25 The total duration of the test was 1000 hours.

Interconnection functionality was measured after 50, 100, 250, 500 and 1000 hours.

30 **Electrical Characteristics:**
The electrical characteristics were studied by monitoring the contact resistance and transit resistance after the reliability tests. Results are summarized **in Figure 9 and 10**. After 1000 temperature cycles no open joints for the chips bonded to both
35 substrates were observed. However, the degradation of the resistance of the 7.5mm square chip increased slowly with the number of cycles, reaching a value twice as large as the initial condition (see **Figure 9a, 10a**). In the case of the 5mm square

chip, the connection resistance was nearly constant. The reason for the change in contact resistance can be attributed to the stress-induced contact spacing changes between the gold ball bumps and the electrodes of the substrate. In comparison with solder joints, where reliability problems arise from fatigue failures during thermal cyclings (CTE differences), adhesive joints tend to be more compliant and less susceptible to fatigue failure. In contrast to temperature cycling, humidity testing caused higher contact resistance values (see **Figure 9b, 10b**). In the case of the FR-4 board (see **Figure 9b**) the values after 1000 hours were independent of the chip size. The measured value was approximately 27mΩ with a small standard deviation of ±4.5mΩ. The results for the flexible polyimide substrate (see **Figure 10b**) exhibit a better stability, especially for the 5mm square chip. Possible causes for the high contact resistance are the change in volume when the adhesive swells in z-axis direction due to moisture absorption or an oxidation effect. To obtain excellent reliability and interconnection stability, a bonding load was selected by the thickness of the adhesive, by the bumpheight and by the given bonding parameters of the adhesives. The force was adjusted until there was no further reduction in contact resistance.

The best results could be achieved with bond forces in the range of 80 to 100g/bump. Despite these high bond forces no cracks occurred during bonding, neither on chip nor on substrate.

Another point to obtain high reliability is to have compliance in the interconnection. This compliance is required to compensate for non-planarities of the substrate and thermal mismatch of the interconnection materials. Under operating conditions the thermal mismatch difference in z-direction between the gold ball bump and the adhesive will expand the adhesive faster than the bumps. This leads to early failures when there is no compliance. Therefore, the behaviour of the flip chip interconnects was checked by a temperature operating test. The specimen was heated up from 25°C to 125°C, in increments of 25°C, and held at each temperature for measuring

the contact resistance.

Figure 11 shows the relationship between the contact resistance of the electrodes and the temperature. The resistance increases gradually for all devices from 5mΩ to approximately 8mΩ. Compared to the first investigation, which was performed at lower bond temperature, no electrical contact failures were observed even after 125°C. The higher contact resistance disappeared when returned to room temperature.

Mechanical Characteristics:
The adhesive strength was evaluated by a tensile tester (Instron 4502) on the rigid printed circuit boards. The board was clamped to a plate and the load was applied directly from above. The peel strength tests were carried out on the 7.5mm square chips employed in the two environmental tests, and compared with a sample stored at room temperature. The results **in Figure 12** show the influence of the environmental tests on the flip chip joint. For all samples the failure mode was an adhesion failure at the interface between the adhesive and the solder mask on the printed circuit board. Cohesive failure was never observed in this test.

Suggested is a flip chip technology using non-conductive adhesives and gold ball bumps or connectors. The concept is to simultaneously attach and interconnect bare chips with gold ball bumps to organic substrates. The chip is fixed by cooling the insulative adhesive. Environmental testing has demonstrated that performance characteristics were acceptable after 1000 hours of continuous exposure to humidity, and were excellent after 1000 temperature cycles. Such stable interconnections can only be realized by the compliance of the flip chip joint. This stability can be achieved by precise control of the bonding parameters such as temperature and pressure. This bonding technique allows quality attachment of bare chips on low cost organic substrates.

Claims:

1. Method for the simultaneous mechanically attaching and electrically connecting of bare chips with stud bumps (10) to organic substrates comprising:
   (a) covering the organic substrate carrying a conductive printed pattern with film (20) consisting of insulative thermosetting/thermoplastic blend adhesive and being non conductive;
   (b) alingning the bumps (10) to the pattern of the substrate;
   (c) bonding the chips face down with its bumps (10) through the adhesive film to the conductive printed pattern on the organic substrate (30) with a load of minimum 20 kg/cm² and at a temperature up to 180°C for 15 to 20 sec.

2. Method according to claim 1, comprising the deforming of the bumps (10), especially in their front section, being softer than their body section.

3. Method according to anyone of the preceeding claims, using a sheet foil of adhesive (20).

4. Method according to anyone of the preceeding claims, using a bonding force in the range of 80 g to 100 g per bump (10).

5. Method according to anyone of the preceeding claims, whereby the bumps have a base (10a) and a peak (10b) section, connected via a conical section (10c).

6. Method according to anyone of the preceeding claims, the bumps being of gold.

7. Method according to anyone of the preceeding claims, the adhesive film (20) being of a thickness of 25 µm or 50 µm, manufactured in a dry film format.

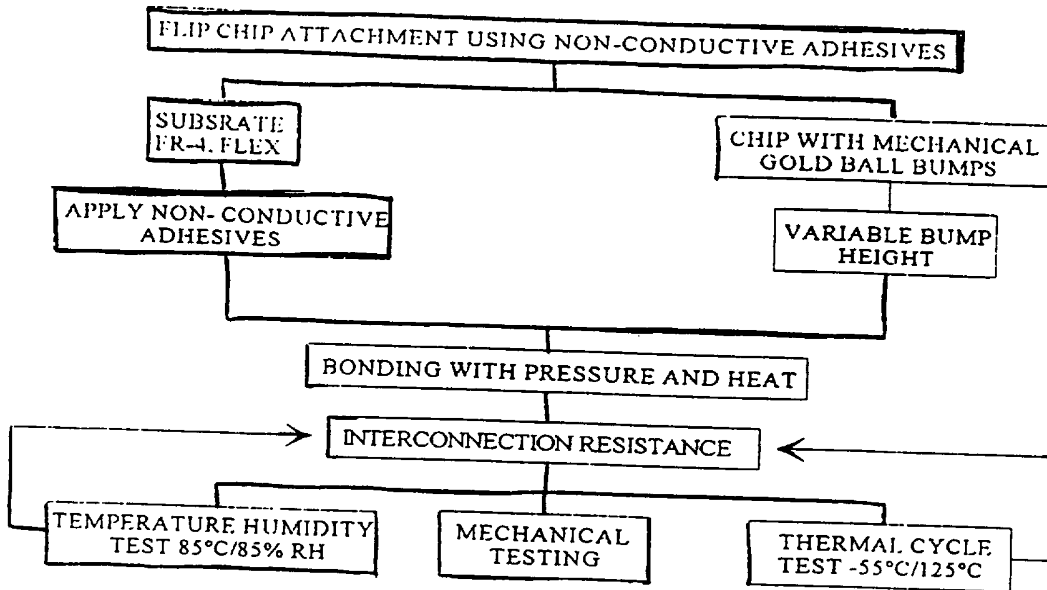

Figure 1

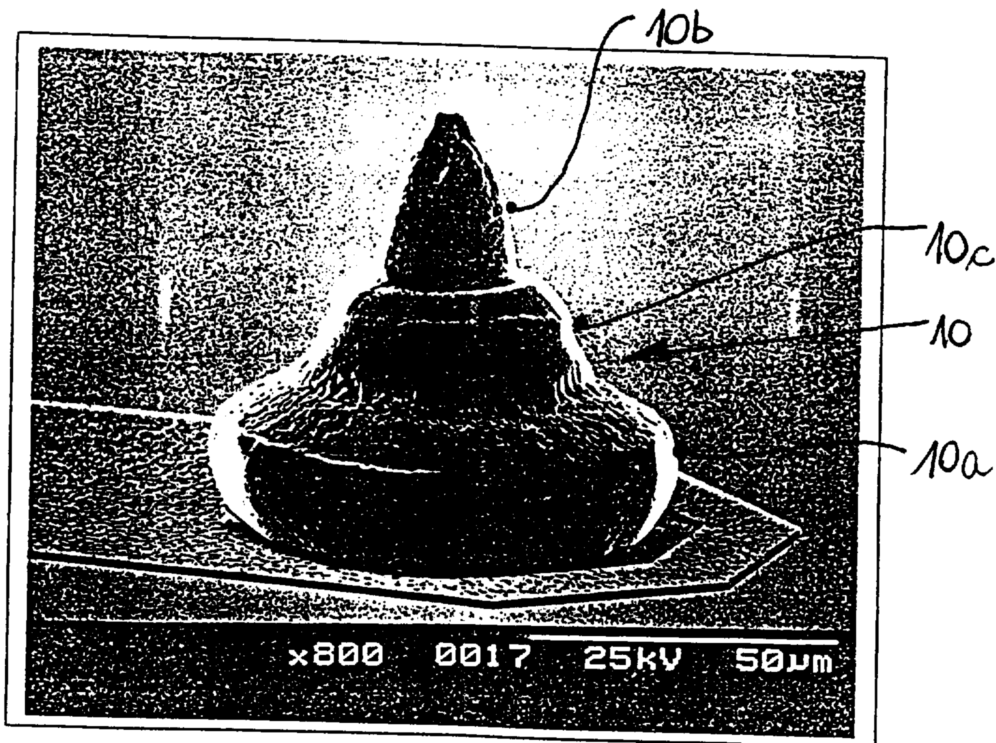

Figure 2a

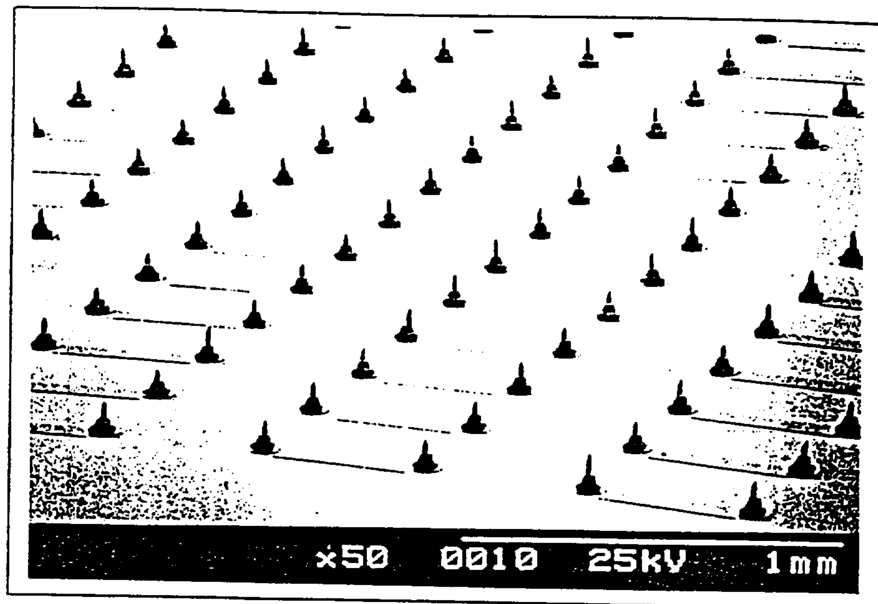

Figure 2b

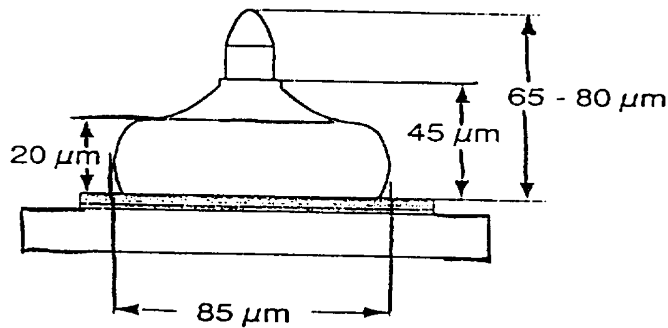

Figure 3

Table 1

	Substrate 1	Substrate 2
Material	FR-4	FLEX (Espanex)
Size	2" x 2"	2" x 2"
Electrode	Cu/Ni/Au	Cu/Ni/Au
	IC	
Size	5.0 x 5.0 mm , 7.5 x 7.5 mm	
Pitch	200 μm, 300 μm	
Pad size	80 μm octagonal	
Bumps	Au stud bumps	

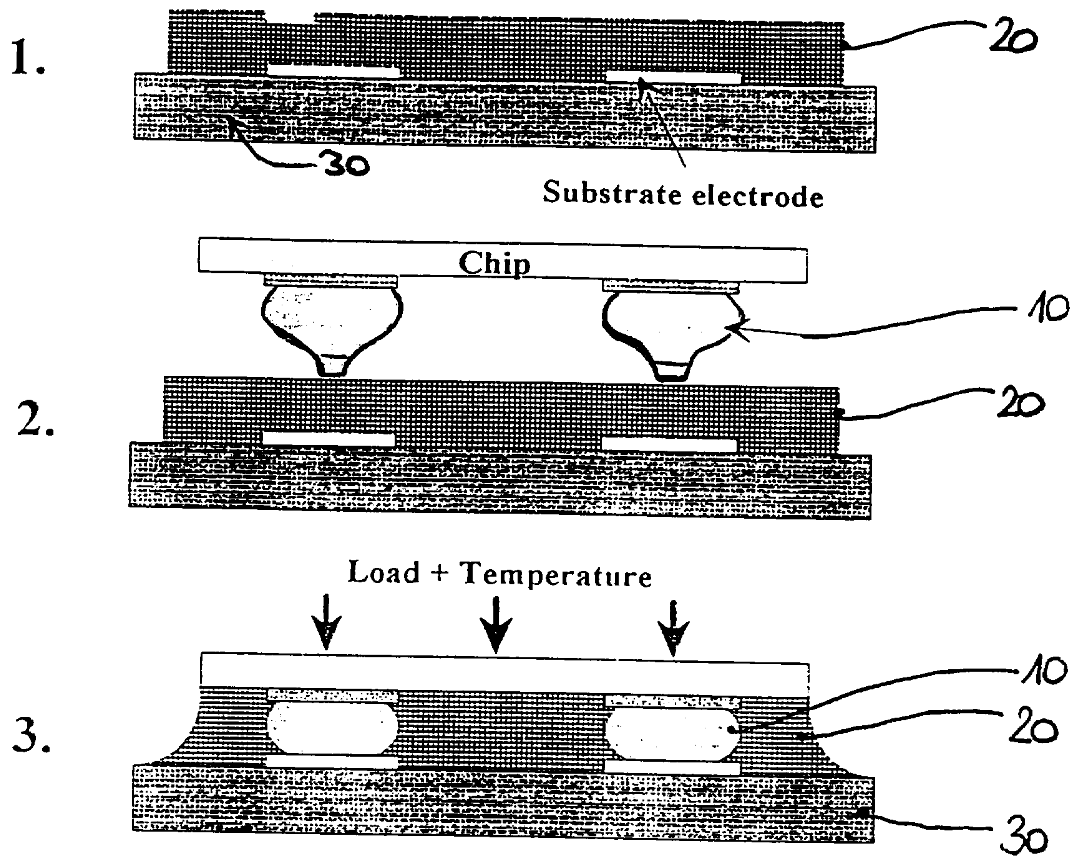

Figure 4

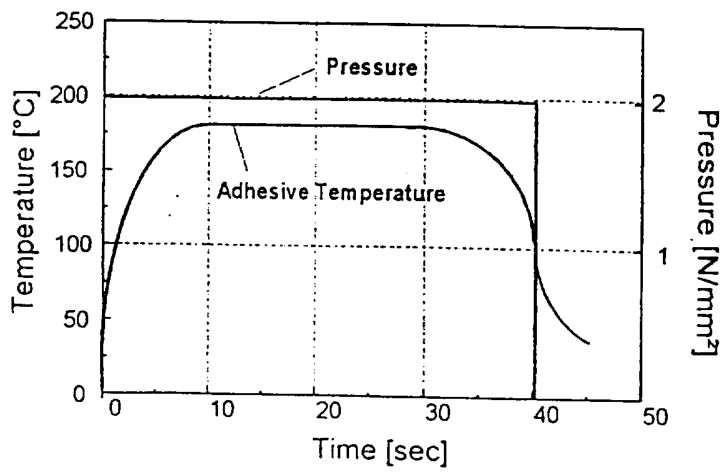

Figure 5

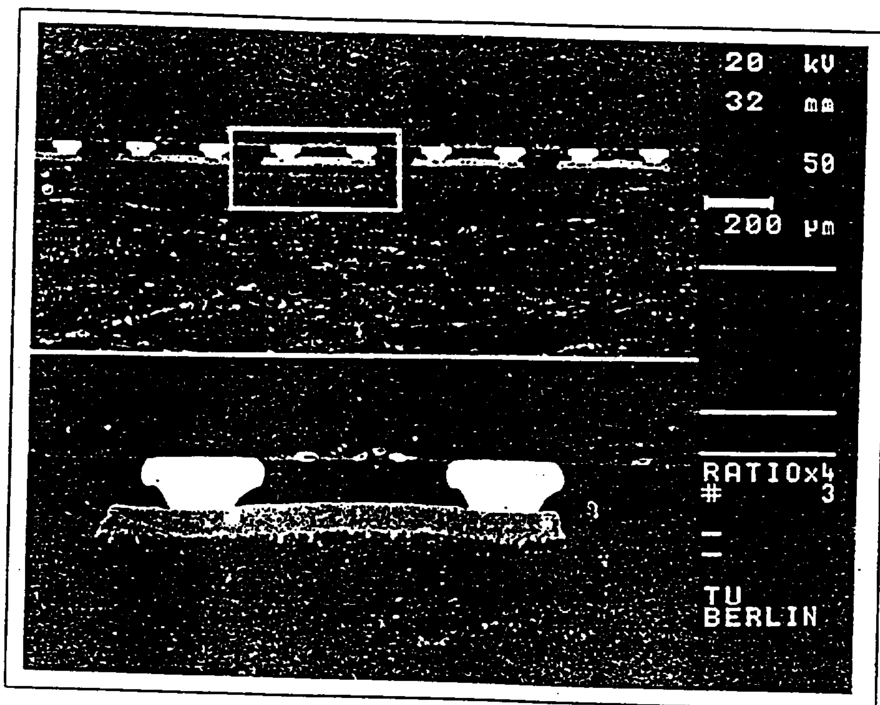

Figure 6a

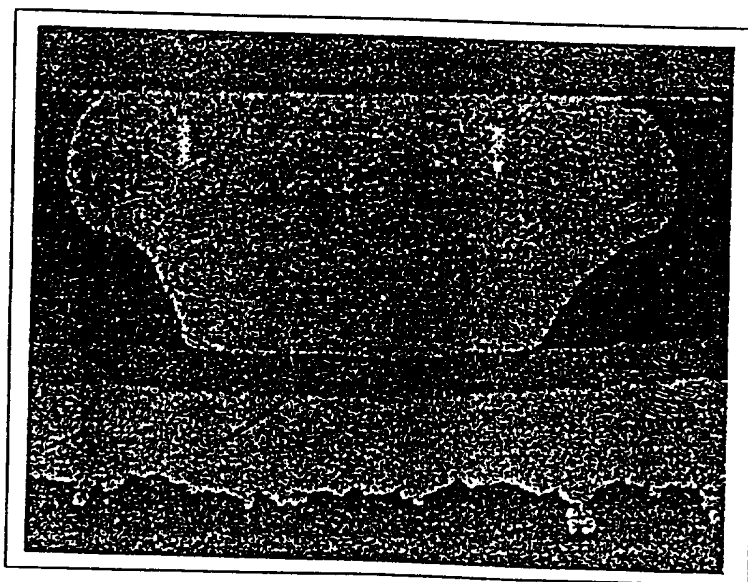

Figure 6b

Table 2:

Items	Specifications
Type	Thermosetting / Thermoplastic Film
Maximum Cont. Operation Temp [°C]	+125°C
Moisture Absorption (85°C/85%RH)	1.2%
Final Bonding	20s at 180°C; 20 kg/cm²

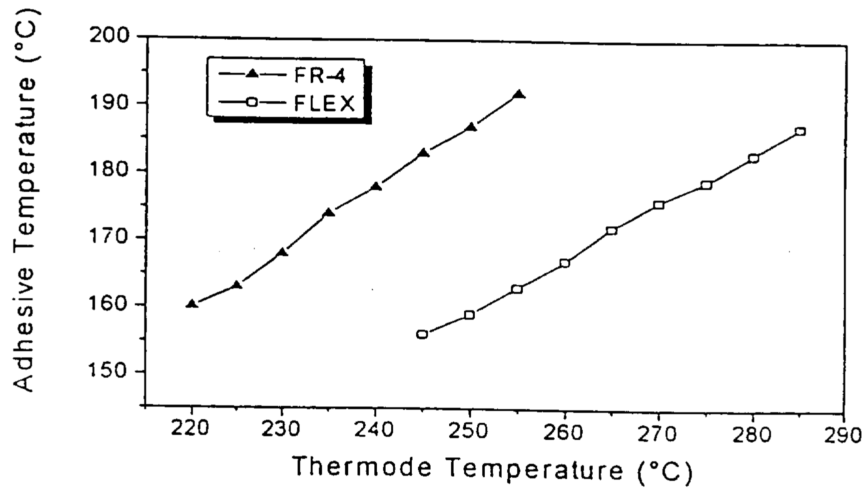

Figure 7

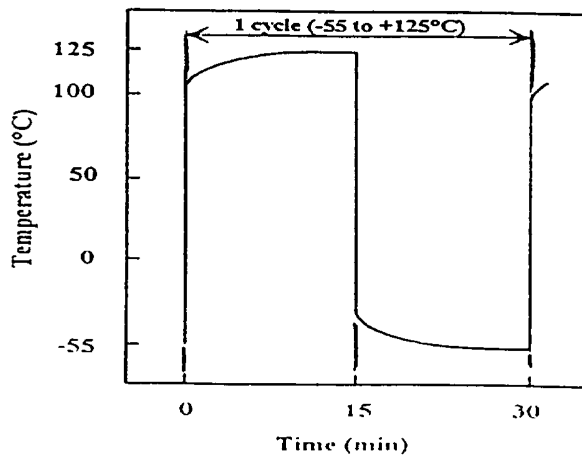

Figure 8:

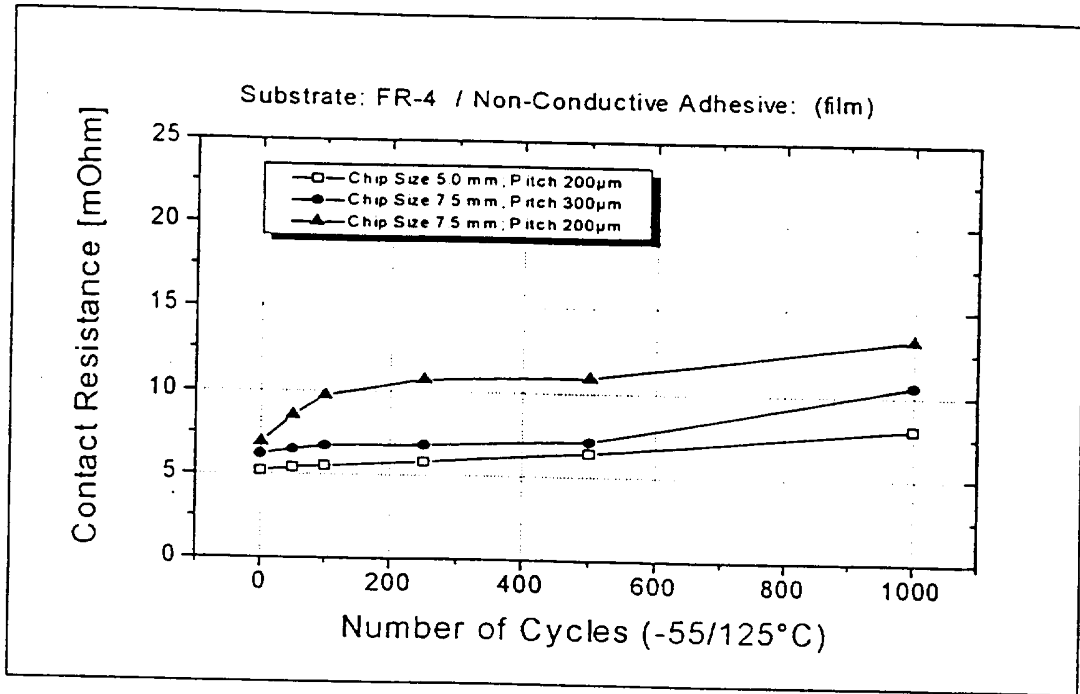

Figure 9a:

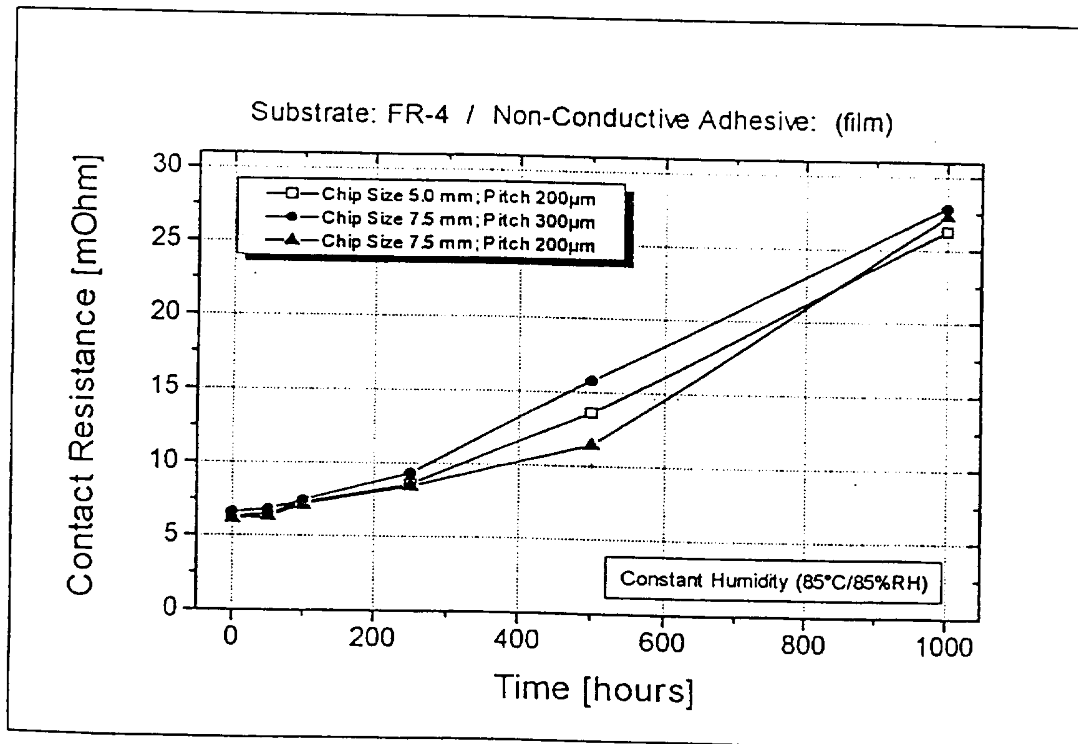

Figure 9b

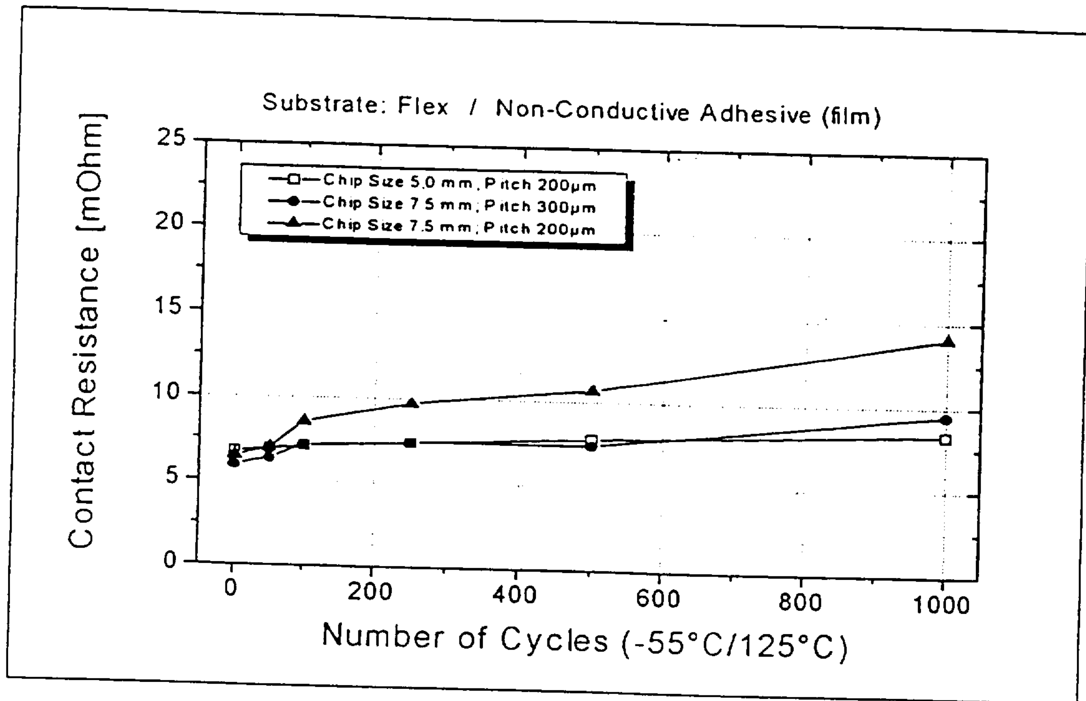

Figure 10a

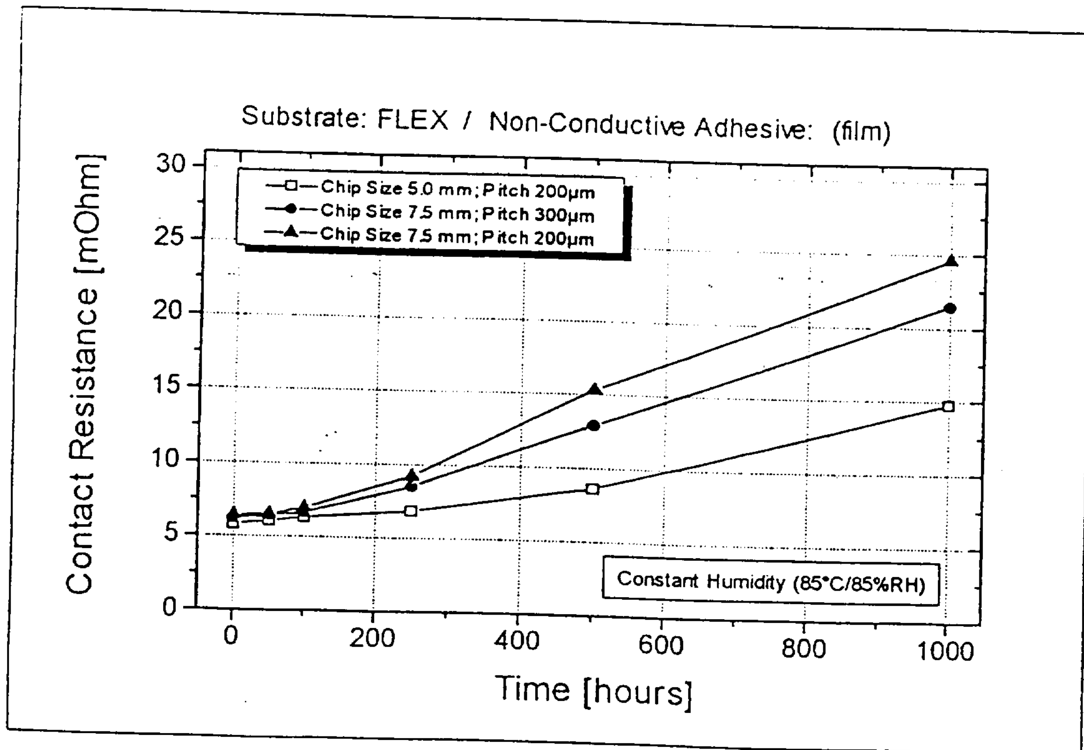

Figure 10b

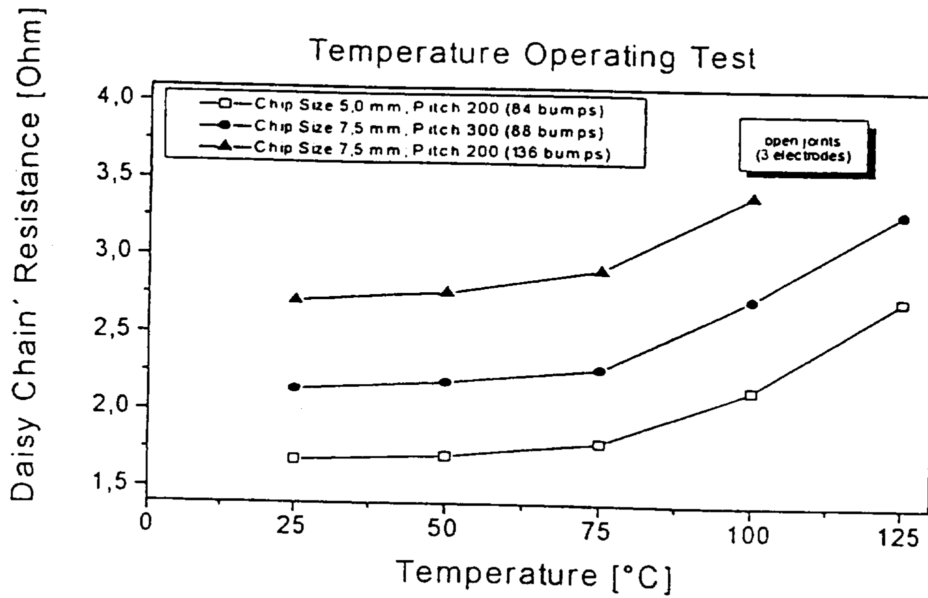

Figure 11:

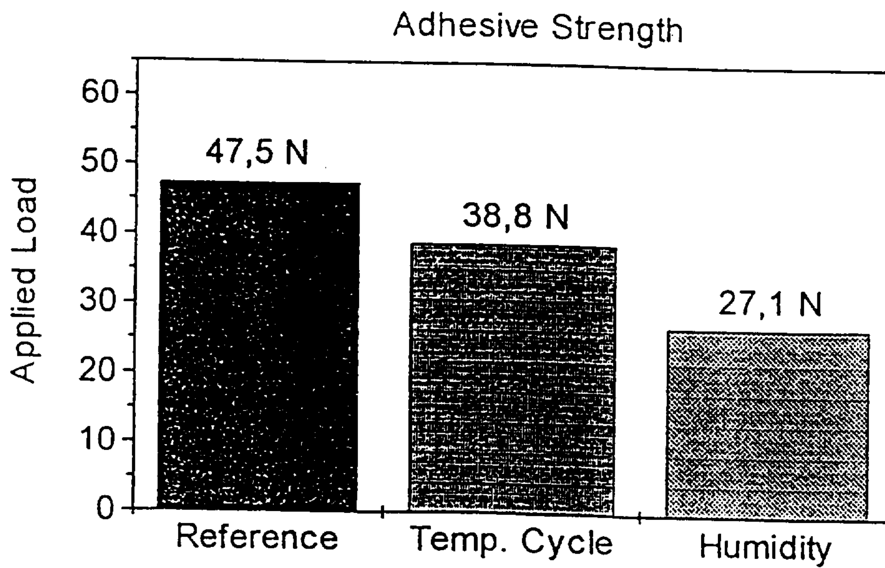

Figure 12

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 95/01388

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/58 H01L21/60

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP,A,0 388 011 (TOSHIBA) 19 September 1990 see column 4, line 29 - column 5, line 8 see column 6, line 40 - line 50	1
A		6
Y	EP,A,0 387 066 (HITACHI) 12 September 1990 see page 4, line 45 - line 55; claim 1	1
A		3,6,7
A	EP,A,0 596 393 (MATSUSHITA) 11 May 1994 see column 8, line 33 - line 49	1,4
A	DE,A,38 29 538 (SIEMENS) 8 March 1990 see claims 1-4; figure 1	1,2,5,6
A	EP,A,0 528 171 (IBM) 24 February 1993	

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
25 July 1995	07.08.95

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

In[illegible]ional Application No

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