



- (51) **International Patent Classification:**
G02B 26/00 (2006.01) *G02B 26/08* (2006.01)
- (21) **International Application Number:**
PCT/US2012/031643
- (22) **International Filing Date:**
30 March 2012 (30.03.2012)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
13/079,487 4 April 2011 (04.04.2011) US
13/079,599 4 April 2011 (04.04.2011) US
- (71) **Applicant (for all designated States except US):** QUALCOMM MEMS TECHNOLOGIES, INC. [US/US]; 5775 Morehouse Drive, San Diego, California 9212-1714 (US).
- (72) **Inventors; and**
- (75) **Inventors/Applicants (for US only):** LEE, Hojin [KR/KR]; 5-401 Cheongsil APT, Daechi-dong, Kangnam-gu, Seoul 135-281 (KR). ZHONG, Fan [US/US]; QUALCOMM MEMS Technologies, Inc., 5775 Morehouse Drive, San Diego, California 92121-1714 (US). TAO, Yi

[CN/US]; QUALCOMM MEMS Technologies, Inc., 5775 Morehouse Drive, San Diego, California 92121-1714 (US).

- (74) **Agent:** ABUMERI, Mark M.; Knobbe Martens Olson & Bear LLP, 2040 Main Street, Fourteenth Floor, Irvine, California 92614 (US).

- (81) **Designated States (unless otherwise indicated, for every kind of national protection available):** AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) **Designated States (unless otherwise indicated, for every kind of regional protection available):** ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,

[Continued on next page]

- (54) **Title:** PIXEL VIA AND METHODS OF FORMING THE SAME

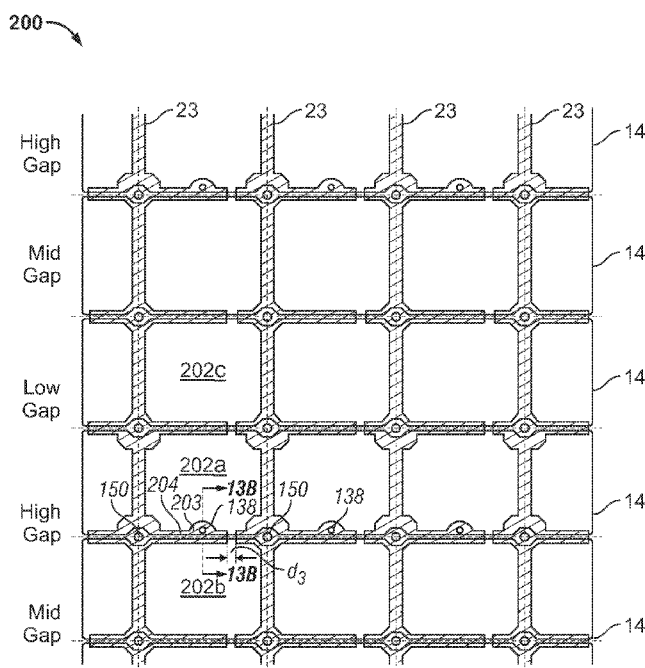


Figure 13A

- (57) **Abstract:** This disclosure provides systems, methods and apparatuses for pixel vias. In one aspect, a method of forming an electromechanical device having a plurality of pixels includes depositing an electrically conductive black mask (23) on a substrate (20) at each of four corners and along at least one edge region of each pixel, depositing a dielectric layer (35) over the black mask, depositing an optical stack (16) including a stationary electrode over the dielectric layer, and depositing a mechanical layer (14) over the optical stack. The method further includes providing a conductive via (138) in a first pixel of the plurality of pixels, the via disposed in the dielectric layer and electrically connecting the stationary electrode to the black mask, the via disposed in a position along an edge of the first pixel, spaced offset from the edge of the first pixel in a direction towards the center of the first pixel.

WO 2012/138577 A1



SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, **Published:**
GW, ML, MR, NE, SN, TD, TG).

— *with international search report (Art. 21(3))*

PIXEL VIA AND METHODS OF FORMING THE SAME

TECHNICAL FIELD

[0001] This disclosure relates to electromechanical systems.

DESCRIPTION OF THE RELATED TECHNOLOGY

[0002] Electromechanical systems include devices having electrical and mechanical elements, actuators, transducers, sensors, optical components (e.g., mirrors) and electronics. Electromechanical systems can be manufactured at a variety of scales including, but not limited to, microscales and nanoscales. For example, microelectromechanical systems (MEMS) devices can include structures having sizes ranging from about a micron to hundreds of microns or more. Nanoelectromechanical systems (NEMS) devices can include structures having sizes smaller than a micron including, for example, sizes smaller than several hundred nanometers. Electromechanical elements may be created using deposition, etching, lithography, and/or other micromachining processes that etch away parts of substrates and/or deposited material layers, or that add layers to form electrical and electromechanical devices.

[0003] One type of electromechanical systems device is called an interferometric modulator (IMOD). As used herein, the term interferometric modulator or interferometric light modulator refers to a device that selectively absorbs and/or reflects light using the principles of optical interference. In some implementations, an interferometric modulator may include a pair of conductive plates, one or both of which may be transparent and/or reflective, wholly or in part, and capable of relative motion upon application of an appropriate electrical signal. In an implementation, one plate may include a stationary layer deposited on a substrate and the other plate may include a reflective membrane separated from the stationary layer by an air gap. The position of one plate in relation to another can change the optical interference of light incident on the interferometric modulator. Interferometric modulator devices have a wide range of applications, and are anticipated to be

used in improving existing products and creating new products, especially those with display capabilities.

[0004] An interferometric device array can include a mechanical layer that is anchored at corners of each pixel. A black mask can be included at corners and between pixels to absorb light in optically inactive regions of each pixel. The black mask region can improve a contrast ratio of the display, while also reducing fill factor. There is a need for interferometric devices having smaller anchoring areas for the mechanical layer and improved fill factor.

SUMMARY

[0005] The systems, methods and devices of the disclosure each have several innovative aspects, no single one of which is solely responsible for the desirable attributes disclosed herein.

[0006] One innovative aspect of the subject matter described in this disclosure can be implemented in a device including an array of pixels, each pixel having a substrate, an electrically conductive black mask disposed on the substrate and masking an optically non-active portion of the pixel at each of four corners of the pixel and along at least one edge region of the pixel, a dielectric layer disposed over the black mask, an optical stack including a stationary electrode disposed over the dielectric layer, and a mechanical layer positioned over the optical stack and defining a cavity between the mechanical layer and the optical stack. The mechanical layer is movable through the cavity between an actuated position and a relaxed position, and the mechanical layer is anchored over the optical stack at each corner of the pixel. The array of pixels includes a first pixel having a conductive via in the dielectric layer electrically connecting the stationary electrode to the black mask, the conductive via disposed in a position along an edge of the first pixel in an optically non-active area of the first pixel. The position of the conductive via is spaced offset from the edge of the first pixel in a direction towards the center of the first pixel.

[0007] In some implementations, the array of pixels further includes a second pixel adjacent the first pixel along the edge of the first pixel, and the second pixel does not include a via in the dielectric layer for electrically connecting the stationary electrode to the black mask. According to some implementations, the first pixel is a high gap pixel and the

second pixel is a mid gap pixel, and the array of pixels further includes a low gap pixel adjacent the high gap pixel on a side of the high gap pixel opposite the mid gap pixel, and the low gap pixel does not include a via in the dielectric layer for electrically connecting the stationary electrode to the black mask.

[0008] Another innovative aspect of the subject matter described in this disclosure can be implemented in a method of forming a display device having a plurality of pixels. The method includes depositing an electrically conductive black mask on a substrate, the black mask masking an optically non-active portion of the pixel at each of four corners of each pixel and along at least one edge region of each pixel. The method further includes depositing a dielectric layer over the black mask, depositing an optical stack including a stationary electrode over the dielectric layer, and depositing the mechanical layer over the optical stack. The mechanical layer defines a cavity between the mechanical layer and the optical stack. The method further includes anchoring the mechanical layer over the optical stack at each corner of each pixel and providing a conductive via in a first pixel of the device, the via disposed in the dielectric layer and electrically connecting the stationary electrode to the black mask. The via is disposed in a position along an edge of the first pixel in an optically non-active area of the first pixel, and the position of the conductive via is spaced offset from the edge of the first pixel in a direction towards the center of the first pixel.

[0009] Another innovative aspect of the subject matter described in this disclosure can be implemented in an electromechanical device that includes a plurality of pixels, each pixel including a substrate, a light absorbing means disposed on the substrate and masking an optically non-active portion of the pixel at each of four corners of the pixel and along at least one edge region of the pixel, a dielectric layer disposed over the light absorbing means, and an optical stack including a stationary electrode disposed over the dielectric layer, and a mechanical layer positioned over the optical stack to define a cavity between the mechanical layer and the optical stack. The mechanical layer is movable through the cavity between an actuated position and a relaxed position, and the mechanical layer is anchored over the optical stack at each corner of the pixel. The array of pixels includes a first pixel having a means in the dielectric layer for electrically connecting the stationary electrode to the light absorbing means, the connecting means disposed in a position along an edge of the

first pixel in an optically non-active area of the first pixel. The position of the connecting means is spaced offset from the edge of the first pixel in a direction towards the center of the first pixel. In some implementations, a distance from a center of the via to the edge of the first pixel ranges between about 1 μm to about 3 μm . In some implementations, the first pixel is a high gap pixel, and wherein the plurality of pixels further includes a mid gap pixel adjacent the first pixel along the edge of the first pixel, and wherein the plurality of pixels further includes a low gap pixel adjacent the first pixel opposite the mid gap pixel, wherein the mid gap and low gap pixels do not include a means in the dielectric layer for electrically connecting the stationary electrode to the black mask.

[0010] Another innovative aspect of the subject matter described in this disclosure can be implemented in a device including an array of pixels, each pixel including a substrate, an electrically conductive black mask disposed on the substrate and masking an optically non-active portion of the pixel at each of four corners of the pixel, a dielectric layer disposed over the black mask, an optical stack including a stationary electrode disposed over the dielectric layer, and a mechanical layer positioned over the optical stack and defining a cavity between the mechanical layer and the optical stack. The mechanical layer is movable through the cavity between an actuated position and a relaxed position, and the mechanical layer is anchored over the optical stack at each corner of the pixel. The array of pixels includes a first pixel having a conductive via in the dielectric layer electrically connecting the stationary electrode to the black mask, the via disposed at a corner of the first pixel offset from where the mechanical layer is anchored over the optical stack in an optically non-active area of the first pixel.

[0011] In some implementations, the array of pixels further includes a second pixel adjacent the first pixel, and the second pixel does not include a conductive via in the dielectric layer for electrically connecting the black mask to the stationary electrode. According to some implementations, the first pixel is a high gap pixel and the second pixel is a mid gap pixel, and the array of pixels further includes a low gap pixel on a side of the mid gap pixel opposite the high gap pixel, and the low gap pixel does not include a conductive via in the dielectric layer for electrically connecting the black mask to the stationary electrode. In some implementations, the via is spaced from where the mechanical layer is anchored over

the optical stack by a distance ranging between about 6 μm to about 8 μm . In some implementations, the via is an opening in the dielectric layer for electrically connecting the conductive bussing layer of the black mask to the stationary electrode of the optical stack.

[0012] Another innovative aspect of the subject matter described in this disclosure can be implemented in a method of forming a device having a plurality of pixels. The method includes depositing an electrically conductive black mask on a substrate to mask an optically non-active portion of the pixel at each of four corners of each pixel, depositing a dielectric layer over the black mask, depositing an optical stack including a stationary electrode over the dielectric layer, depositing a mechanical layer over the optical stack, and anchoring the mechanical layer over the optical stack at each corner of each pixel. The mechanical layer defines a cavity for each pixel between the mechanical layer and the optical stack. The method further includes providing a conductive via in a first pixel of the plurality of pixels, the via in the dielectric layer electrically connecting the stationary electrode to the black mask, the via disposed at a corner of the first pixel, offset from where the mechanical layer is anchored over the optical stack in an optically non-active area of the first pixel.

[0013] In some implementations, the method further includes depositing a sacrificial layer before depositing the mechanical layer and removing the sacrificial layer after depositing the mechanical layer to form the cavity, the sacrificial layer having a thickness selected to define a height of the cavity. According to some implementations, the method further includes forming an anchor hole in the sacrificial layer, the anchor hole defining where the mechanical layer is anchored over the optical stack.

[0014] Another innovative aspect of the subject matter described in this disclosure can be implemented in a device including a plurality of pixels, each pixel including a substrate, a means for absorbing light disposed on the substrate and masking an optically non-active portion of the pixel at each of four corners of the pixel, a dielectric layer disposed over the light absorbing means, and an optical stack including a stationary electrode disposed over the dielectric layer. The array of pixels includes a first pixel having a means for electrically connecting in the dielectric layer the stationary electrode to the light absorbing means, the connecting means disposed at a corner of the first pixel, offset from where the mechanical layer is anchored over the optical stack in an optically non-active area of the first

pixel. In some implementations, the first pixel is a high gap pixel, and the array of pixels further includes a mid gap pixel and a low gap pixel, the mid gap pixel adjacent the high gap pixel and the low gap pixel adjacent the mid gap pixel on a side of the mid gap pixel opposite the high gap pixel, and the mid gap and low gap pixels do not include a means for electrically connecting in the dielectric layer the stationary electrode to the light absorbing means.

[0015] Details of one or more implementations of the subject matter described in this specification are set forth in the accompanying drawings and the description below. Other features, aspects, and advantages will become apparent from the description, the drawings, and the claims. Note that the relative dimensions of the following figures may not be drawn to scale.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] Figure 1 shows an example of an isometric view depicting two adjacent pixels in a series of pixels of an interferometric modulator (IMOD) display device.

[0017] Figure 2 shows an example of a system block diagram illustrating an electronic device incorporating a 3x3 interferometric modulator display.

[0018] Figure 3 shows an example of a diagram illustrating movable reflective layer position versus applied voltage for the interferometric modulator of Figure 1.

[0019] Figure 4 shows an example of a table illustrating various states of an interferometric modulator when various common and segment voltages are applied.

[0020] Figure 5A shows an example of a diagram illustrating a frame of display data in the 3x3 interferometric modulator display of Figure 2.

[0021] Figure 5B shows an example of a timing diagram for common and segment signals that may be used to write the frame of display data illustrated in Figure 5A.

[0022] Figure 6A shows an example of a partial cross-section of the interferometric modulator display of Figure 1.

[0023] Figures 6B–6E show examples of cross-sections of varying implementations of interferometric modulators.

[0024] Figure 7 shows an example of a flow diagram illustrating a manufacturing process for an interferometric modulator.

[0025] Figures 8A–8E show examples of cross-sectional schematic illustrations of various stages in a method of making an interferometric modulator.

[0026] Figure 9 shows an example of a flow diagram illustrating a manufacturing process for an interferometric modulator.

[0027] Figures 10A–10R show examples of cross-sectional schematic illustrations of various stages in a method of making an interferometric modulator.

[0028] Figures 11A–11C show examples of plan view schematic illustrations of various interferometric modulator arrays.

[0029] Figure 12 shows an example of a flow diagram illustrating a manufacturing process for an interferometric modulator.

[0030] Figure 13A shows an example of a plan view schematic illustration of an interferometric modulator array.

[0031] Figure 13B shows an example of a cross-sectional schematic illustration of the interferometric modulator array of Figure 13A taken along the line 13B–13B.

[0032] Figure 14 shows an example of a flow diagram illustrating a manufacturing process for an interferometric modulator.

[0033] Figures 15A and 15B show examples of system block diagrams illustrating a display device that includes a plurality of interferometric modulators.

[0034] Like reference numbers and designations in the various drawings indicate like elements.

DETAILED DESCRIPTION

[0035] The following detailed description is directed to certain implementations for the purposes of describing the innovative aspects. However, the teachings herein can be applied in a multitude of different ways. The described implementations may be implemented in any device that is configured to display an image, whether in motion (e.g., video) or stationary (e.g., still image), and whether textual, graphical or pictorial. More particularly, it is contemplated that the implementations may be implemented in or associated with a variety of electronic devices such as, but not limited to, mobile telephones, multimedia Internet enabled cellular telephones, mobile television receivers, wireless devices,

smartphones, Bluetooth devices, personal data assistants (PDAs), wireless electronic mail receivers, hand-held or portable computers, netbooks, notebooks, smartbooks, tablets, printers, copiers, scanners, facsimile devices, GPS receivers/navigators, cameras, MP3 players, camcorders, game consoles, wrist watches, clocks, calculators, television monitors, flat panel displays, electronic reading devices (e.g., e-readers), computer monitors, auto displays (e.g., odometer display, etc.), cockpit controls and/or displays, camera view displays (e.g., display of a rear view camera in a vehicle), electronic photographs, electronic billboards or signs, projectors, architectural structures, microwaves, refrigerators, stereo systems, cassette recorders or players, DVD players, CD players, VCRs, radios, portable memory chips, washers, dryers, washer/dryers, parking meters, packaging (e.g., electromechanical systems (EMS), MEMS and non-MEMS), aesthetic structures (e.g., display of images on a piece of jewelry) and a variety of electromechanical systems devices. The teachings herein also can be used in non-display applications such as, but not limited to, electronic switching devices, radio frequency filters, sensors, accelerometers, gyroscopes, motion-sensing devices, magnetometers, inertial components for consumer electronics, parts of consumer electronics products, varactors, liquid crystal devices, electrophoretic devices, drive schemes, manufacturing processes, electronic test equipment. Thus, the teachings are not intended to be limited to the implementations depicted solely in the Figures, but instead have wide applicability as will be readily apparent to one having ordinary skill in the art.

[0036] Electromechanical devices having improved fill factor are disclosed. The fill factor of an electromechanical device, or ratio of optically active area of the device relative to the total area of the electromechanical device, can be limited by the area of a light absorbing black mask. The electromechanical device can be an interferometric modulator device including a plurality of pixels and a mechanical layer anchored to an optical stack over the black mask at corners of each pixel. In some implementations, a conductive via is used for electrically connecting a stationary electrode of the device to the black mask. The via is offset from where the mechanical layer is anchored over the optical stack to aid in reducing the area of the black mask. For example, offsetting the via from an anchoring region used to anchor the mechanical layer over the optical stack at a pixel corner can reduce the size of the black mask at the pixel corner, since the anchoring region need not be sized to account for

misalignment between the pixel via and the anchoring region. By reducing the area of the black mask at pixel corners, the optically non-active area of the array can be reduced, thereby improving fill factor. In some implementations, a via is not included in the dielectric layer of every pixel. Rather, the via can be located periodically throughout an interferometric modulator device, for example, near a corner of a pixel configured with a high gap (or cavity) height to reduce the total area of the black mask and to improve fill factor. For example, a via can be located only near a corner of a pixel (or sub-pixel) having the highest gap in a configuration that includes pixels (or sub-pixels) having various gap heights.

[0037] In some other implementations, a conductive via is disposed in a position along an edge of a pixel in an optically non-active area of the pixel, and the via is spaced offset from the edge of the pixel in a direction towards the center of the pixel. The black mask can include a channel extending from a corner of the pixel to the via along the edge of the pixel. A side of the channel can include a widened portion (or a bulge) that is generally wider than the rest of the channel width. The bulge surrounds the footprint of the via which aids in increasing robustness of the via to process variations. In some implementations, the via need not be included along each edge of each pixel. Rather, the via can be provided for only certain edges of certain pixels, for example, in a high gap pixel along an edge shared by the high gap and a mid gap pixel, to reduce the total area of the black mask.

[0038] Particular implementations of the subject matter described in this disclosure can be implemented to realize one or more of the following potential advantages. In some implementations, a pixel array can include improved fill factor and/or a black mask having reduced area. Additionally, some implementations can increase process robustness of a via used for electrically connecting a black mask to a stationary electrode in an interferometric device. Furthermore, some implementations can improve yield of an interferometric device by improving tolerance of the device to manufacturing variation. Moreover, some implementations can be used to reduce the number of vias in a pixel array and/or provide a pixel array having vias over only a fraction of the array.

[0039] An example of a suitable electromechanical systems (EMS) or MEMS device, to which the described implementations may apply, is a reflective display device. Reflective display devices can incorporate interferometric modulators (IMODs) to selectively

absorb and/or reflect light incident thereon using principles of optical interference. IMODs can include an absorber, a reflector that is movable with respect to the absorber, and an optical resonant cavity defined between the absorber and the reflector. The reflector can be moved to two or more different positions, which can change the size of the optical resonant cavity and thereby affect the reflectance of the interferometric modulator. The reflectance spectrums of IMODs can create fairly broad spectral bands which can be shifted across the visible wavelengths to generate different colors. The position of the spectral band can be adjusted by changing the thickness of the optical resonant cavity, i.e., by changing the position of the reflector.

[0040] Figure 1 shows an example of an isometric view depicting two adjacent pixels in a series of pixels of an interferometric modulator (IMOD) display device. The IMOD display device includes one or more interferometric MEMS display elements. In these devices, the pixels of the MEMS display elements can be in either a bright or dark state. In the bright (“relaxed,” “open” or “on”) state, the display element reflects a large portion of incident visible light, e.g., to a user. Conversely, in the dark (“actuated,” “closed” or “off”) state, the display element reflects little incident visible light. In some implementations, the light reflectance properties of the on and off states may be reversed. MEMS pixels can be configured to reflect predominantly at particular wavelengths allowing for a color display in addition to black and white.

[0041] The IMOD display device can include a row/column array of IMODs. Each IMOD can include a pair of reflective layers, i.e., a movable reflective layer and a fixed partially reflective layer, positioned at a variable and controllable distance from each other to form an air gap (also referred to as an optical gap or cavity). The movable reflective layer may be moved between at least two positions. In a first position, i.e., a relaxed position, the movable reflective layer can be positioned at a relatively large distance from the fixed partially reflective layer. In a second position, i.e., an actuated position, the movable reflective layer can be positioned more closely to the partially reflective layer. Incident light that reflects from the two layers can interfere constructively or destructively depending on the position of the movable reflective layer, producing either an overall reflective or non-reflective state for each pixel. In some implementations, the IMOD may be in a reflective

state when unactuated, reflecting light within the visible spectrum, and may be in a dark state when unactuated, reflecting light outside of the visible range (e.g., infrared light). In some other implementations, however, an IMOD may be in a dark state when unactuated, and in a reflective state when actuated. In some implementations, the introduction of an applied voltage can drive the pixels to change states. In some other implementations, an applied charge can drive the pixels to change states.

[0042] The depicted portion of the pixel array in Figure 1 includes two adjacent interferometric modulators **12**. In the IMOD **12** on the left (as illustrated), a mechanical layer or movable reflective layer **14** is illustrated in a relaxed position at a predetermined distance from an optical stack **16**, which includes a partially reflective layer. The voltage V_0 applied across the IMOD **12** on the left is insufficient to cause actuation of the movable reflective layer **14**. In the IMOD **12** on the right, the movable reflective layer **14** is illustrated in an actuated position near or adjacent the optical stack **16**. The voltage V_{bias} applied across the IMOD **12** on the right is sufficient to maintain the movable reflective layer **14** in the actuated position.

[0043] In Figure 1, the reflective properties of pixels **12** are generally illustrated with arrows **13** indicating light incident upon the pixels **12**, and light **15** reflecting from the pixel **12** on the left. Although not illustrated in detail, most of the light **13** incident upon the pixels **12** will be transmitted through the transparent substrate **20**, toward the optical stack **16**. A portion of the light incident upon the optical stack **16** will be transmitted through the partially reflective layer of the optical stack **16**, and a portion will be reflected back through the transparent substrate **20**. The portion of light **13** that is transmitted through the optical stack **16** will be reflected at the movable reflective layer **14**, back toward (and through) the transparent substrate **20**. Interference (constructive or destructive) between the light reflected from the partially reflective layer of the optical stack **16** and the light reflected from the movable reflective layer **14** will determine the wavelength(s) of light **15** reflected from the pixel **12**.

[0044] The optical stack **16** can include a single layer or several layers. The layer(s) can include one or more of an electrode layer, a partially reflective and partially transmissive layer and a transparent dielectric layer. In some implementations, the optical

stack **16** is electrically conductive, partially transparent and partially reflective, and may be fabricated, for example, by depositing one or more of the above layers onto a transparent substrate **20**. The electrode layer can be formed from a variety of materials, such as various metals, for example indium tin oxide (ITO). The partially reflective layer can be formed from a variety of materials that are partially reflective, such as various metals, e.g., chromium (Cr), semiconductors, and dielectrics. The partially reflective layer can be formed of one or more layers of materials, and each of the layers can be formed of a single material or a combination of materials. In some implementations, the optical stack **16** can include a single semi-transparent thickness of metal or semiconductor which serves as both an optical absorber and conductor, while different, more conductive layers or portions (e.g., of the optical stack **16** or of other structures of the IMOD) can serve to bus signals between IMOD pixels. The optical stack **16** also can include one or more insulating or dielectric layers covering one or more conductive layers or a conductive/absorptive layer.

[0045] In some implementations, the layer(s) of the optical stack **16** can be patterned into parallel strips, and may form row electrodes in a display device as described further below. As will be understood by one having skill in the art, the term “patterned” is used herein to refer to masking as well as etching processes. In some implementations, a highly conductive and reflective material, such as aluminum (Al), may be used for the movable reflective layer **14**, and these strips may form column electrodes in a display device. The movable reflective layer **14** may be formed as a series of parallel strips of a deposited metal layer or layers (orthogonal to the row electrodes of the optical stack **16**) to form columns deposited on top of posts **18** and an intervening sacrificial material deposited between the posts **18**. When the sacrificial material is etched away, a defined gap **19**, or optical cavity, can be formed between the movable reflective layer **14** and the optical stack **16**. In some implementations, the spacing between posts **18** may be approximately 1–1000 μm , while the gap **19** may be on the order of less than 10,000 Angstroms ($\text{\AA}$).

[0046] In some implementations, each pixel of the IMOD, whether in the actuated or relaxed state, is essentially a capacitor formed by the fixed and moving reflective layers. When no voltage is applied, the movable reflective layer **14** remains in a mechanically relaxed state, as illustrated by the pixel **12** on the left in Figure 1, with the gap **19** between the

movable reflective layer **14** and optical stack **16**. However, when a potential difference, e.g., voltage, is applied to at least one of a selected row and column, the capacitor formed at the intersection of the row and column electrodes at the corresponding pixel becomes charged, and electrostatic forces pull the electrodes together. If the applied voltage exceeds a threshold, the movable reflective layer **14** can deform and move near or against the optical stack **16**. A dielectric layer (not shown) within the optical stack **16** may prevent shorting and control the separation distance between the layers **14** and **16**, as illustrated by the actuated pixel **12** on the right in Figure 1. The behavior is the same regardless of the polarity of the applied potential difference. Though a series of pixels in an array may be referred to in some instances as “rows” or “columns,” a person having ordinary skill in the art will readily understand that referring to one direction as a “row” and another as a “column” is arbitrary. Restated, in some orientations, the rows can be considered columns, and the columns considered to be rows. Furthermore, the display elements may be evenly arranged in orthogonal rows and columns (an “array”), or arranged in non-linear configurations, for example, having certain positional offsets with respect to one another (a “mosaic”). The terms “array” and “mosaic” may refer to either configuration. Thus, although the display is referred to as including an “array” or “mosaic,” the elements themselves need not be arranged orthogonally to one another, or disposed in an even distribution, in any instance, but may include arrangements having asymmetric shapes and unevenly distributed elements.

[0047] Figure 2 shows an example of a system block diagram illustrating an electronic device incorporating a 3x3 interferometric modulator display. The electronic device includes a processor **21** that may be configured to execute one or more software modules. In addition to executing an operating system, the processor **21** may be configured to execute one or more software applications, including a web browser, a telephone application, an email program, or any other software application.

[0048] The processor **21** can be configured to communicate with an array driver **22**. The array driver **22** can include a row driver circuit **24** and a column driver circuit **26** that provide signals to, e.g., a display array or panel **30**. The cross section of the IMOD display device illustrated in Figure 1 is shown by the lines 1–1 in Figure 2. Although Figure 2 illustrates a 3x3 array of IMODs for the sake of clarity, the display array **30** may contain a

very large number of IMODs, and may have a different number of IMODs in rows than in columns, and vice versa.

[0049] Figure 3 shows an example of a diagram illustrating movable reflective layer position versus applied voltage for the interferometric modulator of Figure 1. For MEMS interferometric modulators, the row/column (i.e., common/segment) write procedure may take advantage of a hysteresis property of these devices as illustrated in Figure 3. An interferometric modulator may use, for example, about a 10-volt potential difference to cause the movable reflective layer, or mirror, to change from the relaxed state to the actuated state. When the voltage is reduced from that value, the movable reflective layer maintains its state as the voltage drops back below, e.g., 10-volts, however, the movable reflective layer does not relax completely until the voltage drops below 2-volts. Thus, a range of voltage, approximately 3 to 7-volts, as shown in Figure 3, exists where there is a window of applied voltage within which the device is stable in either the relaxed or actuated state. This is referred to herein as the “hysteresis window” or “stability window.” For a display array **30** having the hysteresis characteristics of Figure 3, the row/column write procedure can be designed to address one or more rows at a time, such that during the addressing of a given row, pixels in the addressed row that are to be actuated are exposed to a voltage difference of about 10-volts, and pixels that are to be relaxed are exposed to a voltage difference of near zero volts. After addressing, the pixels are exposed to a steady state or bias voltage difference of approximately 5-volts such that they remain in the previous strobing state. In this example, after being addressed, each pixel sees a potential difference within the “stability window” of about 3–7-volts. This hysteresis property feature enables the pixel design, e.g., illustrated in Figure 1, to remain stable in either an actuated or relaxed pre-existing state under the same applied voltage conditions. Since each IMOD pixel, whether in the actuated or relaxed state, is essentially a capacitor formed by the fixed and moving reflective layers, this stable state can be held at a steady voltage within the hysteresis window without substantially consuming or losing power. Moreover, essentially little or no current flows into the IMOD pixel if the applied voltage potential remains substantially fixed.

[0050] In some implementations, a frame of an image may be created by applying data signals in the form of “segment” voltages along the set of column electrodes, in

accordance with the desired change (if any) to the state of the pixels in a given row. Each row of the array can be addressed in turn, such that the frame is written one row at a time. To write the desired data to the pixels in a first row, segment voltages corresponding to the desired state of the pixels in the first row can be applied on the column electrodes, and a first row pulse in the form of a specific “common” voltage or signal can be applied to the first row electrode. The set of segment voltages can then be changed to correspond to the desired change (if any) to the state of the pixels in the second row, and a second common voltage can be applied to the second row electrode. In some implementations, the pixels in the first row are unaffected by the change in the segment voltages applied along the column electrodes, and remain in the state they were set to during the first common voltage row pulse. This process may be repeated for the entire series of rows, or alternatively, columns, in a sequential fashion to produce the image frame. The frames can be refreshed and/or updated with new image data by continually repeating this process at some desired number of frames per second.

[0051] The combination of segment and common signals applied across each pixel (that is, the potential difference across each pixel) determines the resulting state of each pixel. Figure 4 shows an example of a table illustrating various states of an interferometric modulator when various common and segment voltages are applied. As will be readily understood by one having ordinary skill in the art, the “segment” voltages can be applied to either the column electrodes or the row electrodes, and the “common” voltages can be applied to the other of the column electrodes or the row electrodes.

[0052] As illustrated in Figure 4 (as well as in the timing diagram shown in Figure 5B), when a release voltage $V_{C_{REL}}$ is applied along a common line, all interferometric modulator elements along the common line will be placed in a relaxed state, alternatively referred to as a released or unactuated state, regardless of the voltage applied along the segment lines, i.e., high segment voltage V_{S_H} and low segment voltage V_{S_L} . In particular, when the release voltage $V_{C_{REL}}$ is applied along a common line, the potential voltage across the modulator (alternatively referred to as a pixel voltage) is within the relaxation window (see Figure 3, also referred to as a release window) both when the high segment voltage V_{S_H}

and the low segment voltage VS_L are applied along the corresponding segment line for that pixel.

[0053] When a hold voltage is applied on a common line, such as a high hold voltage VC_{HOLD_H} or a low hold voltage VC_{HOLD_L} , the state of the interferometric modulator will remain constant. For example, a relaxed IMOD will remain in a relaxed position, and an actuated IMOD will remain in an actuated position. The hold voltages can be selected such that the pixel voltage will remain within a stability window both when the high segment voltage VS_H and the low segment voltage VS_L are applied along the corresponding segment line. Thus, the segment voltage swing, i.e., the difference between the high VS_H and low segment voltage VS_L , is less than the width of either the positive or the negative stability window.

[0054] When an addressing, or actuation, voltage is applied on a common line, such as a high addressing voltage VC_{ADD_H} or a low addressing voltage VC_{ADD_L} , data can be selectively written to the modulators along that line by application of segment voltages along the respective segment lines. The segment voltages may be selected such that actuation is dependent upon the segment voltage applied. When an addressing voltage is applied along a common line, application of one segment voltage will result in a pixel voltage within a stability window, causing the pixel to remain unactuated. In contrast, application of the other segment voltage will result in a pixel voltage beyond the stability window, resulting in actuation of the pixel. The particular segment voltage which causes actuation can vary depending upon which addressing voltage is used. In some implementations, when the high addressing voltage VC_{ADD_H} is applied along the common line, application of the high segment voltage VS_H can cause a modulator to remain in its current position, while application of the low segment voltage VS_L can cause actuation of the modulator. As a corollary, the effect of the segment voltages can be the opposite when a low addressing voltage VC_{ADD_L} is applied, with high segment voltage VS_H causing actuation of the modulator, and low segment voltage VS_L having no effect (i.e., remaining stable) on the state of the modulator.

[0055] In some implementations, hold voltages, address voltages, and segment voltages may be used which produce the same polarity potential difference across the

modulators. In some other implementations, signals can be used which alternate the polarity of the potential difference of the modulators. Alternation of the polarity across the modulators (that is, alternation of the polarity of write procedures) may reduce or inhibit charge accumulation which could occur after repeated write operations of a single polarity.

[0056] Figure 5A shows an example of a diagram illustrating a frame of display data in the 3x3 interferometric modulator display of Figure 2. Figure 5B shows an example of a timing diagram for common and segment signals that may be used to write the frame of display data illustrated in Figure 5A. The signals can be applied to the, e.g., 3x3 array of Figure 2, which will ultimately result in the line time **60e** display arrangement illustrated in Figure 5A. The actuated modulators in Figure 5A are in a dark-state, i.e., where a substantial portion of the reflected light is outside of the visible spectrum so as to result in a dark appearance to, e.g., a viewer. Prior to writing the frame illustrated in Figure 5A, the pixels can be in any state, but the write procedure illustrated in the timing diagram of Figure 5B presumes that each modulator has been released and resides in an unactuated state before the first line time **60a**.

[0057] During the first line time **60a**: a release voltage **70** is applied on common line 1; the voltage applied on common line 2 begins at a high hold voltage **72** and moves to a release voltage **70**; and a low hold voltage **76** is applied along common line 3. Thus, the modulators (common 1, segment 1), (1,2) and (1,3) along common line 1 remain in a relaxed, or unactuated, state for the duration of the first line time **60a**, the modulators (2,1), (2,2) and (2,3) along common line 2 will move to a relaxed state, and the modulators (3,1), (3,2) and (3,3) along common line 3 will remain in their previous state. With reference to Figure 4, the segment voltages applied along segment lines 1, 2 and 3 will have no effect on the state of the interferometric modulators, as none of common lines 1, 2 or 3 are being exposed to voltage levels causing actuation during line time **60a** (i.e., VC_{REL} – relax and VC_{HOLD_L} – stable).

[0058] During the second line time **60b**, the voltage on common line 1 moves to a high hold voltage **72**, and all modulators along common line 1 remain in a relaxed state regardless of the segment voltage applied because no addressing, or actuation, voltage was applied on the common line 1. The modulators along common line 2 remain in a relaxed state due to the application of the release voltage **70**, and the modulators (3,1), (3,2) and (3,3)

along common line 3 will relax when the voltage along common line 3 moves to a release voltage **70**.

[0059] During the third line time **60c**, common line 1 is addressed by applying a high address voltage **74** on common line 1. Because a low segment voltage **64** is applied along segment lines 1 and 2 during the application of this address voltage, the pixel voltage across modulators (1,1) and (1,2) is greater than the high end of the positive stability window (i.e., the voltage differential exceeded a predefined threshold) of the modulators, and the modulators (1,1) and (1,2) are actuated. Conversely, because a high segment voltage **62** is applied along segment line 3, the pixel voltage across modulator (1,3) is less than that of modulators (1,1) and (1,2), and remains within the positive stability window of the modulator; modulator (1,3) thus remains relaxed. Also during line time **60c**, the voltage along common line 2 decreases to a low hold voltage **76**, and the voltage along common line 3 remains at a release voltage **70**, leaving the modulators along common lines 2 and 3 in a relaxed position.

[0060] During the fourth line time **60d**, the voltage on common line 1 returns to a high hold voltage **72**, leaving the modulators along common line 1 in their respective addressed states. The voltage on common line 2 is decreased to a low address voltage **78**. Because a high segment voltage **62** is applied along segment line 2, the pixel voltage across modulator (2,2) is below the lower end of the negative stability window of the modulator, causing the modulator (2,2) to actuate. Conversely, because a low segment voltage **64** is applied along segment lines 1 and 3, the modulators (2,1) and (2,3) remain in a relaxed position. The voltage on common line 3 increases to a high hold voltage **72**, leaving the modulators along common line 3 in a relaxed state.

[0061] Finally, during the fifth line time **60e**, the voltage on common line 1 remains at high hold voltage **72**, and the voltage on common line 2 remains at a low hold voltage **76**, leaving the modulators along common lines 1 and 2 in their respective addressed states. The voltage on common line 3 increases to a high address voltage **74** to address the modulators along common line 3. As a low segment voltage **64** is applied on segment lines 2 and 3, the modulators (3,2) and (3,3) actuate, while the high segment voltage **62** applied along segment line 1 causes modulator (3,1) to remain in a relaxed position. Thus, at the end

of the fifth line time **60e**, the 3x3 pixel array is in the state shown in Figure 5A, and will remain in that state as long as the hold voltages are applied along the common lines, regardless of variations in the segment voltage which may occur when modulators along other common lines (not shown) are being addressed.

[0062] In the timing diagram of Figure 5B, a given write procedure (i.e., line times **60a–60e**) can include the use of either high hold and address voltages, or low hold and address voltages. Once the write procedure has been completed for a given common line (and the common voltage is set to the hold voltage having the same polarity as the actuation voltage), the pixel voltage remains within a given stability window, and does not pass through the relaxation window until a release voltage is applied on that common line. Furthermore, as each modulator is released as part of the write procedure prior to addressing the modulator, the actuation time of a modulator, rather than the release time, may determine the line time. Specifically, in implementations in which the release time of a modulator is greater than the actuation time, the release voltage may be applied for longer than a single line time, as depicted in Figure 5B. In some other implementations, voltages applied along common lines or segment lines may vary to account for variations in the actuation and release voltages of different modulators, such as modulators of different colors.

[0063] The details of the structure of interferometric modulators that operate in accordance with the principles set forth above may vary widely. For example, Figures 6A–6E show examples of cross-sections of varying implementations of interferometric modulators, including the movable reflective layer 14 and its supporting structures. Figure 6A shows an example of a partial cross-section of the interferometric modulator display of Figure 1, where a strip of metal material, i.e., the movable reflective layer **14** is deposited on supports **18** extending orthogonally from the substrate **20**. In Figure 6B, the movable reflective layer **14** of each IMOD is generally square or rectangular in shape and attached to supports at or near the corners, on tethers **32**. In Figure 6C, the movable reflective layer **14** is generally square or rectangular in shape and suspended from a deformable layer **34**, which may include a flexible metal. The deformable layer **34** can connect, directly or indirectly, to the substrate **20** around the perimeter of the movable reflective layer **14**. These connections are herein referred to as support posts. The implementation shown in Figure 6C has

additional benefits deriving from the decoupling of the optical functions of the movable reflective layer **14** from its mechanical functions, which are carried out by the deformable layer **34**. This decoupling allows the structural design and materials used for the movable reflective layer **14** and those used for the deformable layer **34** to be optimized independently of one another.

[0064] Figure 6D shows another example of an IMOD, where the movable reflective layer **14** includes a reflective sub-layer **14a**. The movable reflective layer **14** rests on a support structure, such as support posts **18**. The support posts **18** provide separation of the movable reflective layer **14** from the lower stationary electrode (i.e., a portion of the optical stack **16** in the illustrated IMOD) so that a gap **19** is formed between the movable reflective layer **14** and the optical stack **16**, for example when the movable reflective layer **14** is in a relaxed position. The movable reflective layer **14** also can include a conductive layer **14c**, which may be configured to serve as an electrode, and a support layer **14b**. In this example, the conductive layer **14c** is disposed on one side of the support layer **14b**, distal from the substrate **20**, and the reflective sub-layer **14a** is disposed on the other side of the support layer **14b**, proximal to the substrate **20**. In some implementations, the reflective sub-layer **14a** can be conductive and can be disposed between the support layer **14b** and the optical stack **16**. The support layer **14b** can include one or more layers of a dielectric material, for example, silicon oxynitride (SiON) or silicon dioxide (SiO₂). In some implementations, the support layer **14b** can be a stack of layers, such as, for example, a SiO₂/SiON/SiO₂ tri-layer stack. Either or both of the reflective sub-layer **14a** and the conductive layer **14c** can include, e.g., an aluminum (Al) alloy with about 0.5% copper (Cu), or another reflective metallic material. Employing conductive layers **14a**, **14c** above and below the dielectric support layer **14b** can balance stresses and provide enhanced conduction. In some implementations, the reflective sub-layer **14a** and the conductive layer **14c** can be formed of different materials for a variety of design purposes, such as achieving specific stress profiles within the movable reflective layer **14**.

[0065] As illustrated in Figure 6D, some implementations also can include a black mask structure **23**. The black mask structure **23** can be formed in optically inactive regions (e.g., between pixels or under posts **18**) to absorb ambient or stray light. The black

mask structure **23** also can improve the optical properties of a display device by inhibiting light from being reflected from or transmitted through inactive portions of the display, thereby increasing the contrast ratio. Additionally, the black mask structure **23** can be conductive and be configured to function as an electrical bussing layer. In some implementations, the row electrodes can be connected to the black mask structure **23** to reduce the resistance of the connected row electrode. The black mask structure **23** can be formed using a variety of methods, including deposition and patterning techniques. The black mask structure **23** can include one or more layers. For example, in some implementations, the black mask structure **23** includes a molybdenum-chromium (MoCr) layer that serves as an optical absorber, a silicon dioxide (SiO₂) layer, and an aluminum alloy that serves as a reflector and a bussing layer, with a thickness in the range of about 30–80 Å, 500–1000 Å, and 500–6000 Å, respectively. The one or more layers can be patterned using a variety of techniques, including photolithography and dry etching, including, for example, carbon tetrafluoromethane (CF₄) and/or oxygen (O₂) for the MoCr and SiO₂ layers and chlorine (Cl₂) and/or boron trichloride (BCl₃) for the aluminum alloy layer. In some implementations, the black mask **23** can be an etalon or interferometric stack structure. In such interferometric stack black mask structures **23**, the conductive reflectors can be used to transmit or bus signals between lower, stationary electrodes in the optical stack **16** of each row or column. In some implementations, a spacer layer **35** can serve to generally electrically isolate the absorber layer **16a** from the conductive layers in the black mask **23**.

[0066] Figure 6E shows another example of an IMOD, where the movable reflective layer **14** is self supporting. In contrast with Figure 6D, the implementation of Figure 6E does not include support posts **18**. Instead, the movable reflective layer **14** contacts the underlying optical stack **16** at multiple locations, and the curvature of the movable reflective layer **14** provides sufficient support that the movable reflective layer **14** returns to the unactuated position of Figure 6E when the voltage across the interferometric modulator is insufficient to cause actuation. The optical stack **16**, which may contain a plurality of several different layers, is shown here for clarity including an optical absorber **16a**, and a dielectric **16b**. In some implementations, the optical absorber **16a** may serve both as a fixed electrode and as a partially reflective layer.

[0067] In implementations such as those shown in Figures 6A–6E, the IMODs function as direct-view devices, in which images are viewed from the front side of the transparent substrate **20**, i.e., the side opposite to that upon which the modulator is arranged. In these implementations, the back portions of the device (that is, any portion of the display device behind the movable reflective layer **14**, including, for example, the deformable layer **34** illustrated in Figure 6C) can be configured and operated upon without impacting or negatively affecting the image quality of the display device, because the reflective layer **14** optically shields those portions of the device. For example, in some implementations a bus structure (not illustrated) can be included behind the movable reflective layer **14** which provides the ability to separate the optical properties of the modulator from the electromechanical properties of the modulator, such as voltage addressing and the movements that result from such addressing. Additionally, the implementations of Figures 6A–6E can simplify processing, such as, e.g., patterning.

[0068] Figure 7 shows an example of a flow diagram illustrating a manufacturing process **80** for an interferometric modulator, and Figures 8A–8E show examples of cross-sectional schematic illustrations of corresponding stages of such a manufacturing process **80**. In some implementations, the manufacturing process **80** can be implemented to manufacture, e.g., interferometric modulators of the general type illustrated in Figures 1 and 6, in addition to other blocks not shown in Figure 7. With reference to Figures 1, 6 and 7, the process **80** begins at block **82** with the formation of the optical stack **16** over the substrate **20**. Figure 8A illustrates such an optical stack **16** formed over the substrate **20**. The substrate **20** may be a transparent substrate such as glass or plastic, it may be flexible or relatively stiff and unbending, and may have been subjected to prior preparation processes, e.g., cleaning, to facilitate efficient formation of the optical stack **16**. As discussed above, the optical stack **16** can be electrically conductive, partially transparent and partially reflective and may be fabricated, for example, by depositing one or more layers having the desired properties onto the transparent substrate **20**. In Figure 8A, the optical stack **16** includes a multilayer structure having sub-layers **16a** and **16b**, although more or fewer sub-layers may be included in some other implementations. In some implementations, one of the sub-layers **16a**, **16b** can be configured with both optically absorptive and conductive properties, such as the combined

conductor/absorber sub-layer **16a**. Additionally, one or more of the sub-layers **16a**, **16b** can be patterned into parallel strips, and may form row electrodes in a display device. Such patterning can be performed by a masking and etching process or another suitable process known in the art. In some implementations, one of the sub-layers **16a**, **16b** can be an insulating or dielectric layer, such as sub-layer **16b** that is deposited over one or more metal layers (e.g., one or more reflective and/or conductive layers). In addition, the optical stack **16** can be patterned into individual and parallel strips that form the rows of the display.

[0069] The process **80** continues at block **84** with the formation of a sacrificial layer **25** over the optical stack **16**. The sacrificial layer **25** is later removed (e.g., at block **90**) to form the cavity **19** and thus the sacrificial layer **25** is not shown in the resulting interferometric modulators **12** illustrated in Figure 1. Figure 8B illustrates a partially fabricated device including a sacrificial layer **25** formed over the optical stack **16**. The formation of the sacrificial layer **25** over the optical stack **16** may include deposition of a xenon difluoride (XeF₂)-etchable material such as molybdenum (Mo) or amorphous silicon (Si), in a thickness selected to provide, after subsequent removal, a gap or cavity **19** (see also Figures 1 and 8E) having a desired design size. Deposition of the sacrificial material may be carried out using deposition techniques such as physical vapor deposition (PVD, e.g., sputtering), plasma-enhanced chemical vapor deposition (PECVD), thermal chemical vapor deposition (thermal CVD), or spin-coating.

[0070] The process **80** continues at block **86** with the formation of a support structure e.g., a post **18** as illustrated in Figures 1, 6 and 8C. The formation of the post **18** may include patterning the sacrificial layer **25** to form a support structure aperture, then depositing a material (e.g., a polymer or an inorganic material, e.g., silicon oxide) into the aperture to form the post **18**, using a deposition method such as PVD, PECVD, thermal CVD, or spin-coating. In some implementations, the support structure aperture formed in the sacrificial layer can extend through both the sacrificial layer **25** and the optical stack **16** to the underlying substrate **20**, so that the lower end of the post **18** contacts the substrate **20** as illustrated in Figure 6A. Alternatively, as depicted in Figure 8C, the aperture formed in the sacrificial layer **25** can extend through the sacrificial layer **25**, but not through the optical stack **16**. For example, Figure 8E illustrates the lower ends of the support posts **18** in contact

with an upper surface of the optical stack **16**. The post **18**, or other support structures, may be formed by depositing a layer of support structure material over the sacrificial layer **25** and patterning to remove portions of the support structure material located away from apertures in the sacrificial layer **25**. The support structures may be located within the apertures, as illustrated in Figure 8C, but also can, at least partially, extend over a portion of the sacrificial layer **25**. As noted above, the patterning of the sacrificial layer **25** and/or the support posts **18** can be performed by a patterning and etching process, but also may be performed by alternative etching methods.

[0071] The process **80** continues at block **88** with the formation of a movable reflective layer or membrane such as the movable reflective layer **14** illustrated in Figures 1, 6 and 8D. The movable reflective layer **14** may be formed by employing one or more deposition steps, e.g., reflective layer (e.g., aluminum, aluminum alloy) deposition, along with one or more patterning, masking, and/or etching steps. The movable reflective layer **14** can be electrically conductive, and referred to as an electrically conductive layer. In some implementations, the movable reflective layer **14** may include a plurality of sub-layers **14a**, **14b**, **14c** as shown in Figure 8D. In some implementations, one or more of the sub-layers, such as sub-layers **14a**, **14c**, may include highly reflective sub-layers selected for their optical properties, and another sub-layer **14b** may include a mechanical sub-layer selected for its mechanical properties. Since the sacrificial layer **25** is still present in the partially fabricated interferometric modulator formed at block **88**, the movable reflective layer **14** is typically not movable at this stage. A partially fabricated IMOD that contains a sacrificial layer **25** also may be referred to herein as an “unreleased” IMOD. As described above in connection with Figure 1, the movable reflective layer **14** can be patterned into individual and parallel strips that form the columns of the display.

[0072] The process **80** continues at block **90** with the formation of a cavity, e.g., cavity **19** as illustrated in Figures 1, 6 and 8E. The cavity **19** may be formed by exposing the sacrificial material **25** (deposited at block **84**) to an etchant. For example, an etchable sacrificial material such as molybdenum (Mo) or amorphous silicon (a-Si) may be removed by dry chemical etching, e.g., by exposing the sacrificial layer **25** to a gaseous or vaporous etchant, such as vapors derived from solid xenon difluoride (XeF₂) for a period of time that is

effective to remove the desired amount of material, typically selectively removed relative to the structures surrounding the cavity **19**. Other etching methods, e.g. wet etching and/or plasma etching, also may be used. Since the sacrificial layer **25** is removed during block **90**, the movable reflective layer **14** is typically movable after this stage. After removal of the sacrificial material **25**, the resulting fully or partially fabricated IMOD may be referred to herein as a “released” IMOD.

[0073] Electromechanical devices having improved fill factor are disclosed. In some implementations, the electromechanical device can be an interferometric device including a pixel array and a mechanical layer that is anchored over an optical stack at each corner of each pixel. A via can be provided in a pixel of the array to electrically connect a stationary electrode to the black mask at a corner of the pixel. The via can be offset from where the mechanical layer is anchored over the optical stack at the corner of the pixel in an optically non-active area of the pixel. Offsetting the via can reduce the area of the black mask relative to a design in which the via overlaps with an anchoring hole used to anchor the mechanical layer over the optical stack, and thus the offset via can be employed in a pixel array to improve fill factor. For example, offsetting the via from the anchor hole can reduce the size of the anchor hole, thereby permitting the area of the black mask at pixel corners to be decreased. Thus, offsetting the via from the anchor hole can increase fill factor by reducing black mask area, thereby improving fill factor by increasing the ratio of optically active area in the pixel array relative to the total area of the array. In some implementations, the via is provided for only some of the pixels (or a fraction of the pixels), thereby further improving fill factor of the pixel array. For example, the via can only be provided at a corner of a pixel with the largest gap size.

[0074] Figure 9 shows an example of a flow diagram illustrating a manufacturing process **100** for an interferometric modulator. The process **100** starts at a block **102**. In a block **104**, a black mask is formed over a substrate. The substrate can be, for example, a transparent substrate including glass or plastic. The black mask can include a variety of materials and/or layers, including glass or a transparent polymeric material which permits images to be viewed through the substrate.

[0075] With continuing reference to Figure 9, the black mask structure can be configured to absorb ambient or stray light in optically inactive regions, such as regions between pixels and/or regions near pixel corners where the mechanical layer bends so as to improve the optical properties of a display device. Additionally, the black mask structure can be conductive and be configured to function as an electrical bussing layer. The black mask structure can include a plurality of layers, as described above.

[0076] In a block **106**, a dielectric layer is provided over the black mask. The dielectric layer can be used to electrically isolate portions of the black mask from one or more subsequently deposited layers. The dielectric layer can be any suitable electrical insulator, including, for example, silicon dioxide (SiO_2), silicon oxynitride (SiON) and/or tetraethyl orthosilicate (TEOS).

[0077] The process **100** illustrated in Figure 9 continues at a block **108**, in which a via is formed in the dielectric layer to the black mask. The via can permit a subsequently deposited layer to contact the black mask to aid in providing, for example, electrical connections for rows in the interferometric modulator array. As will be described in further detail below, vias need not be included for each pixel of the interferometric modulator array. Rather, vias can be provided only for a portion of the pixels of the array to aid in increasing fill factor.

[0078] In a block **110**, an optical stack is formed over the dielectric layer and via. The optical stack includes a stationary electrode, and the portion of the optical stack provided over the via can be used to make electrical connections between the stationary electrode and the black mask.

[0079] The process **100** illustrated in Figure 9 continues to a block **112**, in which a sacrificial layer is formed over the optical stack. The sacrificial layer is later removed to form a gap. The formation of the sacrificial layer over the optical stack may include deposition of a fluorine-etchable material such as molybdenum (Mo) or amorphous silicon (a-Si), in a thickness selected to provide, after subsequent removal, a gap having the desired size. Multiple sacrificial layers can be deposited to achieve a plurality of gap sizes. For example, for an IMOD array, each gap size can represent a different reflected color.

[0080] In a block **114**, an anchoring hole is formed in the sacrificial layer that is offset from the via. The anchoring hole can be formed by removing a portion of the sacrificial layer near a corner of a pixel. The anchoring hole can be used to form a post for supporting a subsequently deposited mechanical layer and/or to permit a self-supporting mechanical layer to contact the optical stack and/or another layer, as will be described in detail below. The anchoring hole formed in block **114** is not aligned with the via formed in block **110**. Rather, the anchoring hole and via are offset, thereby permitting the anchoring hole to have dimensions which are smaller relative to a scheme in which the via and the anchoring hole overlap, since the anchoring hole need not include additional margin to account for alignment with the via. Reducing the dimensions of the anchoring hole can aid in improving fill factor of the interferometric modulator array, since reducing the size of the anchoring hole permits the area of the optically non-active black mask disposed at the pixel corner to be decreased.

[0081] The process **100** illustrated in Figure 9 continues at a block **116** with the formation of a mechanical layer. The mechanical layer can be formed by employing one or more deposition steps, along with one or more patterning, masking, and/or etching steps, as was described earlier.

[0082] The process **100** illustrated in Figure 9 continues at a block **118** with the formation of a cavity or gap. The gap may be formed by exposing the sacrificial material, such as the sacrificial material deposited at the block **112**, to an etchant. For example, an etchable sacrificial material such as molybdenum (Mo), tungsten (W), tantalum (Ta) or polycrystalline silicon (poly-Si) or amorphous silicon (a-Si) may be removed by dry chemical etching.

[0083] After the sacrificial layer is removed, the mechanical layer is typically released and can be moved by electrostatic forces between an actuated and a relaxed position by application of a voltage between the stationary electrode and the mechanical layer. The mechanical layer can be anchored at the corner of a pixel to the optical stack over a portion of the black mask formed in the block **104**.

[0084] The process **100** illustrated in Figure 9 ends at a block **119**. Additional details of the method can be as described below. Many additional steps may be employed before, in the middle of, or after the illustrated sequence, but are omitted for clarity.

[0085] Figures 10A–10R show examples of cross-sectional schematic illustrations of various stages in a method of making an interferometric modulator. In Figure 10A, a black mask structure **23** has been provided over a substrate **20**. The substrate **20** can include a variety of transparent materials, as was described above. One or more layers can be provided on the substrate before providing the black mask structure **23**. For example, as shown in Figure 10A, an etch-stop layer **122** has been provided before providing the black mask structure **23** to serve as an etch-stop when patterning the black mask. In some implementations, the etch-stop layer **122** is an aluminum oxide layer having a thickness in the range of about 50–250 Å, for example, about 160 Å.

[0086] The black mask structure **23** can be configured to absorb ambient or stray light in optically inactive regions (e.g., between pixels) to improve the optical properties of a display device by increasing the contrast ratio. Additionally, the black mask structure **23** can be conductive and be configured to function as an electrical bussing layer.

[0087] With continuing reference to Figure 10A, the black mask structure **23** can include one or more layers. In some implementations, the black mask structure **23** includes an optical absorber layer **23a**, a dielectric layer **23b**, and a bussing layer **23c**. In some implementations, a MoCr layer serves as the optical absorber layer **23a**, a SiO₂ layer serves as the dielectric layer **23b**, and an aluminum alloy layer serves as the bussing layer **23c**, with a thickness in the range of, for example, about 30–80 Å, 500–1000 Å, and 500–6000 Å, respectively.

[0088] Figure 10B illustrates providing a shaping structure **126** over the substrate **20**. The shaping structure **126** can include a buffer oxide layer, such as silicon dioxide (SiO₂). The shaping structure **126** can have, for example, a thickness in the range of about 500–6000 Å. The shaping structure **126** can aid in maintaining a relatively planar profile across the substrate by filling in gaps between bussing or black mask structures **23**. However, the shaping structure **126** can overlap a portion of the black mask structure **23** to aid in forming a kink in the mechanical layer, as will be described in detail later below. In

particular, one or more layers, including the mechanical layer, can be deposited over the shaping structure **126**, thereby substantially replicating one or more geometric features of the shaping structure **126**. For example, as illustrated in Figure 10B, the shaping structure **126** can overlap the black mask structure **23** to form a protrusion **129**, which can produce an upwardly extending wave or kink in a subsequently deposited conformal layer, such as a mechanical layer.

[0089] Although various electromechanical systems devices illustrated herein are shown and described as including the shaping structure **126**, persons having ordinary skill in the art will recognize that the methods of forming a mechanical layer as described herein can be applicable to processes lacking the shaping structure **126**.

[0090] Figure 10C illustrates providing a spacer or dielectric layer **35**. The dielectric layer **35** can include, for example, silicon dioxide (SiO_2), silicon oxynitride (SiON), and/or tetraethyl orthosilicate (TEOS). In some implementations, the thickness of the dielectric layer **35** is in the range of about 3000–6000 Å, however, the dielectric layer **35** can have a variety of thicknesses depending on desired optical properties. The dielectric layer **35** can be removed over a portion above the black mask structure **23** (“above” here referring to the side of the black mask structure **23** opposite the substrate **20**), so as to permit formation of a via for electrically connecting a stationary electrode to the black mask structure **23**, as will be described in further detail below with reference to Figures 10E and 10F.

[0091] Figure 10D illustrates providing a color enhancement structure **134** over the dielectric layer **35**. The color enhancement structure **134** can be selectively provided over various pixel structures. For example, in a multi-color interferometric modulator implementation employing multiple gap heights, the color enhancement structure **134** can be provided over modulators having a particular gap size. In some implementations, the color enhancement structure **134** is a silicon oxynitride (SiON) layer having a thickness ranging between about 1500 Å to about 2500 Å, for example, about 1900 Å. The SiON layer can be patterned using any suitable technique, including, for example, an etch process employing tetrafluoromethane (CF_4) and/or oxygen (O_2).

[0092] One or more layers can be provided on the dielectric layer **35** before providing the color enhancement structure **134**. For example, as shown in Figure 10D, an

etch-stop layer **135** has been provided before providing the color enhancement layer **134**. In some implementations, the etch stop layer **135** is an aluminum oxide layer having a thickness in the range of about 50–250 Å, for example, about 160 Å.

[0093] Figure 10E illustrates forming a via **138** in the dielectric layer **35**. The via **138** can permit a subsequently deposited layer to contact the black mask structure **23**, as will be described in detail below. As shown in Figure 10E, vias need not be included over each region of the black mask **23**. Rather, vias can be placed periodically in the interferometric modulator so as to increase the fill factor of the array.

[0094] Figures 10F and 10G illustrate forming an optical stack **16** over the dielectric layer **35** and the via **138**. The optical stack **16** can include a plurality of layers. For example, the optical stack **16** can include a stationary electrode layer **140**, such as molybdenum-chromium (MoCr), a transparent dielectric layer **141**, such as silicon dioxide (SiO₂), and an etch-stop layer **142**, such as aluminum oxide (AlO_x), for protecting the transparent dielectric layer **141** during subsequent sacrificial layer etch processes and/or attack during sacrificial layer removal processes. The etch-stop layer **142** can be formed from a variety of materials that are partially reflective such as various metals, semiconductors, and dielectrics. The partially reflective layer can be formed of one or more sub-layers, and each of the sub-layers can be formed of a single material or a combination of materials. In some implementations, some or all of the layers of the optical stack **16**, including, for example, the stationary electrode **140**, are patterned into parallel strips, and may form row electrodes in a display device. As illustrated in Figures 10F and 10G, one or more layers of the optical stack **16** may physically and electrically contact the black mask structure **23**. For example, the via **138** permits the stationary electrode **140** to electrically contact the black mask structure **23**.

[0095] Figures 10H–10J illustrate providing and patterning a plurality of sacrificial layers over the optical stack **16**. The sacrificial layers are later removed to form a gap or cavity, as will be discussed below. The use of a plurality of sacrificial layers can aid in the formation of a display device having a multitude of resonant optical gaps. For example, as illustrated, various gap sizes can be created by selectively providing a first sacrificial layer **144**, a second sacrificial layer **145**, and a third sacrificial layer **146**. This can

provide a first gap size (or “high gap”) equal to about a sum of the thicknesses of the first, second and third sacrificial layers **144–146**, a second gap size (or “mid gap”) equal to about a sum of the thicknesses of the second and third sacrificial layers **145, 146**, and a third gap size (or “low gap”) equal to about the thickness of the third sacrificial layer **146**. For an interferometric modulator array, a high gap can correspond to a high gap pixel, a mid gap can correspond to a mid gap pixel, and a low gap can correspond to a low gap pixel. Each of these pixels that are configured with different gap size can produce a different reflected color. Accordingly, such pixels may be referred to herein as high, mid, or low gap pixels.

[0096] The formation of the first, second and third sacrificial layers **144–146** over the optical stack **16** may include deposition of molybdenum (Mo) or amorphous silicon (a-Si). In some implementations, the first sacrificial layer **144** is a molybdenum (Mo) layer having a thickness ranging between about 200 Å to about 1,000 Å, for example, about 400 Å, the second sacrificial layer **145** is a Mo layer having a thickness ranging between about 200 Å to about 1,000 Å, for example, about 400 Å, and the third sacrificial layer **146** is a Mo layer having a thickness ranging between about 600 Å to about 2,000 Å, for example, about 1,600 Å.

[0097] Although Figures 10H–10J are illustrated for a configuration in which the second sacrificial layer **145** is provided over the first sacrificial layer **144** and the third sacrificial layer **146** is provided over the first and second sacrificial layers **144, 145**, other configurations are possible. For example, the first, second and third sacrificial layers **144–146** need not overlap, and more or fewer sacrificial layers can be formed to provide desired gap sizes.

[0098] Figure 10K illustrates patterning the sacrificial layers **144–146** between pixels. The sacrificial layers can be patterned in a variety of ways, including using an etchant, such as chlorine (Cl₂) and/or oxygen (O₂). The portion of the sacrificial layers **144–146** removed between pixels, such as at the corners of pixels, can create anchor holes **150**, which can be used to form a post for supporting a subsequently deposited mechanical layer and/or to aid in anchoring a self-supporting mechanical layer, as will be described below.

[0099] The anchor holes **150** of the illustrated partially fabricated interferometric modulator are not aligned with the via **138**. This can permit the anchor hole **150** to have a

width w_1 which is smaller relative to a scheme in which the via **138** and the anchor hole **150** overlap to form an anchor via, since the anchor hole **150** need not include additional margin to account for alignment with via **138**. Additionally, by offsetting the via **138** and the anchor hole **150**, non-uniformity across pixels related to anchor hole and via misalignment can be avoided.

[0100] Furthermore, as illustrated in Figure 10L, in some implementations the via **138** need not be included over each region of the black mask **23**. Rather, vias can be periodically provided over less than all of the pixels of an array. By reducing the width w_1 of the anchor hole **150** and by reducing the total number of vias **138** in the interferometric modulator array, the total area of the black mask **23** can be reduced, thereby improving the fill factor.

[0101] Figure 10L illustrates providing and patterning a reflective layer **14a** and a support layer **14b** of a mechanical layer. The reflective layer **14a** can be a reflective material including, for example, aluminum alloys. In some implementations, the reflective layer **14a** includes aluminum-copper (AlCu) having copper by weight in the range of about 0.3 % to 1.0%, for example, about 0.5%. The reflective layer **14a** can be any suitable thickness, such as a thickness in the range of about 200 Å to about 500 Å, for example, about 300 Å.

[0102] The support layer **14b** can be used to assist a photolithography process by serving as an antireflection layer and/or to aid in obtaining a desired mechanical flexibility of a fully fabricated mechanical layer. In some implementations, the support layer **14b** is a silicon oxynitride (SiON) layer having a thickness in the range of about 50 Å to about 1,000 Å, for example, about 250 Å.

[0103] Figure 10M illustrates providing an etch-stop layer **154** over the support layer **14b**, over the transparent dielectric layer **141** on the bottom of anchor holes **150**, and over the sacrificial layers **144–146** on the sidewalls of the anchor holes **150**. The etch-stop layer **154** can be, for instance, an aluminum oxide (AlO_x) layer having a thickness in the range of about 100 Å to about 300 Å, for example, 200 Å. The etch-stop layer **154** can be employed to protect layers of the interferometric device from subsequent etching steps. For example, as will be described later below, when the sacrificial layers **144–146** are removed to

release the mechanical layer, the etch-stop layer **154** can protect support layers from an etchant used to remove the sacrificial layers **144–146**.

[0104] Figures 10N–10P illustrate providing and patterning a first support layer **160**, a second support layer **161**, and a third support layer **162**. The first, second, and third support layers **160–162** can be used for a variety of functions. For example, the first, second, and third support layers **160–162** can be used to form support structures, including posts and/or rivets. Furthermore, the first, second, and third support layers **160–162** can be incorporated into all or part of the mechanical layer to aid in achieving a structural rigidity corresponding to a desired actuation voltage and/or to aid in obtaining a self-supporting mechanical layer.

[0105] As illustrated in Figure 10P, a portion **160a** of the first support layer **160** can serve as a support post for a high gap pixel and a mid gap pixel, while a portion **160b** of the first support layer **160** can be included in the mechanical layer of a low gap pixel. By employing the first, second and third support layers **160–162** to serve a variety of functions across pixels of varying gap heights, flexibility in the design of the interferometric device can be improved. In some implementations, the mechanical layer can be self-supporting over certain pixels and can be supported by a support post or other structures over other pixels.

[0106] The sacrificial layers **144–146** can be later removed to form various pixels in the interferometric modulator array. The thickness of the mechanical layer formed above the sacrificial layers can be varied by selectively including the first, second and third support layers **160–162** in the mechanical layer over various pixels of the array. For example, the third support layer **162** can be provided over high gap, mid gap and low gap pixels, the second support layer **161** can be provided over mid and low gap pixels, and the first support layer **160** can be provided over low gap pixels. By varying the thickness of the mechanical layer across pixels of different gap heights, the desired stiffness of the mechanical layer can be achieved for each gap height, which can aid in permitting the same pixel actuation voltage for different sized air-gaps for color display applications.

[0107] The first, second and third support layers **160–162** can be formed by a dielectric material, such as silicon oxynitride (SiON). In some implementations, the

thickness of the first, second and third supporting layers **160–162** can each be in the range of about 600 Å to about 3,000 Å, for example, about 1,000 Å.

[0108] Figure 10Q illustrates providing and patterning a cap layer **14c** to form a completed mechanical layer **14**. The cap layer **14c** can be provided conformally over the supporting layers **160–162** and can have a pattern similar to that of the reflective layer **14a**. Patterning the cap layer **14c** similar to that of the reflective layer **14a** can aid in balancing stresses in the mechanical layer **14**. By balancing stresses in the mechanical layer **14**, the shaping and curvature of the mechanical layer **14** upon removal of the sacrificial layers **144–146** can be controlled, as will be described below. Furthermore, balanced stresses in the mechanical layer **14** can reduce the sensitivity of gap height of a released interferometric modulator to temperature.

[0109] The cap layer **14c** can be a metallic material and can be, for example, the same material as the reflective layer **14a**. In some implementations, the cap layer **14c** includes aluminum-copper (AlCu) having copper by weight in the range of about 0.3 % to 1.0%, for example, about 0.5%, and the thickness of the cap layer **14c** is selected to be in the range of about 200 Å to about 500 Å, for example, about 300 Å.

[0110] As was described above the mechanical layer **14** can include a variety of layers across different pixels of the interferometric modulator array. Additional details of the mechanical layer **14** can be as described below.

[0111] Figure 10R illustrates removal of the sacrificial layers **144–146** to form a first or high gap **19a**, a second or mid gap **19b**, and a third or low gap **19c**. Additional steps can be employed before forming first, second and third gaps **19a–19c**. For example, sacrificial release holes can be formed in the mechanical layer **14** to aid in removing the sacrificial layers **144–146**.

[0112] The gaps **19a–19c** can be formed by exposing the sacrificial layers **144–146** to an etchant, as was described above. The sacrificial layer can be exposed for a period of time that is effective to remove the material, typically selectively relative to the structures surrounding the gaps **19a–19c**. Other selective etching methods, for example, wet etching and/or plasma etching, also can be used.

[0113] The etch-stop layer **154** can protect the first support layer **160** from the sacrificial release chemistry used to remove the sacrificial layers **144–146**. This can permit the first support layer **160** to be a structural material that would otherwise be etched by the release chemistry used to remove the sacrificial layers.

[0114] The dielectric protection layer **142** can protect layers of the optical stack **16**, such as the dielectric layer **141**, from the sacrificial release chemistry used to remove the sacrificial layers **144–146**. Inclusion of the dielectric protection layer **142** can aid reducing or preventing damage to the optical stack during release, thereby improving optical performance.

[0115] The first, second and third gaps **19a–19c** can correspond to cavities that interferometrically enhance different colors. For example, the first, second and third gaps **19a–19c** can have heights selected to interferometrically enhance, for example, blue, red, and green, respectively. The first or high gap **19a** can be associated with a first or high gap pixel **172a**, the second or mid gap **19b** can be associated with a second or mid gap pixel **172b**, and the third or low gap **19c** can be associated with a third or low gap pixel **172c**.

[0116] In order to permit approximately the same actuation voltage to collapse the mechanical layer for each gap size, the mechanical layer **14** can include different materials, number of layers, or thicknesses over each of the gaps **19a–19c**. Thus, as shown in Figure 10R, a portion of the mechanical layer **14** over the high gap **19a** can include the reflective layer **14a**, the support layer **14b**, the etch-stop layer **154**, the third support layer **162** and the cap layer **14c**, while a portion of the mechanical layer **14** over the mid gap **19b** can further include the second support layer **161**. Similarly, in contrast to the portion of the mechanical layer **14** over the high gap **19a**, a portion of the mechanical layer **14** over the low gap **19c** can further include the first and second support layers **160, 161**.

[0117] As described above, the first, second and third support layers **160–162** can serve different functions across different pixels of the interferometric modulator array. For example, the first support layer **160** can be used for supporting the mechanical layer **14** over high and mid gap pixels and for increasing the structural rigidity of low gap pixels. Additionally, the second support layer **161** can be used for supporting the mechanical layer **14** over high gap pixels and for increasing the structural rigidity of mid gap pixels, and the

third support layer can be used for increasing the structural rigidity of low, mid and high gap pixels. Thus, the first portion **160a** of the first support layer **160** serves as a post for supporting the mechanical layer **14** over the high and mid gaps **19a**, **19b**, while the second portion **160b** of the first support layer **160** is included in the mechanical layer **14** over the low gap **19c**. Using a plurality of support layers permits approximately the same actuation voltage to collapse the mechanical layer for each gap size.

[0118] After removal of the sacrificial layers **144–146**, the mechanical layer **14** can become displaced away from the substrate by a launch height and can change shape or curvature at this point for a variety of reasons, such as residual mechanical stresses. As described above, the cap layer **14c** can be used with the reflective layer **14a** to aid in balancing the stresses in the mechanical layer when released. Thus, the cap layer **14c** can have a thickness, composition, and/or stress selected to aid in tuning the launch and curvature of the mechanical layer upon removal of the sacrificial layers **144–146**. Additionally, providing the mechanical layer **14** over the shaping structure **126**, and particularly over the protrusion **129** of Figure 10B, a kink **171** is formed in the mechanical layer **14**. The geometric features of the kink **171** can be controlled by varying the thickness of the shaping structure **126**, thereby controlling the stresses in the mechanical layer **14**. Control of the launch height can allow the selection of a sacrificial layer thickness needed for a particular gap size which is desirable from a fabrication and optical performance standpoint.

[0119] As was described above, the anchor holes **150** of Figure 10K are not aligned with the via **138**. Thus, as shown in Figure 10R, the mechanical layer **14** is anchored to the optical stack **16** over the black mask **23** at a point offset from the via **138**. As described above, anchoring the mechanical layer **14** at a point offset from the via **138** can permit the black mask **23** to be smaller relative to a design in which the mechanical layer **14** is anchored over the black mask **23** in the same region as the via is located. For example, by offsetting the via **138** from an anchoring hole used to anchor the mechanical layer **14**, the size of the anchor hole need not have increased area to account for process alignment with the via **138**. Additionally, by offsetting the via **138** from the anchor hole used to secure the mechanical layer **14**, non-uniformity across pixels related to anchor hole and via

misalignment can be avoided. Thus, by offsetting the via **138** from the anchor hole fill factor of the interferometric modulator array can be improved.

[0120] Furthermore, as illustrated in Figure 10R, the via **138** need not be included in each pixel. Rather, the vias can be provided over less than all of the pixels of an array. For example, as shown in Figure 10R, the via **138** has been included near a corner **123** of the high gap pixel **172a**. Furthermore, vias have not been included at corners of mid gap pixel **172b** or low gap pixel **172c**. By providing vias for less than all of the pixels of the array, the total number of vias in the interferometric modulator array can be reduced, which in turn can reduce the total area of the black mask **23**. Since the black mask **23** is optically opaque, reducing the total area of the black mask **23** improves the fill factor of the pixel array.

[0121] As illustrated in Figure 10R, the black mask **23** has a footprint larger than the footprint of the structures used to support the mechanical layer **14**. For example, the portion **160a** of the first support layer **160** operates as a support post for the portion of the mechanical layer **14** associated with the high gap pixel **172a**, and has a width less than that of the black mask **23** at the corner **123** of the high gap pixel **172a**. The additional width of the black mask **23** around the anchoring region of the mechanical layer can mask a bending portion of the mechanical layer **14** during actuation. For example, when the mechanical layer **14** is actuated, while most of the mechanical layer **14** can be aligned in a plane and can be in contact with the optical stack **16**, a portion of the mechanical layer **14** (e.g., along edges of a pixel) may not be in contact with the optical stack **16**, and thus can interferometrically produce an undesired color if additional black mask is not provided. The portion of the mechanical layer **14** out of contact with the optical stack **16** during actuation can increase for pixels having larger gap heights. For example, the bending region of the high gap pixel **172a** can be greater than that of the low gap pixel **172c**, because the gap **19a** is larger than the gap **19c**.

[0122] In some implementations, vias, such as the via **138**, are included at one or more corners of pixels of the largest gap size. Positioning the vias **138** near corners of pixels of the largest gap size can be advantageous because high gap pixels can have a larger bending region in the actuated state, and thus can have a larger optically inactive area at pixel corners relative to mid and low gap pixels. Thus, in some implementations, the black mask can be

larger at corners of high gap sub-pixels to account for the larger bending region and to provide room for a via. However, since the vias need not be included for each pixel of the array, the total area of the black mask **23** can be reduced, and the fill factor of the interferometric modulator array can be improved.

[0123] The vias, such as the via **138**, can have a variety of shape and sizes. For example, the vias can be shaped as a circle, oval, octagon and/or any other suitable shape. The size of the vias can vary with process. In some implementations, each via **138** has a largest width in the range of about 1.5 μm to about 3.0 μm , for example, about 2.4 μm . Additional details of the vias can be as described below.

[0124] Figures 11A–11C show examples of plan view schematic illustrations of various interferometric modulator arrays. In Figure 11A, an interferometric modulator array **180** is illustrated. The interferometric modulator array **180** includes a plurality of pixels of different gap sizes, including a first gap or high gap pixel **174a**, a second gap or mid gap pixel **174b**, and a third gap or low gap pixel **174c**. The high, mid and low gap pixels **174a–174c** can be similar to the high, mid, and low gap pixels **172a–172c** of Figure 10R. However, the high, mid and low gap pixels **174a–174c** need not be identical to the high, mid, and low gap pixels **172a–172c**.

[0125] As shown in Figure 11A, an electrically conductive black mask is disposed on the substrate at each corner of the high, mid and low gap pixels **174a–174c**. Although not illustrated in Figure 11A, a dielectric layer has been provided over the black mask, and an optical stack including a stationary electrode has been provided over the dielectric layer. The vias **138** are used to electrically contact the stationary electrode of the optical stack to various portions of the black mask **23**.

[0126] The mechanical layer **14** is positioned over the optical stack to define the gap heights of the high, mid, and low gap pixels **174a–174c**. The mechanical layer **14** is anchored over the black mask **23** at each of the corners of the high, mid and low pixels **174a–174c**. For example, the high gap pixel **174a** includes four corners **123a–123d**, and the mechanical layer is anchored over the optical stack at each of the four corners **123a**, **123b**, **123c**, and **123d** at anchoring holes **150a**, **150b**, **150c**, and **150d**, respectively. As described above, the mechanical layer **14** can be anchored over the black mask in a multitude of ways.

[0127] The area of the black mask **23** surrounding each corner of each pixel need not be the same for each pixel of the array **180**. Rather, the area of black mask at a pixel corner can be larger for pixels having a relatively larger gap, such as pixels of the largest gap size, so as to account for increased mechanical layer bending during actuation. For example, the area of the black mask at each of the corners **123a–123d** of the high gap pixel **174a** is larger than the area of the black mask at a corner **123e** of the mid gap pixel **174b** and area of the black mask at a corner **123f** of the low gap pixel **174c**. As shown in Figure 11A, the increased portion or bulge of the black mask at the corner **123a** of the high gap pixel **174a** can be used for providing the via **138**.

[0128] With continuing reference to Figure 11A, in some implementations, the via **138** is positioned at a corner of the high gap pixel **174a** adjacent a mid gap pixel. However, as will be described below with reference to Figures 11B and 11C, the via **138** can be provided in other locations and/or at multiple corners of high gap pixels.

[0129] The distance to the edge of the black mask along a line from the center of the anchoring hole to the center of a pixel can vary depending on the gap height of the pixel. For example, the distance d_1 from the edge of the black mask along a line to the center of the anchoring hole of a high gap pixel can be in the range of about 10 μm to about 12 μm , while the distance d_2 from the edge of the black mask along a line to the center of the anchoring hole of a low or mid gap pixel can be in the range of about 7 μm to about 9 μm .

[0130] With continuing reference to Figure 11A, the black mask **23** can be included in other regions of a pixels, such as along pixel edges, in addition to being provided at pixel corners. The black mask regions along the edges of pixels also can be used to provide electrical connections along a row or column, and can include breaks along one or more edges of each pixel to provide the desired electrical connectivity. For example, the black mask **23** includes a break along an edge bordering the high gap pixel **174a** and the low gap pixel **174c**. In some implementations, the breaks have a length in the range of about 2 μm to about 3 μm .

[0131] As described above, the interferometric device array **180** includes vias offset from the anchoring holes or other structures used to secure the mechanical layer **14**. For example, a via **138** at the corner **123a** of the high gap pixel **174a** is offset from the anchor

hole **150a**. In some implementations, distance from the center of the via to the center of the anchoring hole to which the mechanical layer is secured ranges between about 6 μm to about 8 μm .

[0132] Offsetting the via **138** and the anchor hole can permit the anchor hole to have an area, when viewed from above, which is smaller relative to a scheme in which the via and the anchor hole overlap to form an anchor via. For example, the anchor hole **150a** need not include additional margin to account for alignment with via **138** that is disposed at the corner **123a** of the high gap pixel **174a**. In some implementations, employing circular vias and circular anchor holes, the radius of the anchor hole **150a** is in the range of about 4 μm to about 7 μm , and the radius of the via **138** is in the range of about 2 μm to about 4 μm .

[0133] In Figure 11A, the vias are provided at one corner of each high gap pixel. For example, the high gap pixel **174a** includes the via **138** at a first corner **123a**, but a via has not been included at second, third and fourth corners **123b–123d** of the high gap pixel **174a**.

[0134] Figure 11B illustrates an interferometric modulator array **182** in accordance with another implementation. The interferometric modulator array **182** of Figure 11B is similar to the interferometric modulator array **180** of Figure 11A, except the interferometric modulator array **182** includes vias at two corners of each high gap pixel. For example, the high gap pixel **174a** includes vias **138** at a first corner **123a** and at a second corner **123b**, but a via has not been included at the third and fourth corners **123c, 123d** of the high gap pixel **174a**.

[0135] Figure 11C illustrates an interferometric modulator array **184** in accordance with yet another implementation. The interferometric modulator array **184** of Figure 11C is similar to the interferometric modulator array **180** of Figure 11A, except the interferometric modulator array **184** includes vias at four corners of a high gap pixel. For example, the high gap pixel **174a** includes vias **138** at first, second, third and fourth corners **123a–123d**. Persons having ordinary skill in the art will appreciate that other configurations of the vias **138** are possible in addition to those illustrated in Figures 11A–11C, including, for example, a configuration with three vias per high gap pixel, a configuration in which vias are included for both high gap and mid gap pixels, and/or any other suitable configuration.

[0136] Figure 12 shows an example of a flow diagram illustrating a manufacturing process **190** for an interferometric modulator. The process **190** starts at a block **191**. In a block **192**, a black mask is formed over a substrate. The substrate can be, for example, a transparent substrate, and the black mask structure can be electrically conductive and configured to absorb ambient or stray light in optically inactive pixel regions. The black mask can mask each corner of each pixel in an array of pixels of the interferometric modulator. Additional details of the black mask can be as described above.

[0137] In a block **193**, a dielectric layer is provided over the black mask. The dielectric layer can be used to electrically isolate the black mask from one or more subsequently deposited layers. The dielectric layer can be any suitable electrical insulator, including, for example, silicon dioxide (SiO₂), silicon oxynitride (SiON), and tetraethyl orthosilicate (TEOS). Additional details of the dielectric layer can be as described earlier.

[0138] The process **190** illustrated in Figure 12 continues at a block **194**, in which an optical stack is formed over the dielectric layer. As discussed above, the optical stack of an interferometric modulator can be electrically conductive, partially transparent and partially reflective, and can include a stationary electrode for providing the electrostatic operation for the interferometric modulator device.

[0139] In a block **195**, a mechanical layer is formed over the optical stack. Forming the mechanical layer can include providing a sacrificial layer, depositing one or more layers over the sacrificial layer, and removing the sacrificial layer to release the mechanical layer.

[0140] With continuing reference to Figure 12, the process **190** continues at a block **196**, in which the mechanical layer is anchored over the optical stack at each corner of each pixel of the array. For example, a support post can be formed at corners of a pixel and can be used to anchor the mechanical layer over the optical stack at corners of the pixel. However, the mechanical layer can otherwise be anchored, as was described above.

[0141] In a block **198**, a conductive via is provided in a pixel of the array. The conductive via is in the dielectric layer and electrically connects the stationary electrode to the black mask. The via is disposed at a corner of the pixel, and is offset from where the mechanical layer is anchored over the optical stack in an optically non-active area of the

pixel. Offsetting the via relative to where the mechanical layer is anchored at the corner of the pixel can permit the black mask to be smaller compared to a design in which a via and an anchoring region of the mechanical layer overlap. Additional details of the offset via can be as described earlier. The method ends at a block **199**.

[0142] Figure 13A shows an example of a plan view schematic illustration of an interferometric modulator array **200**. The illustrated interferometric device array **200** includes a first or high gap pixel **202a**, a second or mid gap pixel **202b**, a third or low gap pixel **202c**, a mechanical layer **14**, a black mask **23**, anchoring holes **150**, and vias **138**.

[0143] Although not illustrated to improve figure clarity, a dielectric layer has been provided over the black mask **23**, and an optical stack including a stationary electrode has been provided over the dielectric layer. The vias **138** are used to electrically contact the stationary electrode of the optical stack to various portions of the black mask **23**.

[0144] The black mask **23** is disposed at corners of each pixel, and along portions of pixel edges. The black mask **23** can be used to provide electrical connections along a row or column, and can include breaks along one or more edges of each pixel to provide the desired electrical connectivity. For example, the black mask **23** includes a break along an edge bordering the high gap pixel **202a** and the mid gap pixel **202b**. In some implementations, the breaks have a length d_3 in the range of about 2 μm to about 4 μm .

[0145] In contrast to the pixel arrays of Figures 11A–11C, the pixel array **200** of Figure 13A includes vias disposed along the edges of pixels. For example, a via **138** has been disposed in the high gap pixel **202a** in a channel **204** of the black mask **23** along an edge of high gap pixel **202a** that borders the mid gap pixel **202b**. As shown in Figure 13A, vias need not be included at pixel corners in this implementation. Rather, the via **138** can be included along the edge of a pixel, and can be offset from the edge of the pixel in a direction towards the center of the pixel. Providing vias **138** along the edges of pixels in this manner rather than at pixel corners can aid in improving fill factor of the interferometric device array by reducing the area of the black mask used to mask pixel corners.

[0146] As shown in Figure 13A, not all pixel edges need to include a via. For example, as shown in Figure 13A, vias can be provided only in high gap pixels. In some

implementations, vias are included in high gap pixels along edges of the high gap pixels that border mid gap pixels.

[0147] The vias **138** can be disposed in channels of the black mask running along pixel edges, and a side of the channel including the via **138** can include a black mask patch or bulge **203** surrounding the footprint of the via **138**. By including the bulge **203** in the black mask channel, the vias **138** can become more robust against process variations. For example, the black mask bulge **203** can reduce variation in topology in the area surrounding each via **138**, thereby reducing manufacturing errors related to depositing conformal layers over the vias. As shown in Figure 13A, the vias and bulges can be disposed in high gap pixels. Since high gap pixels can contribute less to reflectance less than low and mid gap pixels, providing a bulge in a high gap pixel can have less impact on brightness relative to a design having a bulge in a mid and/or low gap pixel.

[0148] In some implementations, such as the implementation illustrated in Figure 13A, the via **138** is positioned about half-way along a length of a pixel edge of the high gap pixel **202a**. However, the via **138** can be provided in other location along an edge of a pixel. In some implementations, the via **138** is positioned between about 1/3 to about 2/3 along a length of a pixel edge.

[0149] Figure 13B shows an example of a cross-sectional schematic illustration of the interferometric modulator array of Figure 13A taken along the line 13B–13B. The cross-section includes the high gap pixel **202a**, the mid gap pixel **202b**, the substrate **20**, the black mask channel **204**, the black mask bulge **203**, the via **138**, etch-stop layer **122**, the shaping structure **126**, the dielectric layer **35**, the color enhancement structure **134**, the etch-stop layer **135**, the optical stack **16**, high and mid gaps **19a**, **19b**, the reflective layer **14a**, the support layer **14b**, the etch-stop layer **154**, the second and third support layers **161**, **162**, and the cap layer **14c**. Additional details of the high and mid gap pixels **202a**, **202b** can be similar to those described earlier.

[0150] In some implementations, the width d_4 of the black mask from the edge of the bulge **203** to the edge of the high gap pixel **202a** adjacent the mid gap pixel **202b** is in the range of about 3 μm to about 4 μm , and the width d_5 from the edge of the black mask to the same pixel edge in a region of the black mask not having the bulge **203** is in the range of

about 2 μm to about 3 μm . The bulge **203** can have any suitable area. In some implementations in which the bulge is a portion of a circle, the radius of the bulge is in the range of about 3 μm to about 5 μm .

[0151] The distance d_6 from the edge of via **138** to the edge of the black mask bulge **203** can be selected to reduce variation in topology in the area surrounding the via **138**. For example, the vias **138** can cause topology changes in subsequently deposited conformal layers, such as the layers from the optical stack **16** to the cap **14c** layer. By increasing the distance d_6 , variation in topology can be reduced. In some implementations, the distance d_6 is selected to be in the range of about 2 μm to about 3 μm . The via **138** can be offset from the edge of the pixel in a direction towards the center of the pixel by any suitable distance. In some implementations, the distance d_7 from the center of the via **138** to the edge of the high gap pixel **202a** bordering the mid gap pixel **202b** is in the range of about 1 μm to about 3 μm .

[0152] Figure 14 shows an example of a flow diagram illustrating a manufacturing process **210** for an interferometric modulator. The process **210** starts at a block **211**. In a block **212**, a black mask is formed over a substrate. The substrate can be, for example, a transparent substrate, and the black mask structure can be configured to absorb ambient or stray light in optically inactive regions, such as those between pixels, and can be electrically conductive. The black mask can mask each corner and at least one edge region of each pixel in an array of pixels of the interferometric modulator. Additional details of the black mask can be as described earlier.

[0153] In a block **214**, a dielectric layer is provided over the black mask. The dielectric layer can be used to electrically isolate the black mask from one or more subsequently deposited layers. The dielectric layer can be any suitable electrical insulator, including, for example, silicon dioxide (SiO_2), silicon oxynitride (SiON), and tetraethyl orthosilicate (TEOS). Additional details of the dielectric layer can be as described earlier.

[0154] With continuing reference to Figure 14, the process **210** continues at a block **216**, in which an optical stack is formed over the dielectric layer. As discussed above, the optical stack of an interferometric modulator can be electrically conductive, partially transparent and partially reflective, and can include a stationary electrode for providing the electrostatic operation for the interferometric modulator device.

[0155] In a block **218**, a mechanical layer is formed over the optical stack. Forming the mechanical layer can include providing a sacrificial layer, depositing one or more layers over the sacrificial layer, and removing the sacrificial layer to release the mechanical layer.

[0156] The process **210** illustrated in Figure 14 continues at a block **220**, in which the mechanical layer is anchored over the optical stack at each corner of each pixel of the array. For example, a support post can be formed at corners of a pixel and can be used to anchor the mechanical layer over the optical stack at corners of the pixel and/or the mechanical layer can be self-supporting, as was described above.

[0157] In a block **222**, a via is provided in a pixel of the array. The via is disposed in the dielectric layer and electrically connects the stationary electrode to the black mask. The via is disposed along an edge of the pixel and is offset from the edge of the pixel in a direction towards the center of the pixel. In some implementations, the via is formed in a channel of the black mask that extends along the edge of the pixel from a corner of the pixel to another corner of the pixel, and a side of the channel includes a bulge surrounding a footprint of the via. By including the bulge on a side of the black mask channel surrounding the footprint of the via, the via can become more robust against process variations. For example, the bulge can reduce variation in topology in the area surrounding the via, thereby reducing manufacturing errors related to depositing conformal layers over the via. The bulge can be any suitable shape, including, for example, a portion of a circle, hexagon, octagon, rectangle or trapezoid. In some implementations, the bulge can be included on both sides of the channel. The method ends at a block **223**.

[0158] Figures 15A and 15B show examples of system block diagrams illustrating a display device **40** that includes a plurality of interferometric modulators. The display device **40** can be, for example, a cellular or mobile telephone. However, the same components of the display device **40** or slight variations thereof are also illustrative of various types of display devices such as televisions, e-readers and portable media players.

[0159] The display device **40** includes a housing **41**, a display **30**, an antenna **43**, a speaker **45**, an input device **48**, and a microphone **46**. The housing **41** can be formed from any of a variety of manufacturing processes, including injection molding, and vacuum

forming. In addition, the housing **41** may be made from any of a variety of materials, including, but not limited to: plastic, metal, glass, rubber, and ceramic, or a combination thereof. The housing **41** can include removable portions (not shown) that may be interchanged with other removable portions of different color, or containing different logos, pictures, or symbols.

[0160] The display **30** may be any of a variety of displays, including a bi-stable or analog display, as described herein. The display **30** also can be configured to include a flat-panel display, such as plasma, EL, OLED, STN LCD, or TFT LCD, or a non-flat-panel display, such as a CRT or other tube device. In addition, the display **30** can include an interferometric modulator display, as described herein.

[0161] The components of the display device **40** are schematically illustrated in Figure 15B. The display device **40** includes a housing **41** and can include additional components at least partially enclosed therein. For example, the display device **40** includes a network interface **27** that includes an antenna **43** which is coupled to a transceiver **47**. The transceiver **47** is connected to a processor **21**, which is connected to conditioning hardware **52**. The conditioning hardware **52** may be configured to condition a signal (e.g., filter a signal). The conditioning hardware **52** is connected to a speaker **45** and a microphone **46**. The processor **21** is also connected to an input device **48** and a driver controller **29**. The driver controller **29** is coupled to a frame buffer **28**, and to an array driver **22**, which in turn is coupled to a display array **30**. A power supply **50** can provide power to all components based on the particular display device **40** design.

[0162] The network interface **27** includes the antenna **43** and the transceiver **47** so that the display device **40** can communicate with one or more devices over a network. The network interface **27** also may have some processing capabilities to relieve, e.g., data processing requirements of the processor **21**. The antenna **43** can transmit and receive signals. In some implementations, the antenna **43** transmits and receives RF signals according to the IEEE 16.11 standard, including IEEE 16.11(a), (b), or (g), or the IEEE 802.11 standard, including IEEE 802.11a, b, g or n. In some other implementations, the antenna **43** transmits and receives RF signals according to the BLUETOOTH standard. In the case of a cellular telephone, the antenna **43** is designed to receive code division multiple

access (CDMA), frequency division multiple access (FDMA), time division multiple access (TDMA), Global System for Mobile communications (GSM), GSM/General Packet Radio Service (GPRS), Enhanced Data GSM Environment (EDGE), Terrestrial Trunked Radio (TETRA), Wideband-CDMA (W-CDMA), Evolution Data Optimized (EV-DO), 1xEV-DO, EV-DO Rev A, EV-DO Rev B, High Speed Packet Access (HSPA), High Speed Downlink Packet Access (HSDPA), High Speed Uplink Packet Access (HSUPA), Evolved High Speed Packet Access (HSPA+), Long Term Evolution (LTE), AMPS, or other known signals that are used to communicate within a wireless network, such as a system utilizing 3G or 4G technology. The transceiver **47** can pre-process the signals received from the antenna **43** so that they may be received by and further manipulated by the processor **21**. The transceiver **47** also can process signals received from the processor **21** so that they may be transmitted from the display device **40** via the antenna **43**.

[0163] In some implementations, the transceiver **47** can be replaced by a receiver. In addition, the network interface **27** can be replaced by an image source, which can store or generate image data to be sent to the processor **21**. The processor **21** can control the overall operation of the display device **40**. The processor **21** receives data, such as compressed image data from the network interface **27** or an image source, and processes the data into raw image data or into a format that is readily processed into raw image data. The processor **21** can send the processed data to the driver controller **29** or to the frame buffer **28** for storage. Raw data typically refers to the information that identifies the image characteristics at each location within an image. For example, such image characteristics can include color, saturation, and gray-scale level.

[0164] The processor **21** can include a microcontroller, CPU, or logic unit to control operation of the display device **40**. The conditioning hardware **52** may include amplifiers and filters for transmitting signals to the speaker **45**, and for receiving signals from the microphone **46**. The conditioning hardware **52** may be discrete components within the display device **40**, or may be incorporated within the processor **21** or other components.

[0165] The driver controller **29** can take the raw image data generated by the processor **21** either directly from the processor **21** or from the frame buffer **28** and can re-format the raw image data appropriately for high speed transmission to the array driver **22**. In

some implementations, the driver controller **29** can re-format the raw image data into a data flow having a raster-like format, such that it has a time order suitable for scanning across the display array **30**. Then the driver controller **29** sends the formatted information to the array driver **22**. Although a driver controller **29**, such as an LCD controller, is often associated with the system processor **21** as a stand-alone Integrated Circuit (IC), such controllers may be implemented in many ways. For example, controllers may be embedded in the processor **21** as hardware, embedded in the processor **21** as software, or fully integrated in hardware with the array driver **22**.

[0166] The array driver **22** can receive the formatted information from the driver controller **29** and can re-format the video data into a parallel set of waveforms that are applied many times per second to the hundreds, and sometimes thousands (or more), of leads coming from the display's x-y matrix of pixels.

[0167] In some implementations, the driver controller **29**, the array driver **22**, and the display array **30** are appropriate for any of the types of displays described herein. For example, the driver controller **29** can be a conventional display controller or a bi-stable display controller (e.g., an IMOD controller). Additionally, the array driver **22** can be a conventional driver or a bi-stable display driver (e.g., an IMOD display driver). Moreover, the display array **30** can be a conventional display array or a bi-stable display array (e.g., a display including an array of IMODs). In some implementations, the driver controller **29** can be integrated with the array driver **22**. Such an implementation is common in highly integrated systems such as cellular phones, watches and other small-area displays.

[0168] In some implementations, the input device **48** can be configured to allow, e.g., a user to control the operation of the display device **40**. The input device **48** can include a keypad, such as a QWERTY keyboard or a telephone keypad, a button, a switch, a rocker, a touch-sensitive screen, or a pressure- or heat-sensitive membrane. The microphone **46** can be configured as an input device for the display device **40**. In some implementations, voice commands through the microphone **46** can be used for controlling operations of the display device **40**.

[0169] The power supply **50** can include a variety of energy storage devices as are well known in the art. For example, the power supply **50** can be a rechargeable battery, such

as a nickel-cadmium battery or a lithium-ion battery. The power supply **50** also can be a renewable energy source, a capacitor, or a solar cell, including a plastic solar cell or solar-cell paint. The power supply **50** also can be configured to receive power from a wall outlet.

[0170] In some implementations, control programmability resides in the driver controller **29** which can be located in several places in the electronic display system. In some other implementations, control programmability resides in the array driver **22**. The above-described optimization may be implemented in any number of hardware and/or software components and in various configurations.

[0171] The various illustrative logics, logical blocks, modules, circuits and algorithm steps described in connection with the implementations disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. The interchangeability of hardware and software has been described generally, in terms of functionality, and illustrated in the various illustrative components, blocks, modules, circuits and steps described above. Whether such functionality is implemented in hardware or software depends upon the particular application and design constraints imposed on the overall system.

[0172] The hardware and data processing apparatus used to implement the various illustrative logics, logical blocks, modules and circuits described in connection with the aspects disclosed herein may be implemented or performed with a general purpose single- or multi-chip processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor, or, any conventional processor, controller, microcontroller, or state machine. A processor also may be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. In some implementations, particular steps and methods may be performed by circuitry that is specific to a given function.

[0173] In one or more aspects, the functions described may be implemented in hardware, digital electronic circuitry, computer software, firmware, including the structures disclosed in this specification and their structural equivalents thereof, or in any combination thereof. Implementations of the subject matter described in this specification also can be implemented as one or more computer programs, i.e., one or more modules of computer program instructions, encoded on a computer storage media for execution by, or to control the operation of, data processing apparatus.

[0174] Various modifications to the implementations described in this disclosure may be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other implementations without departing from the spirit or scope of this disclosure. Thus, the claims are not intended to be limited to the implementations shown herein, but are to be accorded the widest scope consistent with this disclosure, the principles and the novel features disclosed herein. The word “exemplary” is used exclusively herein to mean “serving as an example, instance, or illustration.” Any implementation described herein as “exemplary” or provided as examples is not necessarily to be construed as preferred or advantageous over other implementations. Additionally, a person having ordinary skill in the art will readily appreciate, the terms “upper” and “lower” are sometimes used for ease of describing the figures, and indicate relative positions corresponding to the orientation of the figure on a properly oriented page, and may not reflect the proper orientation of the IMOD as implemented.

[0175] Certain features that are described in this specification in the context of separate implementations also can be implemented in combination in a single implementation. Conversely, various features that are described in the context of a single implementation also can be implemented in multiple implementations separately or in any suitable subcombination. Moreover, although features may be described above as acting in certain combinations and even initially claimed as such, one or more features from a claimed combination can in some cases be excised from the combination, and the claimed combination may be directed to a subcombination or variation of a subcombination.

[0176] Similarly, while operations are depicted in the drawings in a particular order, this should not be understood as requiring that such operations be performed in the

particular order shown or in sequential order, or that all illustrated operations be performed, to achieve desirable results. Further, the drawings may schematically depict one more example processes in the form of a flow diagram. However, other operations that are not depicted can be incorporated in the example processes that are schematically illustrated. For example, one or more additional operations can be performed before, after, simultaneously, or between any of the illustrated operations. In certain circumstances, multitasking and parallel processing may be advantageous. Moreover, the separation of various system components in the implementations described above should not be understood as requiring such separation in all implementations, and it should be understood that the described program components and systems can generally be integrated together in a single software product or packaged into multiple software products. Additionally, other implementations are within the scope of the following claims. In some cases, the actions recited in the claims can be performed in a different order and still achieve desirable results.

CLAIMS

What is claimed is:

1. A device comprising:
 - an array of pixels, each pixel having
 - a substrate;
 - an electrically conductive black mask disposed on the substrate and masking an optically non-active portion of the pixel at each of four corners of the pixel and along at least one edge region of the pixel;
 - a dielectric layer disposed over the black mask;
 - an optical stack disposed over the dielectric layer, the optical stack including a stationary electrode; and
 - a mechanical layer positioned over the optical stack and defining a cavity between the mechanical layer and the optical stack, the mechanical layer movable through the cavity between an actuated position and a relaxed position, the mechanical layer anchored over the optical stack at each corner of the pixel,
 - wherein the array of pixels includes a first pixel having a conductive via in the dielectric layer electrically connecting the stationary electrode to the black mask, the conductive via disposed in a position along an edge of the first pixel in an optically non-active area of the first pixel, and wherein the position of the conductive via is spaced offset from the edge of the first pixel in a direction towards the center of the first pixel.
2. The device of claim 1, wherein the array of pixels further includes a second pixel adjacent the first pixel along the edge of the first pixel, wherein the second pixel does not include a via in the dielectric layer for electrically connecting the stationary electrode to the black mask.
3. The device of claim 2, wherein a height of the cavity of the first pixel is greater than a height of the cavity of the second pixel.

4. The device of claim 3, wherein the first pixel is a high gap pixel and the second pixel is a mid gap pixel, and wherein the array of pixels further includes a low gap pixel adjacent the high gap pixel on a side of the high gap pixel opposite the mid gap pixel, and wherein the low gap pixel does not include a via in the dielectric layer for electrically connecting the stationary electrode to the black mask.

5. The device of claim 3, wherein the black mask includes a channel extending from a corner of the pixel to the via along the edge of the first pixel.

6. The device of claim 5, wherein the channel includes a bulge surrounding a footprint of the via.

7. The device of claim 6, wherein a portion of the channel of the black mask including the bulge has a width from an edge of the bulge to the edge of the pixel ranging between about 3 μm to about 4.5 μm .

8. The device of claim 7, wherein a portion of the first channel of the black mask not including the bulge has a width from an edge of the channel of the black mask to the edge of the pixel ranging between about 2 μm to about 3 μm .

9. The device of claim 3, wherein a distance from a center of the via to the edge of the first pixel ranges between about 1 μm to about 3 μm .

10. The device of claim 8, wherein the black mask includes at least one of an optical absorber layer, a dielectric layer, and a conductive bussing layer.

11. The device of claim 10, wherein the via is an opening in the dielectric layer for electrically connecting the conductive bussing layer of the black mask to the stationary electrode of the optical stack.

12. The device of claim 11, further comprising a bias circuit configured to apply a bias voltage, wherein when the bias voltage is applied at least a portion of the mechanical layer is substantially parallel to the substrate.

13. The device of claim 1, further comprising:
a display;
a processor that is configured to communicate with the display, the processor being configured to process image data; and
a memory device that is configured to communicate with the processor.

14. The device of claim 13, further comprising:
a driver circuit configured to send at least one signal to the display; and
a controller configured to send at least a portion of the image data to the driver circuit.

15. The device of claim 14, further comprising an image source module configured to send the image data to the processor.

16. A method of forming a display device having a plurality of pixels, comprising:
depositing an electrically conductive black mask on a substrate, the black mask masking an optically non-active portion of the pixel at each of four corners of each pixel and along at least one edge region of each pixel;
depositing a dielectric layer over the black mask;
depositing an optical stack over the dielectric layer, the optical stack including a stationary electrode;
depositing the mechanical layer over the optical stack, the mechanical layer defining a cavity between the mechanical layer and the optical stack;
anchoring the mechanical layer over the optical stack at each corner of each pixel; and

providing a conductive via in a first pixel of the device, the via disposed in the dielectric layer and electrically connecting the stationary electrode to the black mask, the via disposed in a position along an edge of the first pixel in an optically non-active area of the first pixel, and wherein the position of the conductive via is spaced offset from the edge of the first pixel in a direction towards the center of the first pixel.

17. The method of claim 16, further comprising depositing a sacrificial layer before depositing the mechanical layer and removing the sacrificial layer after depositing the mechanical layer to form the cavity, wherein the sacrificial layer has a thickness selected to define a height of the cavity.

18. The method of claim 17, further comprising forming an anchor hole in the sacrificial layer at each corner of the first pixel, each anchor hole defining where the mechanical layer is anchored over the optical stack at each corner of the first pixel.

19. The method of claim 18, further comprising forming a support post in each anchor hole for supporting the mechanical layer.

20. The method of claim 16, wherein depositing the black mask further includes depositing a channel of the black mask extending from a corner of the pixel to the via along the edge of the first pixel.

21. The method of claim 20, wherein depositing the black mask further includes forming a bulge in the channel surrounding a footprint of the via.

22. The method of claim 16, wherein the first pixel is a high gap pixel, and wherein the plurality of pixels further includes a mid gap pixel adjacent the first pixel along the edge of the first pixel, and wherein the plurality of pixels further includes a low gap pixel adjacent the first pixel opposite the mid gap pixel, wherein the mid gap and low gap pixels do not include a via in the dielectric layer for electrically connecting the stationary electrode to the black mask.

23. The method of claim 16, further comprising forming a reflective layer on a surface of the mechanical layer facing the cavity, the reflective layer and the optical stack forming an interferometric cavity.

24. The method of claim 23, further comprising applying a bias voltage to the optical stack so that at least a portion of the mechanical layer is substantially parallel to the substrate.

25. An electromechanical device comprising:

a plurality of pixels, each pixel including

a substrate;

means for absorbing light disposed on the substrate and masking an optically non-active portion of the pixel at each of four corners of the pixel and along at least one edge region of the pixel;

a dielectric layer disposed over the light absorbing means;

an optical stack disposed over the dielectric layer, the optical stack including a stationary electrode; and

a mechanical layer positioned over the optical stack to define a cavity between the mechanical layer and the optical stack, the mechanical layer movable through the cavity between an actuated position and a relaxed position, the mechanical layer anchored over the optical stack at each corner of the pixel,

wherein the array of pixels includes a first pixel having in the dielectric layer a means for electrically connecting the stationary electrode to the light absorbing means, the connecting means disposed in a position along an edge of the first pixel in an optically non-active area of the first pixel, and wherein the position of the connecting means is spaced offset from the edge of the first pixel in a direction towards the center of the first pixel.

26. The electromechanical device of claim 25, wherein the light absorbing means includes a channel extending from a corner of the pixel to the connecting means along the edge of the first pixel.

27. The electromechanical device of claim 26, wherein the channel includes a bulge surrounding a footprint of the connecting means.

28. The electromechanical device of claim 25, wherein the first pixel is a high gap pixel, and wherein the plurality of pixels further includes a mid gap pixel adjacent the first pixel along the edge of the first pixel, and wherein the plurality of pixels further includes a low gap pixel adjacent the first pixel opposite the mid gap pixel, wherein the mid gap and low gap pixels do not include a means in the dielectric layer for electrically connecting the stationary electrode to the black mask.

1/29

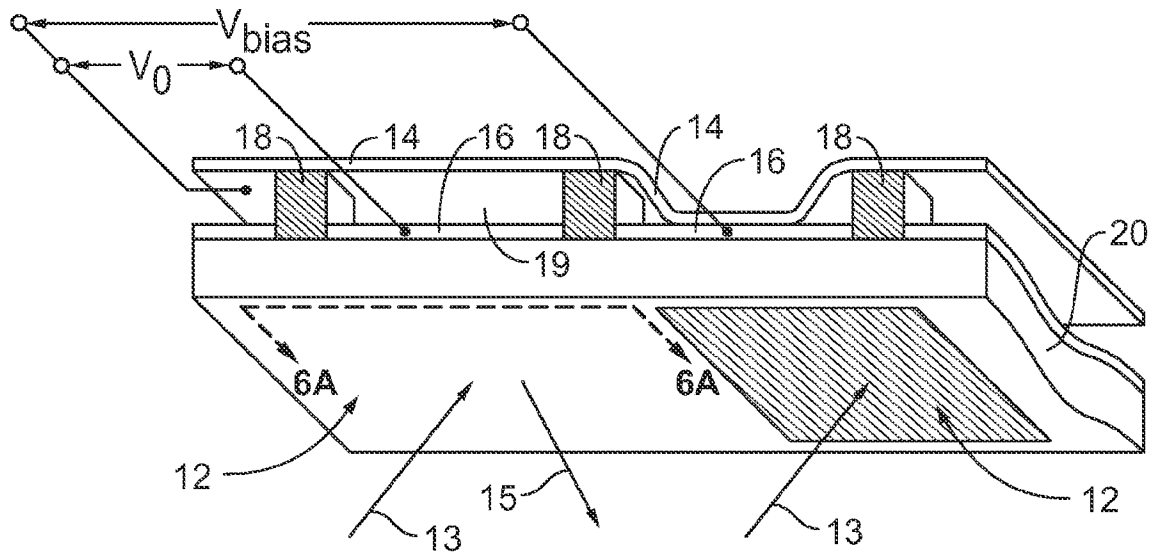


Figure 1

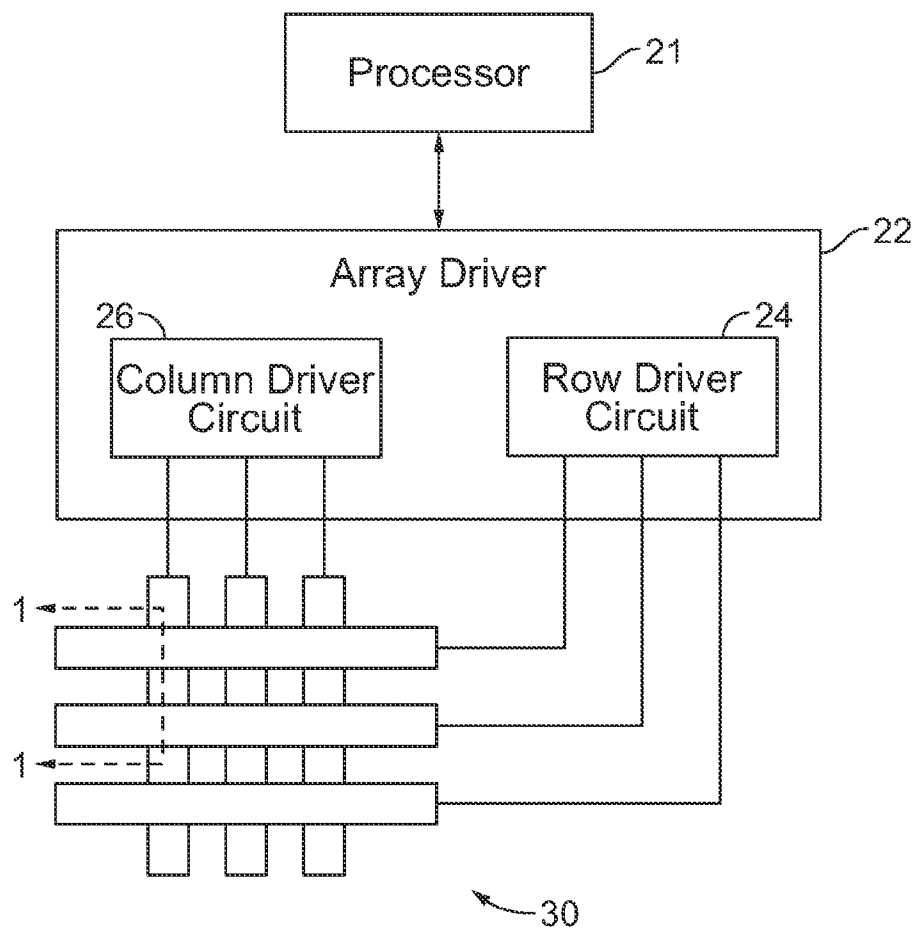


Figure 2

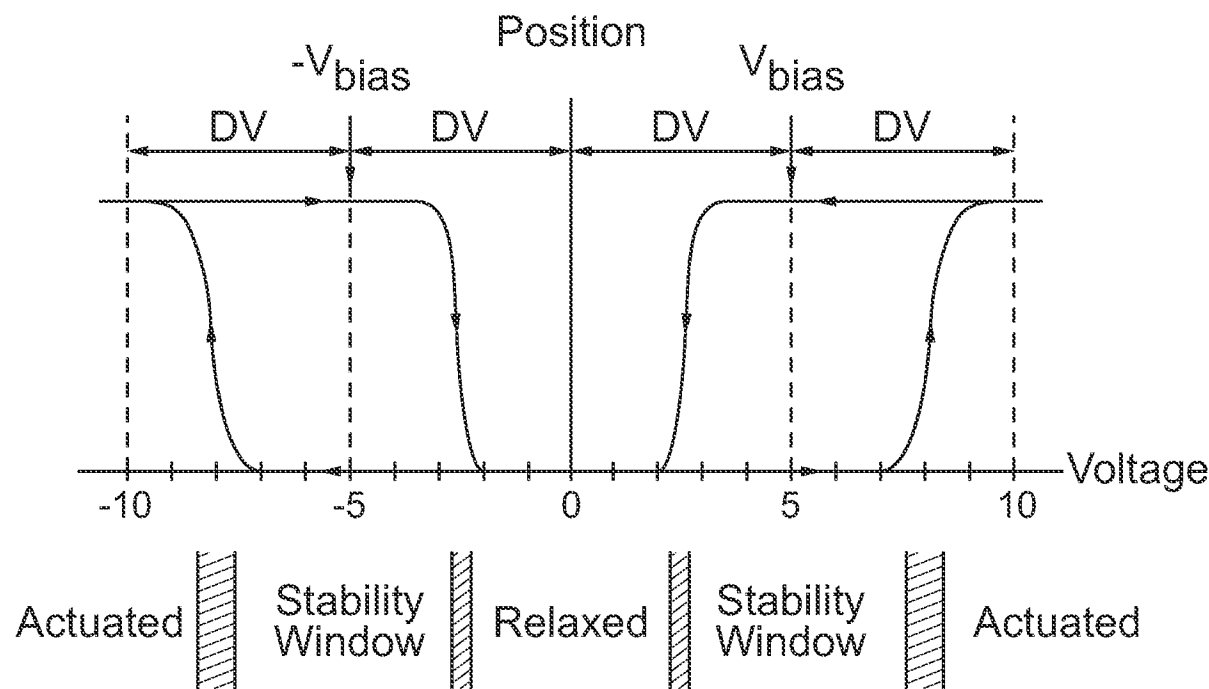


Figure 3

Common Voltages						
Segment Voltages		V_{CADD_H}	V_{CHOLD_H}	V_{CREL}	V_{CHOLD_L}	V_{CADD_L}
	V_{S_H}	Stable	Stable	Relax	Stable	Actuate
	V_{S_L}	Actuate	Stable	Relax	Stable	Stable

Figure 4

3/29

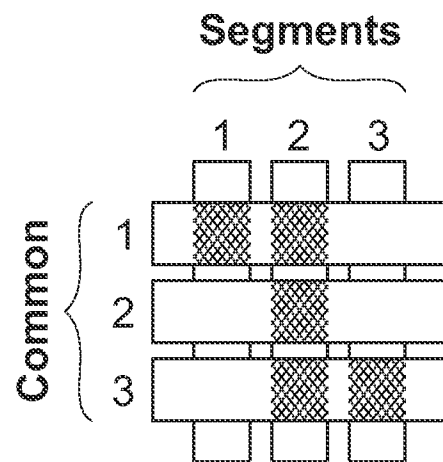


Figure 5A

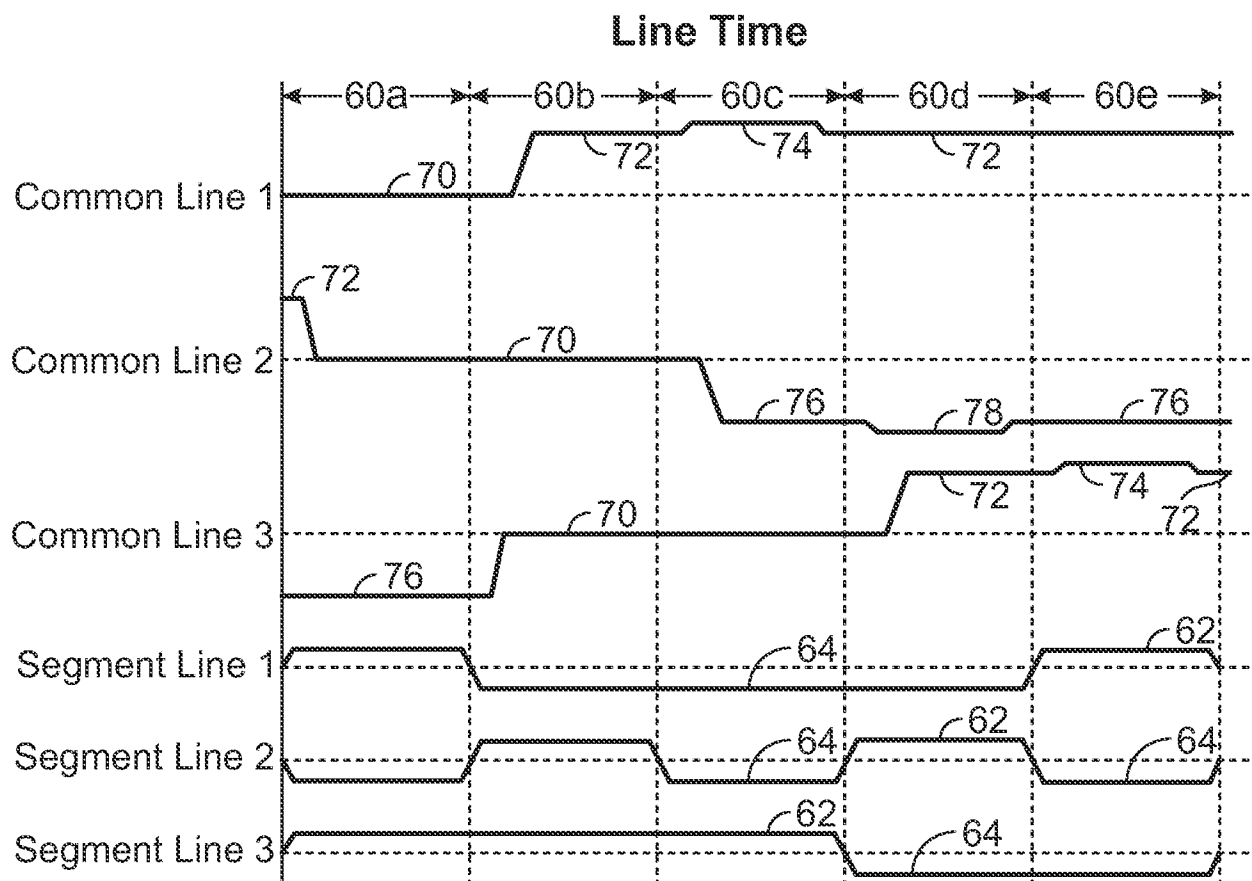


Figure 5B

4/29

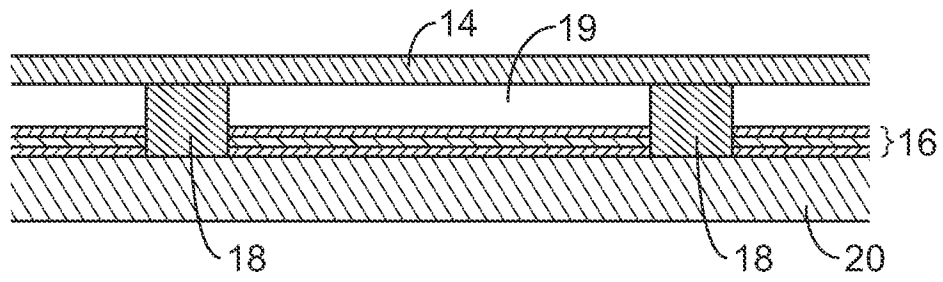


Figure 6A

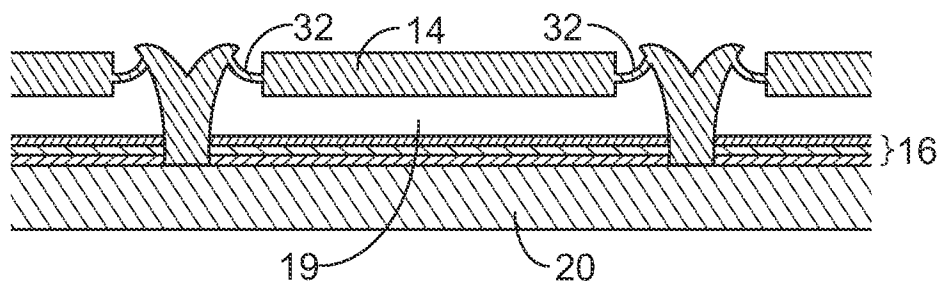


Figure 6B

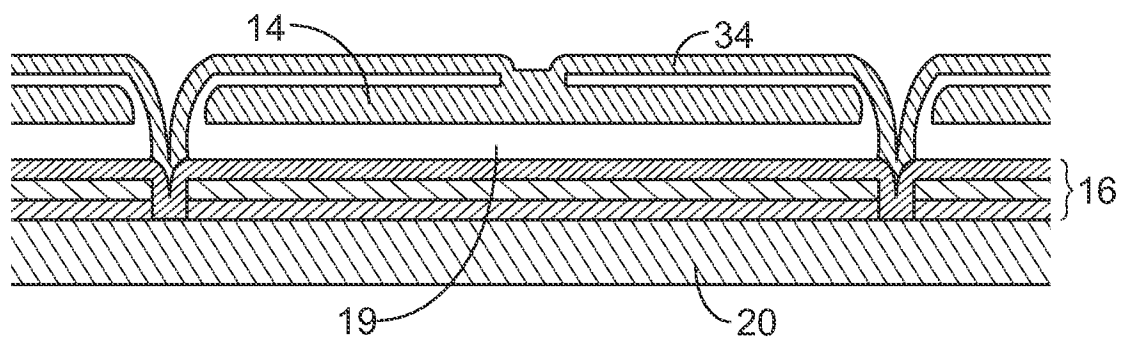


Figure 6C

5/29

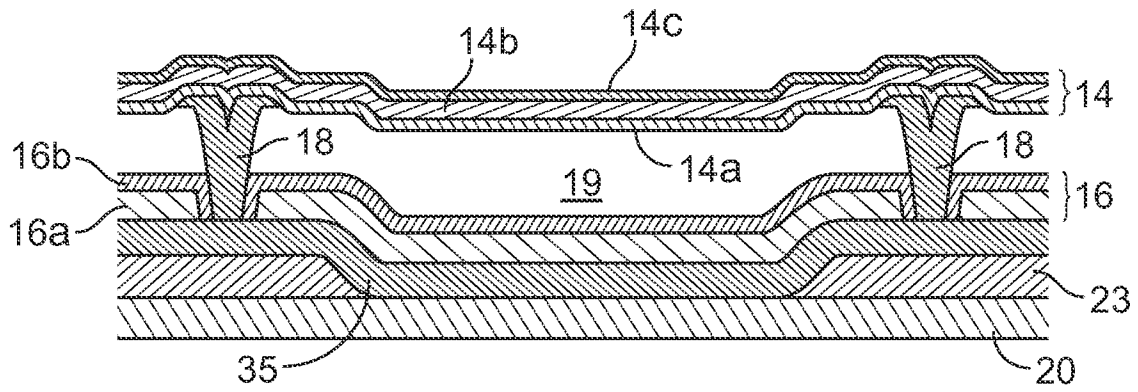


Figure 6D

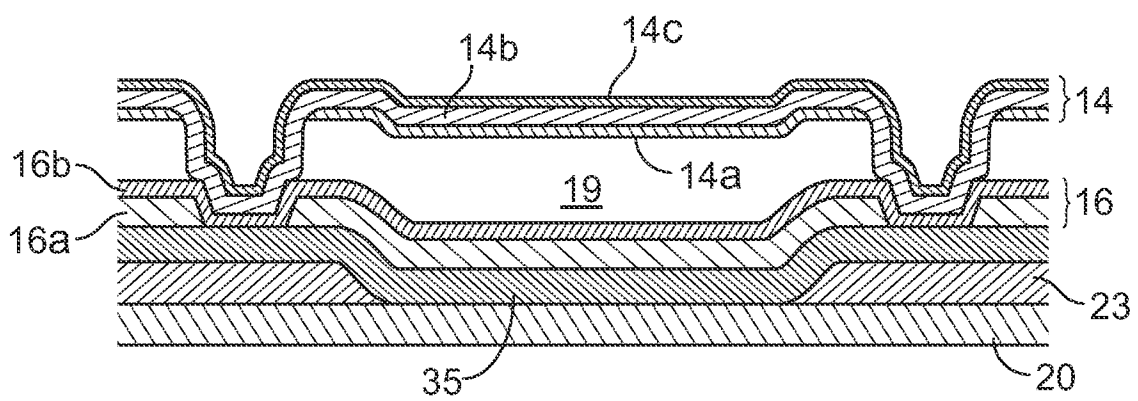


Figure 6E

6/29

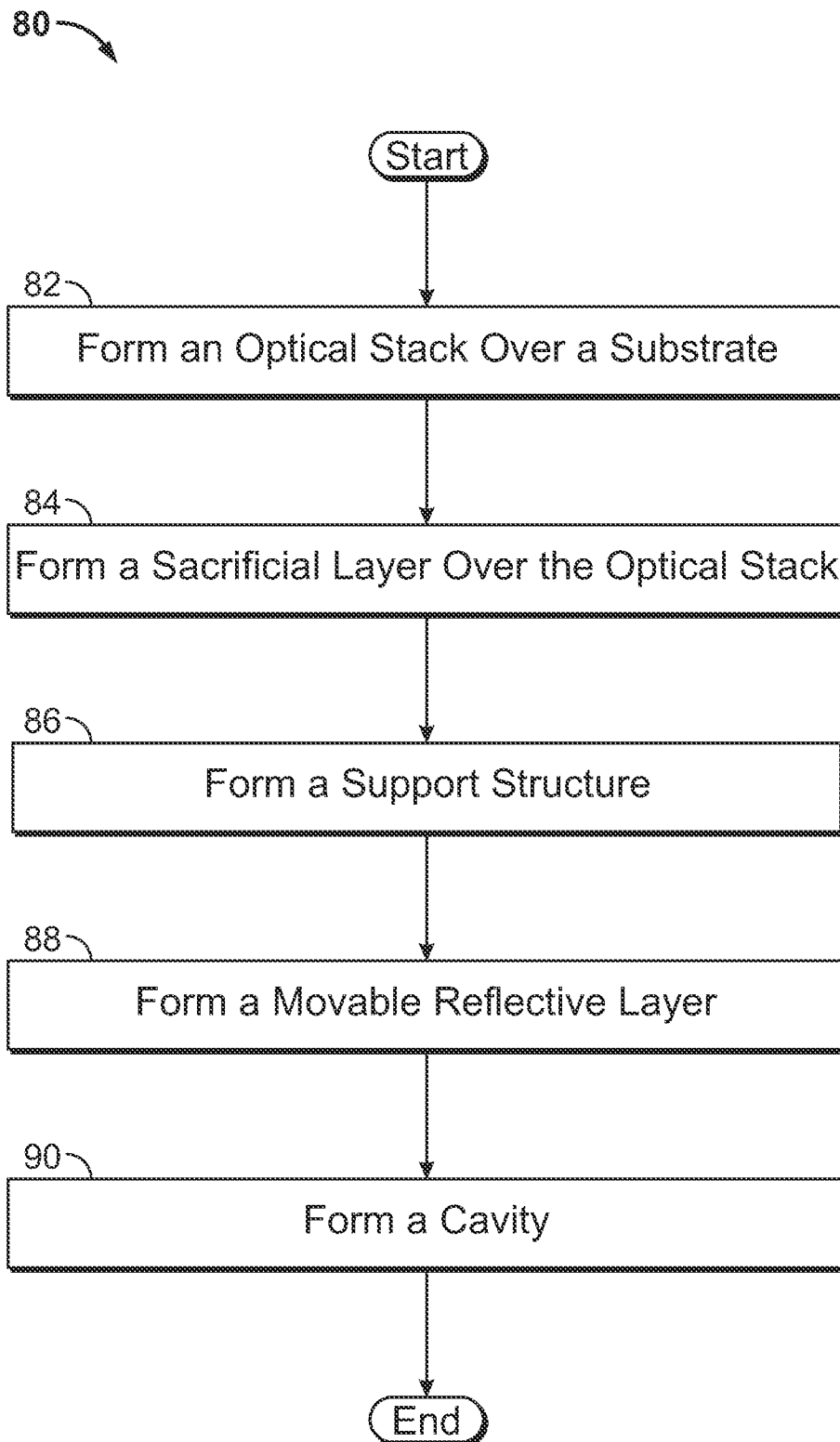


Figure 7

7/29

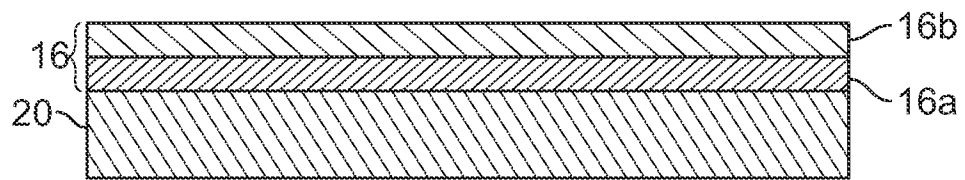


Figure 8A

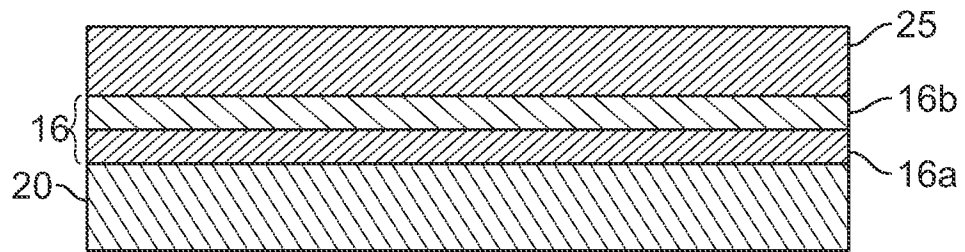


Figure 8B

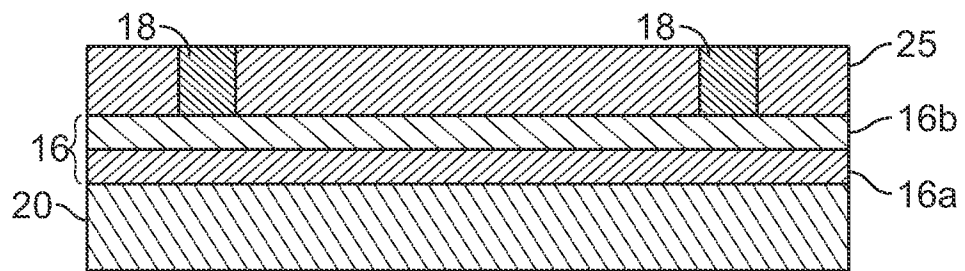


Figure 8C

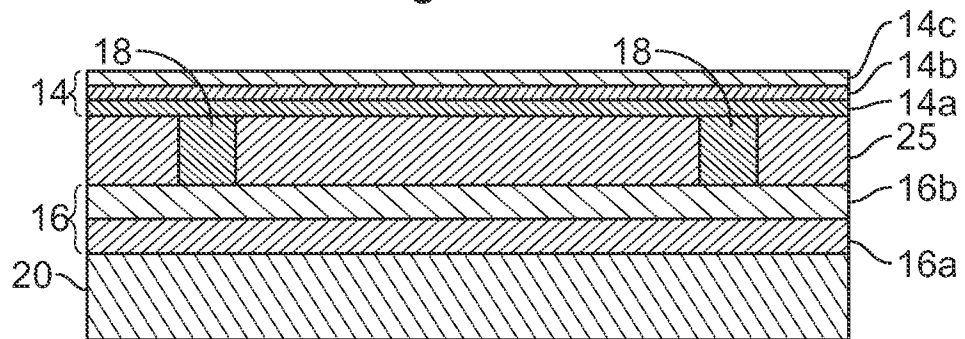


Figure 8D

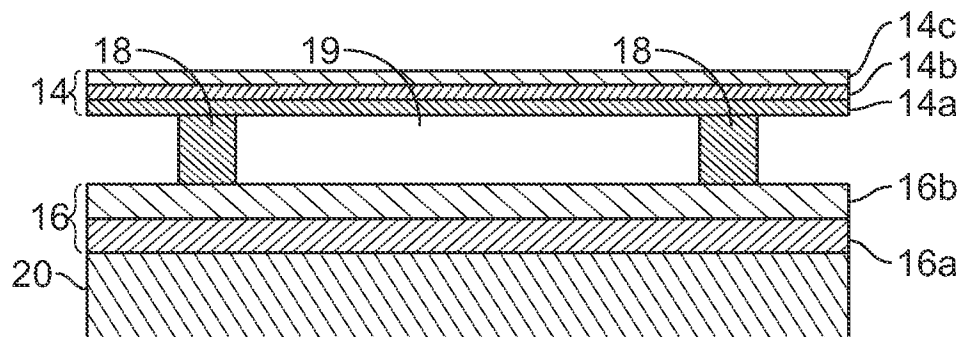


Figure 8E

8/29

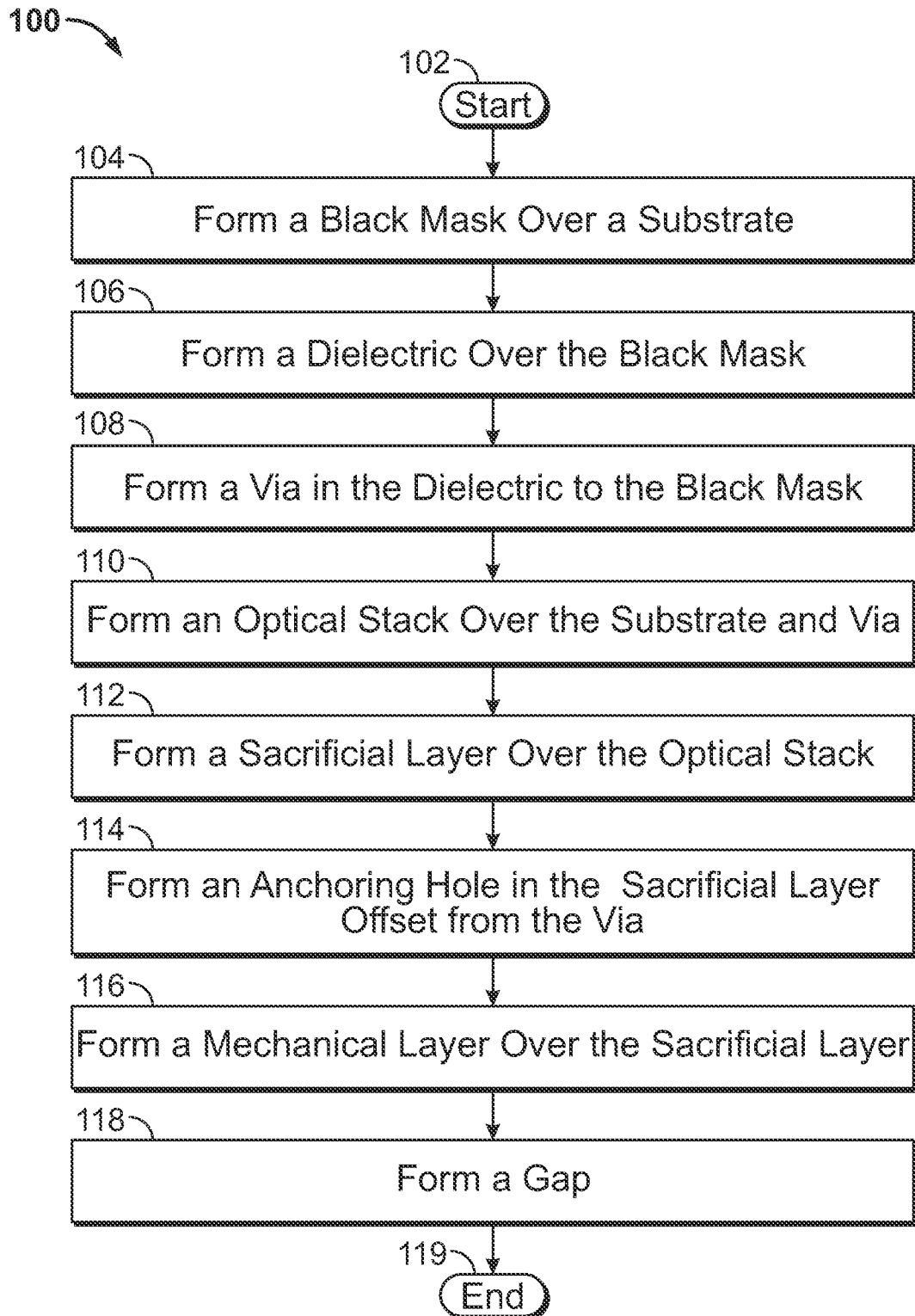


Figure 9

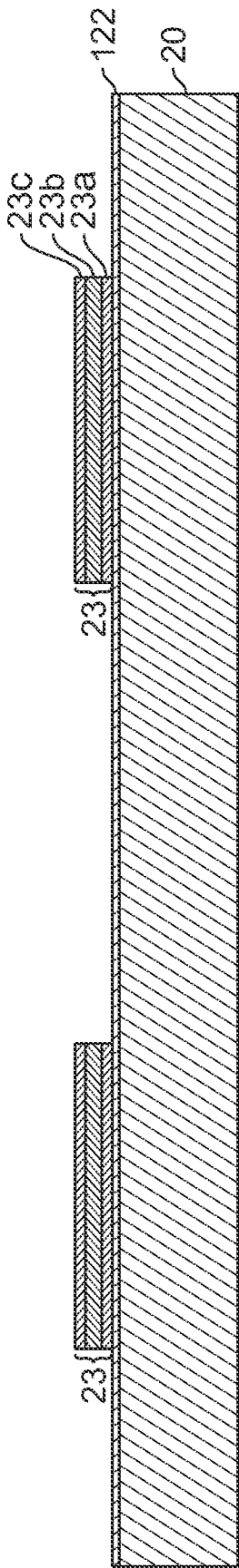


Figure 10A

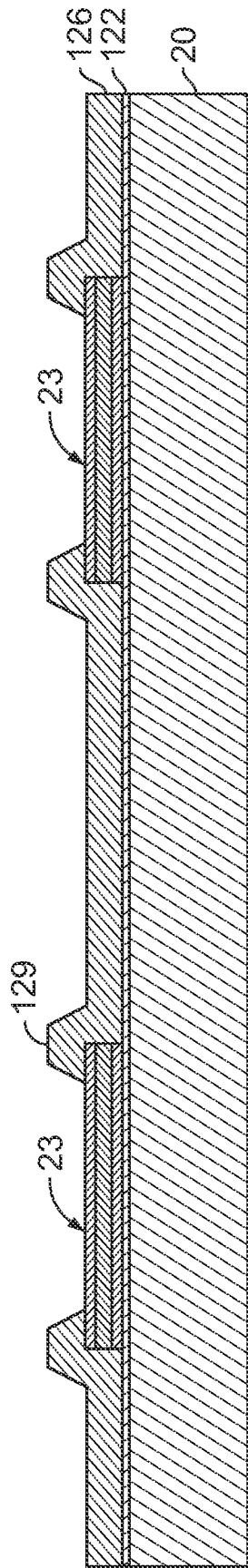


Figure 10B

10/29

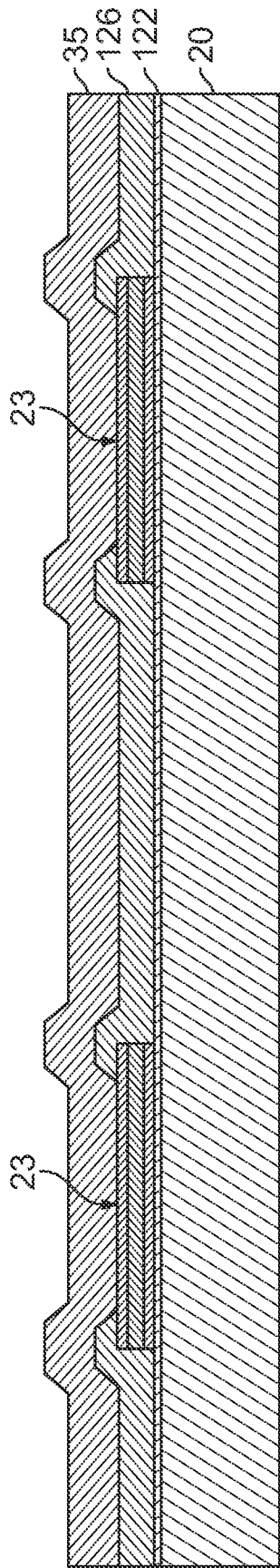


Figure 10C

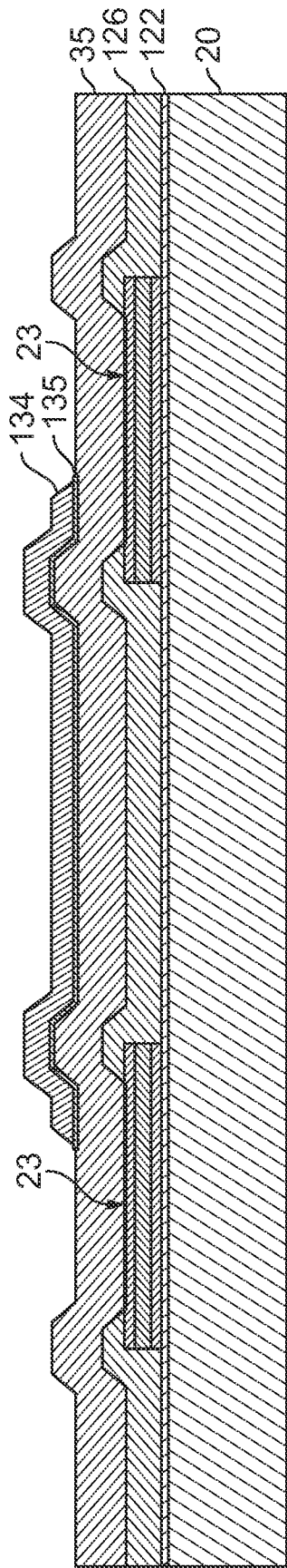


Figure 10D

11/29

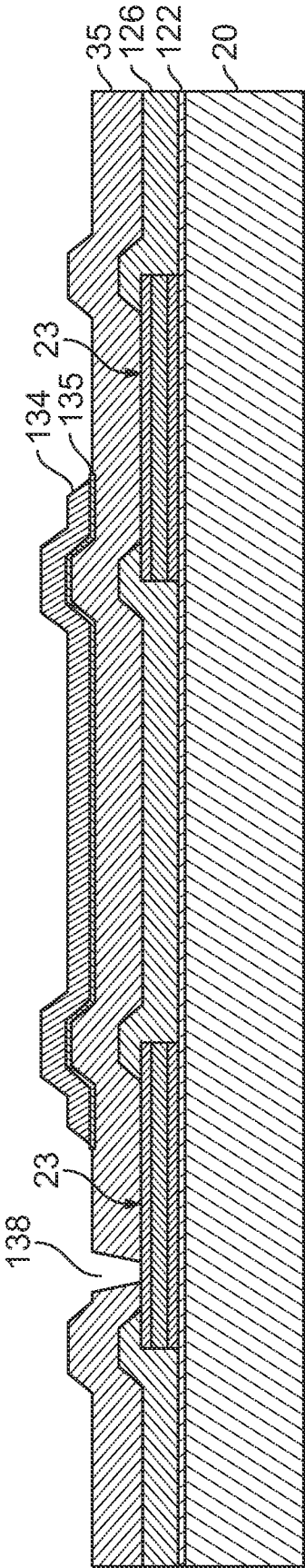


Figure 10E

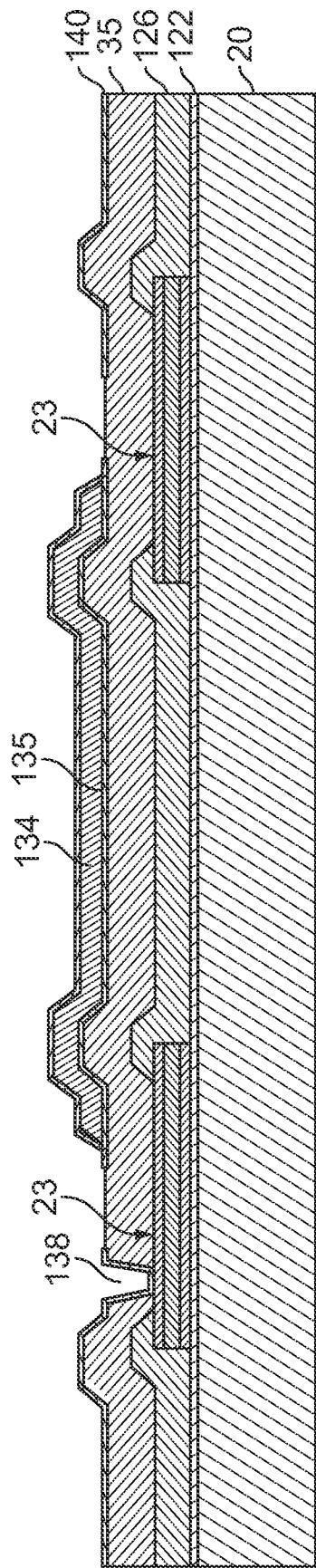


Figure 10F

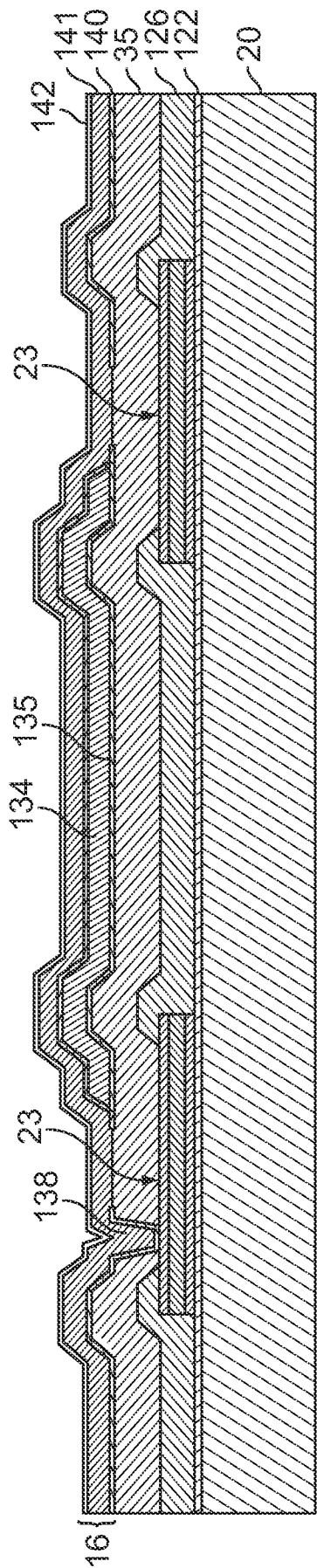


Figure 10G

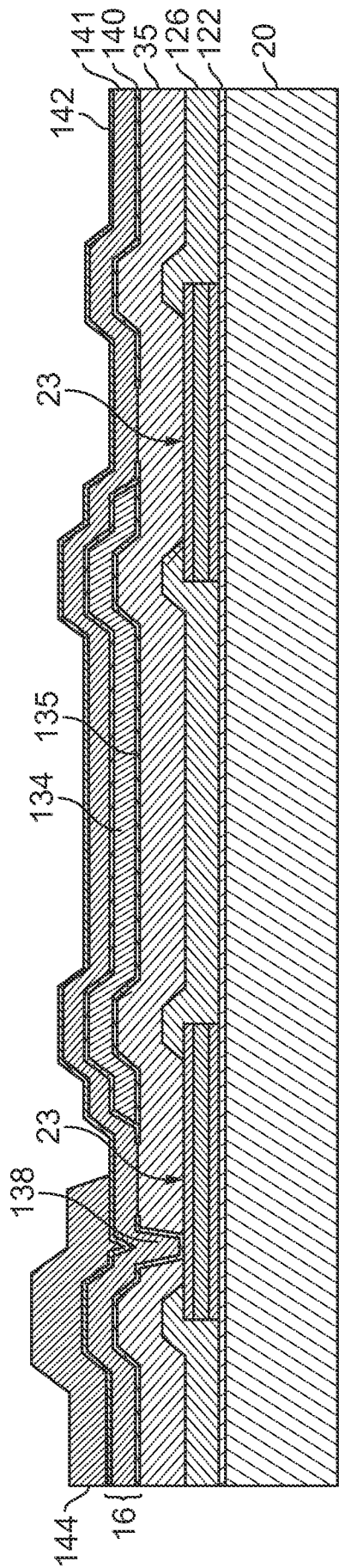


Figure 10H

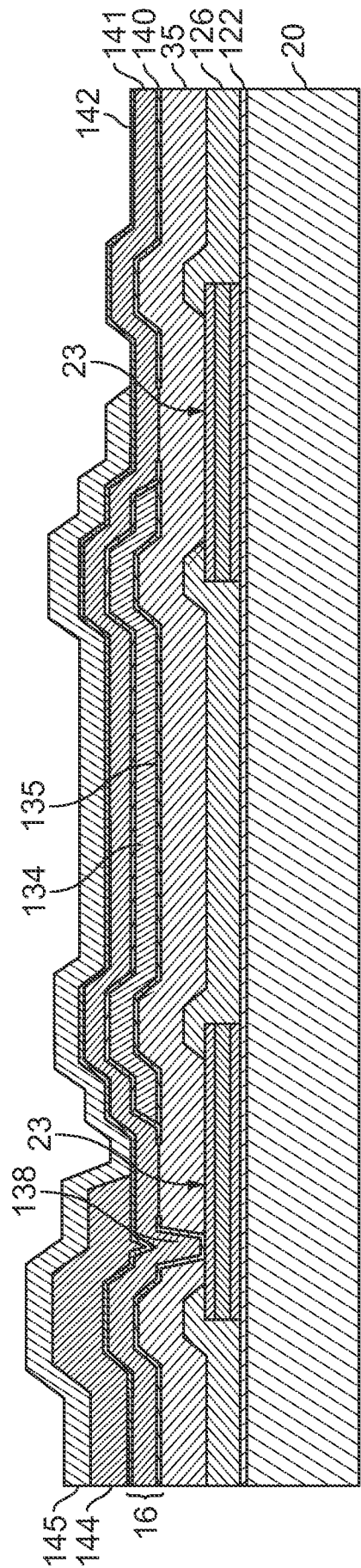


Figure 10I

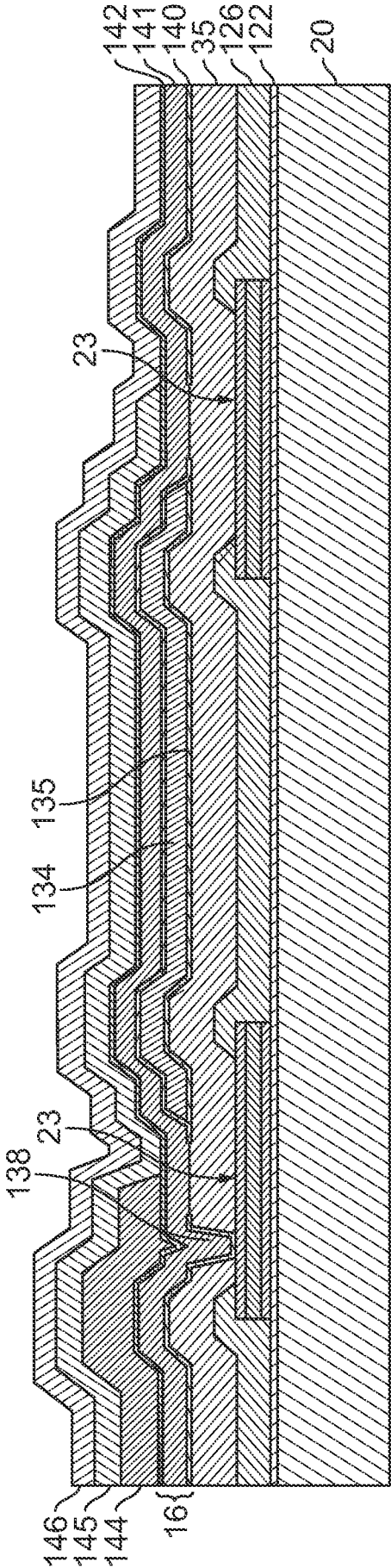


Figure 10J

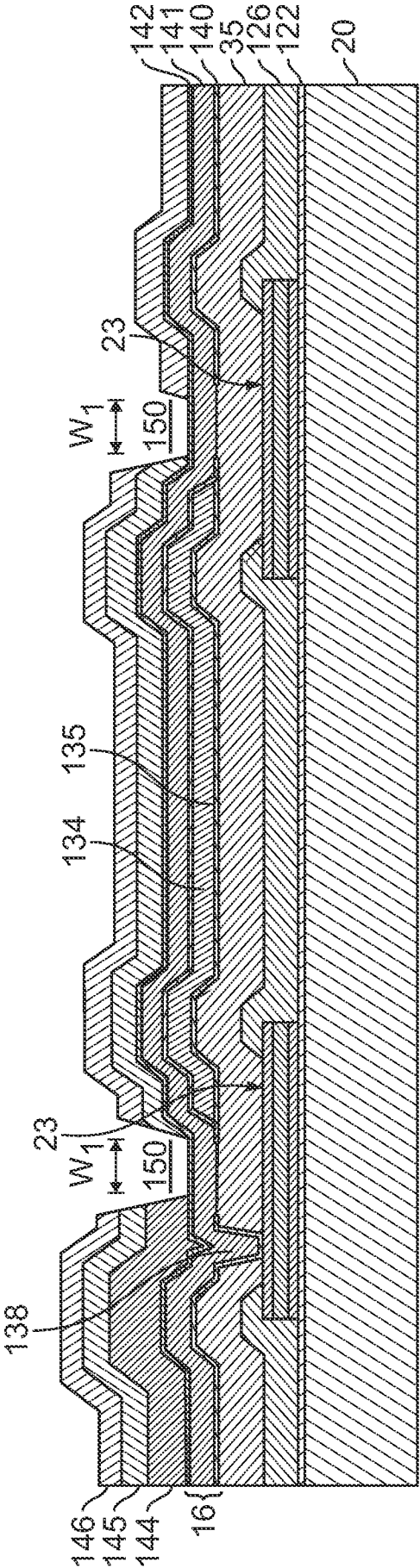


Figure 10K

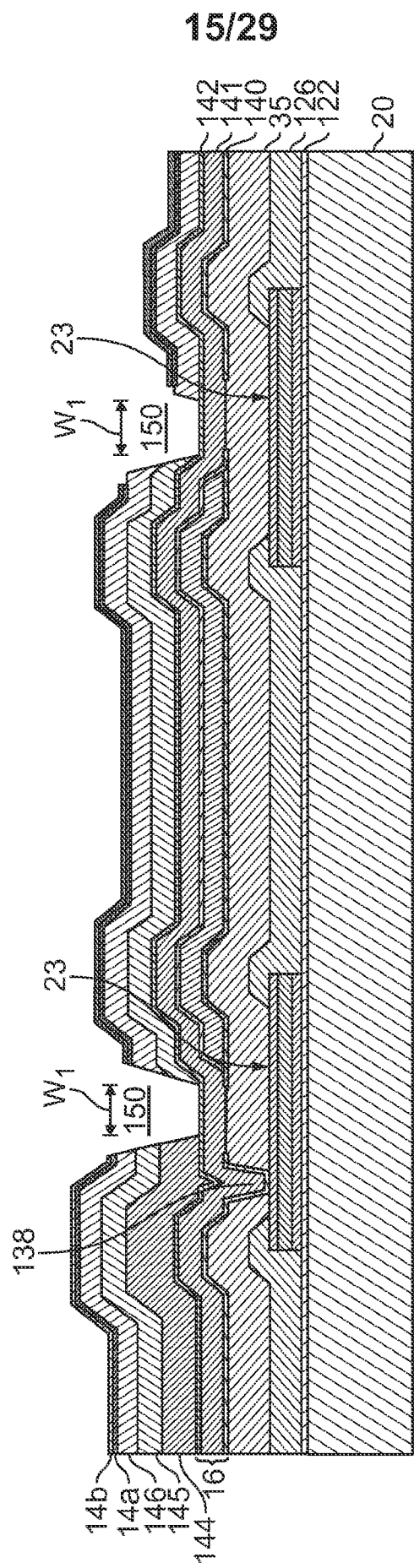


Figure 10L

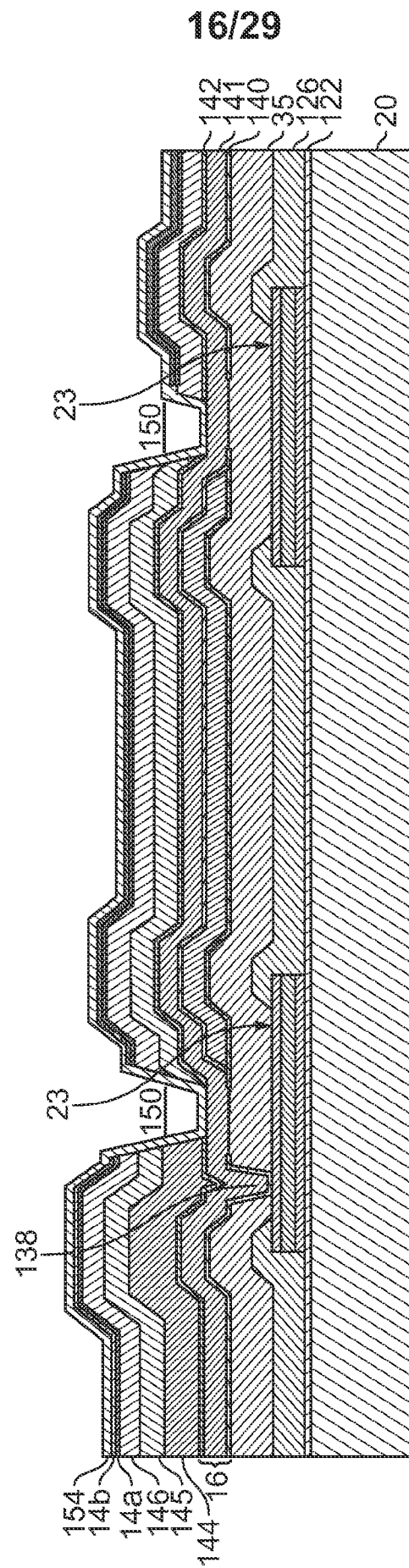


Figure 105

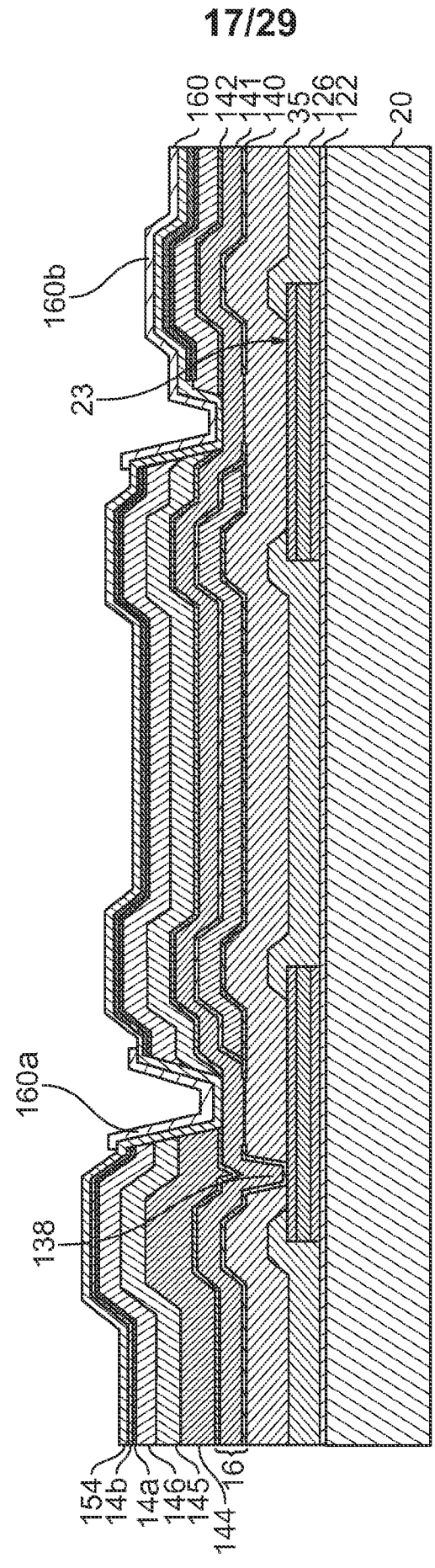


Figure 10N

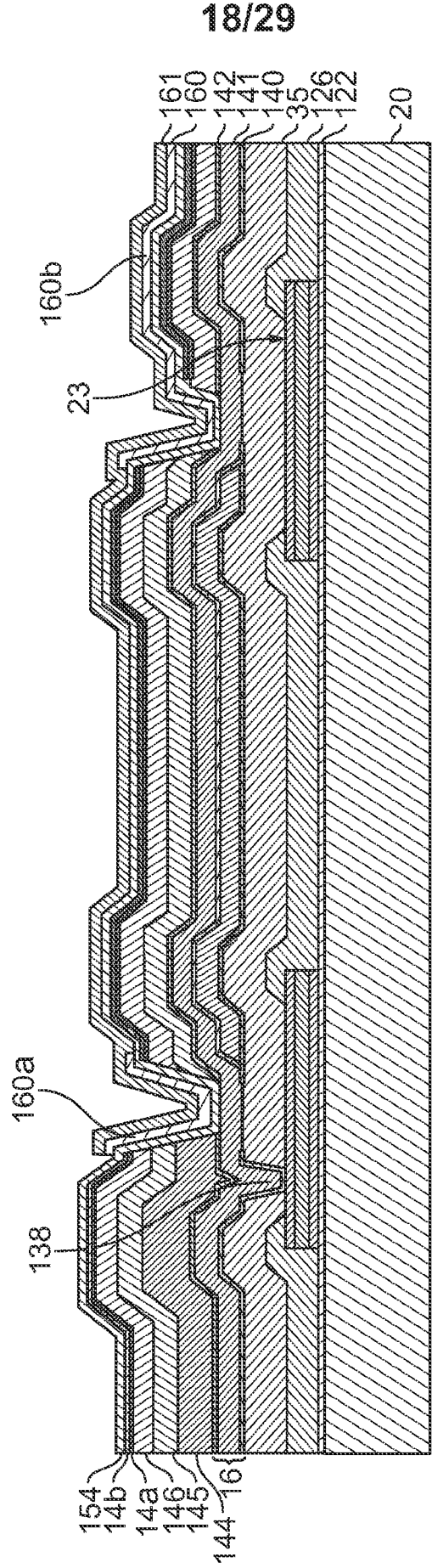


Figure 100

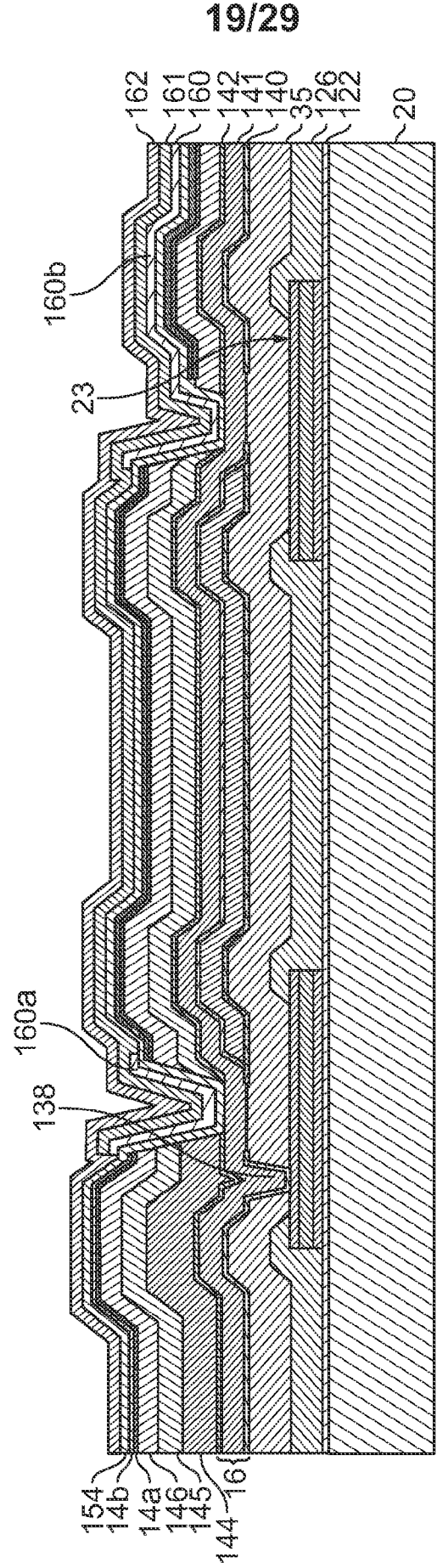
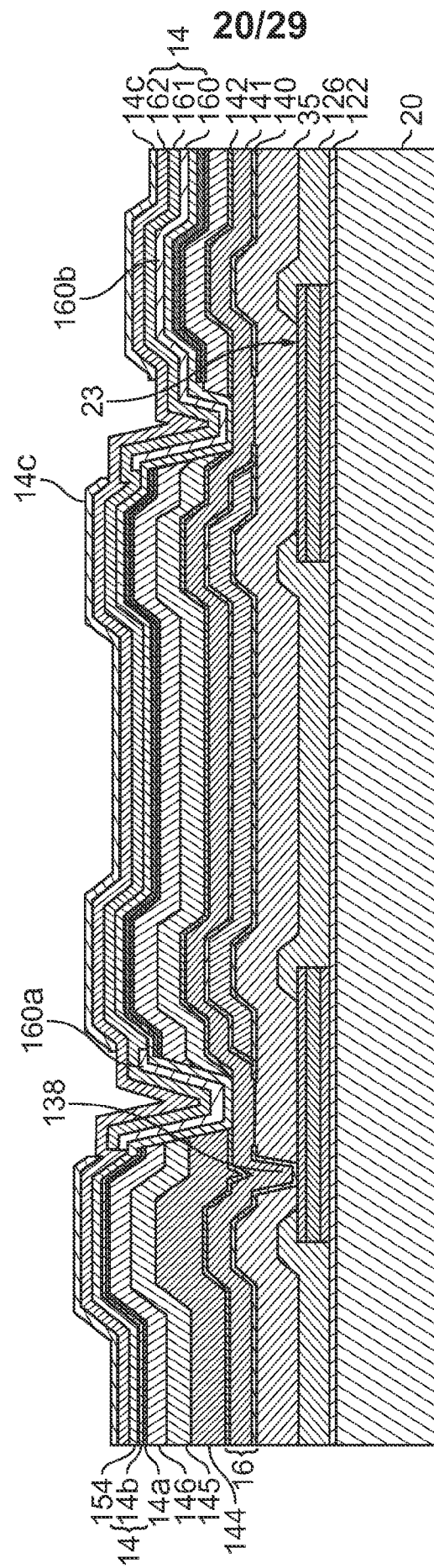


Figure 10P



7. June 1909

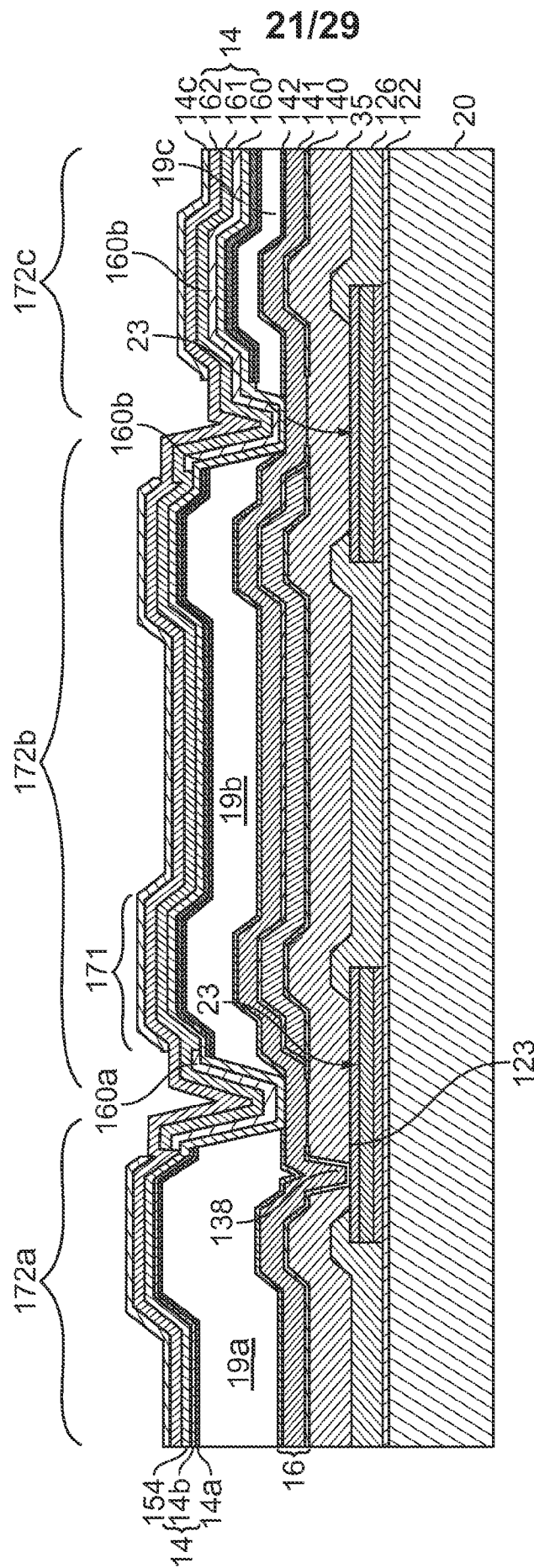


Figure 10R

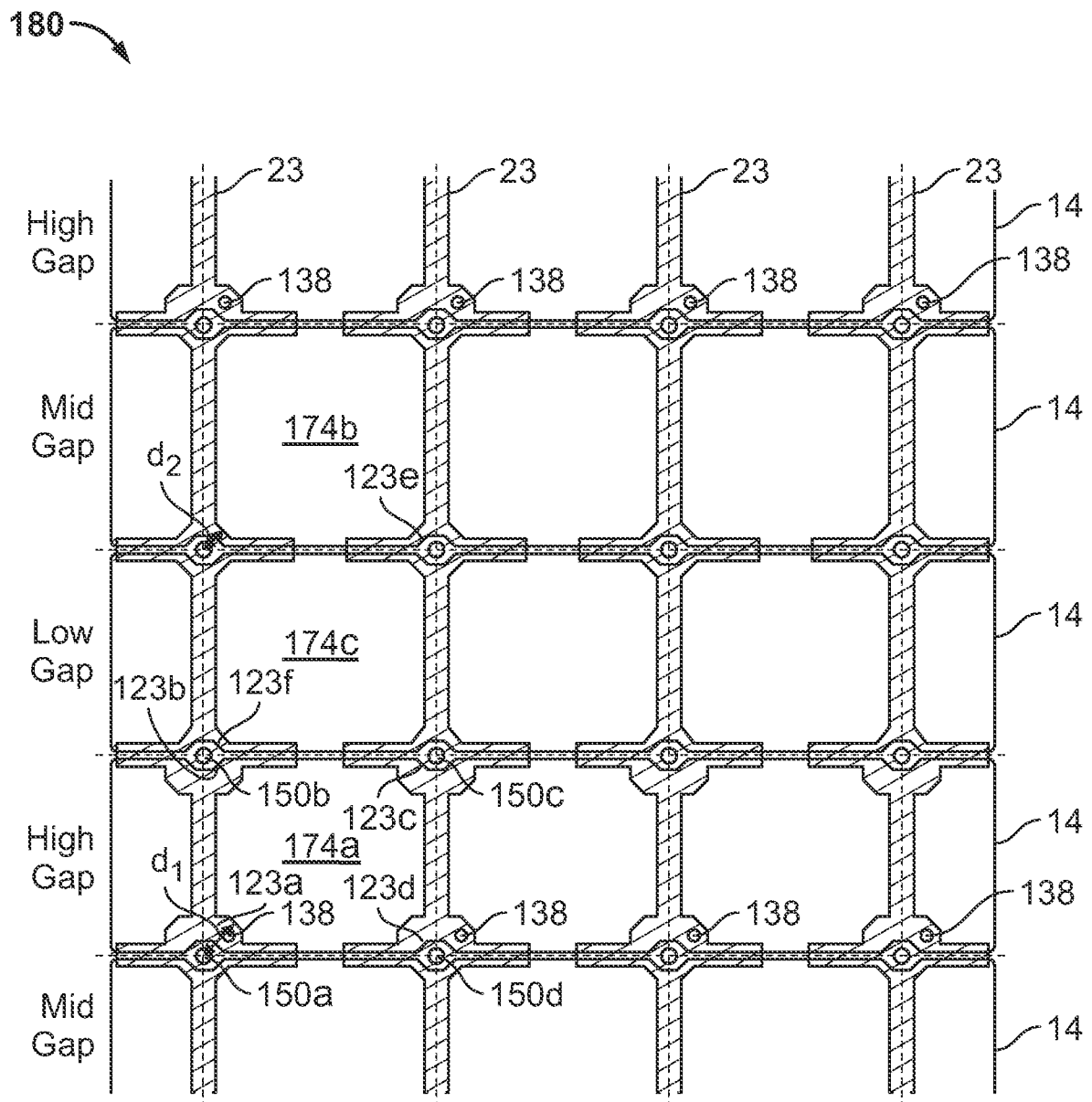


Figure 11A

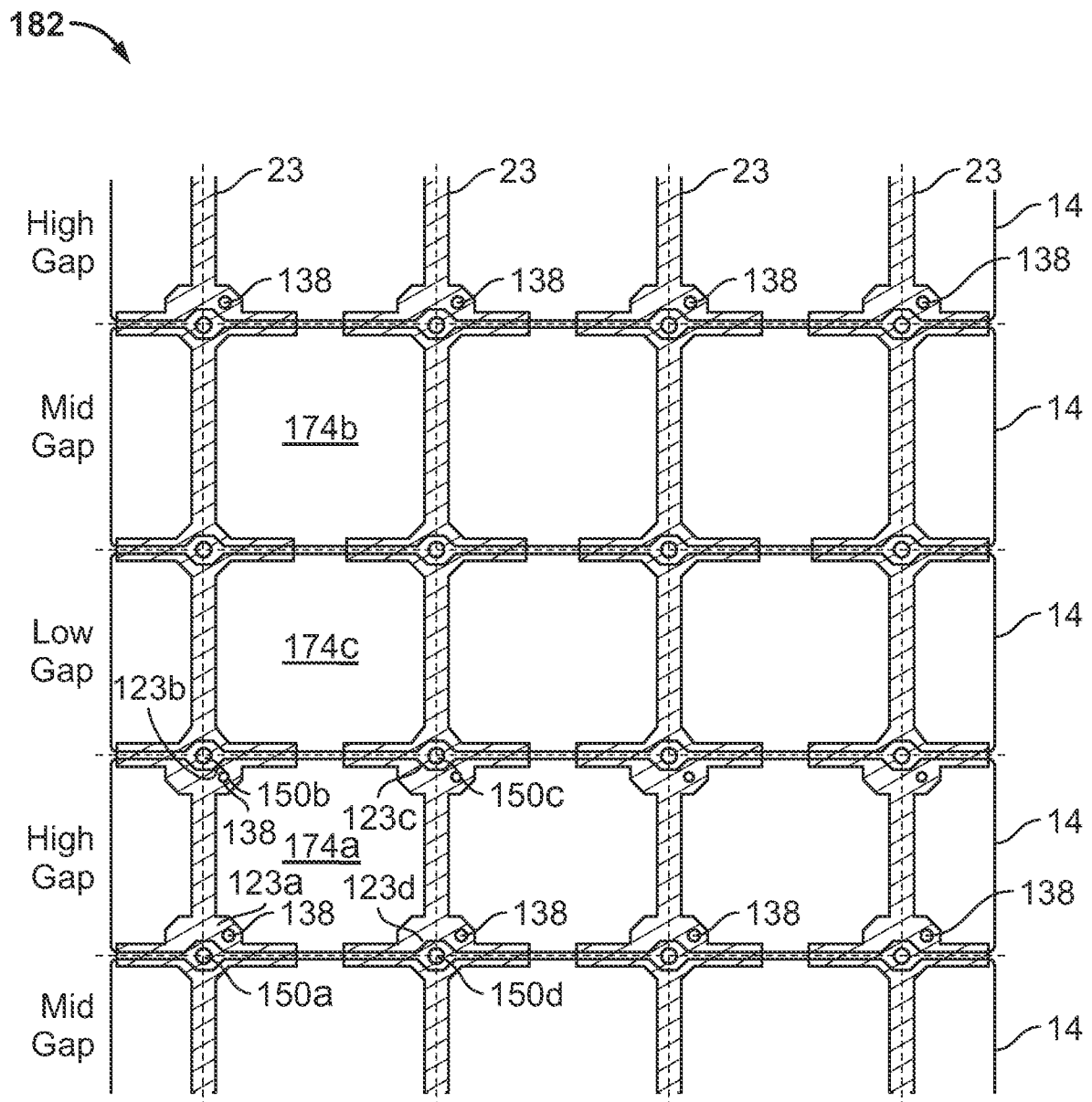


Figure 11B

24/29

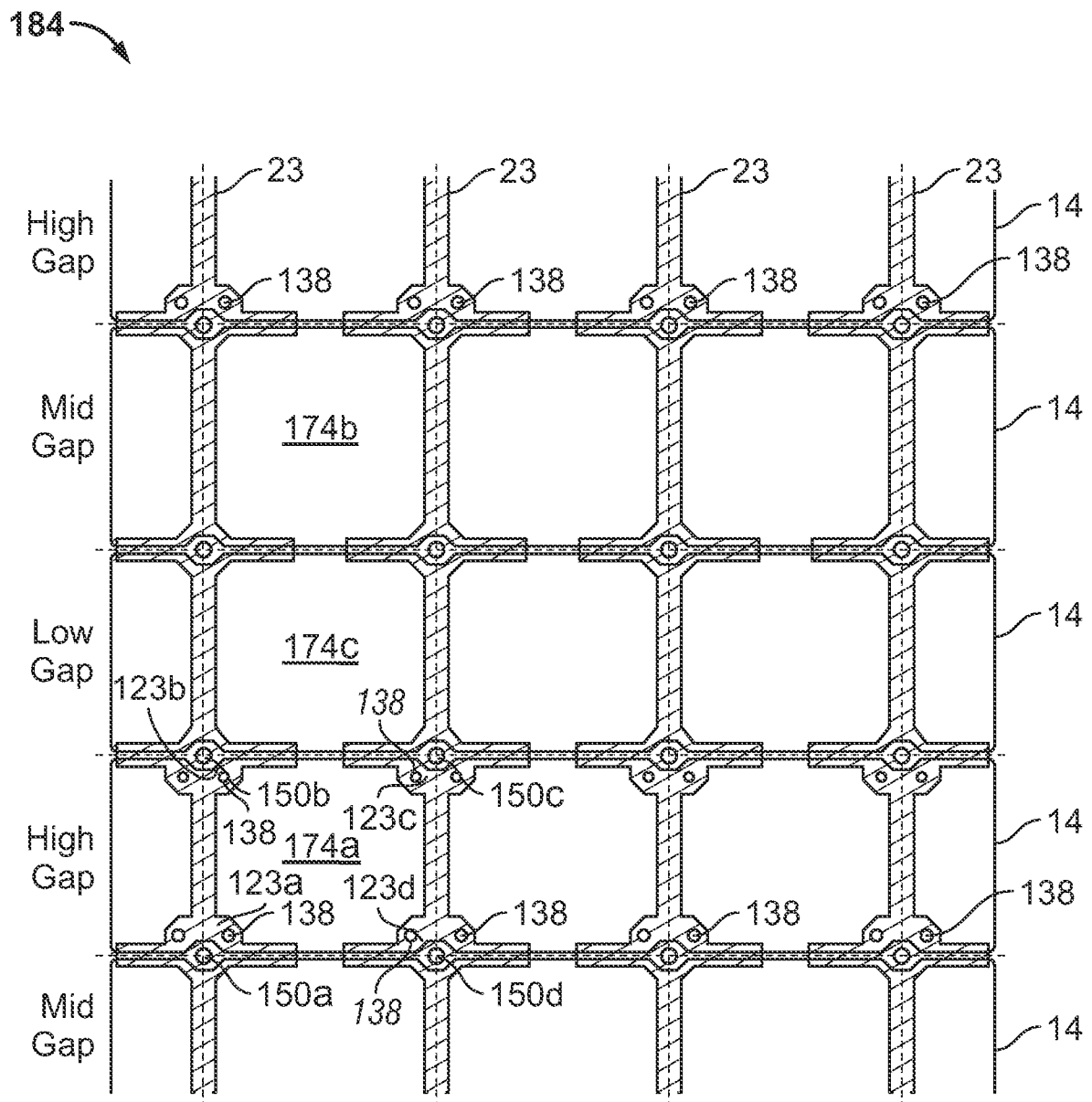


Figure 11C

25/29

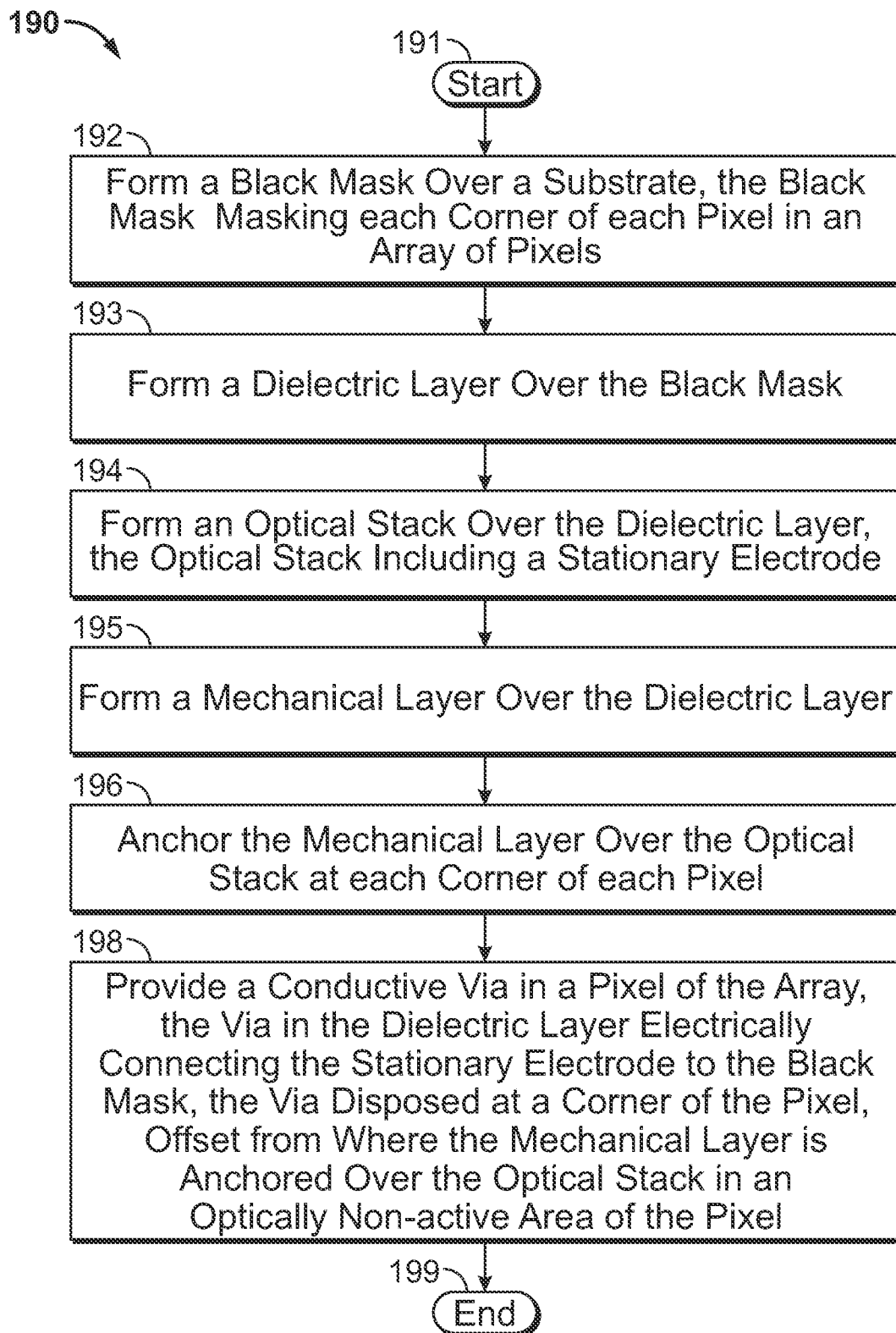


Figure 12

26/29

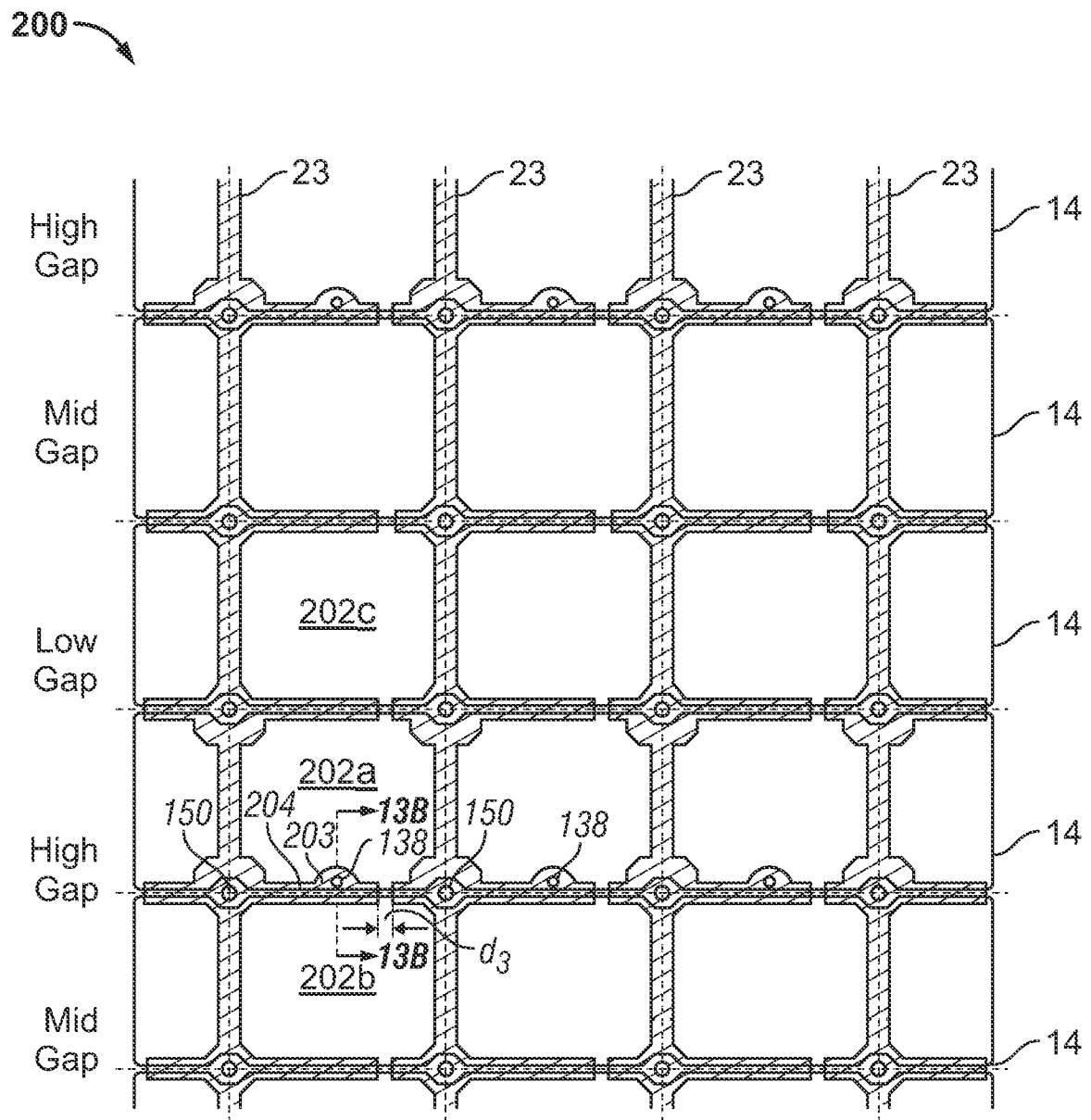


Figure 13A

27/29

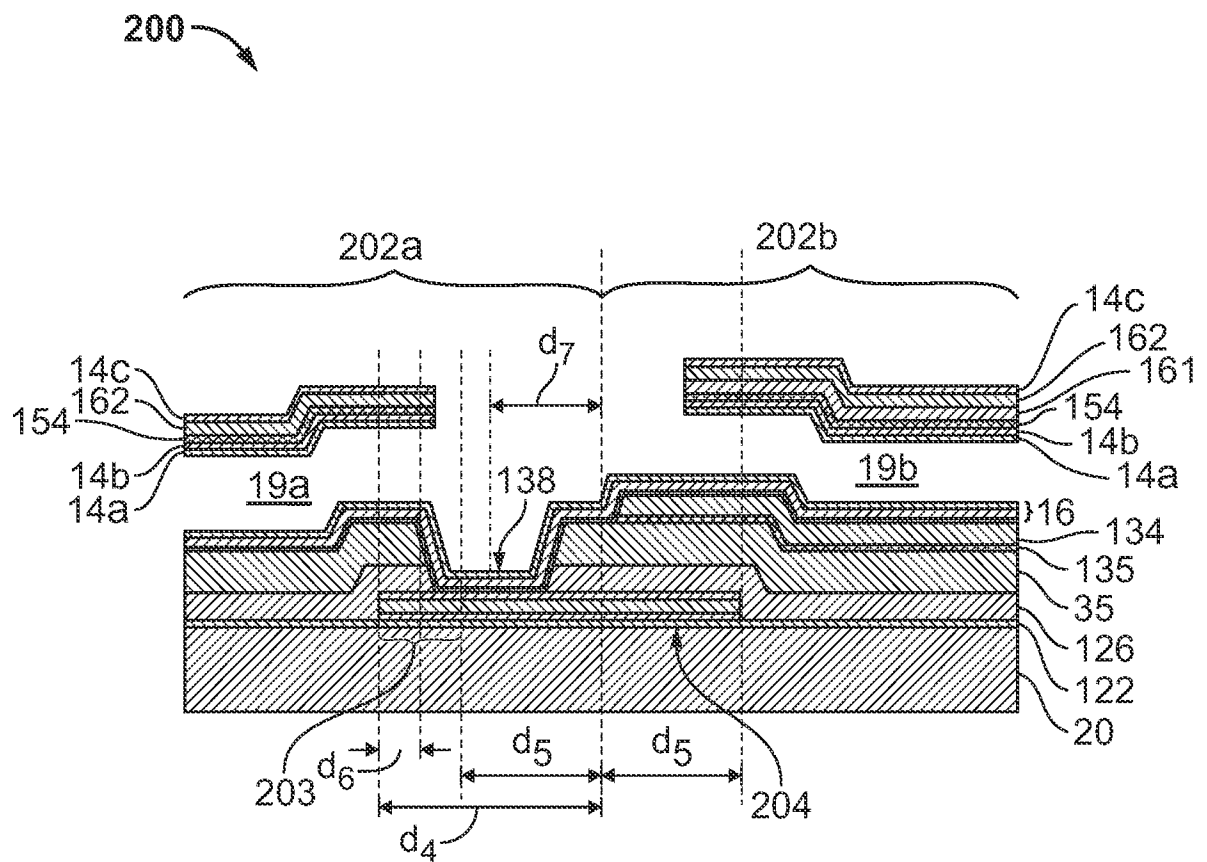


Figure 13B

28/29

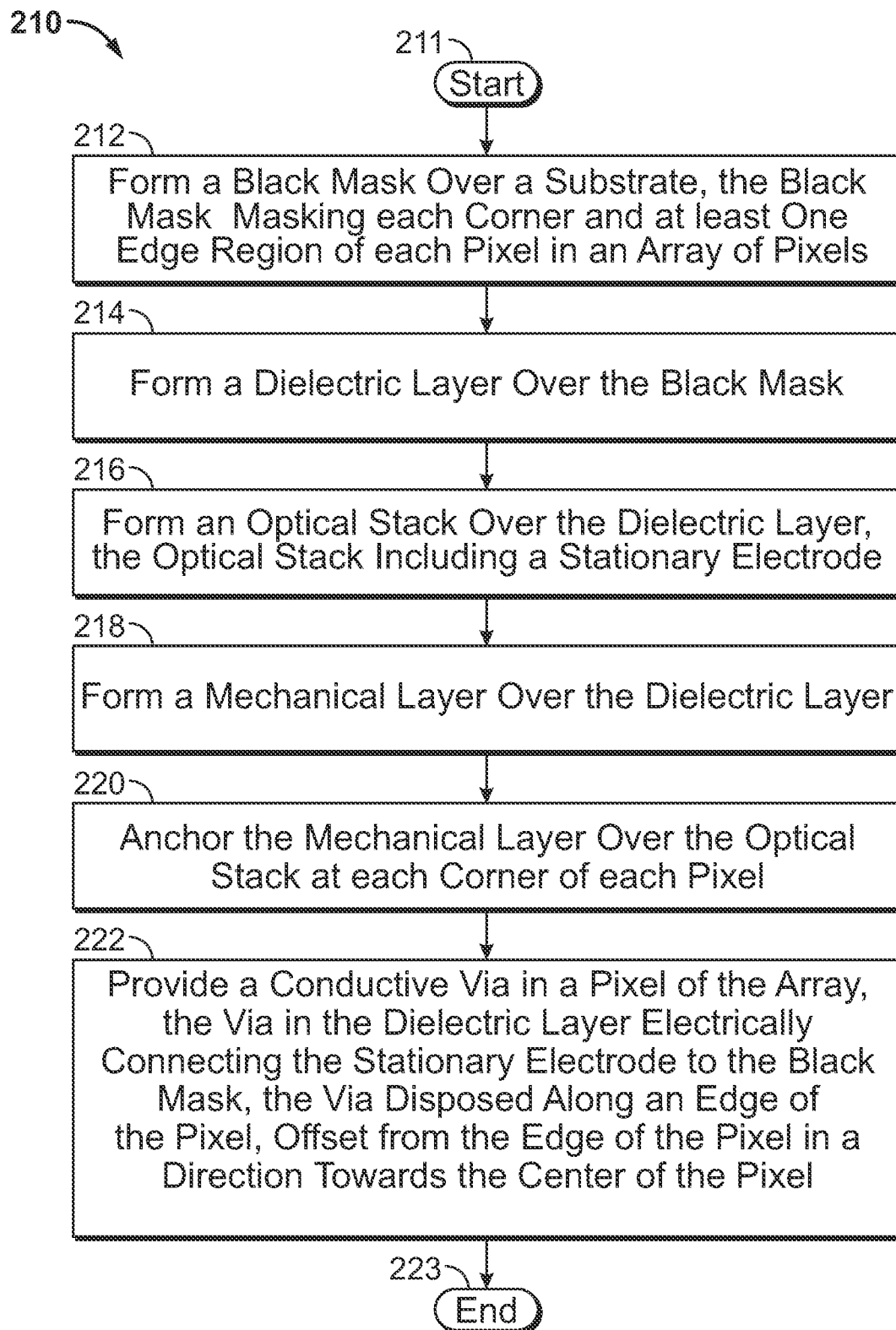


Figure 14

29/29

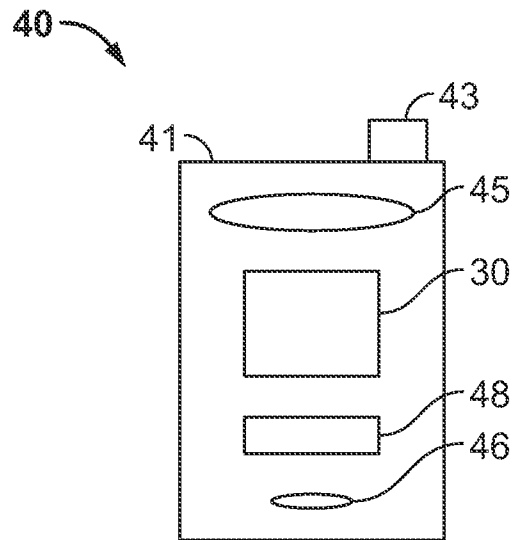


Figure 15A

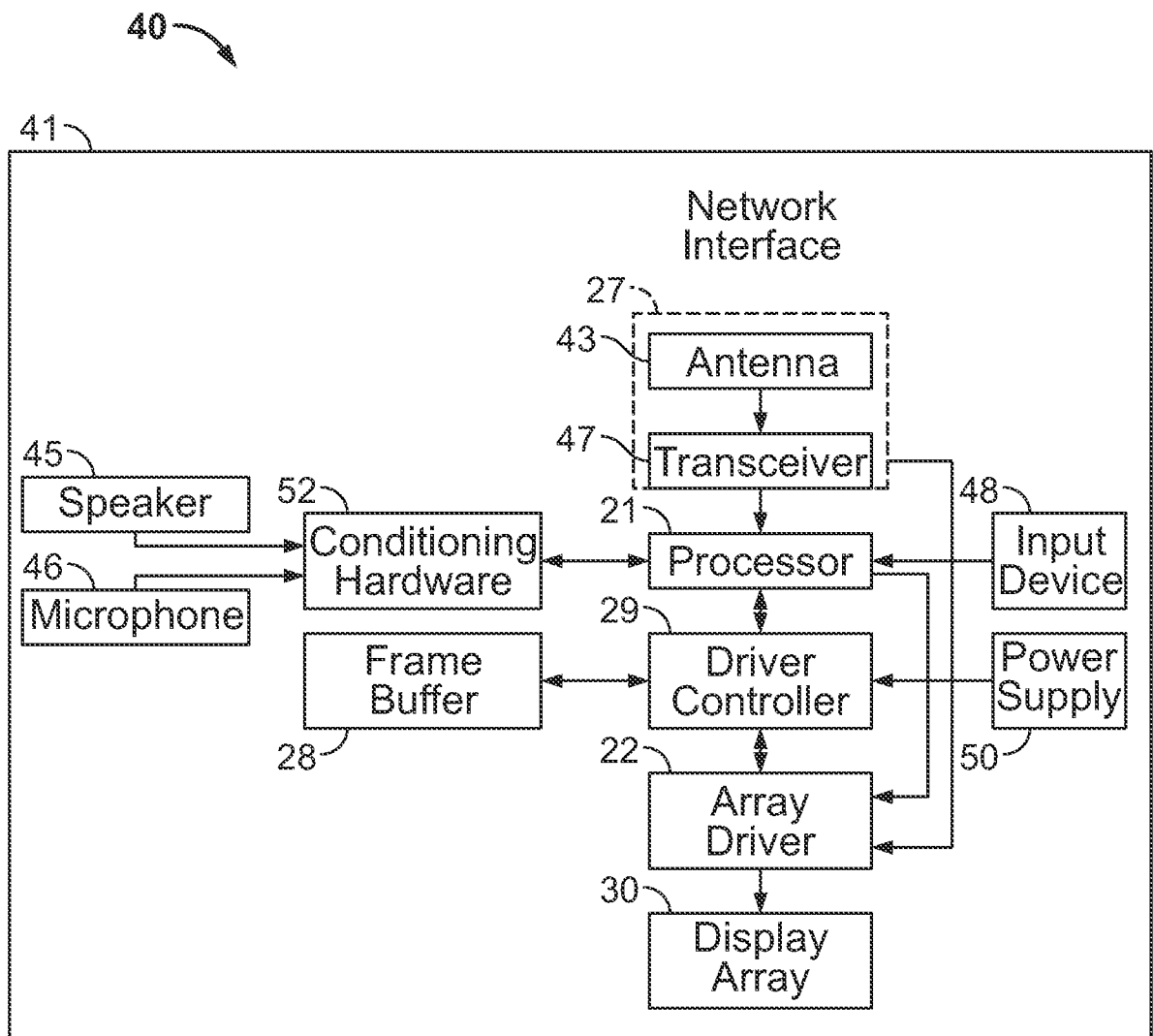


Figure 15B

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2012/031643

A. CLASSIFICATION OF SUBJECT MATTER
INV. G02B26/00 G02B26/08
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G02B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2010/079847 A1 (PATEL SAPNA [US] ET AL) 1 April 2010 (2010-04-01) paragraph [0033] - paragraph [0038]; figure 1 paragraph [0063] - paragraph [0084]; figures 8A,8B,9A,9B -----	1-28
Y	US 6 861 277 B1 (MONROE MICHAEL G [US] ET AL) 1 March 2005 (2005-03-01) paragraph [0042]; figure 5A -----	1-28
A	US 2006/227404 A1 (FAASE KENNETH J [US] ET AL) 12 October 2006 (2006-10-12) paragraph [0043]; figure 5A -----	1
A	US 2008/068699 A1 (MILES MARK W [US]) 20 March 2008 (2008-03-20) abstract; figure 1 -----	1



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

26 June 2012

Date of mailing of the international search report

11/07/2012

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Lehtiniemi, Henry

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2012/031643

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010079847 A1	01-04-2010	US 2010079847 A1	01-04-2010
		WO 2010039660 A2	08-04-2010

US 6861277 B1	01-03-2005	CN 1603225 A	06-04-2005
		EP 1524545 A2	20-04-2005
		JP 2005115370 A	28-04-2005
		TW I238809 B	01-09-2005
		US 6861277 B1	01-03-2005
		US 2005106772 A1	19-05-2005

US 2006227404 A1	12-10-2006	DE 112006000752 T5	24-01-2008
		GB 2441239 A	27-02-2008
		US 2006227404 A1	12-10-2006
		WO 2006110293 A1	19-10-2006

US 2008068699 A1	20-03-2008	US 7297471 B1	20-11-2007
		US 2007269748 A1	22-11-2007
		US 2008068699 A1	20-03-2008
