United States Patent

[11] **3,579,065**

[72] Inventor **Joseph F. Laukaitis**
Rochester, N.Y.

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[73] Assignee **Eastman Kodak Company**
Rochester, N.Y.

[54] **WEB SPEED CONTROL APPARATUS**
4 Claims, 5 Drawing Figs.

[52] **U.S. Cl.** **318/314,** 318/341
[51] **Int. Cl.** **H02p 5/08**
[50] **Field of Search** 318/341, 346, 314, 318; 242/75.51

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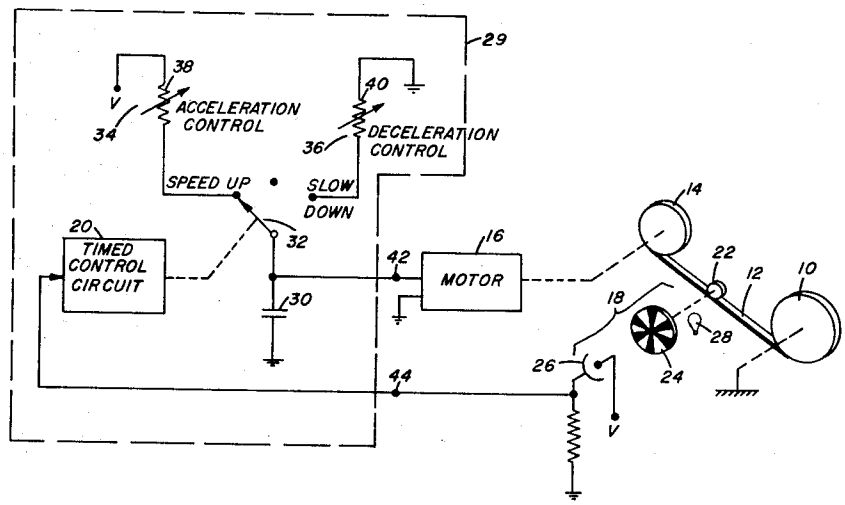
Primary Examiner—Oris L. Rader
Assistant Examiner—Robert J. Hickey
Attorneys—Walter O. Hodsdon, Paul R. Holmes and Robert F. Cody

ABSTRACT: A motor operates to drive a web at a predetermined speed. The speed of the motor is automatically adjusted to assure the proper rate of web speed, such motor being under control of a circuit which not only applies a correction signal to such motor for a "time" dependent on the necessary correction, but also applies such correction through a means the operation of which is itself dependent upon a time constant. This technique permits such broadband control of web speed that accelerating to or decelerating from a reference web speed obtains without hunting. As disclosed the invention uses digital techniques, while incorporating the above-mentioned principles, in such a way that digital-to-analog converter apparatus is obviated.



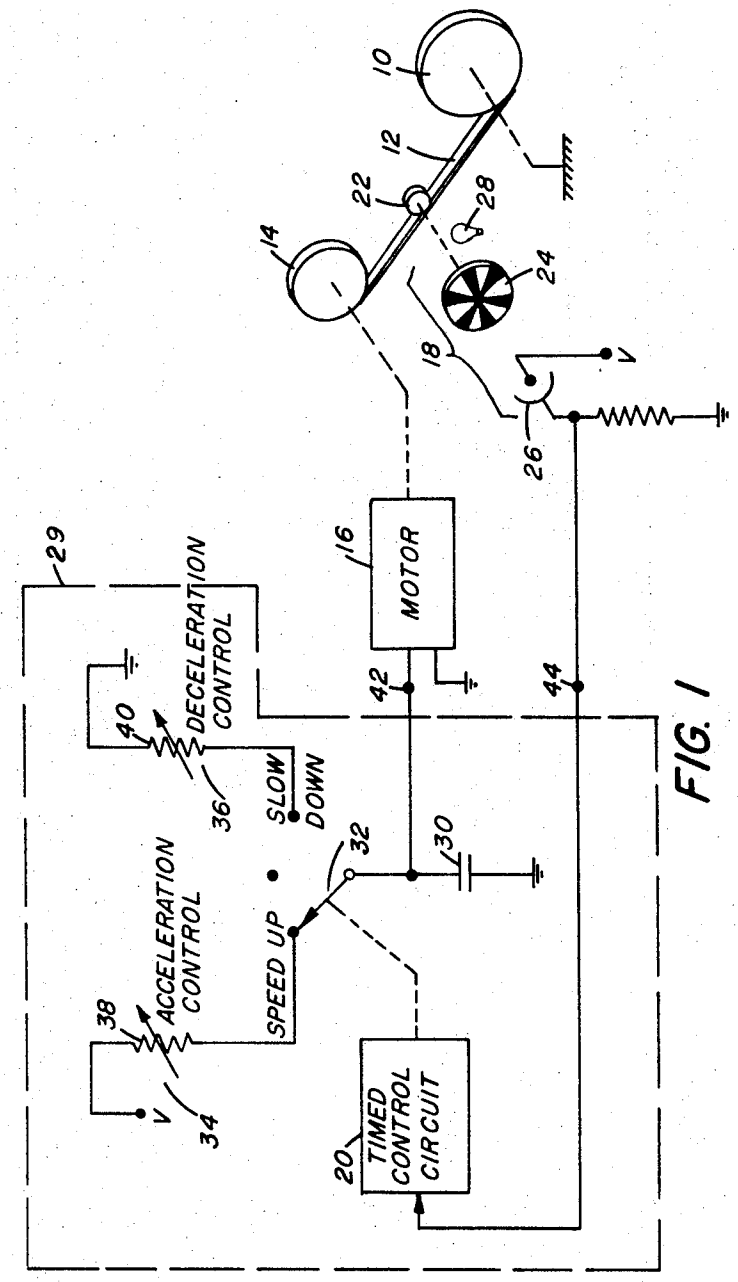


FIG. 1

JOSEPH F. LAUKAITIS
INVENTOR.
BY Paul R. Holmes
Robert F. Cody
ATTORNEYS

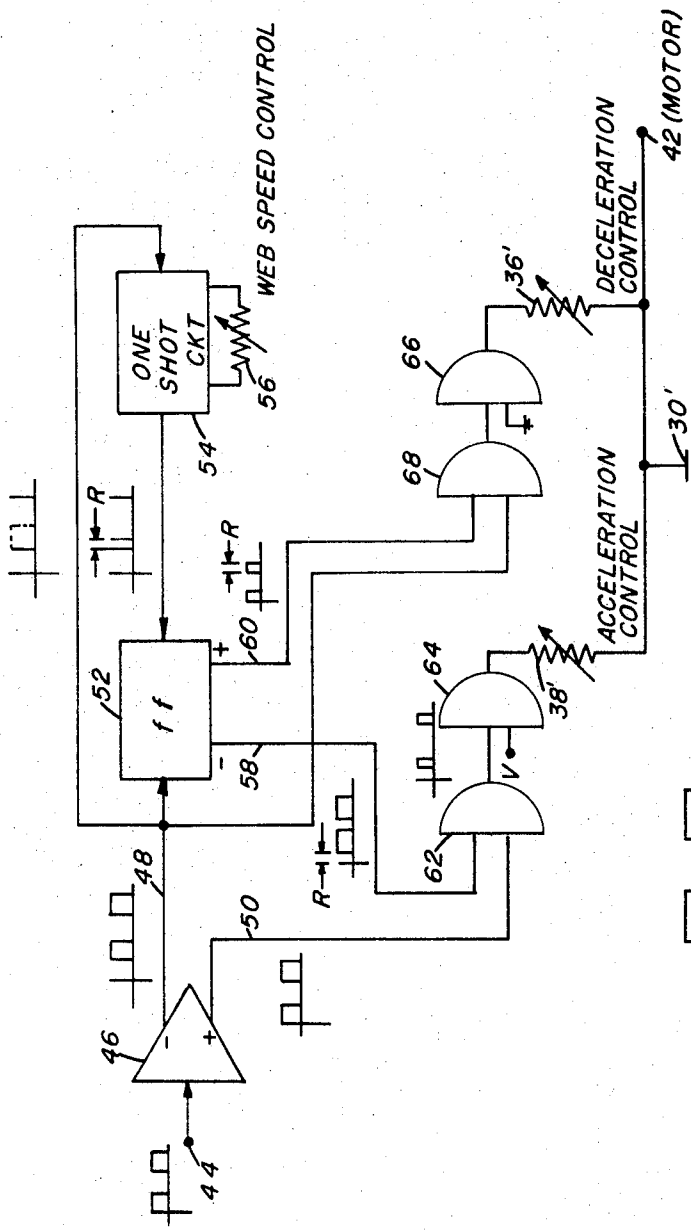


FIG. 2

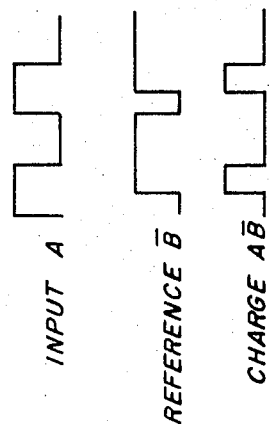


FIG. 3

JOSEPH F. LAUKAITIS
INVENTOR.
BY Walter O. Hodsdon
Paul O. Holmes
Robert E. Cody
ATTORNEYS

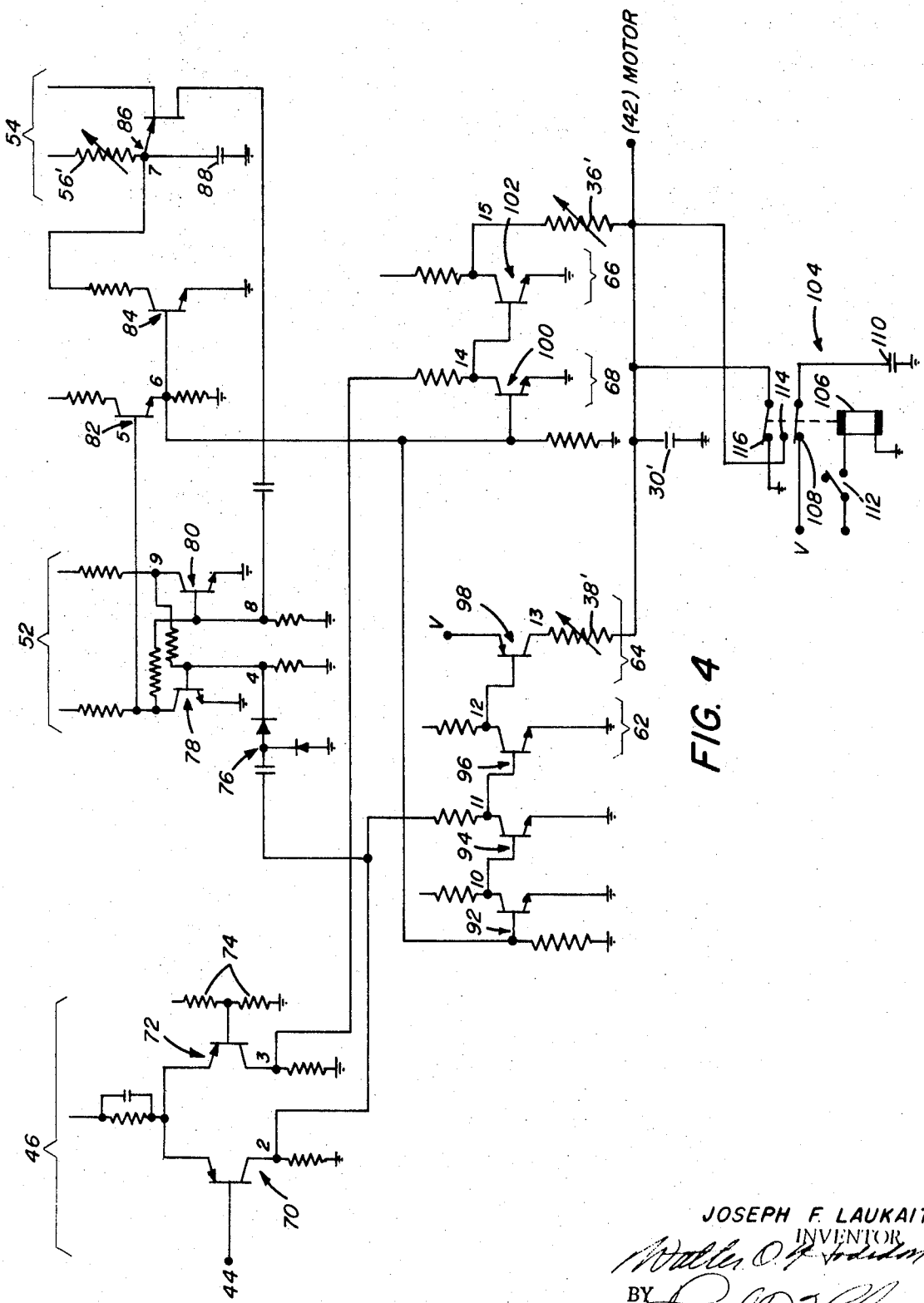


FIG. 4

JOSEPH F. LAUKAITIS
INVENTOR

BY Paul R. Holmes
Robert F. Cody
ATTORNEYS

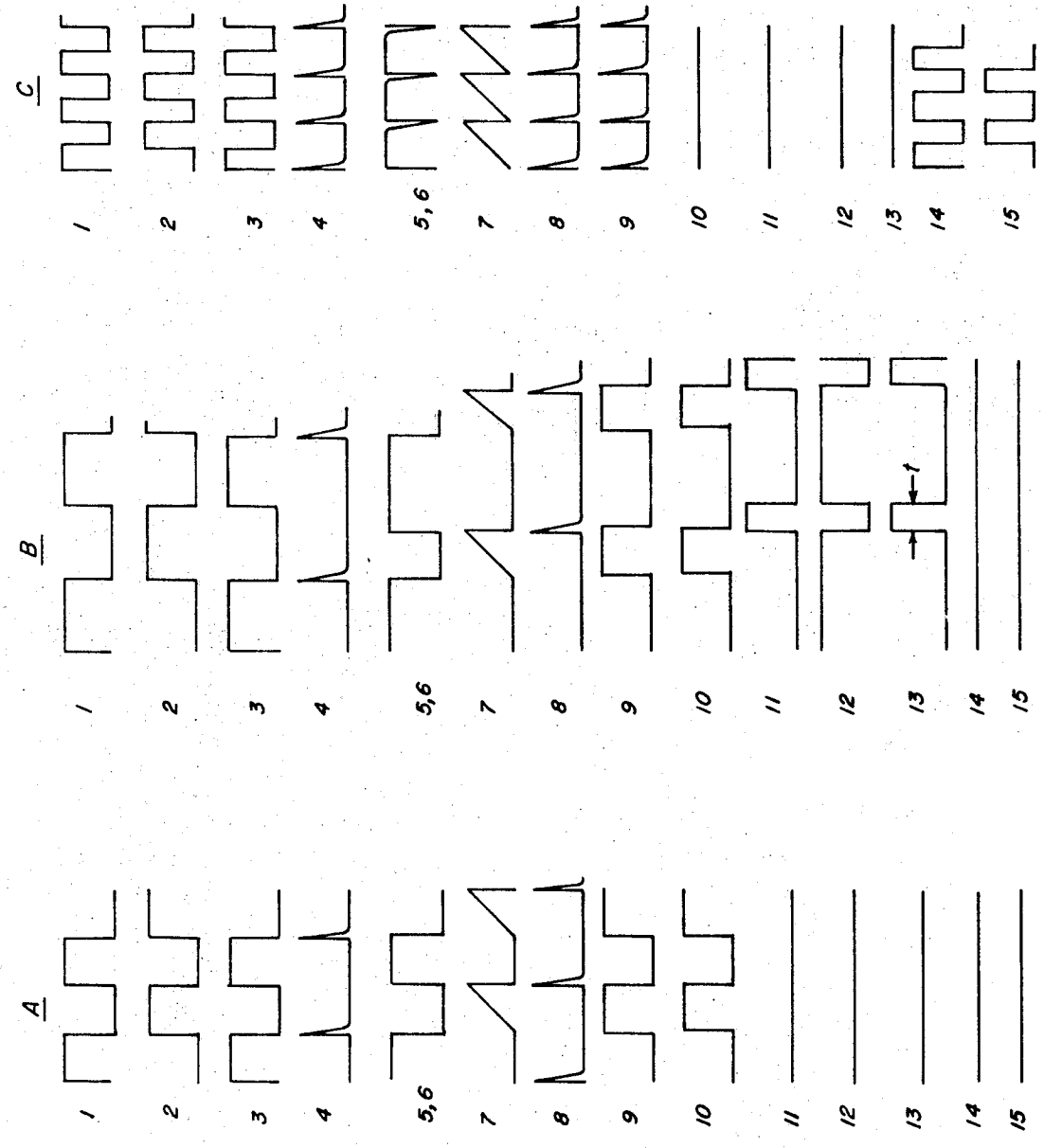


FIG. 5

JOSEPH F. LAUKAITIS
INVENTOR.
BY
Walter O. Hodsdon
Paul M. Holmes
Robert E. Cody
ATTORNEYS

WEB SPEED CONTROL APPARATUS

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates in general to the regulation of the speed of a moving web, say photographic film, and in particular is directed to a circuit which so tightly controls web speed that the web may be rapidly accelerated from a dead stop to a prescribed speed, or rapidly decelerated to a dead stop from such speed, without hunting.

2. Description of the Prior Art

In the manufacture and handling of webs such as photographic films and papers, spooling and respooling operations are commonplace. To assure a high degree of product quality, webs of photographic material must be spooled evenly at various stages during their manufacture, not only so that they may be easily and efficiently handled at subsequent stages, but also to prevent static-producing friction between the spool layers, which static may be ruinous to the photographic web being manufactured.

In a typical environment for the invention, film is to be unwound from a large spool and then directly rewound in smaller strips onto respective smaller spools. To implement such an operation, it is the usual practice to secure the end of the web from the larger spool of film to one of the smaller spools, and then to drive rotationally such smaller spool (while drag braking the larger spool to prevent its free wheeling) at a speed which assures the desired constant rate of film web drive. Thereafter, another—and then another, etc.—of the smaller spools is set up for rewinding. In so winding film web onto a smaller spool, it is necessary to bring quickly the rate at which such smaller spool is driven up to a certain maximum; then to drop the spool speed gradually as such small spool fills up; and then when the small spool has its prescribed length of film, to drop abruptly to zero the rate at which the small spool is driven, whereby the web may then be cut and the whole procedure repeated for a second spool.

To meet the above-stated requirements it has been the usual prior-art practice to employ a clock pulse generator or the like for providing a digital reference count representative of a demand web speed; then to provide a digital count representative of the instantaneous web speed; then to compare such counts to produce a correction count which is converted into an analog voltage for controlling the motor drive of the smaller spool in question. The obvious disadvantages of such a practice are that it requires an auxiliary clock pulse generator; makes count comparisons only after a comparatively large sampling of pulses; and necessitates the use of digital-to-analog converter apparatus.

SUMMARY OF THE INVENTION

The present invention obviates the equipment requirements of the prior art, doing so in a way that—while still employing digital techniques—provides automatically an analog control voltage without need for digital-to-analog converter apparatus; and apparatus according to the invention samples, for web speed correction purposes, on a pulse-to-pulse basis. In implementing the invention a capacitor, having respective charge and discharge time constants for acceleration and deceleration control of the drive motor in question, is charged, or discharged as the case may be, for a (pulse) duration dependent upon the magnitude of the error between a commanded web speed and the instantaneous web speed. It is this use of a double-time constant, together with pulse-to-pulse sampling which provides for the high gain control necessary to get up to the desired web speed quickly; to drop web speed to zero quickly; and provides for the low gain control necessary to lower smoothly and gradually the motor drive speed as the smaller spool in question is filled with web. That is, when getting up to the desired web speed the capacitor not only appears as a very small impedance to the motor control signal, but also the duration for applying the control signal to the control capacitor is maximum; when abruptly dropping the web speed to zero, the capacitor sees a short to ground, and the duration for discharging the capacitor is, again, maximum; when gradually discharging the capacitor as the smaller spool fills, the capacitor is discharged on a pulse-to-pulse basis for comparatively brief increments of time.

In its presently preferred form, the invention provides a train of pulses, the widths of which pulses represent the instantaneous web speed, and employs each pulse of such pulse train to initiate a respective reference pulse. The reference pulses and their respective pulses from the pulse train are applied to logic networks and, when the pulse train pulses are wider than their respective reference pulses, the motor control capacitor is charged for a time proportional to the pulse width difference; when the pulse train pulses are narrower than the reference pulses, the motor control capacitor is discharged for a time proportional to the pulse width difference. Therefore, the logic networks serve to define the durations during which the motor control capacitor may charge or discharge at respective time constants. And since the motor control capacitor charges and discharges in seesaw fashion, any tendency for the web speed to overshoot (or undershoot) the reference web speed is immediately corrected for by a corresponding discharge (or in the case of an undershoot, by a corresponding charge), thereby eliminating hunting.

One object of the invention is to provide an improved motor control circuit.

Another object of the invention is to provide a circuit for use in regulating the speed of a motor adapted to drive a web or the like.

Another object of the invention is to provide, in a motor control circuit, a control capacitor, the duration for charging such capacitor being regulatable as a function of a control error of one sense; and the duration for discharging such capacitor being regulatable as a function of a control error of a different sense.

Another object of the invention is to provide in a motor control circuit a control capacitor, the duration for charging such capacitor being regulatable as a function of a control error of one sense; and the duration for discharging such capacitor being regulatable as a function of a control error of a different sense, such charging and discharging being through circuits having themselves independent time constants.

Another object of the invention is to provide web speed control apparatus employing digital techniques in a way that obviates the need for digital-to-analog converter apparatus.

The invention will be described with reference to the FIGS. wherein

FIG. 1 is a block diagram, partially schematic, illustrating a presently preferred use for the invention,

FIG. 2 is a block diagram of a circuit according to the invention,

FIG. 3 shows waveform diagrams useful in describing the operation of the circuit of FIG. 2,

FIG. 4 is a schematic diagram of the circuit depicted in FIG. 2, and

FIG. 5 shows waveform diagrams which are helpful in understanding the operation of the circuit of FIG. 4.

With reference to FIG. 1, a presently preferred arrangement for the invention has a large spool **10** of web material **12** cooperative with a smaller takeup spool **14**. The spool **10** is provided with an adequate drag brake to prevent its freewheeling; and the spool **14** is rotatably driven by means of a motor **16**. As the motor **16** drives the spool **14**, a photoelectric tachometer **18** produces, in accordance with web speed, a series of pulse signals which are applied to a control circuit **20**. The tachometer **18** includes a wheel **22** driven by means of the web **12**; a spoked light modulator **24**; and a photoelectric cell **26** which is adapted to receive modulated light from a source **28**, producing therefrom a train of pulses, the widths of which pulses are inversely proportional to web speed.

The circuit shown within the dashed lines **29** of FIG. **1** is the functional equivalent of the presently preferred form of the invention indicated in FIGS. **2** and **4**. And as above noted, the

motor 16 which drives the takeup spool 14 is adapted to be driven at a speed(s) which assures a certain rate of travel for the web 12. The motor 16 is driven in accordance with the signal developed across a capacitor 30, such capacitor being chargeable and dischargeable, by means of a switch 32, through respective circuits 34 and 36. To be noted is that the control circuit 20 operates to hold the switch 32 cooperative with either the circuit 34 or with the circuit 36 for a "time" proportional to the amount that the motor 16 speed must increase (to bring the web speed up to its reference speed) or for a "time" proportional to the amount that the motor 16 speed must drop (to hold the reference web speed, or to drop web speed to zero). The impedances (38 and 40) of the charge and discharge circuits 34 and 36 (respectively) cooperate with the capacitor 30 to define respective charge and discharge time constants, and by making such impedances adjustable, the charge and discharge time constants may be finely adjusted to control the acceleration and deceleration of the motor 16 drive, a feature especially desirable if the invention is to be adapted to drive webs under a variety of different setups. Thus, two time-dependent factors, viz. the time during which the switch 32 is in contact with the circuit 34 together with the R(38)C(30) time constant of the circuit 34, effect control of the motor 16 in getting up to the speed necessary to drive the web 12 at its reference speed; and two time-dependent factors, viz. the time during which the switch 32 is in contact with the circuit 36 together with the R(40)C(30) time constant of the circuit 36, effect control of the motor 16 to drop its speed to hold the reference web speed, or to drop such web speed to zero.

At startup, the motor 16 snaps to drive the web 12 at the desired speed, not only because the signal applied to the capacitor 30 sees little or no resistance at that time, but also because the duration for charging, i.e. the duration that the switch 32 contacts the circuit 34, is kept maximum by the control circuit 20. However, since the charge-time duration is adjusted as a function of the error between the instantaneous web speed and the reference web speed, the signal on the capacitor is damped as an inverse function of such error, and attendantly the motor reaches the desired speed without overshooting such speed. To drop web speed to zero, say when the spool 14 is filled, the capacitor 30 is discharged through what appears as a small resistance to ground, and by means of the control circuit 20 such discharging is assisted by keeping the capacitor 30 in contact with the discharge circuit 36 for a long time period. During running, i.e. while holding the reference web speed, the capacitor 30 charges and discharges, as is necessary, in short bursts to hold the reference web speed smoothly under tight control.

Reference should now be had to FIG. 2 which shows a block diagram of the presently preferred form of the invention (see FIG. 4 also), such block diagram being especially helpful for an understanding of the functioning of the circuit of FIG. 4. Circuit components finding corresponding parts in FIG. 1 are similarly noted, but are primed, in FIG. 2; and the circuit of FIG. 2 is adapted to be substituted for the circuit within the dashed lines 29 of FIG. 1 by being coupled to points 42 and 44 of FIG. 1.

The tachometer 18 output pulses are applied to an amplifier 46 which produces respective signals on leads 48 and 50, and which signals are 180° out of phase with one another. By means of suitable wave shaping, the leading edge of the pulse on the lead 48 serves to trigger a flip-flop circuit 52, and to arm a one-shot timing circuit 54 which fires, after a predetermined duration—as determined by a variable resistor 56—to reset the flip-flop circuit 52. Therefore, the flip-flop circuit 52 produces pulses on its output leads 58, 60, each such pulse having a reference duration R (see FIG. 2) which is representative of the desired, or reference, web speed.

The reference pulses on the flip-flop circuit lead 58 are applied to an AND gate 62 together with the signals on the lead 50. With the pulses on the lead 50 of a duration proportional to the instantaneous speed of the web 12, the AND gate 62 does not produce an output so long as the lead 50 and lead 58 pulses are of identical durations. With the speed of the web 12 below the reference web speed, however, the situation depicted in FIG. 3 obtains. The signal A is that which appears on the lead 50; the signal $\overline{B}$ is that which appears on the lead 58. And the signal $A\overline{B}$ is of a duration dependent upon the amount that the web speed is below the reference web speed. The signal $A\overline{B}$ is applied to turn on an AND gate 64 so that a charging potential V may be applied through an acceleration control resistor 38' to pulse a capacitor 30' for a time proportional to the web speed error difference. During the time that the capacitor 30' is being charged to bring the web 12 up to its reference speed, the capacitor 30' is prevented from discharging, via a deceleration control resistor 36', by virtue of a turned-off AND gate 66. That is, since the amplifier 46 output on the lead 48 is negative longer than the flip-flop lead 60 is held positive, and AND gate 68 for arming the discharging AND gate 66 cannot, itself, be actuated.

To appreciate still more fully the operation of apparatus according to the invention, reference should be had to FIGS. 4 and 5. FIG. 4 as above noted shows the circuit the block form of which is shown in FIG. 2; and those character notations which are found in FIG. 2 may also be found in FIG. 3. For sake of simplicity only those bias potentials directly relevant to the concept of the invention are shown in FIG. 4, and it is understood that the application of appropriate biases is well within the scope of those skilled in the art.

The amplifier 46 consists of a pair of transistors 70 and 72, the output signals of which are 180° out of phase with one another. That is, a positive signal applied (point 1) to the base of the transistor 70 turns such transistor off (placing the point 2 of the transistor 70 at ground potential); and since the base of the transistor 72 is negative with respect to the collector of the transistor 72—by virtue of a voltage divider circuit 74—the transistor 72 turns on, thereby placing the point 3 of the transistor 72 above ground. When the input signal (point 1) to the base of the transistor 70 goes negative, the transistor 70 turns on, causing the point 2 of the transistor 70 to go positive. The emitter of the transistor 72 is less positive than the divided voltage applied to the base of the transistor 72, thereby turning the transistor 72 off and placing the point 3 of the transistor 72 at ground potential.

The pulse signals appearing at the point 2 of the transistor 70 are so differentiated in a circuit 76 that the leading edge of each such pulse signal creates a positive going spike signal across the base resistor (point 4) of a first flip-flop transistor 78, turning on the transistor 78. With the transistor 78 turned on, the second transistor 80 of the flip-flop circuit 52 turns off, as is conventional.

When the transistor 78 turns on, a negative square wave signal is applied to a transistor 82, the emitter follower circuit (point 6) of which goes negative also, turning off a transistor 84. With the transistor 84 turned off, i.e. the input (point 7) of a unijunction transistor 86 is not held at ground potential, and therefore a capacitor 88 in the unijunction transistor input circuit is free to charge via a variable resistor 56' and, when the voltage across the capacitor 88 reaches a certain level, the unijunction transistor 86 fires to apply a positive signal across the base resistor of the transistor 80 (point 8). The positive signal at the point 8 of the transistor 80 turns such transistor 80 on, and causes the collector of the transistor 80 to go negative (point 9), which negative potential is applied to turn the transistor 78 off, as is conventional. Thus, by suitably adjusting the RC time constant of the resistor 56'-capacitor 88 circuit, the flip-flop circuit 52 may be made to produce reference square wave pulses, at points 5 and 6 of precise predetermined duration.

The positive reference signals (point 6) are applied to turn signal-inversion transistors 92 and 94 on and off respectively. With the transistor 94 turned off, the signal appearing at point 2 of the transistor 70—which is the web speed representative signal—is applied (point 11) to the base of a transistor 96. Positive signals which appear at the base of the transistor 96

turn the transistor **96** on, causing the signal (point **12**) at the base of the AND gate **64** transistor **98** to go negative. Negative signals which appear at the base of the transistor **98** turn the transistor **98** on, and permit the capacitor **30'** to charge through the adjustable acceleration control resistor **38'** for the durations of such negative signals; conversely, when the transistor **92** is turned off by a negative signal, the transistor **94** is turned on, thereby grounding the speed representative signal which appears at point **11** of the transistor **96**, and causing the transistor **96** to turn off. With the transistor **96** off, the signal at point **12** goes positive to prevent the transistor **98** from conducting to charge the capacitor **30'**.

Aside from being applied to control the charging logic circuits (**62, 64**), the flip-flop pulses of reference duration are also applied to control the operation of the discharging logic circuits (**66, 68**). With a positive reference signal applied to the base of a transistor **100** (AND gate **68**), the transistor **100** turns on, and causes the web speed representative signal from the transistor **72** (point **3**) to be sent to ground; conversely, a negative signal received at the base of the transistor **100** turns the transistor **100** off, and causes the web speed representative signal from the transistor **72** to be applied to a transistor **102** (AND gate **66**). A positive signal at the base of the transistor **102** (point **14**) causes the transister **102** to conduct, thereby permitting the capacitor **30'** to discharge to ground via the adjustable deceleration control resistor **36'**.

FIG. **5** indicates the signal wave forms which may be found at the various points **1—15** on FIG. **4**. FIG. **5A** shows those waveforms which obtain when holding the reference web speed, and indicates that the capacitor **30'** neither charges nor discharges during such operation (waveforms **13, 15**). FIG. **5B** shows those waveforms which obtain when coming up to the reference web speed, indicating that the capacitor **30'** is repeatedly pulsed (pulses of gradually diminishing duration *t*, waveform **13**) as the web is brought up to its reference speed; and indicating further that the capacitor **30'** does not discharge during such operation (waveform **15**). FIG. **5C** shows those waveforms which obtain, for example, when dropping to maintain the reference web speed, indicating that during discharging, the capacitor **30'** is not pulsed (waveform **13**), but is instead repeatedly discharged (in pulses of gradually diminishing duration *t*, waveform **15**).

The circuit of FIG. **4** depends for its operation on the application of web speed pulses to the transistor **70**. When first starting to bring the web up to its reference speed, the tachometer is itself not producing pulses, let alone pulses having durations representative of web speed. Therefore, in this the presently preferred form of the invention, operation of the motor of FIG. **4** is initiated by a startup circuit **104** which "fools" the motor **16** into operation. A relay **106**, when not actuated, permits a voltage V via a relay contact **108** to develop across a capacitor **110**. By actuating the relay **106**, by means of a switch **112**, the capacitor **110** signal is applied, via a relay contact **114**, to actuate the motor and begin the production of a pulse train input to the transistor **70**, and thereby initiate the control of web speed according to the invention.

A relay contact **116** is provided to ground the capacitor **30'** after each successive use of the web speed control motor, whereby such motor will not receive too large a signal input at the start of each subsequent motor actuation.

The invention has been described in detail with particular reference to a preferred embodiment thereof, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention as described hereinabove and as defined in the appended claims. For example, it would be within the scope of the invention, say, to employ the "discharge" pulses (waveform **15**) to operate a relay which periodically opens the control motor circuit, whereby friction and drag will cause the motor (and web) speed to fall off, while increase of the motor (and web) speed is as described above. It would also be within the scope of the invention, say, to employ one or more fixed resistors instead of the adjustable resistors **36'**, **38'**, and **56'**, if certain variables relevant to the use of the circuit in question are substantially invariant. Both of these representative alternatives, to be noted, are within the scope of the invention because they employ dual time-dependent controls during motor speed regulation, and further because they do so in a way that provides the tight control common to digital apparatus without the usual equipment necessary to a typical digital control system.

I claim:

1. A web speed control system comprising:

a. motor means for driving said web,

b. control circuit means for use in increasing and decreasing the speed of said motor means,

c. first pulse-producing means cooperative with said web for producing at least one pulse, the width of which pulse is representative of the speed of said web,

d. second pulse-producing means for producing at least one reference pulse, the width of which reference pulse is representative of a desired speed for said web,

e. means for effecting a comparison between the widths of said pulses produced by said first and second pulse-producing means to produce a motor speed correction signal that is proportional to the difference between the widths of said pulses, and

f. means for applying said correction signal to said circuit means to vary the speed of said motor means,

said means for effecting a comparison between the widths of said pulses being adapted to produce a motor speed correction signal in the form of a pulse, the duration of which is in proportion to the error between the width of said web speed pulse and the width of said reference pulse,

said means for applying said speed correction signal to said motor means being provided with a time constant of operation, said means for applying said speed correction signal to said motor means being a reactive circuit,

said means for effecting a comparison between the widths of said pulses having first and second circuits, said first circuit being responsive to said speed correction signal to energize the reactive element of said reactive circuit when said web speed pulse is of a greater duration than said reference pulse, and said second circuit being responsive to said speed correction signal when said web speed pulse is of a shorter duration than said reference pulse to adjust downwardly the speed of said motor, the signal developed across said reactive element being applied to said circuit means to control the speed of said motor means.

2. The apparatus of claim **1** wherein said reactive circuit is an RC circuit comprising first and second resistors for respectively said first and second circuits, which resistors are connected in parallel with a common capacitor.

3. The apparatus of claim **2** wherein the resistance of said first resistor is adjustable.

4. The apparatus of claim **2** wherein the resistances of both said first and second resistors are adjustable.