AN ELECTRICAL CONNECTION FOR A MICROELECTRONIC CHIP, AND A METHOD FOR MANUFACTURING SUCH A CONNECTION

Abstract: An electrical connection for a microelectronic chip, and a method for manufacturing such a connection. A method of manufacturing an electrical connection for a microelectronic chip, the microelectronic chip 3, 13, 23, 33 comprises at least one connection pad of reduced size 2, 2A, 2B, 2C, 2D, wherein the method of manufacturing comprises the steps of: - adding an additional layer 11, 11’, 11”, 11A, 11B on at least one connection pad, - bonding a wire 8 on the additional layer.
before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.
An electrical connection for a microelectronic chip, and a method for manufacturing such a connection

FIELD OF THE INVENTION
The invention relates to the electrical connection of microelectronic components, in particular the electrical connection of one or several microelectronic chips.

The invention also relates to a method for manufacturing the electrical connection of a microelectronic chip, in particular when using a wire bonding process.

BACKGROUND OF THE INVENTION
The semiconductor industry always seeks to optimize the use of the silicon wafer surface, in particular for integrating more and more circuits on the wafer surface. A way to achieve this goal is focused on decreasing the connection pad size. The connection pads are the elements on a microelectronic chip which enable to connect the integrated circuit to other electronic components (for example other microelectronic chip) or to the microelectronic chip package (for example microelectronic module) or to the electronic boards.

The connection pad size has evolved as follows:
- 200 x 100 μm in the 80’s.
- 120 x 120 μm in the 90’s.
- 90 x 90 μm since year 2000.
- 70 x 70 μm since year 2004.
- 20 x 20 μm is under development.

In view of this evolution, the conventional wire bonding process is more and more difficult, even impossible to implement without damaging the microelectronic chip.

Figure 1 illustrates the electrical connection of the pads of a microelectronic chip to the metallic contact of the substrate by using wire bonding process (also called ball bonding process).

In a first step, a ball 1 of metallic material is formed and thermo-sonic bonded on the connection pad 2 of the chip 3 as shown in the details view of Figure 2.A.
In a second step, the microelectronic chip 3 is placed on the substrate 5, the active face 9 of the microelectronic chip 3 being positioned upside. The face opposite to the active face 9 is glued via a glue layer 7 on the substrate 5.

In a third step, the chip connection pad 2 is wired to the metal area 4 on substrate 5. A stitch 6 is bonded on the metal area 4. Then, the electrical connection between the chip connection pad 2 and substrate metal area 4 is made by a metal wire 8.

The metal wire can be made of gold, palladium, or copper, etc... The standard wire bonding process requires the use of a metal wire having a diameter ranging from 15\(\mu\)m to 35\(\mu\)m. The wire diameter depends in particular on wire length, electrical power, wire loop height.

Ball bonding process requires forming first a ball which measures:
- at least twice the wire diameter before bonding on pad, and
- at least three times the wire diameter after thermo-sonic bonding on pad.

Generally, a wire bonding machine has a global accuracy of about +/- 5\(\mu\)m (X, Y, Z axis accuracy).

The minimum required area to bond has to measure from 55 \(\mu\)m x 55 \(\mu\)m (for 15 \(\mu\)m of wire diameter), 85 \(\mu\)m x 85 \(\mu\)m (for 25\(\mu\)m of wire diameter) to 115 \(\mu\)m x 115 \(\mu\)m (for 35 \(\mu\)m of wire diameter).

As a consequence, with reduced connection pad size and usual wire diameter, there is no ball bonding size reduction and the ball takes a surface greater than the connection pad surface as shown in the details view of Figure 2.B. In this case the microelectronic chip circuit is generally damaged during the bonding process (for example cracks 10 are formed in the active surface as shown on Figure 2.B).

Thus, the only way to perform a conventional wire bonding is to reduce the wire diameter according to the above rules. This leads to mechanical problems (wire too flexible and sagging, wire too brittle and difficult to handle) and electrical problems (wire too resistive and heat effect).

A possible alternative to the conventional wire bonding process is the use of so-called "flip-chip" technology. However, for industry using the conventional wire bonding process the use of the "flip-chip" technology requires a complete manufacturing process change, which requires important investments in new equipments. Also, the "flip-chip" technology is less flexible than the wire bonding process.
SUMMARY OF THE INVENTION

One goal of the invention is to continue using the standard wire bonding process in the frame of narrow connection pads with only minor modification. Another goal of the invention is to keep using the same manufacturing equipment for performing the electrical connection.

According to the invention, at least one additional metallic layer is added on the connection pads before the connection ball and the wire are bonded on the connection pad (yet the metallic layer).

More precisely, the present invention relates to a method of manufacturing an electrical connection for a microelectronic chip, the microelectronic chip comprises at least one connection pad of reduced size, wherein the method of manufacturing comprises the steps of:

- adding an additional layer on the at least one connection pad,
- bonding a wire on the additional layer.

The step of bonding a wire on the additional layer comprises the further step of forming a ball of metallic material on the additional layer.

The invention also relates to an electrical connection for a microelectronic chip obtained with the manufacturing method of the invention. The electrical connection according to the invention comprises at least one connection pad and an additional layer added on the connection pad, the additional layer having a thickness so as to protect the active face of the chip from the connection ball formed and bonded on the additional layer.

Advantageously, the wire is thermo-sonic bonded on the additional layer.

According to an alternative, the additional layer comprises a first sub-layer and a second sub-layer, the first sub-layer being attached to the connection pad, at least one of the sub-layers is made of a metallic material. The layers can be deposited by electro-less metal deposition process (plating) or by electrolyze metal deposition process.
Advantageously, the additional layer has a thickness so as to protect an active surface of the chip from the ball formed on the additional layer. The thickness of the additional layer may vary from 5μm to 10μm.

The metallic material may be Ni, Cu, Au, Pd, Pt or Ag. For example, the first sub-layer can be made of Ni, while the second sub-layer can be made of Au, Pd, Pt or Ag.

The deposition of one or several metallic layers (Nickel, Copper, Gold, Palladium...) compatible with thermo-sonic bonding process, with various layer thicknesses is easy to perform. By using the conventional/standard wire bonding process (the one used with standard pad size) modified according to the invention, it is possible to avoid damaging the chip even with reduced pad size. In particular, the standard wire bonding process can be used for pad size inferior to two times the wire diameter.

Further, the electro-less plating on wafers is a well known and inexpensive process. Thus, with the invention, there is no need to switch to flip-chip process which enables to avoid investing in new equipment. Further, batch processing are still possible. Also, with the use of metal deposition techniques, it is possible to connect pad even on non-planar areas.

**BRIEF DESCRIPTION OF THE DRAWINGS**

The present invention is illustrated by way of example and not limited to the accompanying figures, in which like references indicate similar elements:

Figure 1 schematically illustrates the electrical connection of the pads of a microelectronic chip to the metallic contact of the substrate by using wire bonding process according to the prior art;

Figures 2.A and 2.B schematically illustrate in details the effect of the pad size regarding the ball connection step of the wire bonding process according to the prior art;

Figure 3 schematically illustrates in details a modified connection pad according to a first embodiment of the invention;

Figure 4 schematically illustrates in details a modified connection pad according to a second embodiment of the invention;
Figures 5.A and 5.B show respectively a cross-section view and a top view of a microelectronic chip, after a first step of the method of manufacturing the connection according to the rerouting connection alternative of the invention;
Figures 6.A and 6.B show respectively a cross-section view and a top view of a microelectronic chip, after a second step of the method of manufacturing the connection according to the rerouting connection alternative of the invention;
Figures 7.A and 7.B show respectively a cross-section view and a top view of a microelectronic chip, after a third step of the method of manufacturing the connection according to the rerouting connection alternative of the invention;

DETAILED DESCRIPTION OF THE INVENTION

Figures 3 and 4 are a detailed view of a modified connection pad according to the invention. For sake of clarity, the other elements of a whole microelectronic component as shown on Figure 1 are omitted.

The microelectronic chip 3 comprises an active face 9 positioned upside. The active face comprises the active circuit, for example memories, processor units and interconnection buses. The microelectronic chip 3 also comprises a connection pad 2 for connecting the active circuits of the active face 9 to the external "world", namely other chips or other components.

According to a first embodiment of the invention shown on Figure 3, an additional layer 11 is added on the connection pad 2. The additional layer is obtained through a growth of metallic material. This growth may be perform by known electro-less or electrolyze process. The additional layer 11 has a thickness H.
The metallic material can be Ni, Cu, Au, Pd, Pt or Ag.

According to a second embodiment of the invention shown on Figure 4, the additional layer 11 added on the connection pad 2 comprises a first sub-layer 11' and a second sub-layer 11''.
The first sub-layer 11' is attached to the connection pad 2. The second sub-layer 11'' is attached to the first sub-layer 11'.
The layers can be obtained through a growth of metallic material by known electroless metal deposition process (plating) or by electrolyze metal deposition process. The first sub-layer $11'$ and the second sub-layer $11''$ have a total thickness $H'$. The thickness $H'$ can be made substantially identical to the additional layer thickness $H$.

For example, the first sub-layer $11'$ can be made of Ni. The first sub-layer $11'$ can have a thickness of some $\mu$m. The second sub-layer $11''$ can be made of Au, Pd, Pt or Ag. The second sub-layer $11''$ can be a thin layer acting as a protection layer with regards to oxidation. This second sub-layer $11''$ enables to perform a better wire bonding.

In both embodiments, after the layer(s) deposition, a ball 1 of metallic material is formed and thermo-sonic bonded on the top surface of the layer. In particular, a ball 1 is respectively bonded on the additional layer 11 of the first embodiment, and on the second sub-layer 11'' of the second embodiment.

After the ball formation and bonding step, the standard wire 8 bonding process continues as usual. The subsequent steps were already described in the background section above.

In both embodiments the thickness $H$ or $H'$ is chosen so as to protect the active surface 9 of the chip from the ball formation and bonding. Advantageously, the thickness may vary from $5\mu$m to $10\mu$m. However, higher thickness and lower thickness can be implemented as soon as the active surface does not come in contact with the ball 1.

Figures 5.A to 7.B schematically illustrate the method of manufacturing the electrical connection according to an alternative of the invention. This alternative consists in adding at least one additional layer on the connection pad and creating rerouting connection pad.

Figure 5.A is a cross-section view along line AA of Figure 5.B. Figure 5.B is a top view of a microelectronic chip. According to a first step of the manufacturing process, a microelectronic chip is obtained. The microelectronic chip 13 comprises an active face. The active face comprises the active circuit and connection pads 2A and 2B for connecting the active circuit of the active face to
external components. The active face is protected by a passivation layer 15 of soft or hard like organic or oxide material, while letting an opening for each connection pad.

Figure 6.A - left side is a cross-section view along line AA of Figure 6.B. Figure 6.A - right side is a cross-section view along line BB of Figure 6.B.

Figure 6.B is a top view of a microelectronic chip.
During a second step of the manufacturing method, an additional layer is added on the connection pad 2A and on some part of the passivation layer 15. The additional layer constitutes a rerouting pad 11A. The rerouting pad has a first part with a width substantially equal to the initial pad 2A size and a second part which constitutes an enlarged pad.
Similarly, another additional layer constitutes a rerouting pad 11B.
Both rerouting pads 11A and 11B are obtained for example by known sputtering or metal evaporation process. The rerouting pads 11A and 11B define new paths and new connection pad areas which are compatible in term of surface with the wire bonding process.
Alternatively, the additional layer can be constituted of two sub-layers (not shown) as previously described. A first sub-layer of some \( \mu m \) (for example 5\( \mu m \)) is covered by a thin second sub-layer (for example 0,2 \( \mu m \)).
Additionally, a passivation layer can be coated on the whole surface for protecting the under-layer while letting an opening over each new pad area. The passivation layer can be coated by known spin coating, sputtering or pressure enhanced chemical vapor deposition process.

Figure 7.A - left side is a cross-section view along line AA of Figure 7.B. Figure 7.A - right side is a cross-section view along line BB of Figure 7.B.

Figure 7.B is a top view of a microelectronic chip.
During a third step of the manufacturing method, a ball 1A and 1B of metallic material is formed and thermo-sonic bonded on the top surface of the rerouting pads 11A and 11B respectively.
After the ball formation and bonding step, the standard wire 8 bonding process continues as usual. The subsequent steps were described above and will not be further described.
Figures 8.A, 8.B and 8.C are cross-section views of a complex microelectronic chip according to another embodiment of the invention. According to this so-called "3 dimensions interconnection" embodiment, an additional microelectronic chip 23 or 33 is stacked onto the microelectronic chip 3. Figure 8.A shows the connection to a first microelectronic chip 3. Figure 8.B shows the connection to a second microelectronic chip 23. Figure 8.C shows the stacking of an additional microelectronic chip 33 of smaller dimension than the first microelectronic chip 3 with a rerouting pad 2D. Alternatively, a complex microelectronic chip may comprise a combination of connections (not shown) to a first microelectronic chip 3 and to the second microelectronic chip 23 and/or 33.

In Figure 8.A, the microelectronic chip 3 comprises an active face 9 positioned upside. The active face comprises the active circuit. The microelectronic chip 3 also comprises a connection pad 2 for connecting the active circuits of the active face 9 to the external chips or external components.

The complex microelectronic chip comprises an additional die or wafer 23 coupled to the microelectronic chip 3 via an interface layer 21. The interface layer can be for example an organic glue.

A cavity 22 is etched into the additional die 23 so as to open the way to the connection pad 2.

According to this embodiment of the invention, an additional layer 11 is added on the connection pad 2. The additional layer is obtained through a growth of metallic material. This growth may be performed by known electro-less or electrolyze process. The metallic material can be Ni, Cu, Au, Pd, Pt or Ag.

After the layer deposition, a ball 1 of metallic material is formed and thermo-sonic bonded on the top surface of the layer. After the ball formation and bonding step, the standard wire 8 bonding process continues as usual.

A passivation layer (not shown) may be added so as to avoid possible electrical contact between the die 23 and the connection during the growth (short circuit).

In Figure 8.B, the first microelectronic chip 3 comprises an active face 9 positioned upside, while the second microelectronic chip 23 comprises an active face 29 positioned downside. The active face of both circuits comprises the active circuit. The
microelectronic chip 23 comprises a connection pad 2C for connecting the active circuits of the active face 29 to the external chips or external components. The first microelectronic chip 3 is coupled to the second microelectronic chip 23 via an interface layer 21. The interface layer 21 is made for example of an organic glue.

A cavity 22 is etched into the second microelectronic chip 23 so as to open the way to the connection pad 2C. An additional layer 11 is added on the connection pad 2C. The additional layer is obtained through a growth of metallic material (growth is made via electro-less or electrolyze process).

After the layer deposition, a ball 1 of metallic material is formed and thermo-sonic bonded on the top surface of the layer. After the ball formation and bonding step, the standard wire 8 bonding process continues as usual. A passivation layer (not shown) may be added so as to avoid possible electrical contact between the microelectronic chip 23 and the connection during the growth (short circuit).

Thus, the invention enables to make contact to deep active surface or underneath layer, in particular from the back side of the chip. Also, such complex electrical contact can be made with standard manufacturing equipment.

In Figure 8.C, the first microelectronic chip 3 comprises an active face 9 positioned upside, while a second microelectronic chip of smaller size 33 comprises an active face 39 positioned downside. The active face of both circuits comprises the active circuit. The microelectronic chip 33 comprises a rerouting connection pad 2D for connecting the active circuits of the active face 39 to the external chips or external components.

The first microelectronic chip 3 is coupled to the second microelectronic chip 33 via an interface layer 21. The interface layer 21 is made for example of an organic glue. The connection pad 2D constitutes a new connection path that extends outwards of the area where the first and second microelectronic chip are coupled together. The rerouting connection pad 2D defines a new connection pad area above the first microelectronic chip 3 enabling to connect the active face 39 of the second microelectronic chip of smaller size 33.
An additional layer 11 is added on the connection pad 2D. The additional layer is obtained through a growth of metallic material (growth is made via electro-less or electrolyze process). After the layer deposition, a ball 1 of metallic material is formed and thermo-sonic bonded on the top surface of the layer. After the ball formation and bonding step, the standard wire 8 bonding process continues as usual. A passivation layer (not shown) may be added so as to avoid possible electrical contact between the microelectronic chip 33 and the connection during the growth (short circuit). Thus, the invention enables to make contact to complex chip structure while avoiding any damaging during the wire bonding connection process.

A complex microelectronic chip combining the connections to the active face of respectively the first microelectronic chip and the second microelectronic as described in relation with Figure 8.A, 8.B and 8.C can also be implemented.

Further, the additional layer 11 can be made of two sub-layers as described in the second embodiment here above.

With the electrical connection of the invention, whatever the embodiment or the microelectronic chip complexity, it is possible to connect narrow connection pads using the standard wire bonding process on:
- fragile, brittle or soft surfaces that are typically not able to support the bonding force and temperature, or
- surfaces that do not have enough metal thickness to create a mechanically and electrically satisfactory bonding.
CLAIMS

1. A method of manufacturing an electrical connection for a microelectronic chip, the microelectronic chip (3, 13, 23, 33) comprises at least one connection pad of reduced size (2, 2A, 2B, 2C, 2D), wherein the method of manufacturing comprises the steps of:
   - adding an additional layer (11, 11', 11", 11A, 11B) on the at least one connection pad,
   - bonding a wire (8) on the additional layer.

2. A method of manufacturing an electrical connection for a microelectronic chip according to previous claim, wherein the step of bonding a wire on the additional layer comprises the further step of forming a ball (1, 1A, 1B) of metallic material on the additional layer (11, 11', 11", 11A, 11B).

3. A method of manufacturing an electrical connection for a microelectronic chip according to previous claim, wherein the wire (8) is thermo-sonic bonded on the additional layer (11, 11', 11", 11A, 11B).

4. A method of manufacturing an electrical connection for a microelectronic chip according to any one of the previous claims, wherein the additional layer (11, 11A, 11B) comprises a first sub-layer (11') and a second sub-layer (11"), the first sub-layer being attached to the connection pad (2, 2A, 2B, 2C, 2D), at least one of the sub-layers is made of a metallic material deposited by electro-less metal deposition process.

5. A method of manufacturing an electrical connection for a microelectronic chip according to any one of the claims 1 to 3, wherein the additional layer (11, 11A, 11B) comprises a first sub-layer (11') and a second sub-layer (11"), the first sub-layer being attached to the connection pad (2, 2A, 2B, 2C, 2D), at least one of the sub-layers is made of a metallic material, at least one of the sub-layers is deposited by electrolyze metal deposition process.
6. A method of manufacturing an electrical connection for a microelectronic chip according to any one of the previous claims, wherein the additional layer has a thickness \((H, H')\) so as to protect an active surface \((9, 15, 29, 39)\) of the chip from the ball \((1, 1A, 1B)\) formed on the additional layer.

7. A method of manufacturing an electrical connection for a microelectronic chip according to any one of the previous claims, wherein the thickness \((H, H')\) of the additional layer ranges from \(5\mu m\) to \(10\mu m\).

8. A method of manufacturing an electrical connection for a microelectronic chip according to claim 4, wherein the metallic material is chosen among the group constituted by Ni, Cu, Au, Pd, Pt and Ag.

9. A method of manufacturing an electrical connection for a microelectronic chip according to claim 8, wherein the first sub-layer is made of Ni.

10. A method of manufacturing an electrical connection for a microelectronic chip according to claim 8, wherein the second sub-layer is made of a metallic material chosen among the group constituted by Au, Pd, Pt and Ag.

11. An electrical connection for a microelectronic chip \((3)\) comprising an active face \((9)\), the electrical connection comprises at least one connection pad \((2, 2A, 2B, 2C, 2D)\) and is characterized in that it further comprises an additional layer \((11, 11', 11'', 11A, 11B)\) added on the connection pad 2, the additional layer having a thickness \((H, H')\) so as to protect the active face \((9, 29, 39)\) of the chip \((3, 23, 33)\) from a connection ball \((1, 1A, 1B)\) formed and bonded on the additional layer \((11, 11', 11'', 11A, 11B)\).
**INTERNATIONAL SEARCH REPORT**

### A. CLASSIFICATION OF SUBJECT MATTER
- **IPC 7**: H01L 23/485, H01L 21/603

According to International Patent Classification (IPC) or to both national classification and IPC

### B. FIELDS SEARCHED
- **Minimum documentation searched (classification system followed by classification symbols)**
  - IPC 7: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
- EPO-Internal, WPI Data

### C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>column 2, line 2 - line 19</td>
<td></td>
</tr>
<tr>
<td></td>
<td>column 3, line 24 - column 4, line 51 figure 4</td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>-----</td>
<td>4, 5</td>
</tr>
<tr>
<td>X</td>
<td>US 4 908 685 A (SHIBASAKI ICHIRO ET AL) 13 March 1990 (1990-03-13) column 3, line 6 - line 27</td>
<td>1, 4-10</td>
</tr>
<tr>
<td></td>
<td>column 4, line 26 - line 31</td>
<td></td>
</tr>
<tr>
<td></td>
<td>column 6, line 27 - line 45</td>
<td></td>
</tr>
<tr>
<td></td>
<td>figure 1</td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>-----</td>
<td>2, 3, 11</td>
</tr>
</tbody>
</table>

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents:
  - "**A**" document defining the general state of the art which is not considered to be of particular relevance.
  - "**E**" earlier document but published on or after the international filing date.
  - "**L**" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified).
  - "**O**" document referring to an oral disclosure, use, exhibition or other means.
  - "**P**" document published prior to the international filing date but later than the priority date claimed.

- "**T**" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention.
- "**X**" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone.
- "**Y**" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- "**Z**" document member of the same patent family.

**Date of the actual completion of the international search**

24 September 2004

**Date of mailing of the international search report**

11/10/2004

**Name and mailing address of the ISA**

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx: 31 651 epo nl,
Pax. (+31-70) 340-3016

**Authorized officer**

Morena, E
<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>US 6 144 100 A (BUCKSCH WALTER ET AL) 7 November 2000 (2000-11-07) abstract</td>
<td>1,4-6, 8-10</td>
</tr>
<tr>
<td></td>
<td>column 1, line 24 - line 57 column 2, line 47 - column 3, line 30 column 4,</td>
<td></td>
</tr>
<tr>
<td></td>
<td>line 28 - line 45 figures 3c,4</td>
<td></td>
</tr>
<tr>
<td>A</td>
<td></td>
<td>2,7,11</td>
</tr>
<tr>
<td>X</td>
<td>US 6 506 672 B1 (MERRITT SCOTT A ET AL) 14 January 2003 (2003-01-14) abstract</td>
<td>1,2,4, 7-10</td>
</tr>
<tr>
<td></td>
<td>column 5, line 62 - column 6, line 26 column 8, line 50 - line 66 column 9,</td>
<td></td>
</tr>
<tr>
<td></td>
<td>line 44 - column 10, line 6 column 10, line 47 - line 65 column 12, line 14</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- line 24 figures 7,9</td>
<td></td>
</tr>
<tr>
<td>A</td>
<td></td>
<td>6,11</td>
</tr>
<tr>
<td></td>
<td>'0002!, '0007! paragraphs '0021! - '0027!, '0031! figure 4</td>
<td></td>
</tr>
<tr>
<td>Patent document cited in search report</td>
<td>Publication date</td>
<td>Patent family member(s)</td>
</tr>
<tr>
<td>---------------------------------------</td>
<td>-----------------</td>
<td>-------------------------</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 4082183 B</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 63148646 A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CN 87107402 A ,B</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DE 3787709 D1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DE 3787709 T2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>KR 9100757 B1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>US 5060051 A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 4062474 B</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 61256776 A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 1771517 C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 4062475 B</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 61256777 A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 1780467 C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 4071351 B</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 61269386 A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DE 3590792 T</td>
</tr>
<tr>
<td></td>
<td></td>
<td>WO 8606878 A1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NL 85201325 A ,B</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NL 8520325 T</td>
</tr>
</tbody>
</table>

Form PCT/ISA/210 (patent family annex) (January 2004)