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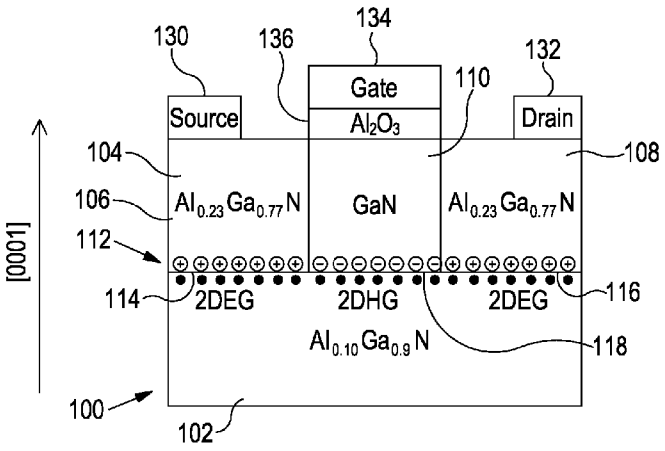

Fig. 1

(57) Abstract: A normally-off transistor comprising a first layer (102) of semiconductor material, a second layer (104) of semiconductor material comprising first (106) and second (108) regions and a third region (110) between the first and second region, a source electrode (130) connected to the first region (104) and a drain electrode (132) connected to the second region (108), and a gate electrode (134) located over the third region (110), wherein the first (104) and second (108) regions are of a material arranged to form a polarization having a first polarity at the interface (114, 116) between the first and second regions and the first semiconductor layer (102), and the third region (110) is of a material arranged to form a polarization having a second polarity opposite to the first polarity at the interface (118) between the third region and the first semiconductor layer of opposite polarity.

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Normally-off Transistors

Field of the Invention

The present invention relates to gallium nitride (GaN) based transistors, and in particular to power transistors.

Background to the Invention

The superior material properties of GaN offer substantial performance improvement over the ubiquitous Silicon based devices for many applications, in particular next-generation advanced power electronics. Conventional high performance GaN transistors are "normally-on". As well as the efficiency limitations of normally-on transistors, they are not suitable for most of the power electronic applications because they are not failsafe. The "normally-on" transistors also require extremely complex gate drive circuits which negatively impacts on system efficiency and size. There is a need to address these key issues to enable GaN transistors to find widespread acceptance across all application segments.

The "normally-off" feature in GaN transistors is typically enabled by a series connection with a conventional "normally-off" silicon transistor; however the performance is limited by the silicon based device in this configuration. A few techniques such as gate recess etching, fluorine implantation, and selective area re-growth can enable development of GaN "normally-off" transistors. However, these techniques suffer from low/insufficient control voltages, non-uniformity, thermal instability and material crystallographic damage that impact device performance, rendering them inadequate for practical power electronic applications.

Summary of the Invention

The present invention provides a normally-off transistor comprising a first layer of semiconductor material, a second layer of semiconductor material comprising first and second regions and a third region between the first and second regions, a source electrode connected to the first region and a drain electrode connected to the second region, and a gate electrode located over the third region, wherein the first and second regions are of a material arranged to form a polarization having a first polarity at the interface between the first and second regions and the first semiconductor layer, and the third region is of a material arranged to form a polarization having a second

polarity opposite to the first polarity at the interface between the third region and the first semiconductor layer of opposite polarity.

The polarization in each of the regions may be arranged to form a carrier gas. The carriers in the carrier gas of the first and second interface regions may be of opposite charge to those in the carrier gas of the third interface region. For example the carrier gas of the first and second interface regions may be an electron gas, and that of the third interface region may be a hole gas, or vice versa.

In this arrangement the gate potential may be variable to invert the polarity of the region in the proximity of the interface between the third region and the first semiconductor layer thereby to turn the transistor on.

The gate electrode may be separated from the third region by an insulating layer, which may be a metal oxide such as aluminium oxide.

The first and second layers may be formed of group III nitride materials. The metal content of the first layer and the three regions of the second layer may be selected so as to provide the polarization.

The first layer may be of AlGaN having the composition $Al_xGa_{(1-x)}N$, the first and second regions of the second layer may be AlGaN having the composition $Al_yGa_{(1-y)}N$, and the third region of the second layer may be AlGaN having the composition $Al_zGa_{(1-z)}N$.

The values of x, y and z may be such that $0<x<1$, $0<y<1$ and $0 \leqq z<1$.

The values of x, y and z may be such that $z<x<y$. The value of z may be zero such that the third region is of GaN.

Alternatively the values of x, y and z may be such that $y<x<z$. The value of y may be zero such that the first and second regions are of GaN.

One of the first and second regions of the second layer may have a further, third, semiconductor layer formed thereon. The third layer may be of a material such that, at

the interface between the third layer and the second layer, polarization occurs which forms a carrier gas at the interface. This third layer, together with the first and second layers, may form a double heterostructure. The carrier gas at this upper interface may be of the opposite charge to that formed at the lower interface between the first semiconductor layer and the first and second regions of the second semiconductor layer. A further electrode may be formed on, or otherwise connected to, the further semiconductor layer, which may form a base electrode. The base electrode may be electrically connected to the gate electrode or the source electrode. The composition of the third layer may be of the same general composition, and it may have the same, or a different, level of doping, as the third region of the second layer.

The first semiconductor layer may include a region below the third layer which is of a different composition to the rest of the first semiconductor layer. This region of the first layer may also be of the general composition $Al_xGa_{(1-x)}N$. The composition of the third layer may be of the same general composition, and it may have the same, or different levels of doping, as the third region of the second layer. The values of x for the third layer and this region of the first layer may be the same. The value of x for this region may still meet the relationship $x<y$. For example x may be zero such that this region of the first layer is GaN.

The system may further comprise any one or more features, in any combination, of the preferred embodiments which are shown in the accompanying drawings, as will now be described.

Brief Description of the Drawings

Figure 1 is a schematic diagram of a transistor according to an embodiment of the invention;

Figure 2 is a further diagram of the transistor of Figure 1 showing the dimensions used in a simulation of the transistor;

Figure 3 is a diagram of electron concentration in the transistor of Figure 2;

Figure 4 is a diagram of hole concentration in the transistor of Figure 2;

Figure 5 shows the transfer characteristics of the transistor of Figure 2;

Figure 6 shows the output characteristics of the transistor of Figure 2;

Figure 7 shows the off-state breakdown characteristics of the transistor of Figure 2;

Figure 8a shows the electric field distribution in the transistor of Figure 2;

Figure 8b shows the electric field profile in the transistor of Figure 2 along the dashed line in Figure 8a;

Figure 9 is a diagram of a PSJ HFET according to a further embodiment of the invention;

Figure 10 shows the electron concentration in the HFET of Figure 9;

Figure 11 shows the hole concentration in the HFET of Figure 9;

Figure 12 shows the transfer characteristic of the transistor of Figure 9;

Figure 13 shows the output characteristic of the transistor of Figure 9;

Figure 14 shows the off-state breakdown characteristic of the transistor of Figure 9;

Figure 15a shows the electric field distribution in the transistor of Figure 9;

Figure 15b shows the electric field profile in the transistor of Figure 9 along the dashed line in Figure 15a;

Figures 16a and 16b show the electron concentration distribution, electron concentration profile, and electric potential profile respectively in a further embodiment of the invention which is a modification to the transistor of Figure 9;

Figure 17 shows the off-state breakdown characteristics of the transistor of Figure 16a;

Figure 18a show the electric field distribution and profile respectively in the transistor of Figure 16a;

Figure 18b shows the electric field profile in the transistor of Figure 16a along the dashed line in Figure 18a;

Figure 19 is a diagram of a transistor according to a further embodiment of the invention;

Figure 20 is a diagram of electron concentration in the transistor of Figure 19;

Figure 21 is a diagram of hole concentration in the transistor of Figure 19;

Figure 22 shows the transfer characteristic of the transistor of Figure 19;

Figure 23 shows the output characteristic of the transistor of Figure 19;

Figures 24a and 24b show the electron concentration distribution, electron concentration profile, and electric potential profile respectively in a further embodiment of the invention which is a modification to the transistor of Figure 19;

Figure 25 shows the off-state breakdown characteristic of the transistor of Figure 19;

Figure 26a shows the electric field distribution in the transistor of Figure 19; and

Figure 26b shows the electric field profile in the transistor of Figure 19 along the dashed line in Figure 26a.

Description of the Preferred Embodiments

Referring to Figure 1, a transistor 100 comprises a first semiconductor layer 102 and a second semiconductor layer 104. The second semiconductor layer 104 is formed of first and second regions 106, 108, and a third region 110 which is between the first and second regions. The first and second regions 106, 108 are each in contact with the third region 110 so that the second layer is continuous though the semiconductor materials making up the different regions may be different. The interface 112 between the first 102 and second 104 layers is therefore also in three regions, a first interface region 114 between the first semiconductor layer 102 and the first region 106 of the second layer, a second interface region 116 between the first semiconductor layer 102 and the second region 108 of the second layer, and a third interface region 118 between the first semiconductor layer 102 and the third region 110 of the second layer. The top of the first layer 102 is in one substantially continuous plane, so that the first, second and third interface regions 114, 116, 118 together form one continuous interface in one plane. The materials of the semiconductor layers are selected so that the first and second interface regions 114, 116 have a spontaneous/piezoelectric polarization of one polarity, and the third interface region 118 has a spontaneous/piezoelectric polarization of the opposite polarity. For example, the first layer 102 may be of AlGaN having a first Al content, the first and second regions 106, 108 of the second layer may be of AlGaN having a second Al content higher than the first, and the third region 110 of the second layer may be of GaN or AlGaN having an Al content lower than the first. This may result in the first and second interface regions having a polarization which forms a 2DEG in the first layer 102 and a 2DHG in the second layer 104 and the third interface region having a polarization which forms a 2DHG in the first layer 102 and a 1DEG in the second layer.

A first electrode 130 may be formed on, or otherwise connected to, the first region 106 of the upper layer 104. A second electrode 132 may be formed on, or otherwise connected to, the second region 108 of the upper layer. These electrodes may be metal, such as titanium or aluminium, and arranged to form an Ohmic contact with the semiconductor material. This allows the first and second electrodes 130, 132 to form a source and drain of the transistor. A third electrode 134 may be formed over the third region 108 of the upper layer. A layer of insulator material 136 may be provided between the third electrode 134 and the semiconductor material 110, so that

the third electrode 134 can form a gate electrode, the electrical potential of which will affect the polarity of the region in the proximity of the third interface region 118, thereby affecting the flow of current between the source 130 and drain 132.

Generalising the composition of the first and second layers, the first layer 102 may be of AlGaN having the composition $Al_xGa_{(1-x)}N$, the first and second regions 106, 108 of the second layer may be AlGaN having the composition $Al_yGa_{(1-y)}N$, and the third region of the second layer may be AlGaN having the composition $Al_zGa_{(1-z)}N$. The values of x, y and z may be such that $z<x<y$. The value of z may be zero such that the third region is of GaN. In the embodiment shown in Figure 1, the value of z is zero, the value of x is 0.10 and the value of y is 0.23.

The first AlGaN layer 102 is arranged with the [0001] crystal orientation in the upward direction towards its top surface which is therefore in the c-plane. The second layer 104 is grown on that top surface so that the top surface forms the interface 112 between the first and second layers 102, 104.

Where $Al_{0.23}Ga_{0.77}N$ (aluminium content = 23%) of the first and second regions 106, 108 of the second layer is grown on the $Al_{0.10}Ga_{0.90}N$ (aluminium content = 10%) of the first layer 102 along the [0001] crystal orientation, the first and second interface regions 114, 116 develop positive polarisation charges in conjunction with a two dimensional electron gas (2DEG) accumulation. When GaN of the third region 110 of the second layer is grown on the $Al_{0.10}Ga_{0.90}N$ of the first layer, the third interface region 118 develops negative polarisation charges in conjunction with a two dimensional hole gas (2DHG) accumulation. The whole of the interface 112 forms a polarization layer with carriers that form the channel of the device, but the presence of holes in the 2DHG under the gate disrupts the conduction path from drain 132 to the source 130, making the device normally-off. Therefore, an application of a positive gate voltage to the gate 134 is required to invert the polarity of the region under the gate 134 to establish a continuous 2D carrier gas, in this case a 2DEG, along the path of conduction from the drain 132 to the source 130. The threshold voltage is determined by the thickness of the gate-insulator 136 and the 2DHG density.

As well as the aluminium content, carrier accumulation and concentration in the 2DEG and 2DHG will further depend on the thickness of the semiconductor layers.

For example, in AlGaN/GaN heterostructures such as those of Figure 1, for an Aluminium content of 23%, the minimum AlGaN thickness (referred to as the Critical thickness) has to be ~ 5 nm, before 2DEG accumulation takes place at the interface). As the Al content increases, the critical thickness decreases.

It will be appreciated that the architecture of the device of Figure 1 is that of an n-channel Metal-Insulator-Semiconductor Heterostructure Field Effect Transistor (MIS-HFET) with Al_2O_3 as the Gate insulator 136. The normally-off feature is achieved through a combination of polarisation engineering and selective area growth (SAG).

As an alternative to the n-channel device of Figure 1, the semiconductor materials can be selected so as to form a p-channel device. For example, in a device similar to that of Figure 1, the values of x, y and z may be such that $y<x<z$. The value of y may be zero such that the first and second regions are of GaN. This arrangement results in a device similar to that of Figure 1, but with a 2DHG formed under the first and second regions of the top layer and a 2DEG below the third region.

Referring to Figure 2, detailed TCAD simulations were performed to study this architecture using Silvaco ATLAS. The physical models included for simulation of the on-state characteristics were – POLAR (Spontaneous Polarisation), CALC.STRAIN (Piezoelectric Polarisation), SRH (Shockley-Read-Hall, carrier generation-recombination), and ALBRCT.N to model electron mobility (SILVACO ATLAS, TCAD Examples - GANFET [Online]. Available: http://www.silvaco.com/examples/tcad/section21/example3/index.html.)

The simulated structure is shown in Figure 2, with each feature corresponding to a feature in Figure 1 being indicated by the same reference numeral as in Figure 1. The width of the device (perpendicular to the plane of Figure 2) was set as 1 mm. The III-V nitride layers were defined as undoped. The thickness of Gate insulator Al_2O_3 136 was defined as 10 nm. Thickness of the $Al_{0.23}Ga_{0.77}N$ layers 104, 108 as well as the GaN layers 110 was set as 20 nm. Electron and hole distribution within the device structure at thermal equilibrium are shown in Figures 3 and 4 respectively. The simulated transfer and output characteristics have been shown in Figures 5 and 6 respectively. The simulated value of the threshold voltage (VTH) obtained is about 3.5 V, which is in the desired range for most high voltage power electronic applications.

Electrical characteristics were also simulated under off-state conditions. The physical models included for simulation of the off-state characteristics were – POLAR (Spontaneous Polarisation), CALC.STRAIN (Piezoelectric Polarisation), SRH (Shockley-Read-Hall, carrier generation-recombination), FERMI (Fermi-Dirac statistics), FLDMOB to model field dependent electron mobility, and IMPACT SELB (Selberherr impact ionisation model for simulating avalanche breakdown)(SILVACO ATLAS, TCAD Examples - GANFET [Online]. Available: http://www.silvaco.com/examples/tcad/section21/example2/index.html.). Equal impact ionisation co-efficients/parameters were assumed for GaN and AlGaN regions in the model.

As can be seen in Figures 8a and 8b, there is substantial electric field crowding at the Drain-side edge of the Gate and the device enters the breakdown regime at a drain-source voltage V_{DS} ~ 50 V, as can be inferred from Figure 7 and Figures 8a and 8b (Critical electric field for GaN is ~ 3 MV/cm). The behaviour is as expected for lateral devices without field modulating schemes.

Referring to Figure 9, which shows another embodiment of the invention, and in which features corresponding to those in Figure 2 are shown by the same reference numerals increased by 100, the device may comprise a first semiconductor layer 202 of AlGaN and a second semiconductor layer 204 made up of three regions 206, 208, 210. The compositions of the first layer 202 and of the first, second and third regions 206, 208, 210 of the second region may be the same as the corresponding parts of the embodiment of Figure 2. These may therefore form a heterointerface 212 between the first 202 and second 204 layer with a polarization layer having opposite polarity under the third region 210 of the second layer. An insulating layer 236 and gate 234 may be formed on the third GaN region 210 of the second layer 204. The second region 208 of the second layer 204, which may be of AlGaN, may have a thickened area 204a. A p-GaN layer 240 may be formed on part of the second region 208 of the second layer 204, for example on the thickened area 204a, and a further electrode 242 may be formed on the p-GaN layer 240. The electrode 242 may form a base electrode. The p-GaN layer 240 may be spaced apart from the third region 210 of the first layer and from the drain electrode 232.

A second heterointerface 244 may be formed between the second region 208 of the second layer 204 and the p-GaN layer 240. This heterointerface 244 may form a polarization layer having the opposite polarity to that between the second region 208 of the second layer and the first layer 202, e.g. it may form a 2DHG over the part of the 2DEG which is formed at the second interface region 216. The area of the second heterointerface 244, and the corresponding area of the second region 208 of the second layer 204, may form an area of double heterointerface, or polarization super junction, in which the two interfaces 216, 244 have carrier gases of opposite charge. This area of double heterointerface may be between the gate electrode and the drain electrode. Therefore the electrical voltage applied to the base electrode 242 may be used to cause depletion of the carriers in the area of the double heterointerface. This may be used to increase the breakdown voltage of the device.

The device may therefore have the structure of polarization super junction (PSJ) HFET. It may consist in general terms of an undoped GaN/AlGaN/GaN double-heterostructure with a p-GaN third layer 240. This double heterostructure may be over an area between, and space apart from, the gate electrode 234 and the drain electrode 232. The 'GaN' may more generally comprise AlGaN with a lower Al content than the 'AlGaN' layer. The PSJ HFET may have four electrodes namely: gate 234, drain 232, source 230, and base 242. The drain 232 and source 230 electrodes may form ohmic contacts to the 2DEG and the gate 234 may be formed through a Schottky contact. The basic differences between conventional HFETs and the PSJ HFET of Figure 9 are the additional base electrode 242 and the presence of the 2DHG induced by negative polarisation charge at the upper GaN/AlGaN heterointerface. The base 242 may make an ohmic contact to the 2DHG through the top p-GaN layer 240 and can be electrically connected to the gate 234 or source 230. In the on-state, with an applied drain bias, current flows from the drain 232 to source 230 through the 2DEG as in conventional HFETs. The device of Figure 9 is a normally off device and functions in the same way as the device of Figure 1. However, in the off state, with a further increase in drain voltage, the drift region below the p-GaN layer is fully depleted maintaining charge balance between the intrinsic polarisation charges at the GaN/AlGaN and AlGaN/GaN interfaces, and a flat electric field distribution can be achieved.

In a simulation of the device of Figure 9, the thickness of the thickened area 204a of $Al_{0.23}Ga_{0.77}N$ under the p-GaN layer 240 was defined as 50 nm. The thickness and doping density in the p-GaN layer 240 were defined as 40 nm and 3 x 1017/cm3 respectively (assuming 1% of dopant activation when physically doped as 3 x 1019/cm3 as in a standard PSJ HFET). Base contact was defined as perfectly Ohmic and the rest of the regions were defined as described above with reference to Figure 2. Electron and hole distribution within the device structure at thermal equilibrium are shown in Figures 10 and 11 respectively. The simulated transfer and output characteristics are shown in Figures 12 and 13 respectively. The simulated value of the threshold voltage (VTH) obtained is ~ 3.5 V. Breakdown characteristics of the device are shown in Figure 14. The distribution of the electric field and its profile at VGS = 0 V and VDS = 400 V are shown in Figures 15a and 15b. There is substantial electric field crowding at the drain-side edge of the double heterostructure and the device enters the breakdown regime at VDS ~ 400 V, as can be inferred from Figure 14 and Figure 15b (Critical electric field for GaN is ~ 3 MV/cm). The non-uniform distribution of electric field can primarily be attributed to the difference in the magnitude of the polarisation charges at the top interface 244 of $GaN/Al_{0.23}Ga_{0.77}N$ and the bottom interface 216 of $Al_{0.23}Ga_{0.77}N/Al_{0.10}Ga_{0.90}N$ which leads to a condition of charge imbalance.

In a modification to the device shown in Figure 9, the p-GaN layer 240 may be replaced by a layer of p-AlGaN having same aluminium content as the first semiconductor layer 202, which may be $Al_{0.10}Ga_{0.90}N$. In this modified case the device operates in a very similar manner to that of Figure 9. Referring to Figures 16a and 16b some important aspects of the operation of this modification of the device of Figure 9 will now be described.

Firstly, the path of current conduction under on-state conditions is illustrated in Figure 18a using a dashed arrow in Figure 16a. The main region of current conduction under the Gate is along the Al_2O_3/GaN interface. This behaviour is common to all of the embodiments shown herein. Secondly, substantial depletion of electrons (by a few orders of magnitude at VGS = 10 V and VDS = 10 V) is observed under the PSJ region (double heterostructure layers), i.e. in the region of the p-GaN (or p-AlGaN) layer 240 as shown in Figure 16b. This is because a PN junction is formed by the 2DHG and 2DEG intrinsically in this region, and the PN junction essentially becomes

reverse biased under this operating condition. This leads to substantial potential drop closer to the edge of the PSJ layer as pinch-off of the conduction path occurs in this region. The Drain current saturation is determined by this phenomenon, rather than the pinch-off that occurs at the Drain-side edge of the Gate electrode in conventional lateral transistors.

The breakdown characteristics of the modified Figure 9 device are shown in Figure 17.

Distribution of the electric field and its profile at V_{GS} = 0 V and V_{DS} = 800 V in the modified Figure 9 device are shown in Figures 18a and 18b.

As shown in Figure 18b, the electric field distribution is substantially more uniform in this device architecture, which is what leads to the high breakdown voltage as shown in Figure 17, and the field profile obtained is very similar to what is obtained in conventional normally-on PSJ HFETs based on GaN/AlGaN/GaN (buffer) double heterostructures.

Referring to Figure 19, in a further modification to the device of Figure 9, the first semiconductor layer 302, rather than being uniform over substantially the whole area of the device, comprises an intermediate region of GaN below the p-GaN third layer 340. Apart from this, the modification is the same as the device of Figure 9 and corresponding parts are indicated by the same reference numerals increased by 100.

The thickness and doping density in the p-GaN layer were defined as 40 nm and 3 x 1017/cm3 respectively. In the simulated structure shown in Figure 19, a GaN/AlGaN/GaN double heterostructure, as employed in conventional “normally-on” PSJ HFETs, has been integrated with the “normally-off” device structure. The rest of the regions were defined as described above with reference to Figure 9.

Electron and hole distribution within the device of Figure 19 at thermal equilibrium are shown in Figures 20 and 21 respectively. The simulated transfer

and output characteristics are shown in Figures 22 and 23 respectively. The simulated value of the threshold voltage VTH obtained is ~ 3.5 V.

Electron distribution within the device structure at V_{GS} = 10 V and V_{DS} = 10 V is shown in Figure 24a, and the profiles of electron concentration and electrical potential at the bottom AlGaN/GaN interface are shown in Figure 24b.

As observed in the device of Figure 19, depletion of electrons (by ~ two orders of magnitude at VGS = 10 V and VDS = 10 V) is observed under the PSJ region (double heterostructure layers) as shown in Fig. 2.30 (b). However, it's not as significant in the region close to the edge of the PSJ layer. Therefore in this architecture, the Drain current saturation is primarily determined by pinch-off that occurs at the Drain-side edge of the Gate electrode.

Breakdown characteristics of the device are shown in Figure 25.

Distribution of the electric field and its profile at V_{GS} = 0 V and V_{DS} = 800 V are shown in Figures 26a and 26b. As shown in Figure 26a the electric field distribution is quite similar to what was observed in the device of Figure 9. This is a result of matched polarisation charges within the double heterostructures in both these designs

Claims

1. A normally-off transistor comprising a first layer of semiconductor material, a second layer of semiconductor material comprising first and second regions and a third region between the first and second region, a source electrode connected to the first region and a drain electrode connected to the second region, and a gate electrode located over the third region, wherein the first and second regions are of a material arranged to form a polarization having a first polarity at the interface between the first and second regions and the first semiconductor layer, and the third region is of a material arranged to form a polarization having a second polarity opposite to the first polarity at the interface between the third region and the first semiconductor layer of opposite polarity.

2. A transistor according to claim 1 wherein the polarization in each of the regions is arranged to form a carrier gas and the carriers in the carrier gas of the first and second interface regions are of opposite charge to those in the carrier gas of the third interface region.

3. A transistor according to claim 2 wherein the carrier gas of the first and second interface regions is an electron gas, and that of the third interface region is a hole gas.

4. A transistor according to any preceding claim wherein the potential of the gate electrode is variable to invert the polarity of the polarization at the interface between the third region and the first semiconductor layer thereby to turn the transistor on.

5. A transistor according to any preceding claim wherein the first and second layers are be formed of group III nitride materials, and the metal content of the first layer and the three regions of the second layer are selected so as to provide the polarization.

6. A transistor according to any preceding claim wherein the first layer is of AlGaN having the composition $Al_xGa_{(1-x)}N$, the first and second regions of the second layer are of AlGaN having the composition $Al_yGa_{(1-y)}N$, and the third region of the second layer is of AlGaN having the composition $Al_zGa_{(1-z)}N$.

7. A transistor according to claim 6 wherein the values of x, y and z are such that $z<x<y$.

8. A transistor according to claim 6 wherein the values of x, y and z are such that $y<x<z$.

9. A transistor according to any preceding claim wherein one of the first and second regions of the second layer has a further semiconductor layer formed thereon, and the further layer is of a material such that, at the interface between the further layer and the second layer polarization occurs which forms a carrier gas at the interface which is of opposite charge to that formed at the interface between the first semiconductor layer and the first and second regions of the second semiconductor layer.

10. A transistor according to claim 9 wherein a further electrode is formed on, or otherwise connected to, the further semiconductor layer.

11. A transistor according to claim 10 wherein the further electrode is electrically connected to the gate electrode or the source electrode.

12. A transistor according to any one of claims 9 to 11 wherein the first layer and the further semiconductor layer are arranged to form a double heterostructure with said part of the first or second region of the second layer of semiconductor material.

13. A transistor according to any one of claims 9 to 12 wherein the first semiconductor layer includes an intermediate region below the further semiconductor layer which is of a different composition to the rest of the first semiconductor layer.

14. A transistor according to claim 13 wherein the intermediate region of the first layer is of the general composition $Al_xGa_{(1-x)}N$.

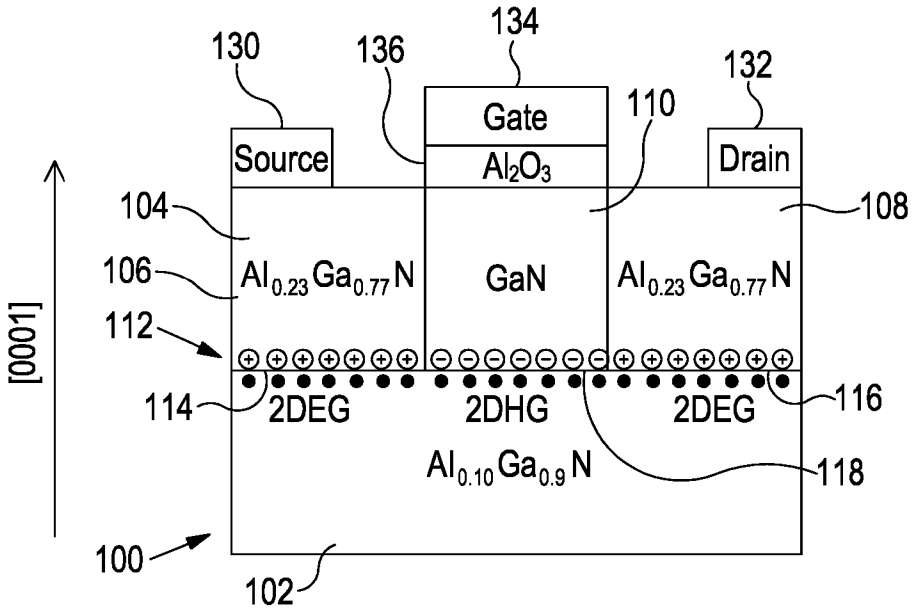
130
136
134
132
Gate
110
Source
Al_2O_3
Drain
104
108
106
$Al_{0.23}Ga_{0.77}N$
GaN
$Al_{0.23}Ga_{0.77}N$
112
[0001]
114
2DEG
2DHG
2DEG
116
$Al_{0.10}Ga_{0.9}N$
118
100
102

Fig. 1

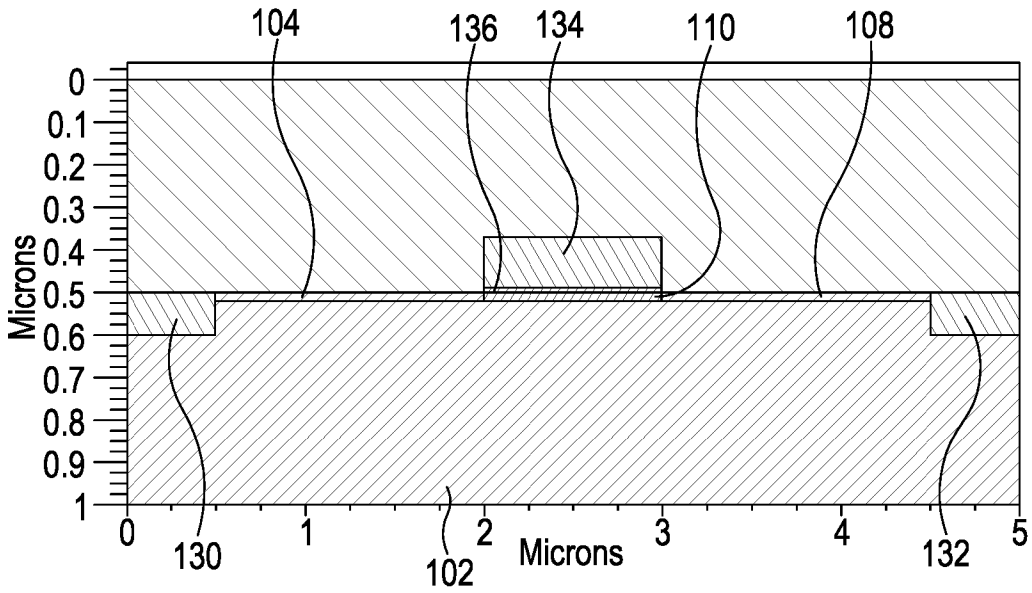
104
136
134
110
108
Microns
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0
1
2
3
4
5
Microns
130
102
132

Fig. 2

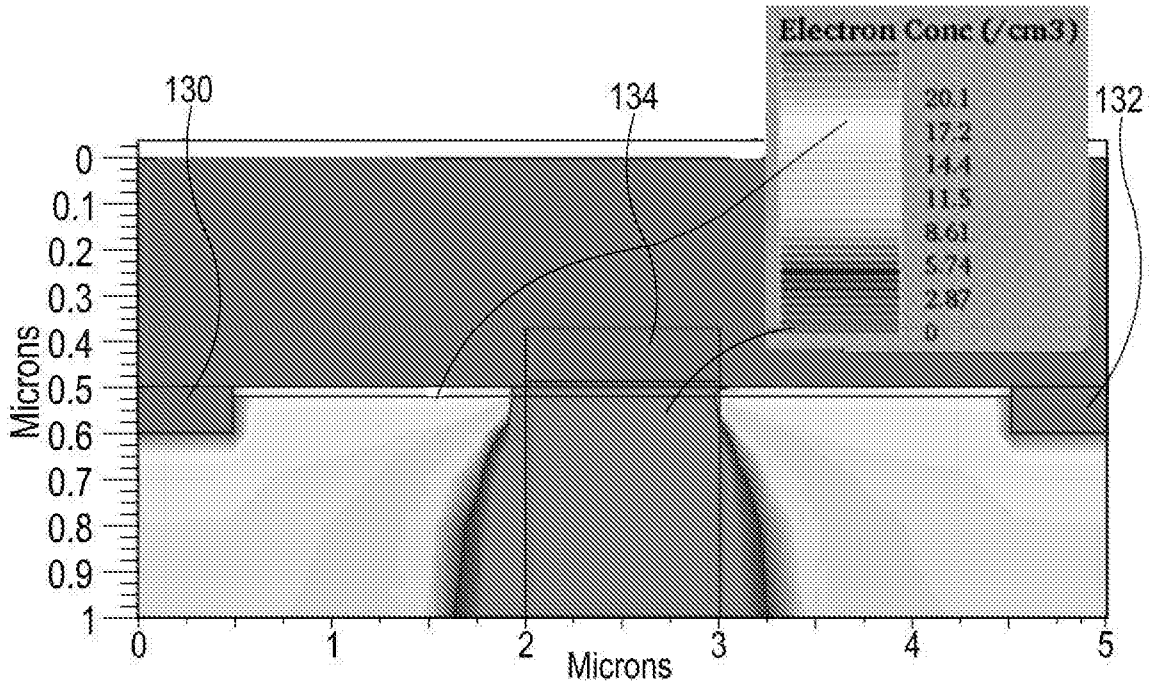
Electron Conc (/cm3)
20.1
17.2
14.4
11.5
8.61
5.74
2.87
0
130
134
132
Microns
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0
1
2
3
4
5
Microns

Fig. 3

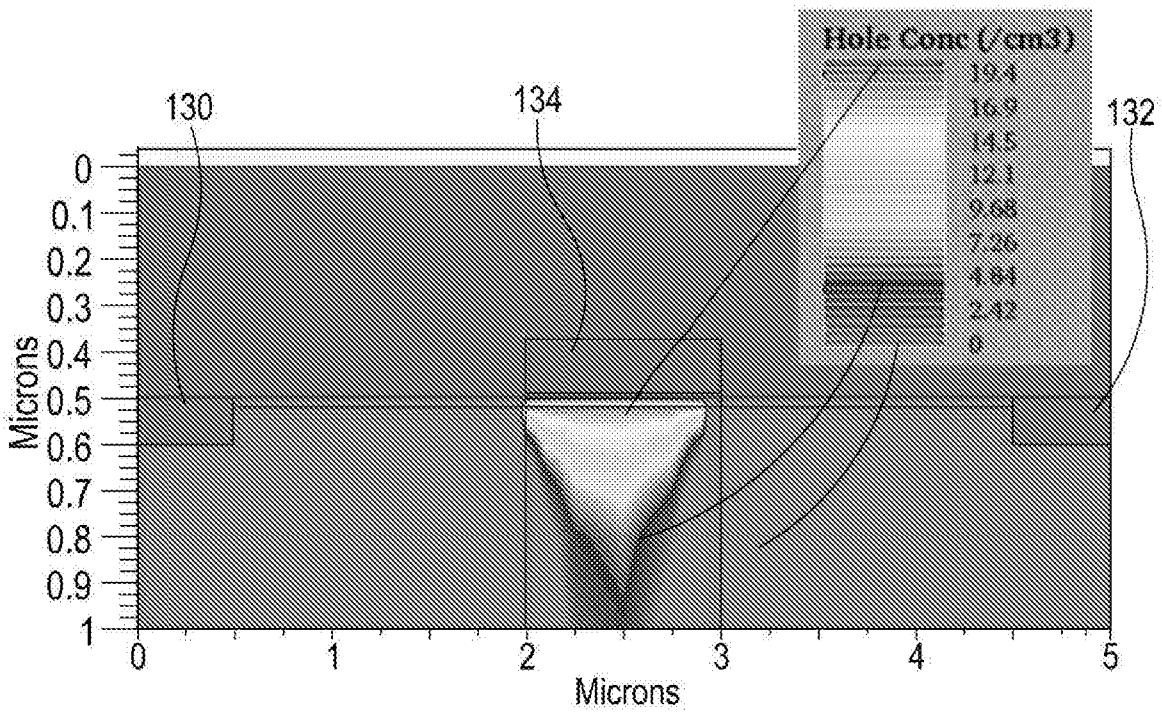
Hole Conc (/cm3)
19.4
16.9
14.5
12.1
9.68
7.26
4.84
2.42
0
130
134
132
Microns
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0
1
2
3
4
5
Microns

Fig. 4

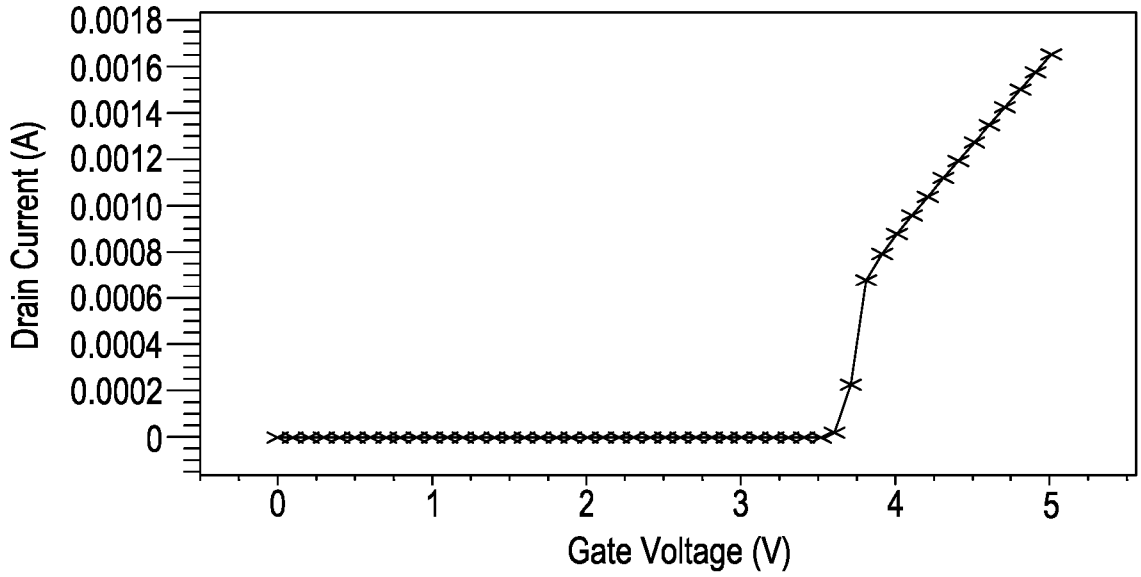
Drain Current (A)
0.0018
0.0016
0.0014
0.0012
0.0010
0.0008
0.0006
0.0004
0.0002
0
0
1
2
3
4
5
Gate Voltage (V)

Fig. 5

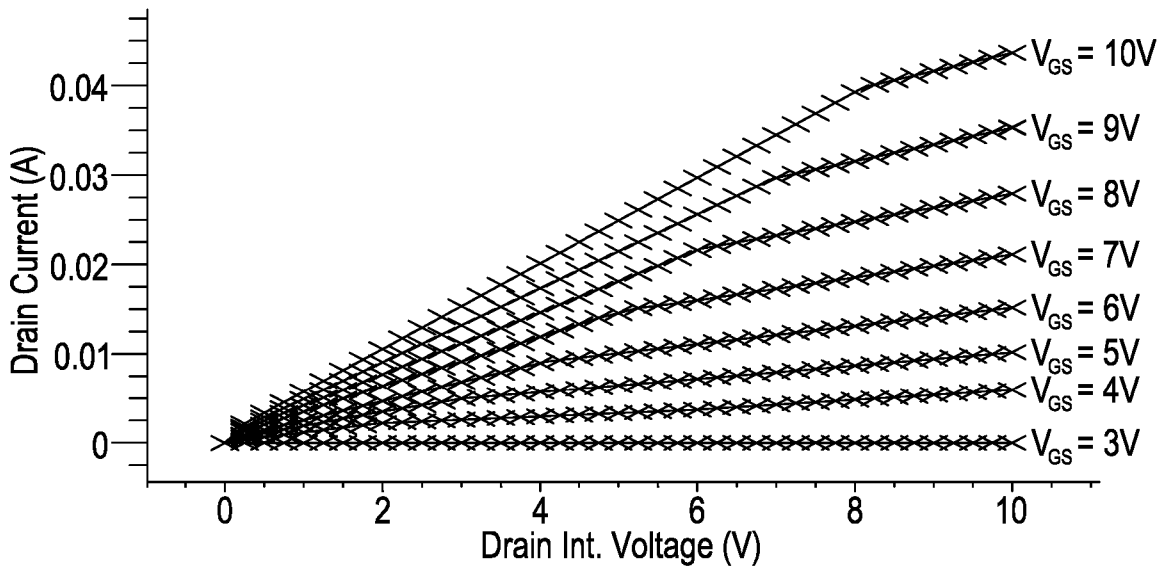
Drain Current (A)
0.04
0.03
0.02
0.01
0
0
2
4
6
8
10
Drain Int. Voltage (V)
V_{GS} = 10V
V_{GS} = 9V
V_{GS} = 8V
V_{GS} = 7V
V_{GS} = 6V
V_{GS} = 5V
V_{GS} = 4V
V_{GS} = 3V

Fig. 6

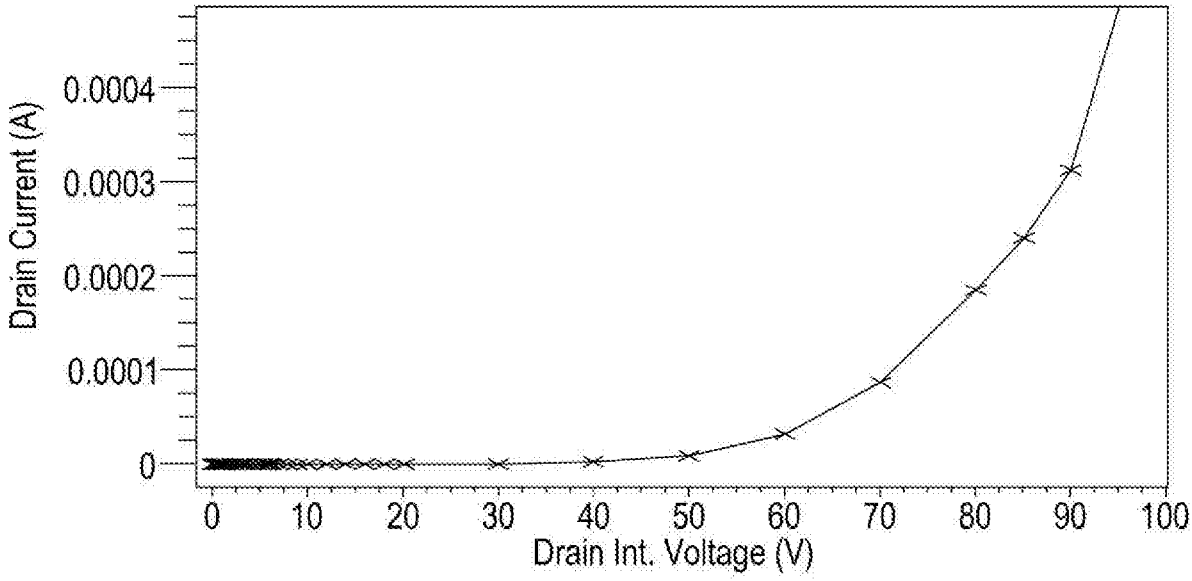

Fig. 7

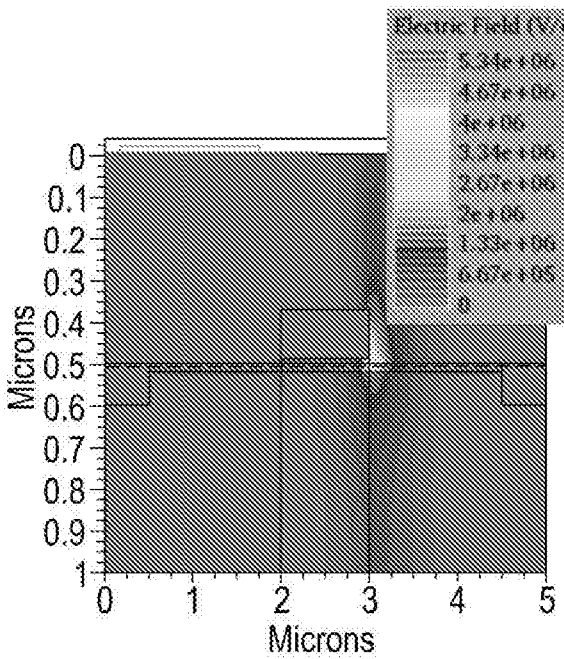

Fig. 8a

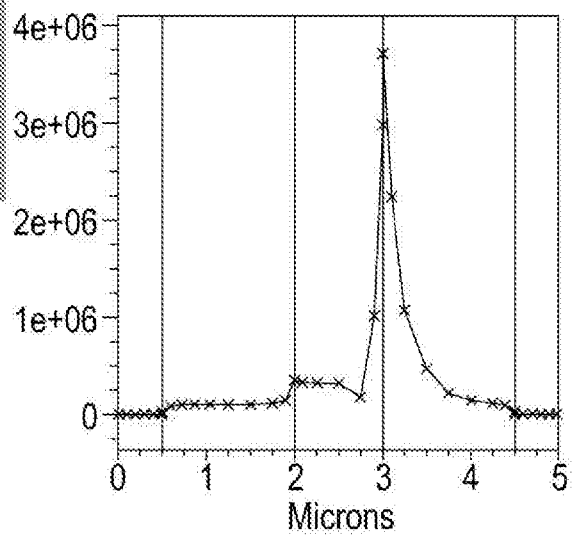

Fig. 8b

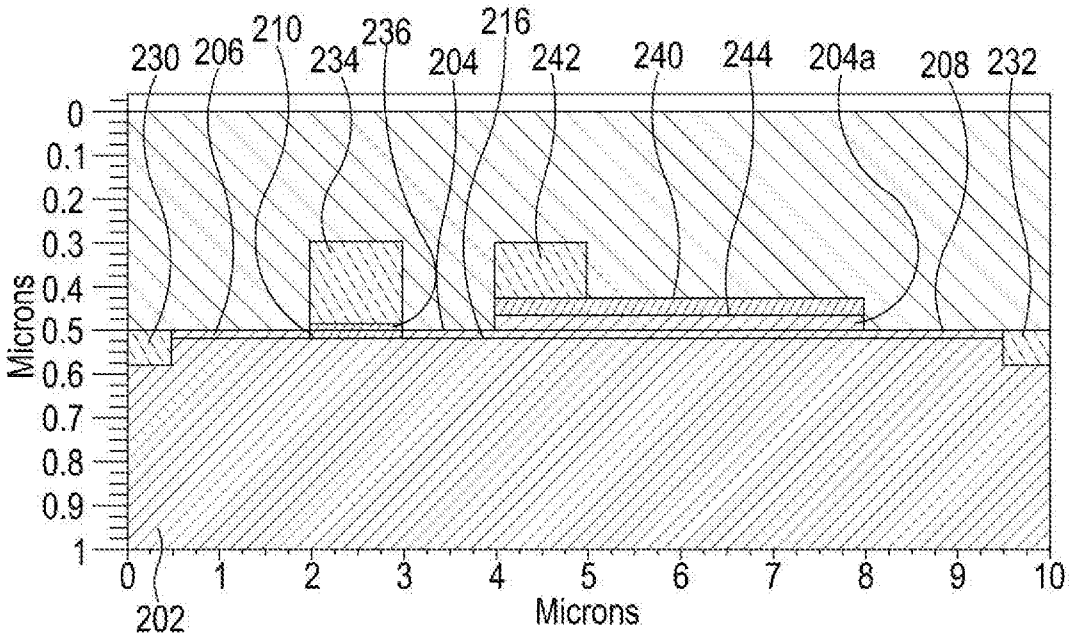
230
206
210
234
236
204
216
242
240
244
204a
208
232
202
Microns
Microns
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0
1
2
3
4
5
6
7
8
9
10

Fig. 9

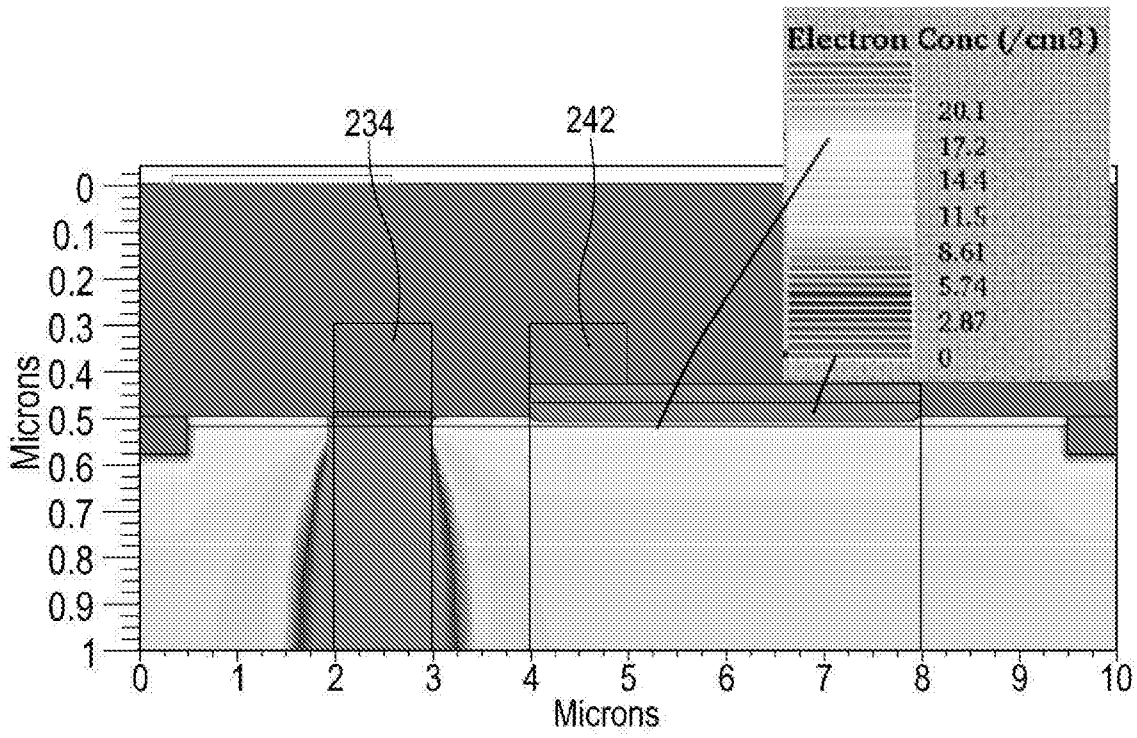
Electron Conc (/cm3)
20.1
17.2
14.4
11.5
8.61
5.74
2.87
0
234
242
Microns
Microns
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0
1
2
3
4
5
6
7
8
9
10

Fig. 10

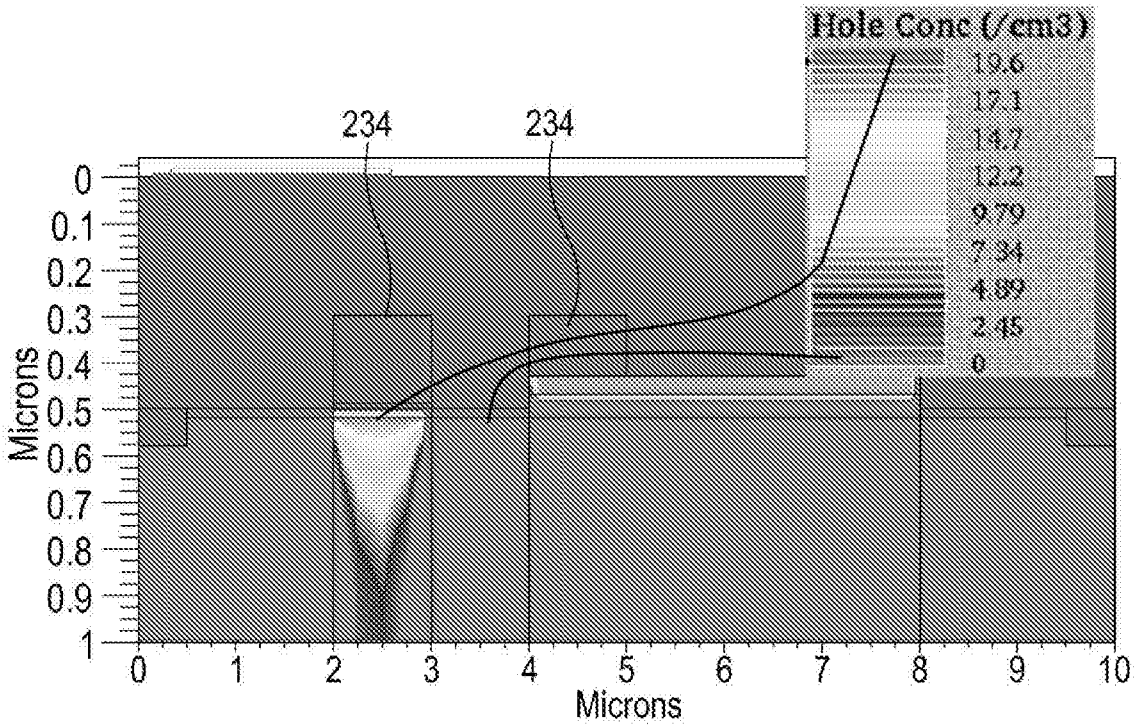
Hole Conc (/cm3)
19.6
17.1
14.7
12.2
9.79
7.34
4.89
2.45
0
234
234
Microns
Microns
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0
1
2
3
4
5
6
7
8
9
10

Fig. 11

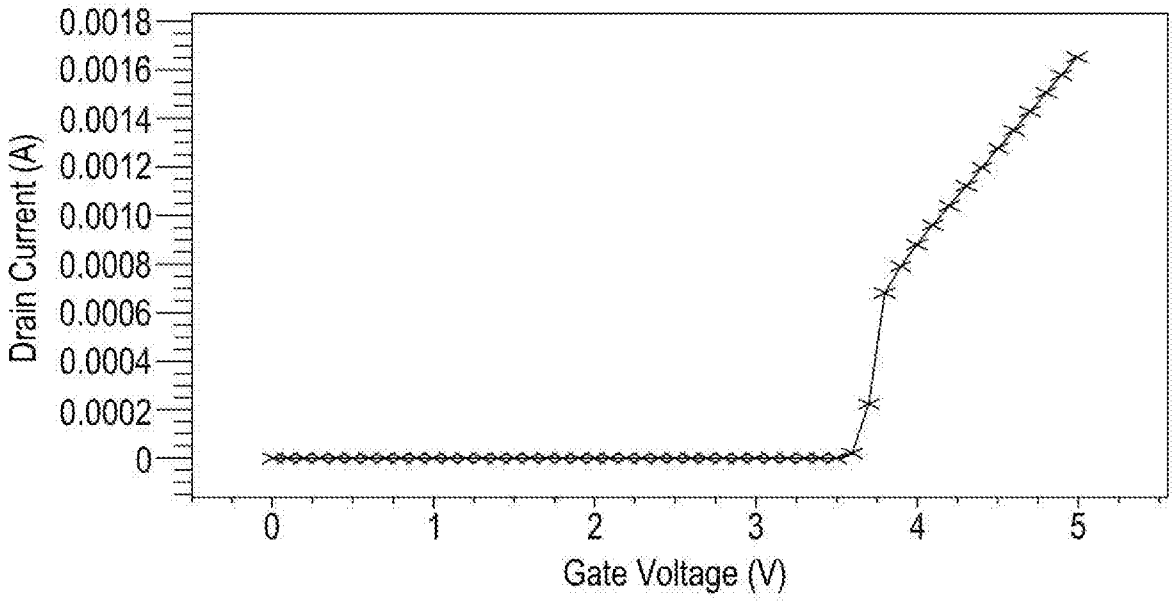
Drain Current (A)
Gate Voltage (V)
0.0018
0.0016
0.0014
0.0012
0.0010
0.0008
0.0006
0.0004
0.0002
0
0
1
2
3
4
5

Fig. 12

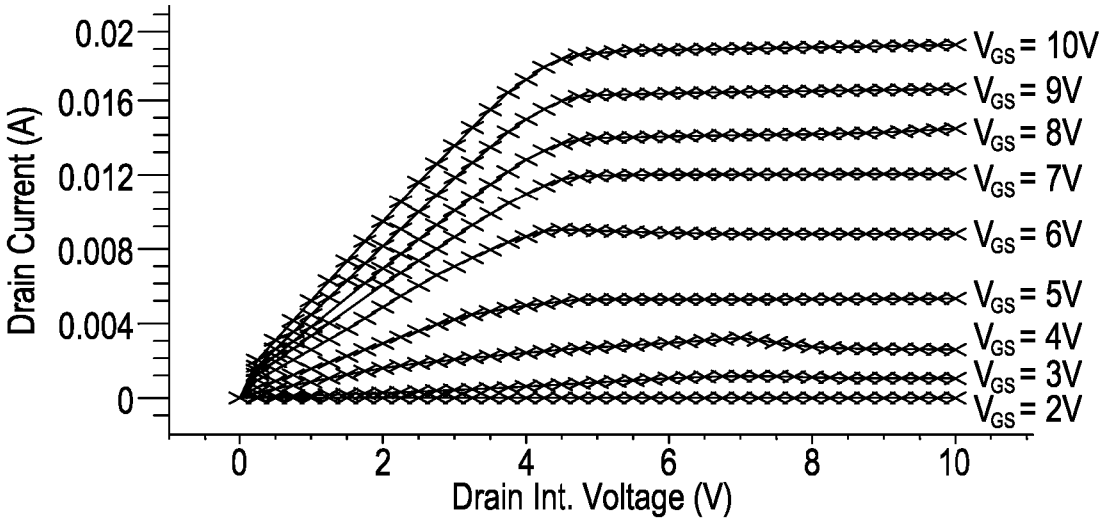
Drain Current (A)
0.02
0.016
0.012
0.008
0.004
0
0
2
4
6
8
10
Drain Int. Voltage (V)
V_{GS} = 10V
V_{GS} = 9V
V_{GS} = 8V
V_{GS} = 7V
V_{GS} = 6V
V_{GS} = 5V
V_{GS} = 4V
V_{GS} = 3V
V_{GS} = 2V

Fig. 13

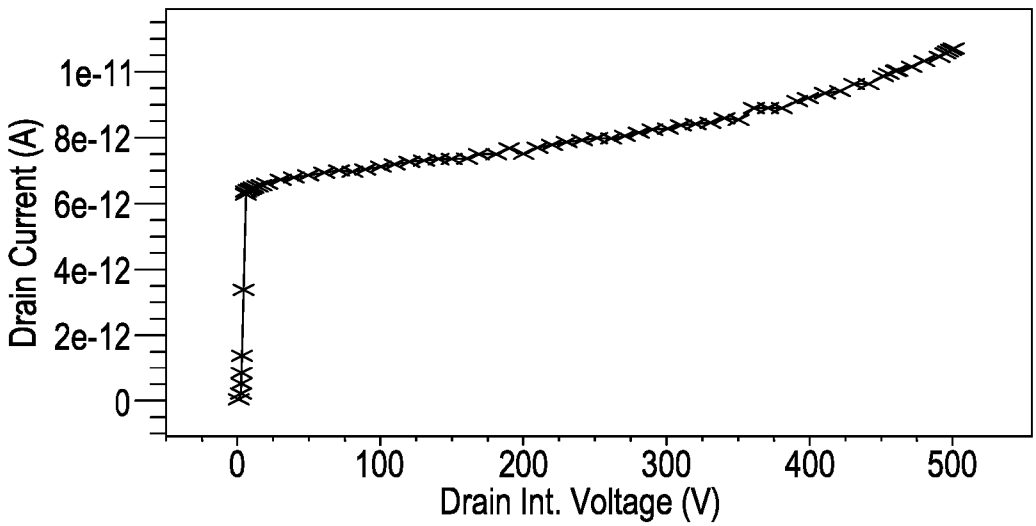
Drain Current (A)
1e-11
8e-12
6e-12
4e-12
2e-12
0
0
100
200
300
400
500
Drain Int. Voltage (V)

Fig. 14

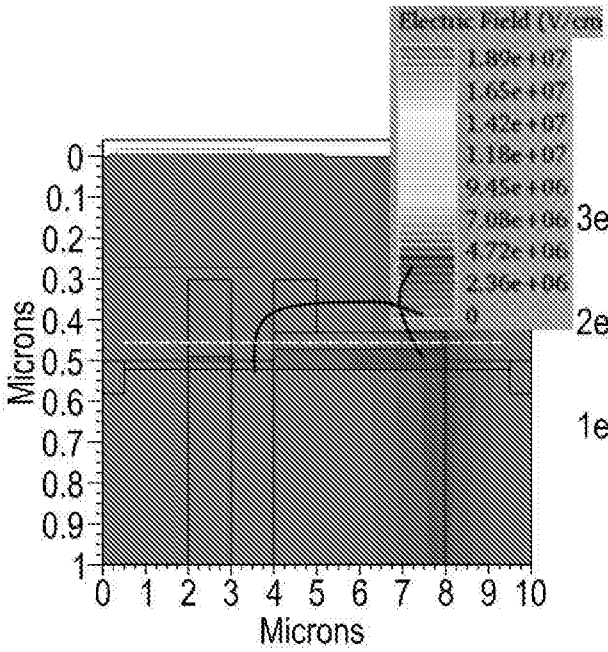

Fig. 15a

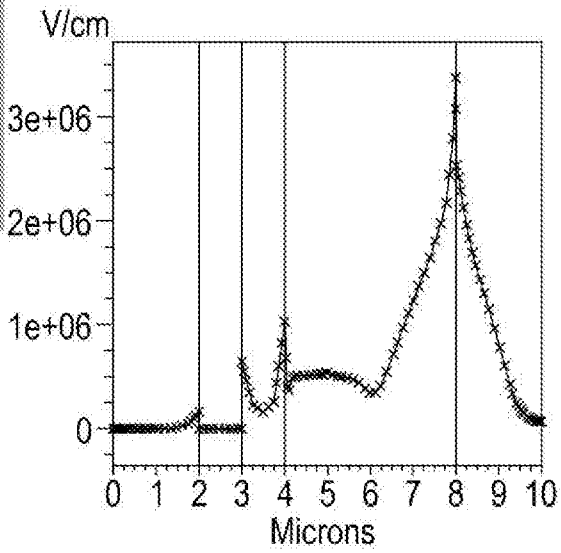

Fig. 15b

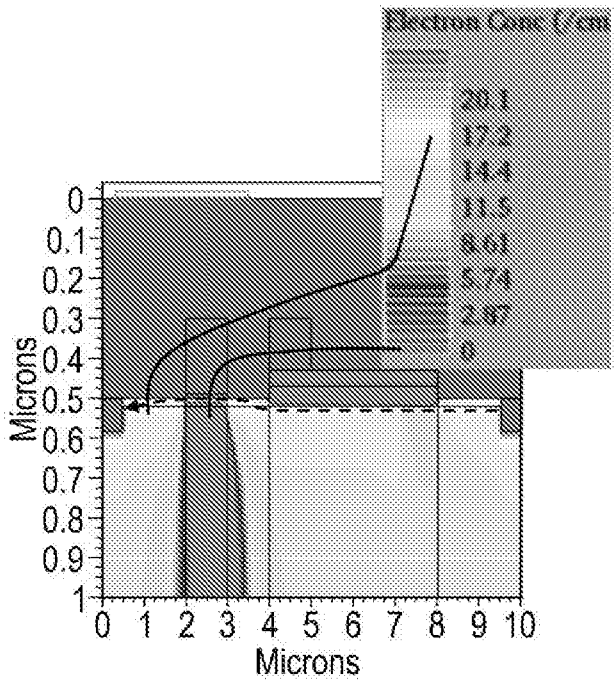

Fig. 16a

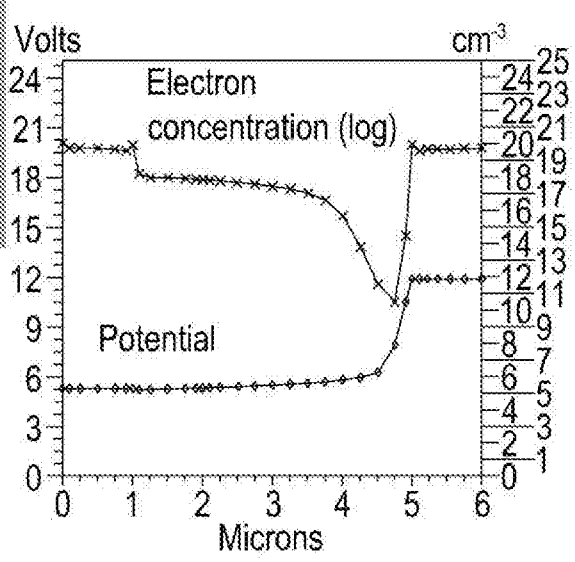

Fig. 16b

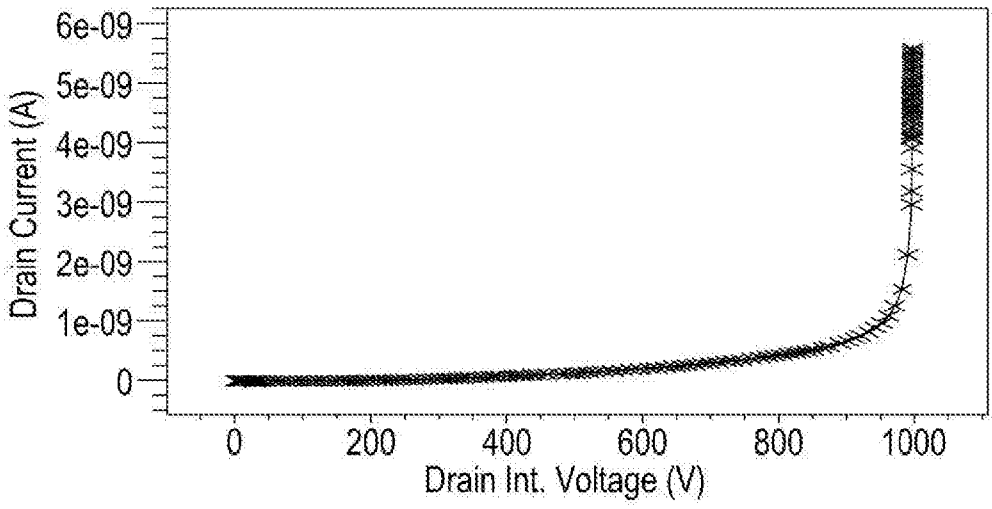

Fig. 17

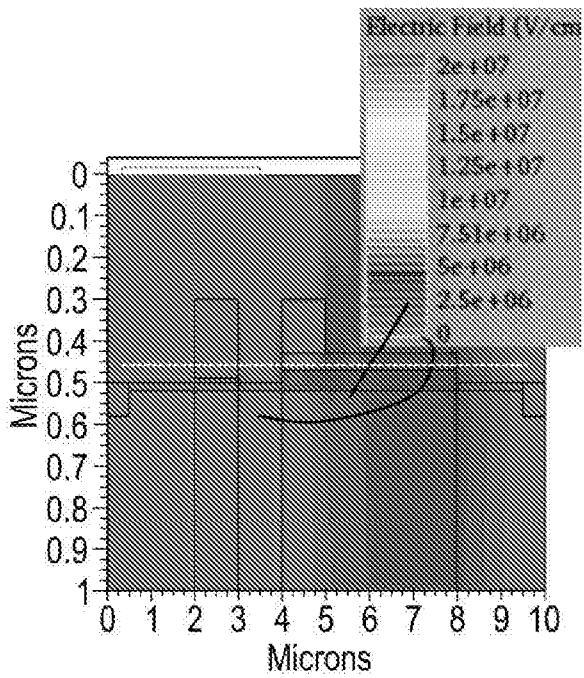

Fig. 18a

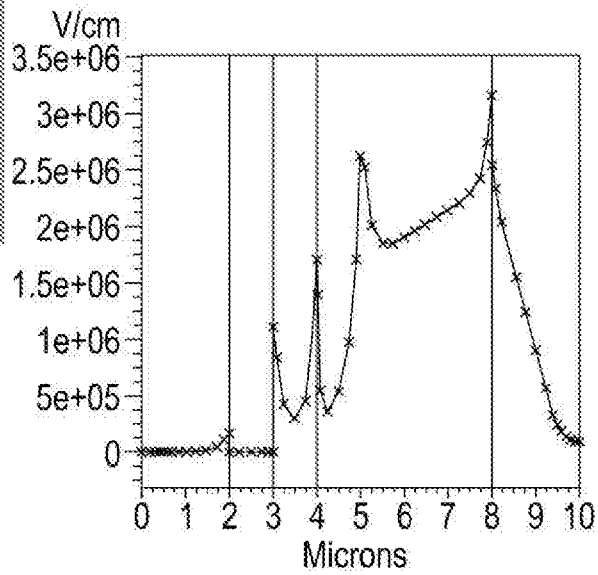

Fig. 18b

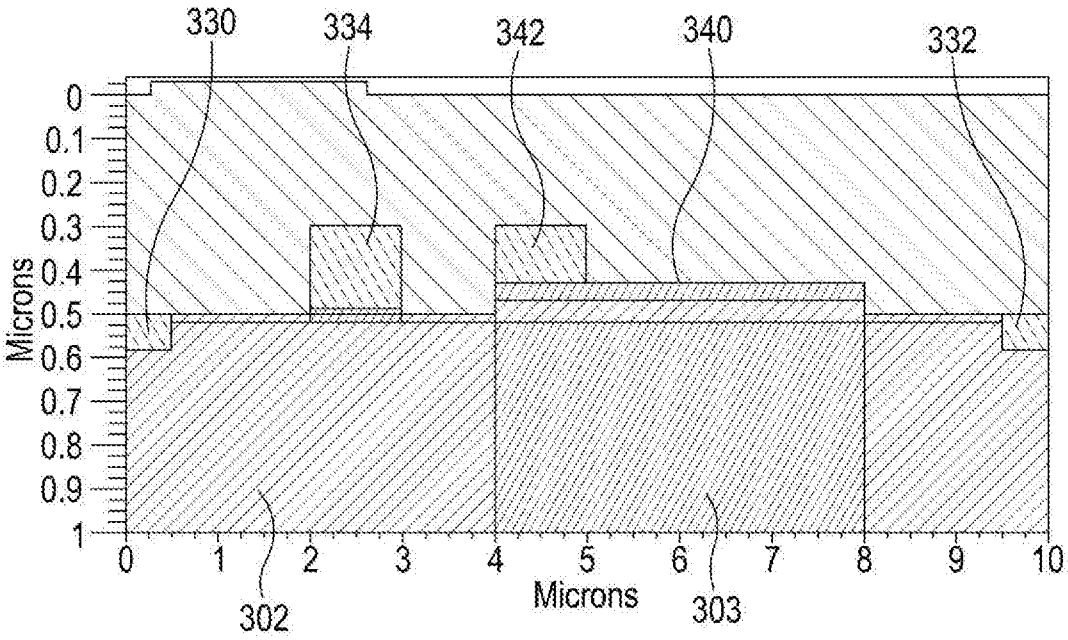
330
334
342
340
332
Microns
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0 1 2 3 4 5 6 7 8 9 10
Microns
302
303

Fig. 19

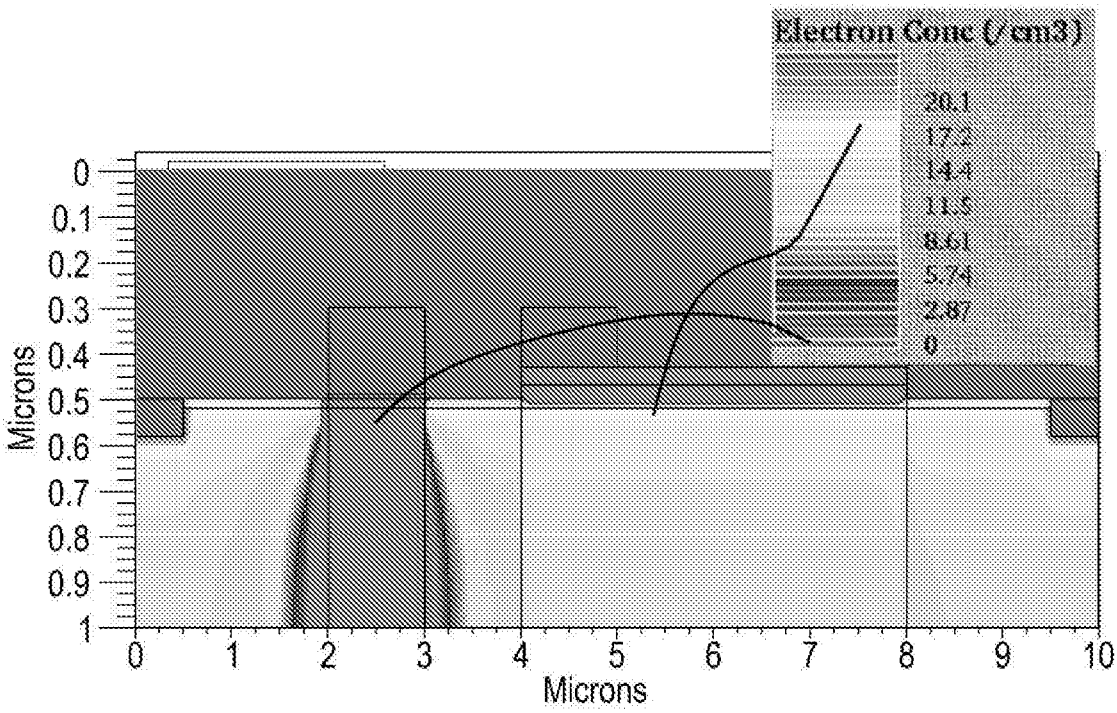
Electron Conc (/cm3)
20.1
17.2
14.4
11.5
8.61
5.74
2.87
0
Microns
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0 1 2 3 4 5 6 7 8 9 10
Microns

Fig. 20

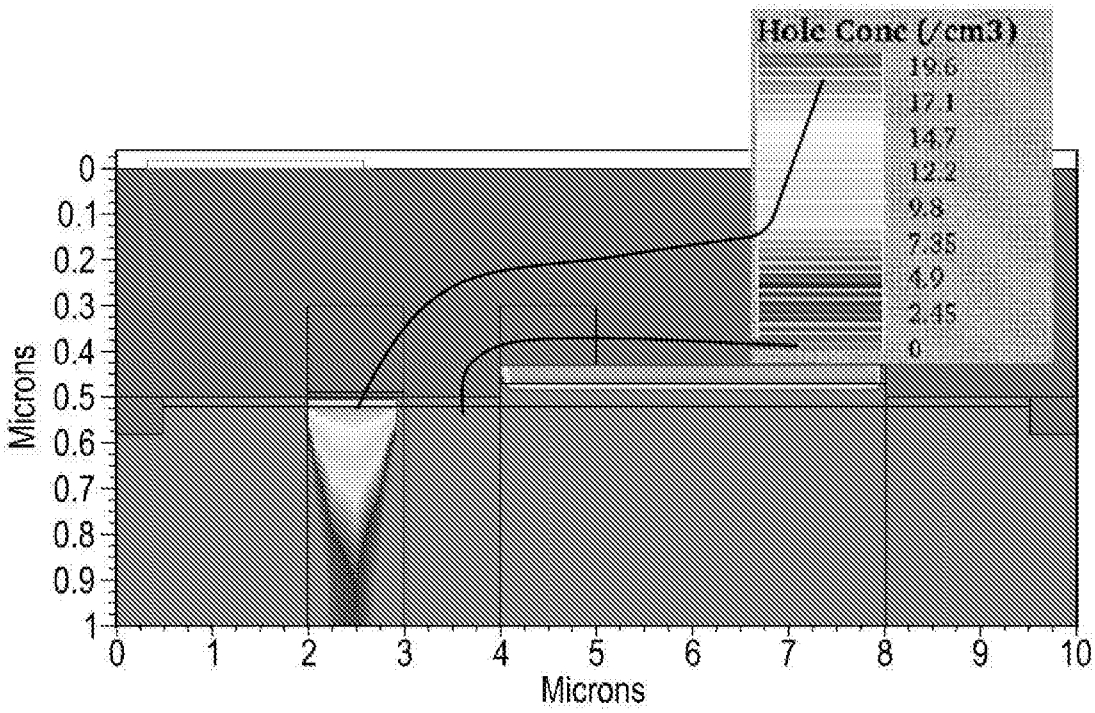
Hole Conc (/cm3)
19.6
17.1
14.7
12.2
9.8
7.35
4.9
2.45
0
Microns
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0
1
2
3
4
5
6
7
8
9
10
Microns

Fig. 21

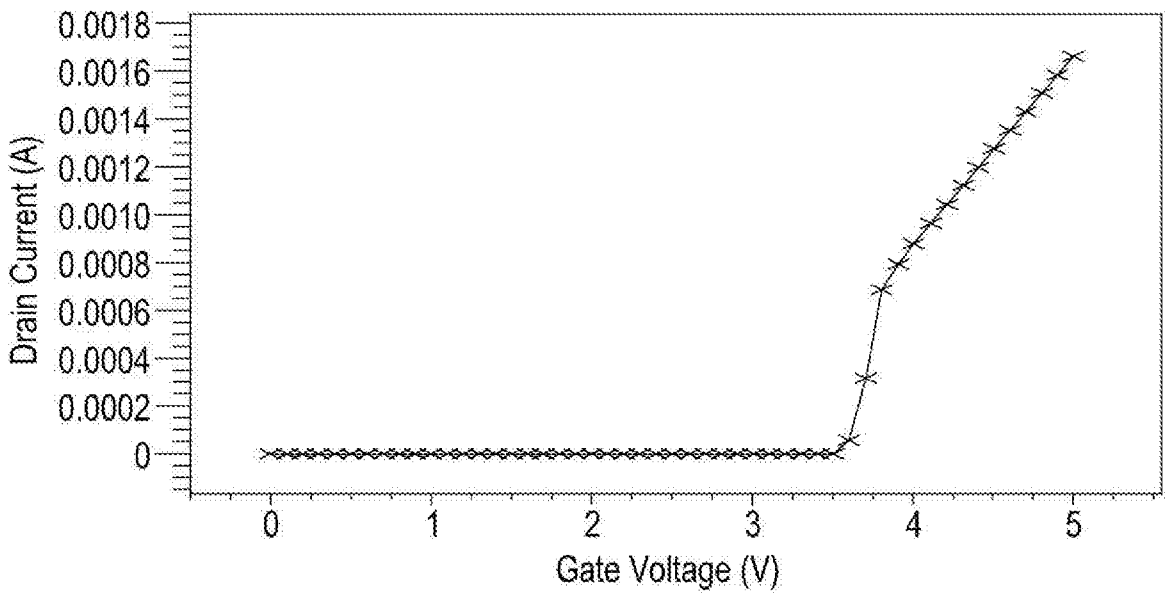
Drain Current (A)
0.0018
0.0016
0.0014
0.0012
0.0010
0.0008
0.0006
0.0004
0.0002
0
0
1
2
3
4
5
Gate Voltage (V)

Fig. 22

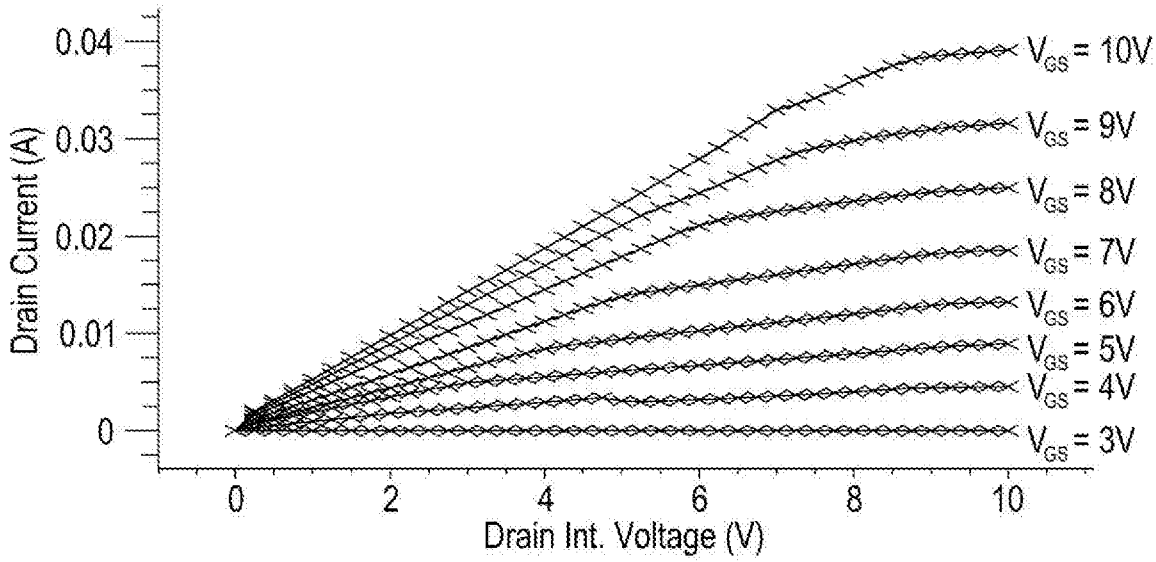

Fig. 23

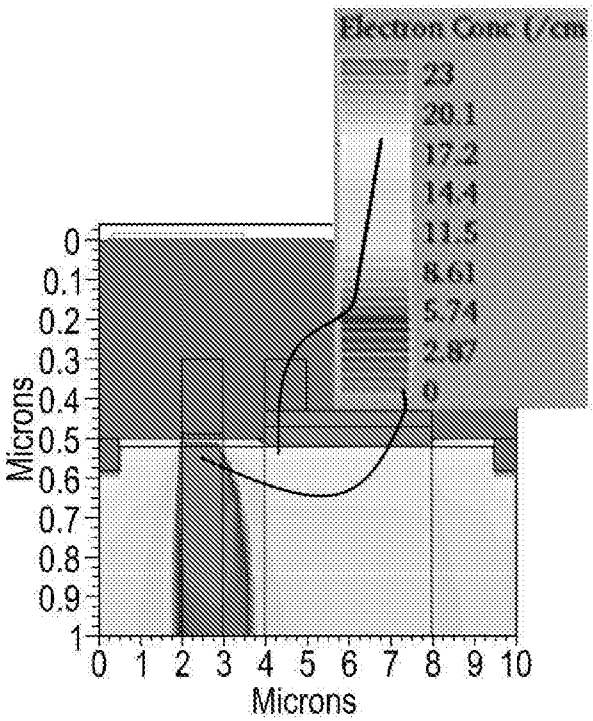

Fig. 24a

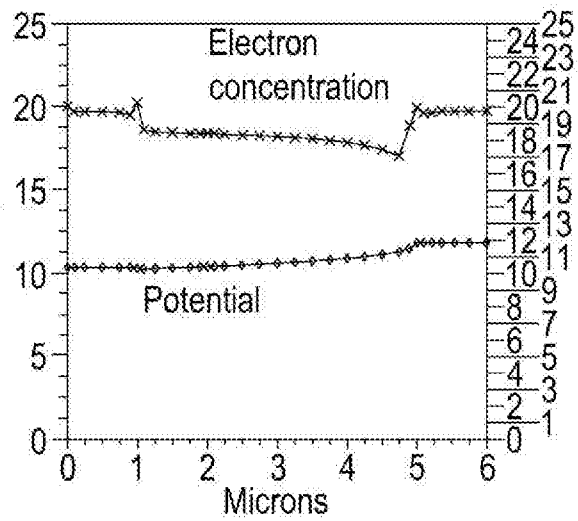

Fig. 24b

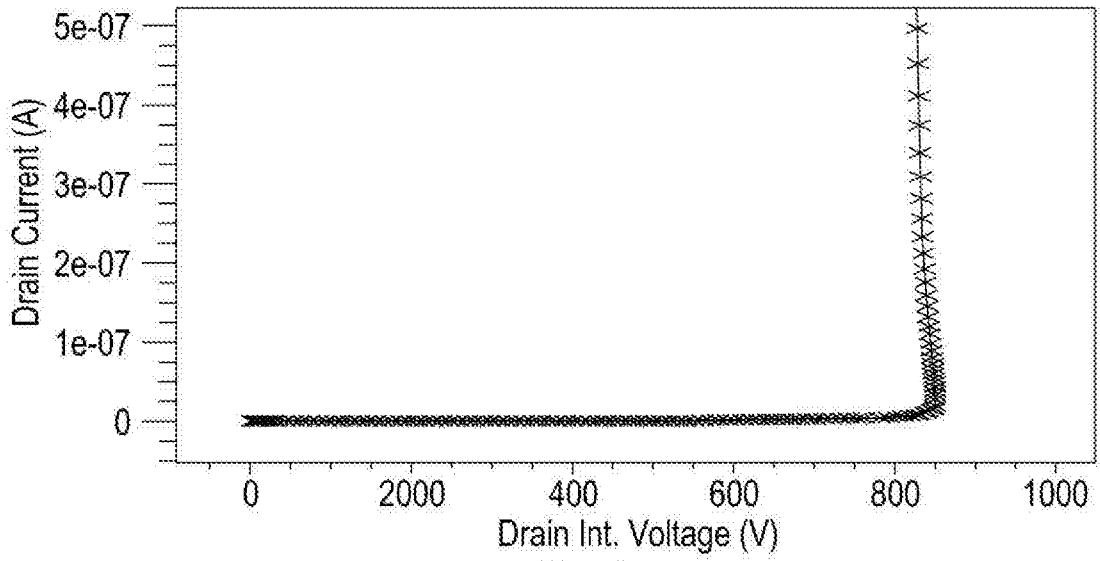

Fig. 25

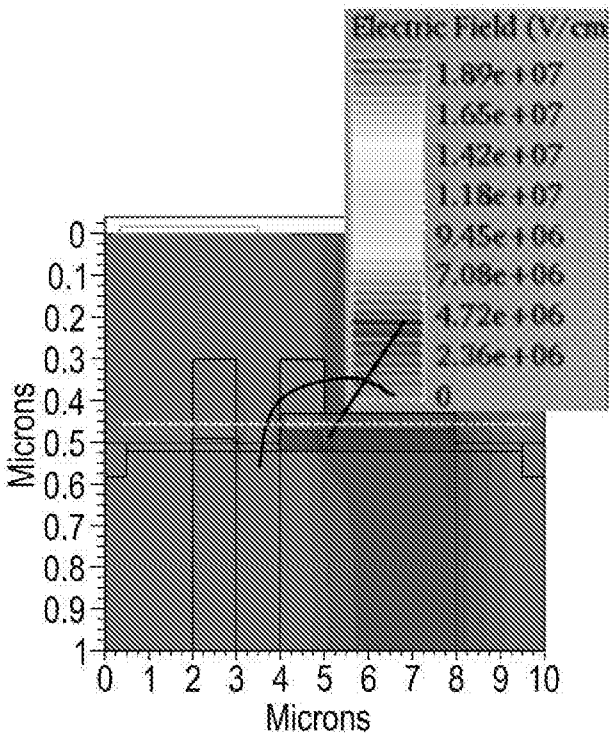

Fig. 26a

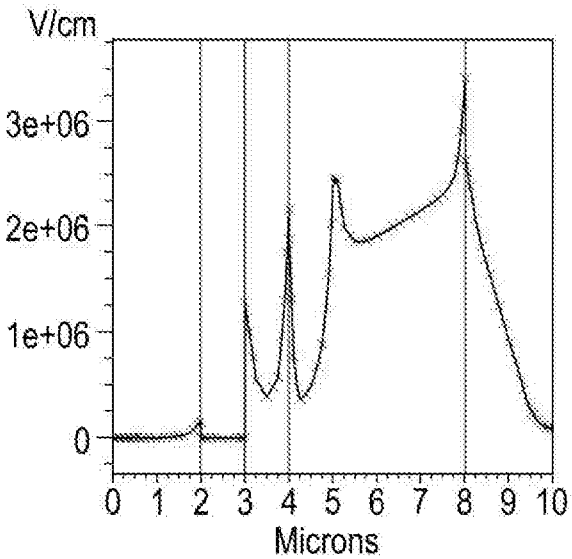

Fig. 26b

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2017/050682

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/778 H01L29/20
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2010/090225 A1 (SATO KEN [JP]) 15 April 2010 (2010-04-15) paragraph [0017] - paragraph [0023]; figure 1 -----	1-8 9-14
Y	AKIRA NAKAJIMA ET AL: "GaN-Based Super Heterojunction Field Effect Transistors Using the Polarization Junction Concept", IEEE ELECTRON DEVICE LETTERS, IEEE SERVICE CENTER, NEW YORK, NY, US, vol. 32, no. 4, 1 April 2011 (2011-04-01), pages 542-544, XP011363948, ISSN: 0741-3106, DOI: 10.1109/LED.2011.2105242 figure 1 -----	9-14

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 May 2017	30/05/2017

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Diaz Alvarez, C

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/GB2017/050682

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010090225 A1	15-04-2010	JP 2010098047 A	30-04-2010
		US 2010090225 A1	15-04-2010