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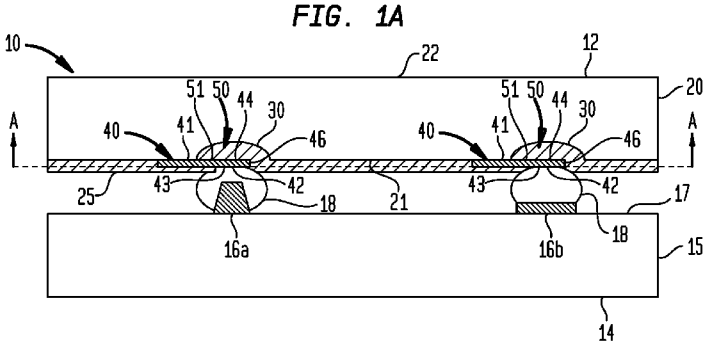
(54) **Title**: COMPLIANT INTERCONNECTS IN WAFERS

FIG. 1A



(57) **Abstract**: A microelectronic unit 12 includes a substrate 20 and an electrically conductive element 40. The substrate 20 can have a CTE less than 10 ppm/°C, a major surface 21 having a recess 30 not extending through the substrate, and a material 50 having a modulus of elasticity less than 10 GPa disposed within the recess. The electrically conductive element 40 can include a joining portion 42 overlying the recess 30 and extending from an anchor portion 41 supported by the substrate 20. The joining portion 42 can be at least partially exposed at the major surface 21 for connection to a component 14 external to the microelectronic unit 12.

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COMPLIANT INTERCONNECTS IN WAFERS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a continuation of U.S. Patent Application No. 12/962,806, filed on December 8, 2010, the disclosure of which is hereby incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to stacked microelectronic assemblies and methods of making such assemblies, and to components useful in such assemblies.

[0003] Semiconductor chips are commonly provided as individual, prepackaged units. A standard chip has a flat, rectangular body with a front surface having contacts connected to the active circuitry of the chip. Each individual chip typically is mounted in a package which, in turn, is mounted on a circuit panel such as a printed circuit board and which connects the contacts of the chip to conductors of the circuit panel. In many conventional designs, the chip package occupies an area of the circuit panel considerably larger than the area of the chip itself. As used in this disclosure with reference to a flat chip having a front surface, the "area of the chip" should be understood as referring to the area of the front surface.

[0004] In "flip chip" designs, the front surface of the chip confronts a surface of a package substrate, *i.e.*, a chip carrier, and the contacts on the chip are bonded directly to contacts of the chip carrier by solder balls or other connecting elements. In turn, the chip carrier can be bonded to a circuit panel through terminals overlying the front surface of the chip. The "flip chip" design provides a relatively compact arrangement; each chip occupies an area of the circuit panel equal to or slightly larger than the area of the chip's front surface, such as disclosed, for example, in certain embodiments of commonly-assigned U.S. Pat. Nos.

5,148,265, 5,148,266, and 5,679,977, the disclosures of which are incorporated herein by reference.

[0005] Besides minimizing the planar area of the circuit panel occupied by microelectronic assembly, it is also desirable to produce a chip package that presents a low overall height or dimension perpendicular to the plane of the circuit panel. Such thin microelectronic packages allow for placement of a circuit panel having the packages mounted therein in close proximity to neighboring structures, thus reducing the overall size of the product incorporating the circuit panel.

[0006] It has also been proposed to package plural chips in a "stacked" arrangement, *i.e.*, an arrangement where plural chips are placed one on top of another. In a stacked arrangement, several chips can be mounted in an area of the circuit panel that is less than the total area of the chips. Certain stacked chip arrangements are disclosed, for example, in certain embodiments of the aforementioned U.S. Pat. Nos. 5,148,265, 5,679,977, and U.S. Pat. No. 5,347,159, the disclosure of which is incorporated herein by reference. U.S. Pat. No. 4,941,033, also incorporated herein by reference, discloses an arrangement in which chips are stacked on top of another and interconnected with one another by conductors on so-called "wiring films" associated with the chips.

[0007] Conventional chip contacts may have reliability challenges because of a non-optimal stress distribution at the contact and a mismatch of the coefficient of thermal expansion (CTE) between a semiconductor chip, for example, and the structure to which the chip is bonded. For example, when conductive contacts at a surface of a semiconductor chip are insulated by a relatively thin and stiff dielectric material, significant stresses may be present at the contacts. In addition, when the semiconductor chip is bonded to conductive elements of a polymeric substrate, the electrical connections

between the chip and the higher CTE structure of the substrate will be under stress due to CTE mismatch.

[0008] Size is a significant consideration in any physical arrangement of chips. The demand for more compact physical arrangements of chips has become even more intense with the rapid progress of portable electronic devices. Merely by way of example, devices commonly referred to as "smart phones" integrate the functions of a cellular telephone with powerful data processors, memory and ancillary devices such as global positioning system receivers, electronic cameras, and local area network connections along with high-resolution displays and associated image processing chips. Such devices can provide capabilities such as full internet connectivity, entertainment including full-resolution video, navigation, electronic banking and more, all in a pocket-size device. Complex portable devices require packing numerous chips into a small space. Moreover, some of the chips have many input and output connections, commonly referred to as "I/O's." These I/O's must be interconnected with the I/O's of other chips. The interconnections should be short and should have low impedance to minimize signal propagation delays. The components which form the interconnections should not greatly increase the size of the assembly. Similar needs arise in other applications as, for example, in data servers such as those used in internet search engines. For example, structures which provide numerous short, low-impedance interconnects between complex chips can increase the bandwidth of the search engine and reduce its power consumption.

[0009] Despite the advances that have been made in semiconductor contact formation and interconnection, there is still a need for improvements in order to minimize the size of semiconductor chips, while enhancing electrical interconnection reliability. These attributes of the present

invention are achieved by the construction of the microelectronic packages as described hereinafter.

BRIEF SUMMARY OF THE INVENTION

[0010] In accordance with an aspect of the invention, a microelectronic unit can include a substrate and an electrically conductive element. The substrate can have a CTE less than 10 ppm/°C, a major surface having a recess not extending through the substrate, and a material having a modulus of elasticity less than 10 GPa disposed within the recess. The electrically conductive element can include a joining portion overlying the recess and extending from an anchor portion supported by the substrate. The joining portion can be at least partially exposed at the major surface for connection to a component external to the microelectronic unit.

[0011] In one embodiment, the substrate can have a CTE less than 7 ppm/°C. In a particular embodiment, the joining portion can be movable so as to reduce stresses on the joining portion, such as may be present during operation, manufacturing, or testing of the microelectronic unit. In an exemplary embodiment, the substrate can consist essentially of one material selected from the group consisting of: semiconductor, glass, and ceramic. In one embodiment, the substrate can include a plurality of active semiconductor devices and the conductive element can be electrically connected with at least one of the plurality of active semiconductor devices. In a particular embodiment, the material disposed within the recess can include at least one material selected from the group consisting of: polyimide, silicone, and epoxy.

[0012] In an exemplary embodiment, the recess may not extend through the substrate. In one embodiment, the joining portion can extend in a direction substantially parallel to the major surface of the substrate. In a particular

embodiment, the anchor portion and the joining portion can extend in the same direction. In an exemplary embodiment, the conductive element can be electrically coupled with a conductive via extending towards a second surface of the substrate opposite the major surface. In one embodiment, the conductive via can be exposed at the second surface. In a particular embodiment, the conductive via can extend within a hole in the substrate extending from the second surface to the major surface.

[0013] In one embodiment, the hole can include a first opening extending from the major surface towards the second surface and a second opening extending from the first opening to the second surface. Inner surfaces of the first and second openings can extend in first and second directions relative to the major surface, respectively, to define a substantial angle. In an exemplary embodiment, a stacked assembly can include at least first and second microelectronic units, the second microelectronic unit being stacked with the first microelectronic unit, with the substrate of the first microelectronic unit therein being electrically connected with a substrate of the second microelectronic unit. In a particular embodiment, the stacked assembly can further include a conductive mass electrically coupled to the joining portion of the first microelectronic unit and a conductive element of the second microelectronic unit.

[0014] In accordance with another aspect of the invention, a microelectronic assembly can include a substrate and an electrically conductive element. The substrate can have a CTE less than 10 ppm/°C, a major surface having a recess not extending through the substrate, and a material having a modulus of elasticity less than 10 GPa disposed within the recess. The electrically conductive element can have an anchor portion fixed relative to the substrate, a joining portion at least partially overlying the recess, and a

connecting portion extending downwardly from the joining portion to the anchor portion. The joining portion can extend in a direction away from the anchor portion and can be exposed at the major surface for connection to a component external to the microelectronic unit. The connecting portion can have a contour not conforming to a contour of an inner surface of the recess.

[0015] In an exemplary embodiment, the substrate can have a CTE less than 7 ppm/°C. In one embodiment, the joining portion can be movable so as to reduce stresses on the joining portion, such as may be present during operation, manufacturing, or testing of the microelectronic unit. In a particular embodiment, the substrate can consist essentially of one material selected from the group consisting of: semiconductor, glass, and ceramic. In one embodiment, the substrate can include a plurality of active semiconductor devices and the conductive element can be electrically connected with at least one of the plurality of active semiconductor devices. In an exemplary embodiment, the connecting portion can extend into the recess.

[0016] In a particular embodiment, the conductive element can be electrically coupled with a conductive via extending towards a second surface of the substrate opposite the major surface. In one embodiment, the conductive via can be exposed at the second surface. In an exemplary embodiment, the conductive via can extend within a hole in the substrate extending from the second surface to the major surface. In a particular embodiment, the hole can include a first opening extending from the major surface towards the second surface and a second opening extending from the first opening to the second surface. Inner surfaces of the first and second openings can extend in first and second directions relative to the major surface, respectively, to define a substantial angle. In one embodiment, the anchor portion can have a

contour conforming to a contour of an inner surface of the hole. In an exemplary embodiment, the joining portion can define an internal aperture.

[0017] In one embodiment, the aperture can extend through the joining portion into the connecting portion. In a particular embodiment, at least a portion of the aperture can be filled with a dielectric material. In an exemplary embodiment, a stacked assembly can include at least first and second microelectronic units, the second microelectronic unit being stacked with the first microelectronic unit, with the substrate of the first microelectronic unit therein being electrically connected with a substrate of the second microelectronic unit. In a particular embodiment, the stacked assembly can further include a conductive mass electrically coupled to the joining portion of the first microelectronic unit and a conductive element of the second microelectronic unit.

[0018] In accordance with yet another aspect of the invention, a method of fabricating a microelectronic unit can include the steps of forming an electrically conductive element supported on a major surface of a substrate having a CTE less than 10 ppm/°C, removing material supporting at least a joining portion of the conductive element from the major surface to form a recess not extending through the substrate, and depositing a material within the recess having a modulus of elasticity less than 10 GPa. The joining portion may not be supported by the substrate while an anchor portion of the conductive element adjacent the joining portion may be supported by the substrate. The joining portion can be at least partially exposed at the major surface of the substrate for connection to a component external to the microelectronic unit.

[0019] In one embodiment, the substrate can have a CTE less than 7 ppm/°C. In an exemplary embodiment, the substrate can

consist essentially of one material selected from the group consisting of: semiconductor, glass, and ceramic. In a particular embodiment, the substrate can include a plurality of active semiconductor devices, and the step of forming the conductive element can electrically connect the conductive element with at least one of the plurality of active semiconductor devices. In an exemplary embodiment, the step of forming the conductive element can be performed such that the joining portion is disposed substantially parallel to the major surface. In one embodiment, the method can further include the steps of removing material from the substrate to form a hole extending from the major surface to a second surface of the substrate opposite the major surface, and forming a conductive via extending within the hole such that the conductive via is electrically coupled with the conductive element and extends towards the second surface.

[0020] In a particular embodiment, the step of removing material from the substrate to form a hole can include forming a first opening extending from the major surface towards the second surface and a second opening extending from the first opening to the second surface. The inner surfaces of the first and second openings can extend in first and second directions relative to the major surface, respectively, to define a substantial angle. In one embodiment, a method of fabricating a stacked assembly including at least first and second microelectronic units can further include the step of electrically connecting the substrate of the first microelectronic unit to a substrate of the second microelectronic unit.

[0021] In accordance with still another aspect of the invention, a method of fabricating a microelectronic unit can include the steps of removing material from a substrate having a CTE less than 10 ppm/°C to form a hole extending from a major surface of the substrate to a second surface opposite

the major surface, forming an electrically conductive element having a joining portion extending above and supported on the major surface, an anchor portion fixed relative to the substrate, and a connecting portion extending downwardly from the joining portion to the anchor portion, removing material supporting at least a joining portion of the conductive element from the major surface to form a recess such that the joining portion at least partially overlies the recess, and depositing a material within the recess having a modulus of elasticity less than 10 GPa. A surface of the connecting portion can have a contour conforming to a contour of an inner surface of the hole. The contour of the surface of the connecting portion may not conform to a contour of an inner surface of the recess. The joining portion can be at least partially exposed at the major surface of the substrate for connection to a component external to the microelectronic unit.

[0022] In a particular embodiment, the substrate can have a CTE less than 7 ppm/°C. In an exemplary embodiment, the method of fabricating a microelectronic unit can further include, before the step of forming the conductive element, forming a conductive via extending within the hole and extending towards the second surface, such that the step of forming the conductive element electrically couples the conductive element with the conductive via. In one embodiment, the step of forming the conductive element can be performed such that the joining portion is non-centered relative to the connecting portion. In a particular embodiment, the substrate can consist essentially of one material selected from the group consisting of: semiconductor, glass, and ceramic. In an exemplary embodiment, the substrate can includes a plurality of active semiconductor devices, and the step of forming the conductive element can electrically connect the conductive element with at least one of the

plurality of active semiconductor devices. In one embodiment, the step of forming the conductive element can be performed such that the joining portion defines an internal aperture. In a particular embodiment, the step of forming the conductive element can be performed such that the aperture extends through the joining portion into the connecting portion.

[0023] In one embodiment, the method of fabricating a microelectronic unit can further include the step of depositing a dielectric material into at least a portion of the aperture. In a particular embodiment, the step of removing material from the substrate to form a hole can include forming a first opening extending from the major surface towards the second surface and a second opening extending from the first opening to the second surface. The inner surfaces of the first and second openings can extend in first and second directions relative to the major surface, respectively, to define a substantial angle. In an exemplary embodiment, a method of fabricating a stacked assembly including at least first and second microelectronic units can further include the step of electrically connecting the substrate of the first microelectronic unit to a substrate of the second microelectronic unit.

[0024] Further aspects of the invention provide systems which incorporate microelectronic structures according to the foregoing aspects of the invention, composite chips according to the foregoing aspects of the invention, or both in conjunction with other electronic devices. For example, the system may be disposed in a single housing, which may be a portable housing. Systems according to preferred embodiments in this aspect of the invention may be more compact than comparable conventional systems.

[0025] Further aspects of the invention provide modules that can include a plurality of microelectronic assemblies according to the foregoing aspects of the invention. Each

module can have a common electrical interface for transport of signals to and from each of said microelectronic assemblies.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] FIG. 1A is a side sectional view illustrating a stacked assembly having a contact structure in accordance with an embodiment of the invention.

[0027] FIG. 1B is one embodiment of a corresponding bottom-up sectional view of the stacked assembly of FIG. 3A taken along the line A-A.

[0028] FIG. 1C is another embodiment of a corresponding bottom-up sectional view of the stacked assembly of FIG. 3A taken along the line A-A.

[0029] FIG. 1D is yet another embodiment of a corresponding bottom-up sectional view of the stacked assembly of FIG. 3A taken along the line A-A.

[0030] FIGS. 2A-2D are sectional views illustrating stages of fabrication in accordance with the embodiment of the invention depicted in FIG. 1A.

[0031] FIG. 3A is a side sectional view illustrating a stacked assembly having a contact structure in accordance with an embodiment of the invention.

[0032] FIG. 3B is one embodiment of a corresponding bottom-up sectional view of the stacked assembly of FIG. 1A taken along the line B-B.

[0033] FIG. 3C is another embodiment of a corresponding bottom-up sectional view of the stacked assembly of FIG. 1A taken along the line B-B.

[0034] FIG. 3D is yet another embodiment of a corresponding bottom-up sectional view of the stacked assembly of FIG. 1A taken along the line B-B.

[0035] FIGS. 4A-4E are sectional views illustrating stages of fabrication in accordance with the embodiment of the invention depicted in FIG. 3A.

[0036] FIG. 5 is a top perspective view of a substrate having a pad electrically connected with a chip in accordance with the present invention.

[0037] FIG. 6 is a side sectional view illustrating a substrate having a contact structure in accordance with another embodiment of the invention.

[0038] FIG. 7 is a schematic depiction of a module according to one embodiment of the invention; and

[0039] FIG. 8 is a schematic depiction of a system according to one embodiment of the invention.

DETAILED DESCRIPTION

[0040] With reference to FIG. 1A, a stacked microelectronic assembly 10 according to an embodiment of the present invention includes a first microelectronic unit 12 and a second microelectronic unit 14. In some embodiments, the first and second microelectronic units 12 and 14 may be a semiconductor chip, a wafer, a dielectric substrate, or the like. For example, one or both of the first microelectronic unit 12 and the second microelectronic unit 14 can include a memory storage element. As used herein, a "memory storage element" refers to a multiplicity of memory cells arranged in an array, together with circuitry usable to store and retrieve data therefrom, such as for transport of the data over an electrical interface.

[0041] The first microelectronic unit 12 includes a substrate 20 having a recess 30 extending from a major surface 21 partially through the substrate towards a second surface 22 opposite the major surface, and a conductive element 40 having an anchor portion 41 supported by the substrate, a joining portion 42 extending from the anchor portion, the joining portion at least partially overlying the recess 30 and at least partially exposed at the major surface for interconnection with a component external to the first microelectronic unit, and an end portion 46. As shown, the

end portion 46 is located at an end of the joining portion 42. A dielectric region 50 overlies an inner surface 31 at least within the recess 30.

[0042] In FIG. 1A, the directions parallel to the major surface 21 are referred to herein as "horizontal" or "lateral" directions, whereas the directions perpendicular to the front surface are referred to herein as upward or downward directions and are also referred to herein as the "vertical" directions. The directions referred to herein are in the frame of reference of the structures referred to. Thus, these directions may lie at any orientation to the normal or gravitational frame of reference. A statement that one feature is disposed at a greater height "above a surface" than another feature means that the one feature is at a greater distance in the same orthogonal direction away from the surface than the other feature. Conversely, a statement that one feature is disposed at a lesser height "above a surface" than another feature means that the one feature is at a smaller distance in the same orthogonal direction away from the surface than the other feature.

[0043] The substrate 20 preferably has a coefficient of thermal expansion ("CTE") less than $10*10^{-6}$/°C (or ppm/°C). In a particular embodiment, the substrate 20 can have a coefficient of thermal expansion ("CTE") less than $7*10^{-6}$/°C (or ppm/°C). The substrate 20 preferably consists essentially of a material such as semiconductor, glass, or ceramic. In embodiments wherein the substrate 20 is made of a semiconductor, such as silicon, a plurality of active semiconductor devices (*e.g.*, transistors, diodes, etc.) can be disposed in an active semiconductor region thereof located at and/or below the major surface 21 or the second surface 22. The thickness of the substrate 20 between the major surface 21 and the second surface 22 typically is less than 200 µm, and

can be significantly smaller, for example, 130 µm, 70 µm or even smaller.

[0044] The substrate 20 can further include a dielectric layer disposed between the major surface 21 and at least one conductive element 40. A dielectric layer can overlie the second surface 22. Such a dielectric layer can electrically insulate conductive elements from the substrate 20. One or both of these dielectric layers can be referred to as a "passivation layer" of the first microelectronic unit 12. The dielectric layer can include an inorganic or organic dielectric material or both. The dielectric layer may include an electrodeposited conformal coating or other dielectric material, for example, a photoimageable polymeric material, for example, a solder mask material.

[0045] The microelectronic element 12 can include one or more conductive elements 40 exposed at the major surface 21 of the substrate 20. The joining portion 42 of each conductive element 40 can be exposed at the major surface 21 for interconnection with a component external to the first microelectronic element 12, such as the second microelectronic element 14. While not specifically shown in the figures, active semiconductor devices in the substrate 20 can be conductively connected to the joining portions 42. The active semiconductor devices, thus, can be accessible conductively through wiring incorporated extending within or above one or more dielectric layers of the substrate 20. The conductive elements 40 (and any of the other conductive elements described herein) can be made from any electrically conductive metal, including for example, copper or gold.

[0046] As shown, for example, in FIG. 1C, the joining portion 42' can have the bottom-view shape of a conductive bond pad, *e.g.*, a thin flat member. Each joining portion 42 can have any bottom-view shape, including for example, a rectangular trace shape, as shown in FIG. 1B, a circular pad

shape, as shown in FIG. 1C, an oval shape, a square shape, a triangular shape, or a more complex shape. In other embodiments, the joining portion 42 can be any other type of conductive contact, including for example, a conductive post.

[0047] The joining portion 42 can be aligned with the recess 30 and can be disposed wholly or partly within an area of the substrate 20 defined by the recess. As seen in FIG. 1A, the joining portion 42 is wholly disposed within an area defined by the recess 30. As shown, a plane defined by a top surface 43 of the joining portion 42 is substantially parallel to a plane defined by the major surface 21 of the substrate 20. As shown, a bottom surface 44 of the joining portion 42 is located at a plane defined by the major surface 21 of the substrate 20. In other embodiments, the bottom surface 44 of the joining portion 42 can be located above or below the plane defined by the major surface 21. The end portion 46 of the conductive element 40 is not supported by the substrate 20, such that the end portion can be cantilevered with respect to the anchor portion 41. Such an unsupported end portion 46 of the joining portion 42 that overlies the major surface 21 and is located adjacent to the dielectric region 50 can be free to move relative to the supported anchor portion 41, such that the joining portion 42 can function as a cantilever.

[0048] As used in this disclosure, a statement that an electrically conductive element is "exposed at" a surface of a substrate or a dielectric element overlying a surface of the substrate indicates that the electrically conductive element is available for contact with a theoretical point moving in a direction perpendicular to the surface of the dielectric element toward the surface of the dielectric element from outside the dielectric element. Thus, a terminal or other conductive element which is exposed at a surface of a dielectric element may project from such surface; may be flush

with such surface; or may be recessed relative to such surface and exposed through a hole or depression in the dielectric.

[0049] While essentially any technique usable for forming conductive elements can be used to form the conductive elements described herein, particular techniques as discussed in greater detail in the commonly owned U.S. Patent Application Serial No. 12/842,669, filed July 23, 2010, can be employed, which is hereby incorporated by reference herein. Such techniques can include, for example, selectively treating a surface with a laser or with mechanical processes such as milling or sandblasting so as to treat those portions of the surface along the path where the conductive element is to be formed differently than other portions of the surface. For example, a laser or mechanical process may be used to ablate or remove a material such as a sacrificial layer from the surface only along a particular path and thus form a groove extending along the path. A material such as a catalyst can then be deposited in the groove, and one or more metallic layers can be deposited in the groove.

[0050] The end portion 46 of the conductive element 40 is shown in the figures as not extending laterally (*i.e.*, in a direction parallel to the major surface 21 of the substrate 20) beyond an outer boundary 32 (FIG. 1B) of the recess 30. In any of the embodiments disclosed herein, the end portion of the conductive element and/or the joining portion can extend laterally beyond the outer boundary of the recess. In one embodiment, an end of the joining portion can be coupled to a conductive trace (not shown) that extends laterally beyond the outer boundary of the corresponding recess, but the joining portion can still be movable relative to the corresponding substrate in the manner described below.

[0051] The recess 30 extends from the major surface 21 partially through the substrate 20 towards the second surface 22. The inner surface 31 of the recess 30 can extend from the

major surface 21 through the substrate 20 at any angle. Preferably, the inner surface 31 extends from the major surface 21 at an angle between 0 and 90 degrees to the horizontal plane defined by the major surface 21. The inner surface 31 can have a constant slope or a varying slope. For example, the angle or slope of the inner surface 31 relative to the horizontal plane defined by the major surface 21 can decrease in magnitude (*i.e.*, become less positive or less negative) as the inner surface 31 penetrates further towards the second surface 22.

[0052] The recess 30 can have any bottom-view shape, including for example, an oval, as shown in FIG. 1B, or a circle, as shown in FIG. 1C. In the embodiment shown in FIG. 1B, recess 30 has a width W in a first lateral direction along the major surface 21, and the recess has a length L in a second lateral direction along the major surface transverse to the first lateral direction, the length being greater than the width. In some examples, the recess 30 can have any three-dimensional shape, including for example, a cylinder, a cube, a prism, or a frustoconical shape, among others.

[0053] In a particular embodiment, the recess 30 can be a rectangular channel with a plurality of joining portions 42 at least partially overlying the recess, as shown in FIG. 1D. Any number of joining portions 42 can overlie a single recess 30, and the joining portions can be arranged in any geometric configuration overlying a single recess. For example, three joining portions 42 can be arranged along a common axis overlying a single recess 30, as shown in FIG. 1D.

[0054] In the embodiments shown, the dielectric region 50 fills the recess 30 such that a contour of the dielectric region conforms to a contour of the recess (*i.e.*, the shape of the inner surface 31 of the recess). The dielectric region 50 can provide good dielectric isolation with respect to the substrate 20. The dielectric region 50 can be compliant,

having a sufficiently low modulus of elasticity and sufficient thickness such that the product of the modulus and the thickness provide compliancy. Preferably, the joining portion 42 of the conductive element 40 at least partially overlies the dielectric region 50. A compliant dielectric region 50 can allow the joining portion 42 of the conductive element 40 to flex or move somewhat relative to the substrate 20 and the anchor portion 41 of the conductive element supported thereon when an external load is applied to the joining portion. In that way, the bond between the joining portions 42 of the first microelectronic unit 12 and terminals of the second microelectronic unit 14 may be able to better withstand thermal strain due to mismatch of the coefficient of thermal expansion ("CTE") between the first and second microelectronic units.

[0055] As used herein in connection with a joining portion of a conductive element, "movable" shall mean that the joining portion is capable of being displaced relative to the major surface of the substrate by an external load applied thereto, to the extent that the displacement appreciably relieves or reduces mechanical stresses, such as those caused by differential thermal expansion during operation, manufacturing, or testing of the microelectronic unit which would be present in the electrical connection with the conductive element absent such displacement.

[0056] The degree of compliancy provided by the product of the thickness of the dielectric region 50 and its modulus of elasticity can be sufficient to compensate for strain applied to the joining portions 42 due to thermal expansion mismatch between the first microelectronic unit 12 and the second microelectronic unit 14 to which the first microelectronic unit is mounted through the joining portions. An underfill (not shown) can be provided between an outer surface 51 of the

dielectric region 50 and such second microelectronic unit 14 to enhance resistance to thermal strain due to CTE mismatch.

[0057] In the embodiments shown, the outer surface 51 (FIG. 1A) of the dielectric region 50 is located within a plane defined by the major surface 21 of the substrate 20. Alternatively, the outer surface 51 of the dielectric region 50 can extend above a plane defined by the major surface 21 of the substrate 20, or the outer surface of the dielectric region can be recessed below a plane defined by the major surface of the substrate.

[0058] A dielectric layer 25 can overlie the major surface 21 of the substrate 20 and portions of the conductive elements 40 that are not the joining portions 42, to provide good dielectric isolation with respect to the substrate and the portions of the conductive elements that are not the joining portions. The dielectric layer 25 can include an inorganic or organic dielectric material or both. In a particular embodiment, the dielectric layer 25 can include the same compliant dielectric material as the dielectric region 50. In an exemplary embodiment, the dielectric layer 25 can be formed continuously with the dielectric region 50.

[0059] The second microelectronic unit 14 can include a substrate 15 and conductive contacts 16a and 16b at least partially exposed at a major surface 17 of the substrate for interconnection with joining portions 42 of the first microelectronic unit 12. By providing joining portions 42 in the first microelectronic unit 12 and rear conductive contacts 14 in the second microelectronic unit 14, a plurality of microelectronic units can be stacked one on top of the other to form the stacked microelectronic assembly 10. In such arrangement, the joining portions 42 are aligned with the conductive contacts 16a and 16b.

[0060] As shown in FIG. 1A, the conductive contact 16a is a conductive post. The conductive post 16a can be any type of

conductive post and may have any shape, including a frustoconical shape. The base and tip of each conductive post 16a may be substantially circular or have a different shape, *e.g.*, oblong. Other examples of conductive posts can be used, as shown and described in the commonly-owned U.S. patent application no. 12/832,376, filed on July 8, 2010. The conductive contact 16b is shown as a conductive pad. The conductive pad 16b can have any shape, including circular, square, oblong, rectangular, or a more complex shape.

[0061] Connection between the first microelectronic unit 12 and the second microelectronic unit 14 can be through conductive masses 18. The dielectric layer 25 and the dielectric region 50 at the major surface 21 of the substrate 20 and a dielectric layer (*e.g.*, a passivation layer) overlying the major surface 17 of the substrate 15 can provide electrical isolation between the first microelectronic unit 12 and the second microelectronic unit 14 except where interconnection is provided.

[0062] The conductive masses 18 can comprise a fusible metal having a relatively low melting temperature, *e.g.*, solder, tin, or a eutectic mixture including a plurality of metals. Alternatively, the conductive masses 18 can include a wettable metal, *e.g.*, copper or other noble metal or non-noble metal having a melting temperature higher than that of solder or another fusible metal. Such wettable metal can be joined with a corresponding feature, *e.g.*, a fusible metal feature of an interconnect element such as the second microelectronic unit 14 to externally interconnect the first microelectronic unit 12 to such interconnect element. In a particular embodiment, the conductive masses 18 can include a conductive material interspersed in a medium, *e.g.*, a conductive paste, *e.g.*, metal-filled paste, solder-filled paste or isotropic conductive adhesive or anisotropic conductive adhesive.

[0063] A method of fabricating the microelectronic assembly 10 (FIGS. 1A-1D) will now be described, with reference to FIGS. 2A-2D. As illustrated in FIG. 2A, the first microelectronic unit 12 includes the substrate 20 and one or more conductive elements 40 overlying the major surface 21. The conductive elements 40 may be insulated from the substrate 20 by a dielectric layer such as a passivation layer (not shown).

[0064] In the stage of fabrication illustrated in FIG. 2B, a dielectric layer 25 is formed on the major surface 21 of the substrate 20 and serves as an etch mask layer where it is desired to preserve remaining portions of the major surface. For example, the dielectric layer 25 can be a photoimageable layer, *e.g.*, a photoresist layer, that is deposited and patterned to cover only portions of the major surface 21, after which a timed etch process can be conducted to form the recess 30. The joining portion 42 of each conductive element 40 can remain at least partially exposed at the major surface 21 (*i.e.*, not covered by the dielectric layer 25) for connection to a component external to the first microelectronic unit 12.

[0065] Various methods can be used to form the dielectric layer 25. In one example, a flowable dielectric material is applied to the major surface 21 of the substrate 20, and the flowable material is then more evenly distributed across the major surface during a "spin-coating" operation, followed by a drying cycle which may include heating. In another example, a thermoplastic film of dielectric material can be applied to the major surface 21 after which the assembly is heated, or is heated in a vacuum environment, *i.e.*, placed in an environment under lower than ambient pressure. In another example, vapor deposition can be used to form the dielectric layer 25.

[0066] In still another example, the assembly including the substrate 20 can be immersed in a dielectric deposition bath

to form a conformal dielectric coating or dielectric layer 25. As used herein, a "conformal coating" is a coating of a particular material that conforms to a contour of the surface being coated, such as when the dielectric layer 25 conforms to a contour of the major surface 21. An electrochemical deposition method can be used to form the conformal dielectric layer 25, including for example, electrophoretic deposition or electrolytic deposition.

[0067] In one example, an electrophoretic deposition technique can be used to form the conformal dielectric coating, such that the conformal dielectric coating is only deposited onto exposed conductive and semiconductive surfaces of the assembly. During deposition, the semiconductor device wafer is held at a desired electric potential and an electrode is immersed into the bath to hold the bath at a different desired potential. The assembly is then held in the bath under appropriate conditions for a sufficient time to form an electrodeposited conformal dielectric layer 25 on exposed surfaces of the substrate which are conductive or semiconductive, including but not limited to along the major surface 21. Electrophoretic deposition occurs so long as a sufficiently strong electric field is maintained between the surface to be coated thereby and the bath. As the electrophoretically deposited coating is self-limiting in that after it reaches a certain thickness governed by parameters, *e.g.*, voltage, concentration, etc. of its deposition, deposition stops.

[0068] Electrophoretic deposition forms a continuous and uniformly thick conformal coating on conductive and/or semiconductive exterior surfaces of the assembly. In addition, the electrophoretic coating can be deposited so that it does not form on a remaining passivation layer overlying the major surface 21, due to its dielectric (nonconductive) property. Stated another way, a property of electrophoretic

deposition is that is does not form on a layer of dielectric material overlying a conductor provided that the layer of dielectric material has sufficient thickness, given its dielectric properties. Typically, electrophoretic deposition will not occur on dielectric layers having thicknesses greater than about 10 microns to a few tens of microns. The conformal dielectric layer 25 can be formed from a cathodic epoxy deposition precursor. Alternatively, a polyurethane or acrylic deposition precursor could be used. A variety of electrophoretic coating precursor compositions and sources of supply are listed in Table 1 below.

Table 1

ECOAT NAME	**POWERCRON 645**	**POWERCRON 648**	**CATHOGUARD 325**
MANUFACTURERS			
MFG	PPG	PPG	BASF
TYPE	CATHODIC	CATHODIC	CATHODIC
POLYMER BASE	EPOXY	EPOXY	EPOXY
LOCATION	Pittsburgh, PA	Pittsburgh, PA	Southfield, MI
APPLICATION DATA			
Pb/Pf-free	Pb-free	Pb or Pf-free	Pb-free
HAPs, g/L		60-84	COMPLIANT
VOC, g/L (MINUS WATER)		60-84	<95
CURE	20 min/175C	20 min/175C	
FILM PROPERTIES			
COLOR	Black	Black	Black
THICKNESS, µm	10-35	10-38	13-36
PENCIL HARDNESS		2H+	4H
BATH CHARACTERISTICS			
SOLIDS, % wt.	20 (18-22)	20 (19-21)	17.0-21.0
pH (25C)	5.9 (5.8-6.2)	5.8 (5.6-5.9)	5.4-6.0
CONDUCTIVITY (25C) µS	1000-1500	1200-1500	1000-1700
P/B RATIO	0.12-0.14	0.12-0.16	0.15-0.20
OPERATION TEMP., C	30-34	34	29-35
TIME, sec	120-180	60-180	120+
ANODE	SS316	SS316	SS316
VOLTS		200-400	>100
ECOAT NAME	**ELECTROLAC**	**LECTRASEAL DV494**	**LECTROBASE 101**
MANUFACTURERS			
MFG	MACDERMID	LVH COATINGS	LVH COATINGS
TYPE	CATHODIC	ANODIC	CATHODIC
POLYMER BASE	POLYURETHANE	URETHANE	URETHANE
LOCATION	Waterbury, CT	Birmingham, UK	Birmingham, UK
APPLICATION DATA			
Pb/Pf-free		Pb-free	Pb-free
HAPs, g/L			
VOC, g/L (MINUS WATER)			
CURE	20 min/149C	20 min/175C	20 min/175C
FILM PROPERTIES			
COLOR	Clear (+dyed)	Black	Black
THICKNESS, µm		10-35	10-35
PENCIL HARDNESS	4H		
BATH CHARACTERISTICS			
SOLIDS, % wt.	7.0 (6.5-8.0)	10-12	9-11
pH (25C)	5.5-5.9	7-9	4.3
CONDUCTIVITY (25C) µS	450-600	500-800	400-800

P/B RATIO			
OPERATION TEMP., C	27-32	23-28	23-28
TIME, sec			60-120
ANODE	SS316	316SS	316SS
VOLTS	40, max		50-150

[0069] In another example, the dielectric layer can be formed electrolytically. This process is similar to electrophoretic deposition, except that the thickness of the deposited layer is not limited by proximity to the conductive or semiconductive surface from which it is formed. In this way, an electrolytically deposited dielectric layer can be formed to a thickness that is selected based on requirements, and processing time is a factor in the thickness achieved.

[0070] Thereafter, in the stage of fabrication illustrated in FIG. 2C, the recess 30 can be formed extending downwardly from the major surface 21 towards the second surface 22 of the substrate 20. The recess 30 can be formed for example, by selectively etching the substrate 20 to remove material of the substrate, after forming a mask layer (*e.g.*, the dielectric layer 25) where it is desired to preserve remaining portions of the major surface 21. The recess 30 can be formed such that material of the substrate 20 supporting at least the joining portion 42 is removed.

[0071] The inner surfaces 31 of the recess 30, extending downwardly from the major surface 21 towards the second surface 22, may be sloped, *i.e.*, may extend at angles other a normal angle (right angle) to the major surface, as shown in FIG. 2C. Wet etching processes, *e.g.*, isotropic etching processes and sawing using a tapered blade, among others, can be used to form recesses 30 having sloped inner surfaces 31. Laser ablation, mechanical milling, chemical etching, plasma etching, directing a jet of fine abrasive particles towards the substrate 20, among others, can also be used to form the recesses 30 (or any other hole or opening described herein) having sloped inner surfaces 31.

[0072] Alternatively, instead of being sloped, the inner surfaces of the recess 30 may extend in a vertical or substantially vertical direction downwardly from the major surface 21 substantially at right angles to the major surface. Anisotropic etching processes, laser ablation, mechanical removal processes, *e.g.*, milling, ultrasonic machining, directing a jet of fine abrasive particles towards the substrate 20, among others, can be used to form recesses 30 having essentially vertical inner surfaces.

[0073] Thereafter, in the stage of fabrication illustrated in FIG. 2D, the dielectric region 50 is formed inside the recess 30. The dielectric region 50 can include an inorganic material, a polymeric material, or both. Optionally, the dielectric region 50 can be formed such that the exposed outer surface 51 of the region is co-planar or substantially co-planar with the major surface 21 of the substrate 20 or an exposed surface of the dielectric layer 25. For example, a self-planarizing dielectric material can be deposited in the recess 30, *e.g.*, by a dispensing or stenciling process. In another example, a grinding, lapping, or polishing process can be applied to the major surface 21 of the substrate 20 or the exposed surface of the dielectric layer 25 after forming the dielectric region 50 to planarize the surface of the dielectric region 50 to the major surface 21 or the exposed surface of the dielectric layer 25.

[0074] Thereafter, referring again to FIG. 1A, the first microelectronic unit 12 can be stacked on top of the second microelectronic unit 14, thereby forming the stacked microelectronic assembly 10. As described above, connection between the first microelectronic unit 12 and the second microelectronic unit 14 can be through conductive masses 18. The conductive masses 18 can provide an electrical connection between the joining portions 42 of the first microelectronic unit 12 and the conductive contacts 16a and 16b of the second

microelectronic unit 14. In such arrangement, the joining portions 42 are aligned with the conductive contacts 16a and 16b.

[0075] Referring now to FIG. 3A, a stacked microelectronic assembly 110 according to another embodiment of the present invention includes a first microelectronic unit 112 and a second microelectronic unit 114. The microelectronic units 112 and 114 can have similar functions as the microelectronic units 12 and 14 described above.

[0076] The first microelectronic unit 112 includes a substrate 120 having a recess 130a and 130b extending from a major surface 121 partially through the substrate towards a second surface 122 opposite the major surface, and conductive elements 140a and 140b each having a respective anchor portion 141a or 141b supported by the substrate, a respective joining portion 142a or 142b at least partially overlying the respective recess 130a or 130b and at least partially exposed at the major surface for interconnection with a component external to the first microelectronic unit, one or more respective connecting portions 145a or 145b extending between the anchor and joining portions, and end portions 146. As shown, the end portions 146 are located at an end of each joining portion 142a and 142b. A dielectric region 150 overlies an inner surface 131 at least within the recess 130a or 130b.

[0077] The substrate 120 further includes a hole 160 extending from the opening 130 to the second surface 122 and a conductive via 170 extending within the hole from the respective anchor portion 141a or 141b to the second surface. The conductive via 170 includes a contact portion 180 exposed at the second surface 122 for interconnection with a component external to the stacked microelectronic assembly 110.

[0078] The substrate 120 has similar properties as the substrate 20 described above with reference to FIGS. 1A

through 2D. For example, the substrate 120 preferably has a CTE less than 10 ppm/°C, and the substrate 120 preferably consists essentially of a material such as a semiconductor, glass or ceramic. In embodiments wherein the substrate 120 is made of a semiconductor, such as silicon, a plurality of active semiconductor devices can be disposed therein. The substrate 120 can further include a dielectric layer (*e.g.*, a "passivation layer") overlying the major surface 121 and/or the second surface 122.

[0079] The microelectronic element 112 can include one or more conductive elements 140a and 140b exposed at the major surface 121 of the substrate 120. The joining portions 142a and 142b of the respective conductive elements 140a and 140b can be exposed at the major surface 121 for interconnection with a component external to the first microelectronic element 112, such as the second microelectronic element 114. Active semiconductor devices in the substrate 120 can be conductively connected to the joining portions 142a and 142b.

[0080] Each joining portion 142a and 142b can have any bottom-view shape. As shown, for example, in FIG. 3B, the joining portions 142a and 142b can have the shape of a conductive bond pad, *e.g.*, a thin flat member, or a portion of a conductive bond pad. For example, the joining portion 142b shown in FIGS. 3B and 3C has a round, solid bottom-view shape. The joining portion 142a shown in FIG. 3B has a round bottom-view shape with an aperture 147 extending therethrough. The joining portion segments 142a' shown in FIG. 3C together have a round bottom-view shape, with the aperture 147 extending therethrough and gaps 148 extending between adjacent joining portion segments.

[0081] The joining portions 142a and 142b can have other bottom-view shapes, including, for example, a rectangular trace shape or rectangular trace shape portions. For example, the joining portion 142b" shown in FIG. 3D has a rectangular

trace shape. The joining portions 142a" shown in FIG. 3D are rectangular trace-shaped portions having the aperture 147 located therebetween. The joining portions 142a and 142b can alternatively have more complex shapes. In other embodiments, the joining portions 142a and 142b can be any other type of conductive contact, including for example, a conductive post.

[0082] The joining portions 142a and 142b can be aligned with the respective recess 130a or 130b and can be disposed wholly or partly within an area of the substrate 120 defined by the recess. As seen in FIG. 3A, the joining portions 142a and 142b are wholly disposed within an area defined by the respective recess 130a or 130b. As shown, a plane defined by top surfaces 143a and 143b of the respective joining portions 142a or 142b are substantially parallel to a plane defined by the major surface 121 of the substrate 120. As shown, bottom surfaces 144a and 144b of the respective joining portions 142a or 142b are located at a plane defined by the major surface 121 of the substrate 120. In other embodiments, the bottom surfaces 144a and 144b can be located above or below the plane defined by the major surface 121.

[0083] The connecting portions 145a and 145b extend downwardly from the respective joining portions 142a or 142b to the respective anchor portion 141a or 141b. At least a portion of the connecting portions 145a and 145b have a contour not conforming to a contour of the inner surfaces 131 of the respective recess 130a or 130b. In a particular embodiment, there can be a single trace-shaped connecting portion 145b extending from the anchor portion 141b to the joining portion 142b. In alternative embodiments, there can be any number of connecting portions extending from the anchor portion. For example, in one embodiment, the connecting portion 145a can have a hollow frustoconical shape with an internal aperture 147, such as in the embodiment shown in FIG. 3B. In another embodiment, there can be four individual

connecting portions extending between a single anchor portion 141a and respective joining portions such as the joining portions 142a' shown in FIG. 3C. In still another embodiment, there can be two individual connecting portions extending between a single anchor portion 141a and respective joining portions such as the joining portions 142a" shown in FIG. 3D. The joining portions 142a and 142b preferably are non-centered relative to the respective connecting portions 145a or 145b, such that the end portion 146 of the respective conductive element 140a or 140b can be cantilevered with respect to the respective anchor portion 141a or 141b.

[0084] The recesses 130a and 130b are similar to the recess 30 shown and described above with reference to FIGS. 1A through 2D. The recesses 130a and 130b extend from the major surface 121 partially through the substrate 120 towards the second surface 122. The inner surfaces 131 of the recesses 130a and 130b can extend from the major surface 121 through the substrate 120 at any angle. Preferably, the inner surfaces 131 extend from the major surface 121 at an angle between 0 and 90 degrees to the horizontal plane defined by the major surface 121.

[0085] The recesses 130a and 130b can have any bottom-view shape, including for example, an oval, such as the recess 130b shown in FIGS. 1B-1D, or a circle, such as the recess 130a shown in FIGS. 1B and 1C. In some examples, the recesses 130a and 130b can have any three-dimensional shape, including for example, a cylinder, a cube, a prism, or a frustoconical shape, among others. In a particular embodiment, the recesses 130a and 130b can be a rectangular channel with a plurality of respective joining portions 142a and 142b at least partially overlying the recess, in a configuration similar to that of the joining portions 42 shown in FIG. 1D.

[0086] The dielectric region 150 has similar possible configurations and properties as the dielectric region 50

shown and described above with reference to FIGS. 1A through 2D. For example, in the embodiments shown in FIGS. 3A-3D, the dielectric region 150 fills the recesses 130a and 130b such that a contour of the dielectric region conforms to a contour of the recess (*i.e.*, the shape of the inner surfaces 131 of the recesses). The dielectric region 150 can be compliant, having a sufficiently low modulus of elasticity and sufficient thickness such that the product of the modulus and the thickness provide compliancy. Preferably, the joining portions 142a and 142b at least partially overlie the dielectric region 150, such that the joining portions can be movable relative to the substrate 120.

[0087] Similar to the dielectric layer 25 described above with reference to FIGS. 1A through 2D, a dielectric layer 125 can overlie the major surface 121 of the substrate 120 and portions of the conductive elements 140a and 140b that are not the joining portions 142a and 142b, to provide good dielectric isolation with respect to the substrate and the portions of the conductive elements that are not the joining portions.

[0088] As shown in FIGS. 3A-3D, the hole 160 is staged, including a first opening 161 extending from the opening 130 towards the second surface 122 and a second opening 162 extending from the first opening to the second surface. The staged hole 160 can have any of the structures shown and described in greater detail in the commonly owned U.S. Patent Application Serial No. 12/842,717, filed July 23, 2010, and the commonly owned U.S. Patent Application Publication No. 2008/0246136, which are hereby incorporated by reference herein. In other embodiments, such as the hole 60b shown and described with reference to FIG. 6, the hole can have a more simple non staged structure.

[0089] The first opening 161 extends from the recess 130 partially through the substrate 120 towards the second surface 122. The first opening 161 includes inner

surfaces 163 that extend from the recess 130 through the substrate 120 at an angle between 0 and 90 degrees to the horizontal plane defined by the major surface 121. The inner surfaces 163 can have a constant slope or a varying slope. For example, the angle or slope of the inner surfaces 163 relative to the horizontal plane defined by the major surface 121 can decrease in magnitude (*i.e.*, become less positive or less negative) as the inner surfaces 163 penetrate further towards the second surface 122. As shown, for example, in FIG. 4D, the first opening 161 has a width W1 at the recess 130 and a width W2 where the first opening meets the second opening 162 that is less than W1 such that the first opening is tapered in a direction from the major surface 121 towards the second surface 122. In other examples, the first opening can have a constant width, or the first opening can be tapered in a direction from the second surface towards the front surface. The first opening 161 can have any three-dimensional shape, including for example, cubic, cylindrical, frustoconical, or a prism, among others.

[0090] The second opening 162 extends from the first opening 161 partially through the substrate 120 towards the second surface 122. The second opening 162 includes inner surfaces 164 that extend from the first opening 161 through the substrate 120 at an angle between 0 and 90 degrees to the horizontal plane defined by the major surface 121. Similar to the inner surfaces 163 described above, the inner surfaces 164 can have a constant slope or a varying slope. As shown, for example, in FIG. 4D, the second opening 162 has a width W3 where the second opening meets the first opening 161 and a width W4 at the second surface 122 that is greater than W3 such that the first opening is tapered in a direction from the second surface 122 towards the major surface 121. In other examples, the second opening can have a constant width, or the second opening can be tapered in a direction from the front

surface towards the second surface. The second opening 162 can have any three-dimensional shape, including for example, cubic, cylindrical, frustoconical, or a prism, among others.

[0091] In a particular embodiment, the inner surfaces 163 and 164 can extend in first and second directions relative to the major surface 121, respectively, to define a substantial angle. Any number of first openings 161 can extend from a single second opening 162, and any number of second openings can extend from a single first opening. The first and second openings 161 and 162 can be arranged in any geometric configuration relative to each other and relative to the substrate 120. Particular examples of various first and second opening configurations and methods of forming these configurations are described in the aforementioned commonly owned U.S. Patent Application Serial No. 12/842,717 and U.S. Patent Application Publication No. 2008/0246136.

[0092] The anchor portions 141a and 141b of the respective conductive elements 140a and 140b preferably have contours that conform to a contour of the respective first opening 161, such that the anchor portions have positions that are fixed relative to the substrate 120. An anchor portion 141a or 141b can serve as a fulcrum about which an attached joining portion 142a or 142b can pivot when put under mechanical stress such as that caused by differential thermal expansion relative to an attached microelectronic unit.

[0093] The conductive via 170 extends through the hole 160 between the respective anchor portion 141a or 141b and the second surface 122. As shown in FIG. 3A, the conductive via 170 can fill all of the volume within the second opening 162 inside of an optional dielectric layer (not shown) that can electrically insulate the substrate 120 from the conductive via. The conductive via 170 can conform to the contour of the second opening 162. The conductive via 170 may have a cylindrical or frustoconical shape. The conductive via 170

can be made from a metal or an electrically conductive compound of a metal, including for example, copper or gold.

[0094] In other embodiments (not shown), a contour of the conductive via 170 (*i.e.*, the shape of the outer surface of the conductive via) does not conform to a contour of the second opening 162 (*i.e.*, the shape of the inner surface 164 of the second opening). In such non-conformal conductive via embodiments, the conductive via 170 can have any shape, including for example, a cylindrical shape, frustoconical shape, or a combination of a cylindrical and a frusto-conical shape at different distances from the second surface 122.

[0095] The conductive via 170 can be solid or hollow. In some embodiments, the conductive via can include an internal space that is filled with a dielectric material. For example, the conductive via 170 can be formed by depositing a metal overlying the inner surface 164 of the second opening 162, thereby producing a conductive layer overlying the inner surface second opening. Particular examples of various conductive via configurations and methods of forming these configurations are described in the aforementioned commonly owned U.S. Patent Application Serial No. 12/842,717 and U.S. Patent Application Publication No. 2008/0246136.

[0096] The conductive vias 170 each include a contact portion 180 exposed at the second surface 122 for interconnection with a component external to the stacked microelectronic assembly 110. In some embodiments, each conductive via 170 can be electrically coupled to a separate conductive contact exposed at the second surface 122.

[0097] The second microelectronic unit 114 is similar to the second microelectronic unit 14 shown and described above with reference to FIG. 1A. The second microelectronic unit 114 can include a substrate 115 and conductive contacts 116 at least partially exposed at a major surface 117 of the

substrate for interconnection with the joining portions 142a and 142b of the first microelectronic unit 112.

[0098] As shown in FIG. 3A, the conductive contacts 116 are conductive pads. The conductive pads 116 can have any shape, including circular, square, oblong, rectangular, or a more complex shape. In particular embodiments, the conductive contacts 116 can be any type of conductive contact, including, for example, a conductive post such as the conductive post 16a shown in FIG. 1A. Other examples of conductive posts can be used, as shown and described in the commonly-owned U.S. patent application no. 12/832,376, filed on July 8, 2010.

[0099] Connection between the first microelectronic unit 112 and the second microelectronic unit 114 can be through conductive masses 118, in a manner similar to that described with reference to FIGS. 1A through 2D. The dielectric layer 125 and the dielectric region 150 at the major surface 121 of the substrate 120 and a dielectric layer (e.g., a passivation layer) overlying the major surface 117 of the substrate 115 can provide electrical isolation between the first microelectronic unit 112 and the second microelectronic unit 114 except where interconnection is provided.

[0100] A method of fabricating the microelectronic assembly 110 (FIGS. 3A-3D) will now be described, with reference to FIGS. 4A-4D. In the stage of fabrication illustrated in FIG. 4A, the first microelectronic unit 112 includes the substrate 120. The holes 160 can be formed extending from the major surface 121 to the second surface 122 of the substrate 120 by removing material from the substrate. In a particular embodiment, the first opening 161 can be formed extending inwardly from the major surface 121, and the second opening can be formed extending inwardly from the second surface 122. In other embodiments, either or both of the first and second openings 161 and 162 can be formed from either the major or second surfaces 121 and 122.

[0101] The holes 160 can be formed in a similar manner and using similar processes as described above with respect to forming the recess 30. For example, the holes 160 can be formed by selectively etching the substrate 120 to remove material of the substrate, after forming a mask layer where it is desired to preserve remaining portions of the major surface 121. Similar to the recess 30, the inner surfaces 163 and 164 of the first and second openings 161 and 162 can extend at any constant or variable angle relative to the major surface 121.

[0102] Although not shown, a dielectric layer can optionally be formed on the major surface 121 of the substrate 120 and/or overlying the inner surfaces 163 and 164 of the first and second openings 161 and 162 to provide electrical isolation of the conductive elements 140a and 140b and the conductive vias 170 from the substrate. Such a dielectric layer can be formed using any of the various methods described above with reference to the dielectric layer 25 shown in FIG. 2B. Such a dielectric layer can be in addition of or instead of a passivation layer that may already be overlying the major surface 121 of the substrates 120.

[0103] In the stage of fabrication illustrated in FIG. 4B, the anchor portions 141a and 141b and the respective connecting portions 145a and 145b of the conductive elements 140a and 140b can be formed within the first openings 161, the joining portions 142a and 142b can be formed overlying the major surface 121, and the conductive vias 170 can be formed within the second openings 162, with the contact portion 180 exposed at the second surface 122. Each of the anchor portions 141a and 141b, the connecting portions 145a and 145b, the joining portions 142a and 142b, and the conductive vias 170 can be formed in a single metal deposition process or separate processes. In an embodiment where the conductive vias 170 are electrically coupled to separate conductive contacts exposed at the second surface 122, such conductive

contacts can be formed in a single metal deposition process along with the conductive elements 140a and 140b and the conductive vias, or such conductive contacts can be formed in a separate process.

[0104] An exemplary method of forming the conductive elements 140a and 140b and the conductive vias 170 involves depositing a metal layer by one or more of sputtering a primary metal layer onto exposed surfaces of the substrate 120, plating, or mechanical deposition. Mechanical deposition can involve the directing a stream of heated metal particles at high speed onto the surface to be coated. This step can be performed by blanket deposition onto the major surface 121 and the inner surfaces 163 and 164, for example. In one embodiment, the primary metal layer includes or consists essentially of aluminum. In another particular embodiment, the primary metal layer includes or consists essentially of copper. In yet another embodiment, the primary metal layer includes or consists essentially of titanium. One or more other exemplary metals can be used in a process to form the conductive elements 140a and 140b and the conductive vias 170. In particular examples, a stack including a plurality of metal layers can be formed on one or more of the afore-mentioned surfaces. For example, such stacked metal layers can include a layer of titanium followed by a layer of copper overlying the titanium (Ti-Cu), a layer of nickel followed by a layer of copper overlying the nickel layer (Ni-Cu), a stack of nickel-titanium-copper (Ni-Ti-Cu) provided in similar manner, or a stack of nickel-vanadium (Ni-V), for example.

[0105] In a particular embodiment, the joining portions 142a and 142b can be deposited onto the major surface 121 of the substrate 120 before removing any material from the substrate, for example, as shown in the stage of fabrication illustrated in FIG. 2A. In such an embodiment, the holes 160 can be formed, for example, by etching through the joining

portions 142a and/or 142b and then etching into the substrate 120. After the holes 160 are formed through the joining portions 142a and/or 142b, the connecting portions 145a and 145b, the anchor portions 141a and 141b, and the conductive vias 170 can be formed as described above.

[0106] In the stage of fabrication illustrated in FIG. 4C, the dielectric layer 125 is formed on the major surface 121 of the substrate 120 and serves as an etch mask layer where it is desired to preserve remaining portions of the major surface. The dielectric layer 125 can be formed using any of the various methods described above with reference to the dielectric layer 25 shown in FIG. 2B. The joining portions 142a and 142b can remain at least partially exposed at the major surface 121 (*i.e.*, not covered by the dielectric layer 125) for connection to a component external to the first microelectronic unit 112.

[0107] Thereafter, in the stage of fabrication illustrated in FIG. 4D, the recesses 130 can be formed in a similar manner and using similar processes as described above with respect to forming the recess 30. For example, the recesses 130 can be formed by selectively etching the substrate 120 to remove material of the substrate, after forming a mask layer (*e.g.*, the dielectric layer 25) where it is desired to preserve remaining portions of the major surface 121. The recess 130 can be formed such that material of the substrate 120 supporting at least the joining portions 142a and 142b is removed. Similar to the recess 30, the inner surfaces 131 of the recesses 130 can extend at any constant or variable angle relative to the major surface 121.

[0108] As shown in FIG. 4D, the recesses 130 can be formed such that they do not extend as far from the major surface 121 as the first openings 161, such that contours of the anchor portions 141a and 141b conform to a contour of the remaining part of the inner surface 163 of the first opening. In a

particular embodiment, the recesses 130 can be formed such that they extend at least as far from the major surface 121 as the first openings 121, such that the contours of the anchor portions 141a and 141b do not conform to contours of any inner surfaces of the substrate 120. In such an embodiment, the anchor portions 141a and 141b can be fixed to the substrate 120 through the attachment between the anchor portions and the conductive vias 170 that can have contours that conform to contours of the inner surfaces 164 of the second openings 162.

[0109] Thereafter, in the stage of fabrication illustrated in FIG. 4E, the dielectric regions 150 can be formed inside the recesses 130 in a similar manner and using similar processes as described above with respect to forming the dielectric region 50 inside the recess 30. For example, the dielectric region 150 can be formed such that an exposed outer surface 151 of the region is co-planar or substantially co-planar with the major surface 121 of the substrate 120 (as shown in FIG. 4E) or an exposed surface of the dielectric layer 125.

[0110] Thereafter, referring again to FIG. 3A, the first microelectronic unit 112 can be stacked on top of the second microelectronic unit 114, thereby forming the stacked microelectronic assembly 110. As described above, connection between the first microelectronic unit 112 and the second microelectronic unit 114 can be through conductive masses 118. The conductive masses 118 can provide an electrical connection between the joining portions 142a and 142b of the first microelectronic unit 112 and the conductive contacts 16 of the second microelectronic unit 114. In such arrangement, the joining portions 142a and 142b are aligned with the respective conductive contacts 16.

[0111] As shown in FIG. 5, a base portion 241 and a joining portion 242 of a conductive element 240 is shown that is suitable for use in any of the embodiments described above

with reference to FIGS. 1A-4E. The joining portion 242 extends from the base portion 241 of the conductive element 240. The base portion 241 can be, for example, part of the joining portion 142a or 142b described above with reference to the first microelectronic unit 112 shown in FIG. 3A, or part of the anchor portion 41 described above with reference to the first microelectronic unit 12 shown in FIG. 1A. The base portion 241 can be connected to other conductive elements located beneath the major surface 221 of the substrate 220 or beneath an outer surface 251 of the dielectric region 250. In the embodiment shown in FIG. 5, the base portion 241 includes a segment 243 that is compliant or movable in a direction of a plate defined by the major surface 221, such that the segment is capable of being displaced in a direction along the major surface 221 by an external load applied thereto.

[0112] Referring now to FIG. 6, a first microelectronic assembly 12' according to another embodiment is similar to the first microelectronic assembly 12 shown in FIG. 1A, except that the conductive elements 40' are electrically connected to conductive vias 70a and 70b extending between the major surface 21 and the second surface 22 of the substrate 20'.

[0113] The substrate 20' includes holes 60a and 60b extending from the major surface 21 and the second surface 22, and the conductive vias 70a and 70b extend within the respective holes from respective anchor portions 41' of the conductive elements 40' to the second surface. Each conductive via 70a and 70b includes a contact portion 80 exposed at the second surface 22 for interconnection with a component external to the first microelectronic unit 12'. The hole 60a is a staged hole similar to the holes 160 shown in FIG. 3A, except that the openings 30 do not overlap with either of the holes 60a or 60b, so the holes 60a and 60b extend from the second surface 22 to the major surface 21, rather than from the second surface to a respective opening.

The hole 60b is not staged, *i.e.*, the hole 60b can be formed, for example, in a single etching or other process of removing material from the substrate 20'.

[0114] Similar to the first microelectronic assembly 12 shown in FIG. 1A, each conductive element 40 includes a joining portion 42 that can be exposed at the major surface 21 for interconnection with a component external to the first microelectronic element 12'. Also similar to the first microelectronic assembly 12, the dielectric regions 50 can be compliant, such that each joining portion 42 can be movable relative to the substrate 20'.

[0115] FIG. 7 depicts a module 300 including at least two microelectronic assemblies 310 arranged together in one unit having an electrical interface 320 for transport of signals to and from each of the microelectronic assemblies 310. The electrical interface can include one or more contacts usable for transport of signals or reference potentials, e.g., power and ground, which are common to each of the microelectronic elements therein. The microelectronic assemblies 310 may be any of the assemblies described above. In a particular example, the module 300 can be a dual in-line memory module ("DIMM") or single in-line memory module ("SIMM") having one or more portions thereof sized for insertion into a corresponding slot of other connector of a system, such as can be provided on a motherboard. In such DIMM or SIMM, the electrical interface can have contacts 330 that are suitable for mating with a plurality of corresponding spring contacts within such slot connector. Such spring contacts can be disposed on single or multiple sides of each slot to mate with corresponding module contacts. Various other modules and interconnection arrangements are possible in which a module may have unstacked or stacked microelectronic assemblies, or which may have parallel or serial electrical interfaces, or a combination of parallel and serial electrical interfaces for

transport of electrical signals to and from the module. Any kind of electrical interconnection arrangement between the module 300 and a further system interface is contemplated by the invention.

[0116] The microelectronic assemblies described above can be utilized in construction of diverse electronic systems, as shown in FIG. 8. For example, a system 400 in accordance with a further embodiment of the invention includes a microelectronic assembly 406 as described above in conjunction with other electronic components 408 and 410. In the example depicted, component 408 is a semiconductor chip whereas component 410 is a display screen, but any other components can be used. Of course, although only two additional components are depicted in FIG. 8 for clarity of illustration, the system may include any number of such components. The microelectronic assembly 406 may be any of the assemblies described above. In a further variant, any number of such microelectronic assemblies may be used.

[0117] Microelectronic assembly 406 and components 408 and 410 are mounted in a common housing 401, schematically depicted in broken lines, and are electrically interconnected with one another as necessary to form the desired circuit. In the exemplary system shown, the system includes a circuit panel 402 such as a flexible printed circuit board, and the circuit panel includes numerous conductors 404, of which only one is depicted in FIG. 8, interconnecting the components with one another. However, this is merely exemplary; any suitable structure for making electrical connections can be used.

[0118] The housing 401 is depicted as a portable housing of the type usable, for example, in a cellular telephone or personal digital assistant, and screen 410 is exposed at the surface of the housing. Where structure 406 includes a light-sensitive element such as an imaging chip, a lens 411 or other optical device also may be provided for routing light to the

structure. Again, the simplified system shown in FIG. 8 is merely exemplary; other systems, including systems commonly regarded as fixed structures, such as desktop computers, routers and the like can be made using the structures discussed above.

[0119] The vias and via conductors disclosed herein can be formed by processes such as those disclosed in greater detail in the co-pending, commonly assigned United States Patent Application Nos. 12/842,587, 12/842,612, 12/842,651, 12/842,669, 12/842,692, and 12/842,717, filed July 23, 2010, and in published U.S. Patent Application Publication No. 2008/0246136, the disclosures of which are incorporated by reference herein.

[0120] Although the invention herein has been described with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present invention. It is therefore to be understood that numerous modifications may be made to the illustrative embodiments and that other arrangements may be devised without departing from the spirit and scope of the present invention as defined by the appended claims.

[0121] It will be appreciated that the various dependent claims and the features set forth therein can be combined in different ways than presented in the initial claims. It will also be appreciated that the features described in connection with individual embodiments may be shared with others of the described embodiments.

INDUSTRIAL APPLICABILITY

[0122] The present invention enjoys wide industrial applicability including, but not limited to, microelectronic units and methods of fabricating microelectronic units.

CLAIMS

1. A microelectronic unit, comprising:

a substrate having a CTE less than 10 ppm/°C, a major surface having a recess not extending through the substrate, and a material having a modulus of elasticity less than 10 GPa disposed within the recess; and

an electrically conductive element including a joining portion overlying the recess and extending from an anchor portion supported by the substrate, the joining portion being at least partially exposed at the major surface for connection to a component external to the microelectronic unit.

2. The microelectronic unit as claimed in claim 1, wherein the substrate has a CTE less than 7 ppm/°C.

3. The microelectronic unit as claimed in claim 1, wherein the joining portion is movable so as to reduce stresses on the joining portion, such as may be present during operation, manufacturing, or testing of the microelectronic unit.

4. The microelectronic unit as claimed in claim 1, wherein the substrate consists essentially of one material selected from the group consisting of: semiconductor, glass, and ceramic.

5. The microelectronic unit as claimed in claim 1, wherein the substrate includes a plurality of active semiconductor devices and the conductive element is electrically connected with at least one of the plurality of active semiconductor devices.

6. The microelectronic unit as claimed in claim 1, wherein the material disposed within the recess includes at least one material selected from the group consisting of: polyimide, silicone, and epoxy.

7. The microelectronic unit as claimed in claim 1, wherein the recess does not extend through the substrate.

8. The microelectronic unit as claimed in claim 1, wherein the joining portion extends in a direction substantially parallel to the major surface of the substrate.

9. The microelectronic unit as claimed in claim 1, wherein the anchor portion and the joining portion extend in the same direction.

10. The microelectronic unit as claimed in claim 9, wherein the conductive element is electrically coupled with a conductive via extending towards a second surface of the substrate opposite the major surface.

11. The microelectronic unit as claimed in claim 10, wherein the conductive via is exposed at the second surface.

12. The microelectronic unit as claimed in claim 10, wherein the conductive via extends within a hole in the substrate extending from the second surface to the major surface.

13. The microelectronic unit as claimed in claim 12, wherein the hole includes a first opening extending from the major surface towards the second surface and a second opening extending from the first opening to the second surface, wherein inner surfaces of the first and second openings extend in first and second directions relative to the major surface, respectively, to define a substantial angle.

14. A stacked assembly including at least first and second microelectronic units, the first microelectronic unit being as claimed in claim 1, the second microelectronic unit being stacked with the first microelectronic unit, with the substrate of the first microelectronic unit therein being electrically connected with a substrate of the second microelectronic unit.

15. A stacked assembly as claimed in claim 14, further comprising a conductive mass electrically coupled to the

joining portion of the first microelectronic unit and a conductive element of the second microelectronic unit.

16. A system comprising a structure according to claim 1 and one or more other electronic components electrically connected to the structure.

17. A system as claimed in claim 16, further comprising a housing, said structure and said other electronic components being mounted to said housing.

18. A module including a plurality of microelectronic assemblies according to any one of claim 1, the module having a common electrical interface for transport of signals to and from each of said microelectronic assemblies.

19. A method of fabricating a microelectronic unit, comprising:

forming an electrically conductive element supported on a major surface of a substrate having a CTE less than 10 ppm/°C;

removing material supporting at least a joining portion of the conductive element from the major surface to form a recess not extending through the substrate, such that the joining portion is not supported by the substrate while an anchor portion of the conductive element adjacent the joining portion is supported by the substrate; and

depositing a material within the recess having a modulus of elasticity less than 10 GPa,

wherein the joining portion is at least partially exposed at the major surface of the substrate for connection to a component external to the microelectronic unit.

20. The method as claimed in claim 19, wherein the substrate has a CTE less than 7 ppm/°C.

21. The method as claimed in claim 19, wherein the substrate consists essentially of one material selected from the group consisting of: semiconductor, glass, and ceramic.

22. The method as claimed in claim 19, wherein the substrate includes a plurality of active semiconductor devices, and the step of forming the conductive element electrically connects the conductive element with at least one of the plurality of active semiconductor devices.

23. The method as claimed in claim 19, wherein the step of forming the conductive element is performed such that the joining portion is disposed substantially parallel to the major surface.

24. The method as claimed in claim 19, further comprising:

removing material from the substrate to form a hole extending from the major surface to a second surface of the substrate opposite the major surface; and

forming a conductive via extending within the hole such that the conductive via is electrically coupled with the conductive element and extends towards the second surface.

25. The method as claimed in claim 24, wherein the step of removing material from the substrate to form a hole includes forming a first opening extending from the major surface towards the second surface and a second opening extending from the first opening to the second surface, wherein inner surfaces of the first and second openings extend in first and second directions relative to the major surface, respectively, to define a substantial angle.

26. A method of fabricating a stacked assembly including at least first and second microelectronic units, the first microelectronic unit being fabricated as claimed in claim 19, further comprising the step of electrically connecting the substrate of the first microelectronic unit to a substrate of the second microelectronic unit.

27. A method of fabricating a microelectronic unit, comprising:

removing material from a substrate having a CTE less than 10 ppm/°C to form a hole extending from a major surface of the substrate to a second surface opposite the major surface;

forming an electrically conductive element having a joining portion extending above and supported on the major surface, an anchor portion fixed relative to the substrate, and a connecting portion extending downwardly from the joining portion to the anchor portion, a surface of the connecting portion having a contour conforming to a contour of an inner surface of the hole;

removing material supporting at least a joining portion of the conductive element from the major surface to form a recess such that the joining portion at least partially overlies the recess, and such that the contour of the surface of the connecting portion does not conform to a contour of an inner surface of the recess; and

depositing a material within the recess having a modulus of elasticity less than 10 GPa,

wherein the joining portion is at least partially exposed at the major surface of the substrate for connection to a component external to the microelectronic unit.

28. The method as claimed in claim 27, wherein the substrate has a CTE less than 7 ppm/°C.

29. The method as claimed in claim 27, further comprising, before the step of forming the conductive element, forming a conductive via extending within the hole and extending towards the second surface, such that the step of forming the conductive element electrically couples the conductive element with the conductive via.

30. The method as claimed in claim 27, wherein the step of forming the conductive element is performed such that the joining portion is non-centered relative to the connecting portion.

31. The method as claimed in claim 27, wherein the substrate consists essentially of one material selected from the group consisting of: semiconductor, glass, and ceramic.

32. The method as claimed in claim 27, wherein the substrate includes a plurality of active semiconductor devices, and the step of forming the conductive element electrically connects the conductive element with at least one of the plurality of active semiconductor devices.

33. The method as claimed in claim 27, wherein the step of forming the conductive element is performed such that the joining portion defines an internal aperture.

34. The method as claimed in claim 33, wherein the step of forming the conductive element is performed such that the aperture extends through the joining portion into the connecting portion.

35. The method as claimed in claim 34, further comprising depositing a dielectric material into at least a portion of the aperture.

36. The method as claimed in claim 27, wherein the step of removing material from the substrate to form a hole includes forming a first opening extending from the major surface towards the second surface and a second opening extending from the first opening to the second surface, wherein inner surfaces of the first and second openings extend in first and second directions relative to the major surface, respectively, to define a substantial angle.

37. A method of fabricating a stacked assembly including at least first and second microelectronic units, the first microelectronic unit being fabricated as claimed in claim 27, further comprising the step of electrically connecting the substrate of the first microelectronic unit to a substrate of the second microelectronic unit.

FIG. 1A

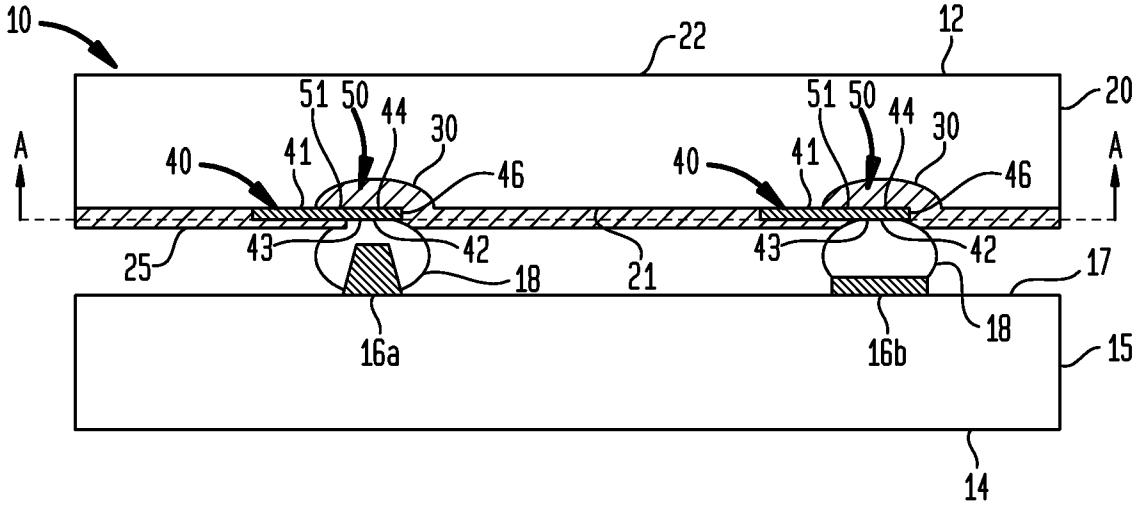

FIG. 1B

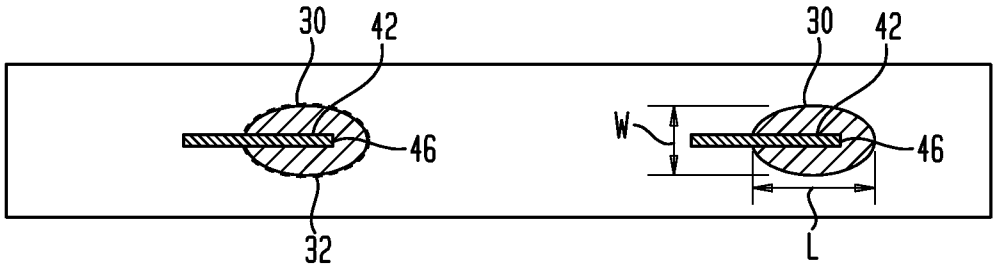

FIG. 1C

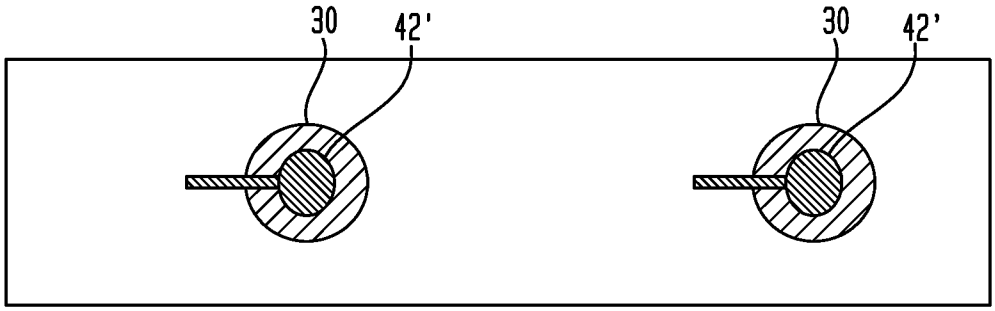

FIG. 1D

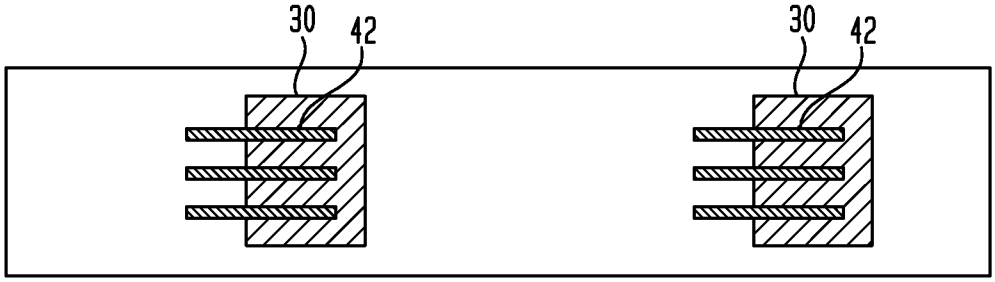

FIG. 2A

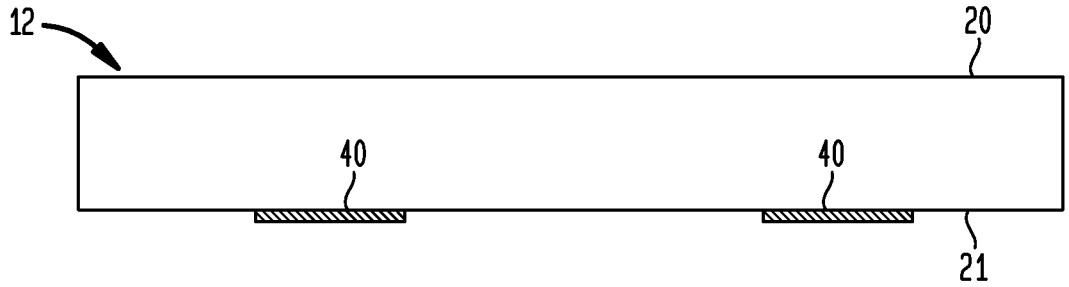

FIG. 2B

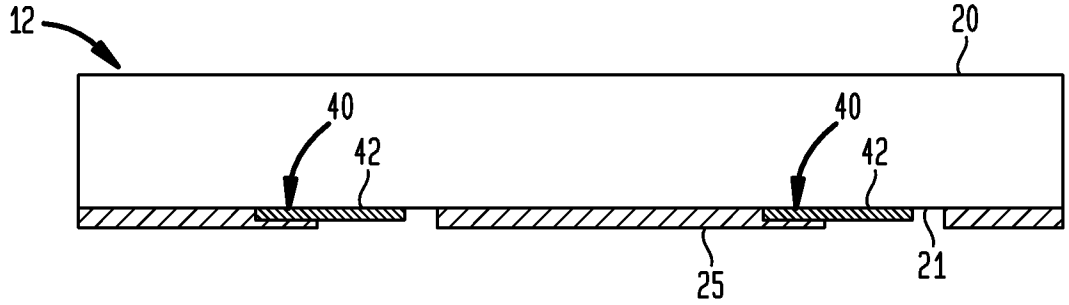

FIG. 2C

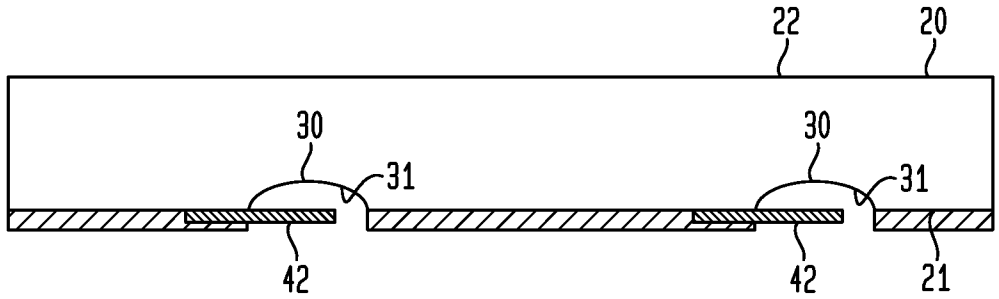

FIG. 2D

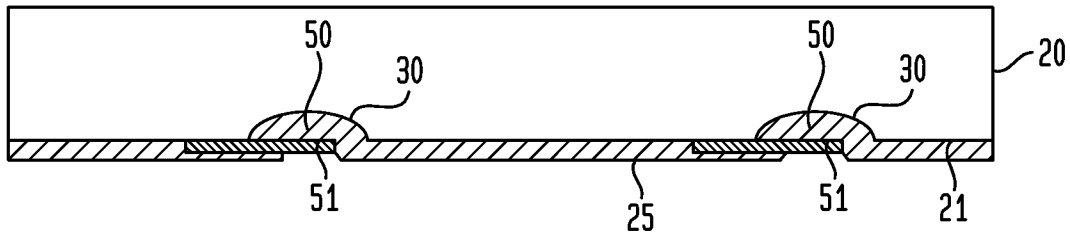

FIG. 3A

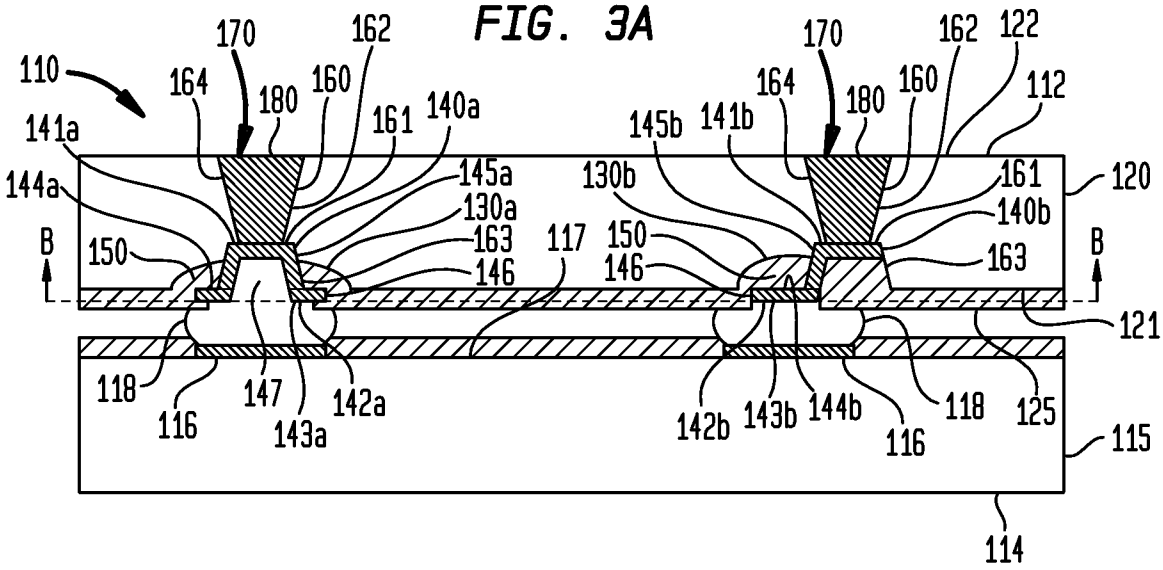

FIG. 3B

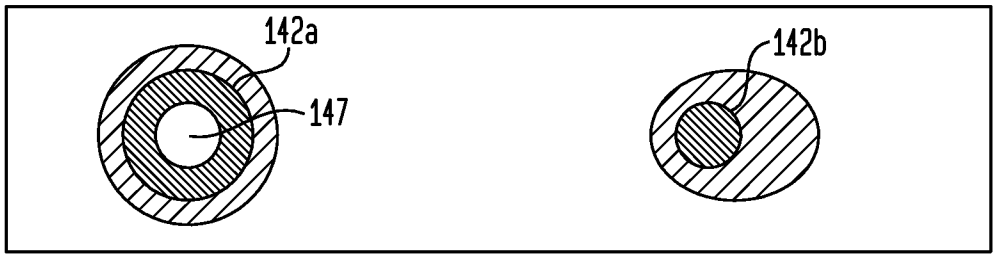

FIG. 3C

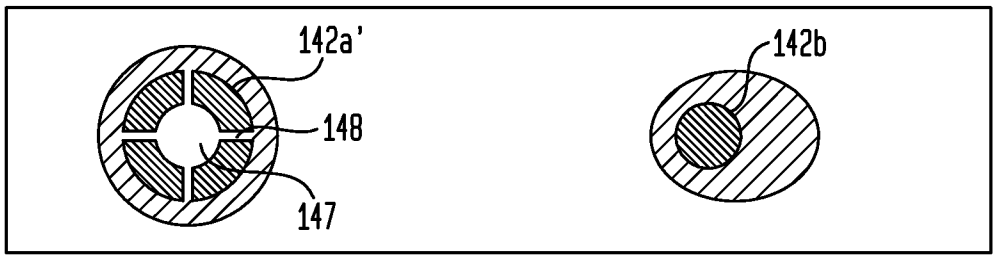

FIG. 3D

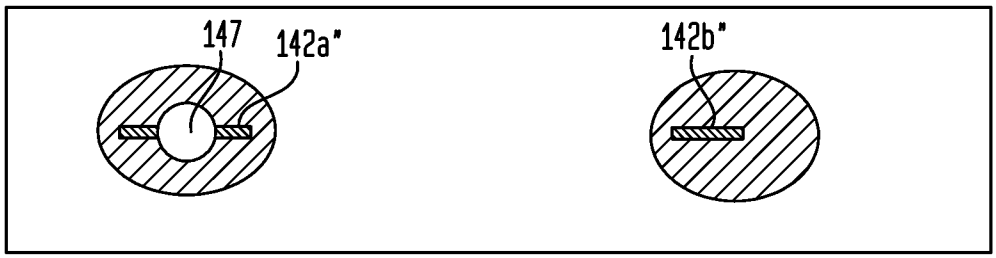

FIG. 4A

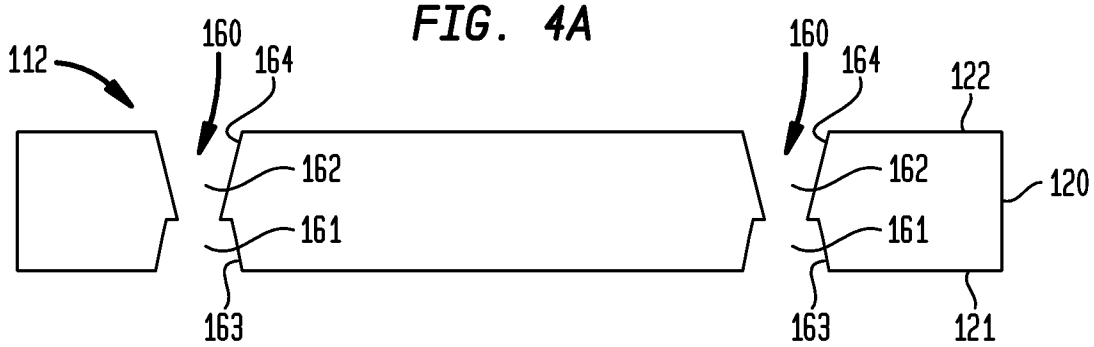

FIG. 4B

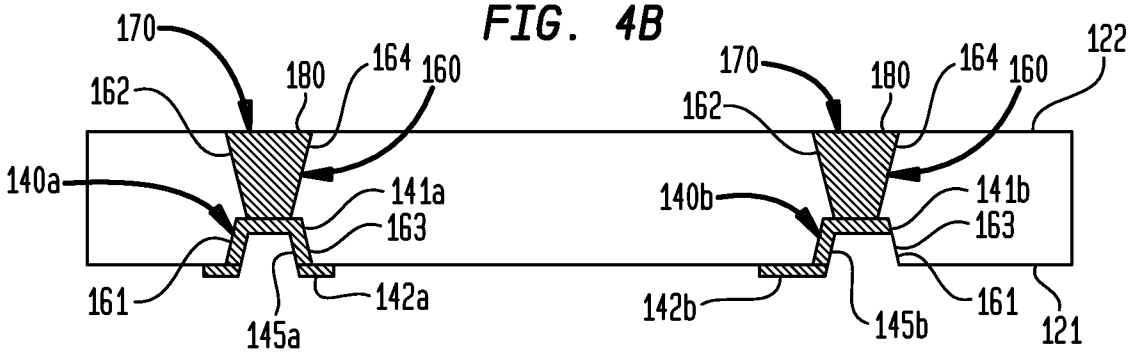

FIG. 4C

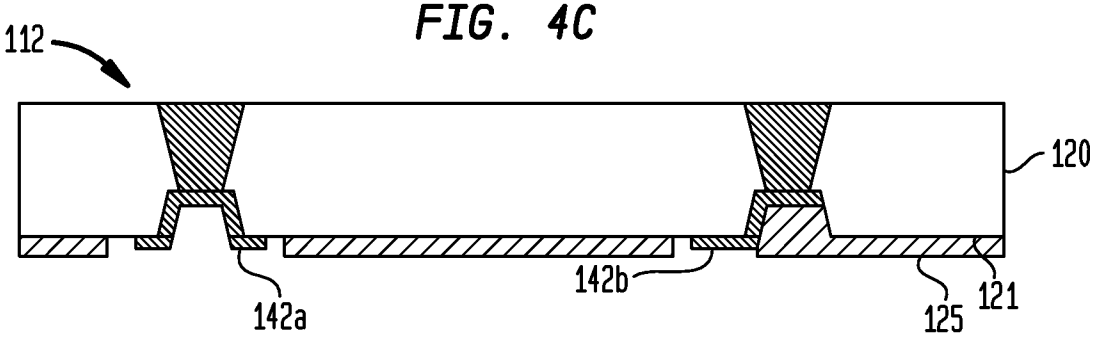

FIG. 4D

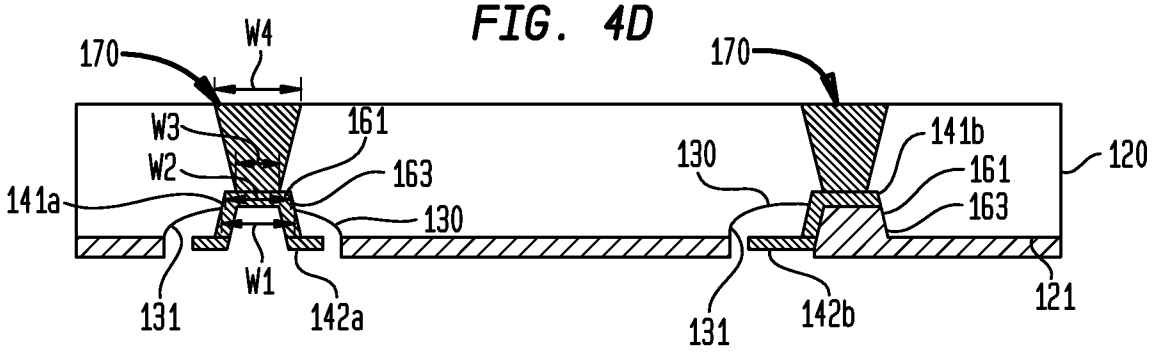

FIG. 4E

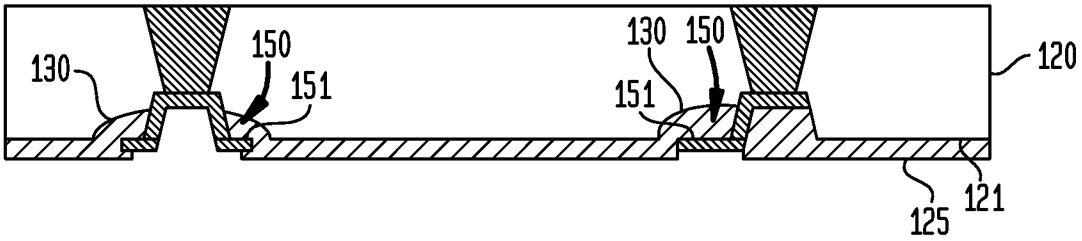

FIG. 5

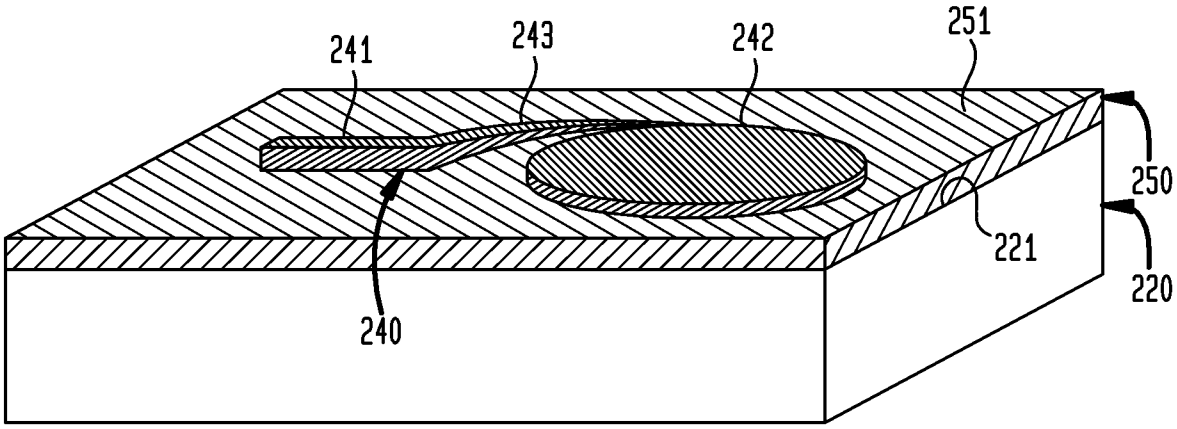

FIG. 6

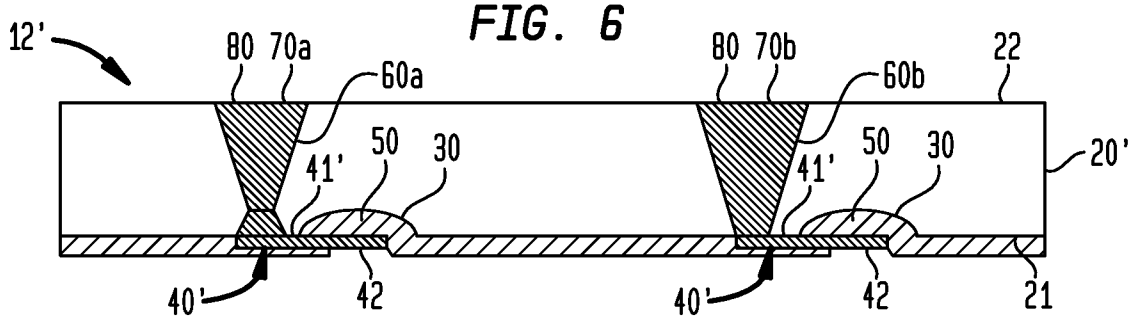

FIG. 7

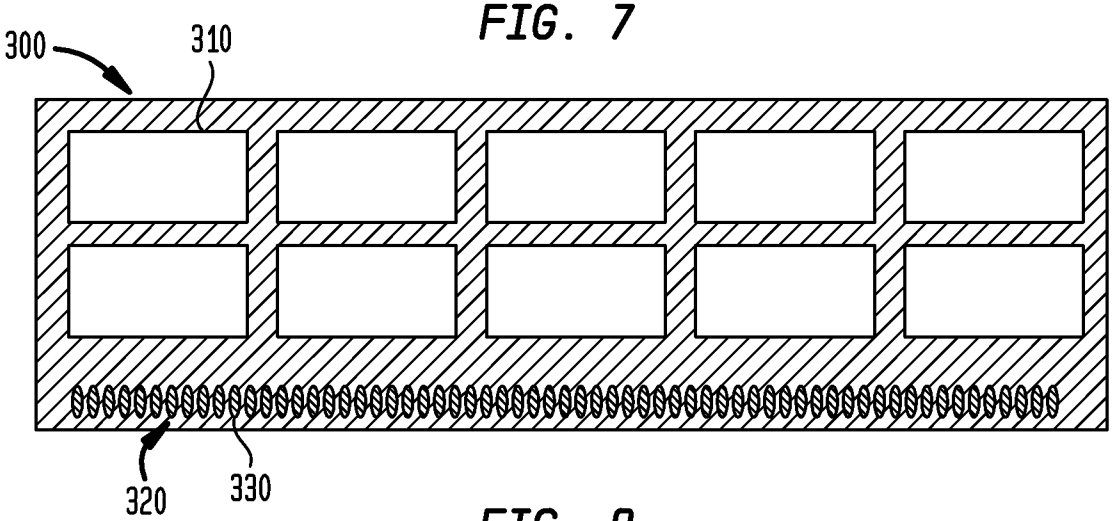

FIG. 8