Nov. 12, 1963 A. E. BREWSTER 3,110,895

CODERS FOR ELECTRIC PULSE CODE MODULATION SYSTEMS

Filed June 9, 1960

FIG. 1.

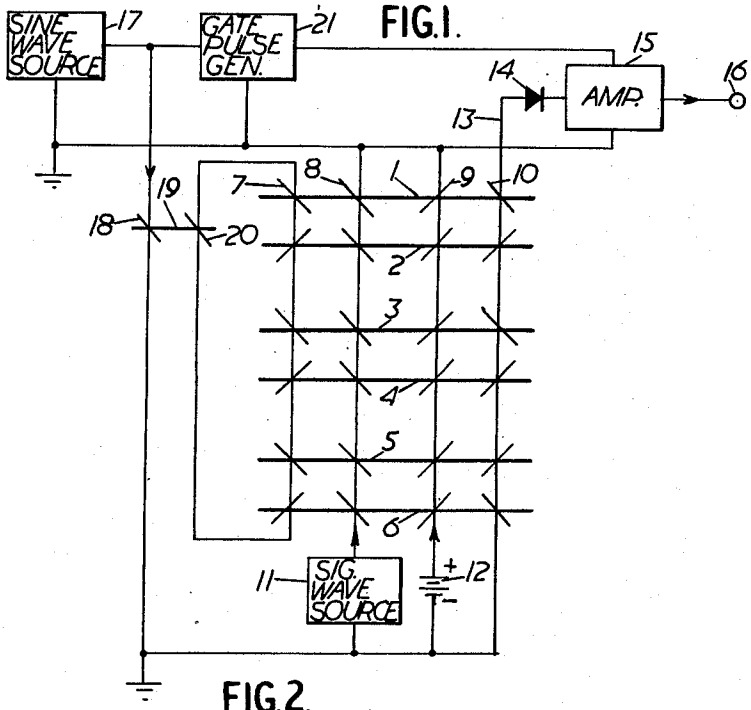
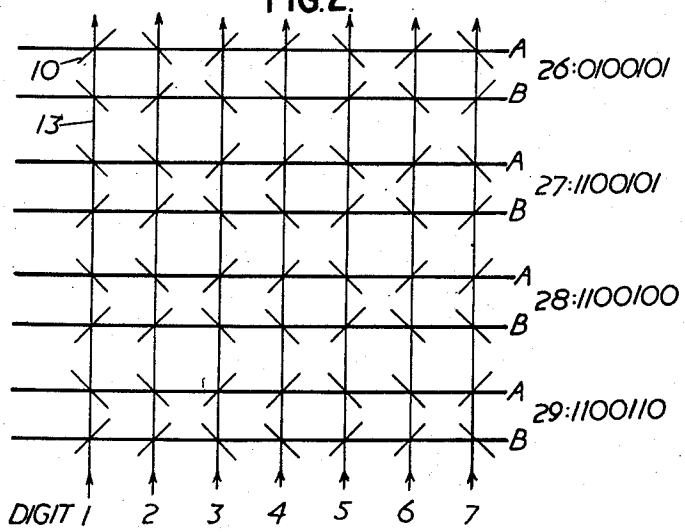


FIG. 2.



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CODERS FOR ELECTRIC PULSE CODE MODULATION SYSTEMS

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10 Claims. (Cl. 340—347)

The present invention relates to magnetic trigger devices such as are used, for example, in coding arrangements for electric pulse code modulation systems of communication.

The invention consists in an improvement in, or modification of, the invention described and claimed in the specification of co-pending application of A. E. Brewster, assigned to the same assignee as the present application, entitled "Magnetic Trigger Devices," Serial No. 840,770 filed September 17, 1959, which for convenience will be referred to as the parent specification.

In the pulse coders employing magnetic core trigger devices, described in the specification of copending application of A. E. Brewster, assigned to the same assignee as the present application, entitled "Magnetic Information Storage Arrangement," Serial No. 819,089, filed June 9, 1959, the quantising levels are determined by a group of cores of saturable ferromagnetic material, such as a ferrite material, with appropriate windings, one core corresponding to each level. The cores are all differently biassed, and the signal wave to be coded is supplied to windings on all the cores. The arrangement is such that all the cores are saturated except the one in which the flux due to the signal wave substantially cancels the bias flux. This core is the only one which can be triggered by an applied sampling pulse, and the core bears output digit windings which generate the digit pulse combination appropriate to the corresponding signal level.

This arrangement has proved inadequate when the signal wave variations are relatively rapid, because spurious outputs may be obtained directly in response to these variations, and also because the variations may effectively annul the effect of the sampling pulse, so that no core is triggered, and a code combination is missed out. The parent specification describes an arrangement in which a pair of cores is used to define each signal level, by which these difficulties are overcome.

The type of coder concerned, whether or not incorporating the features of the parent specification, has also another defect which is due to the fact that the hysteresis loop of the ferromagnetic material of which the cores are composed departs from the ideal rectangular form. The basic assumption which is made is that when the triggering pulse is applied to the cores, no appreciable flux change occurs in any core except the one which is triggered, that is, has its condition of saturation reversed. In practice, however, a core is never completely saturated, so that the flux continues to increase as the applied field is increased above the assumed "saturation" point; and further the curvature at the upper and lower "knees" of the curve is not negligible and increases this effect. It follows that in response to a sampling pulse, every core besides the one which is triggered produces a "sneak" pulse which is not negligible.

In order to minimize the effect of these "sneak" pulses it has been hitherto necessary to use large quantum bias increments for the cores of successive levels, and this results in the use of large currents in the windings. Considerable power dissipation therefore occurs with excessive temperature rise. This has reacted indirectly on the choice of the core material and on the core size, so that the hysteresis losses are large and the speed of operation is reduced. Furthermore, the necessity for supplying large currents means that the controlling circuits must have relatively large power capacity.

These difficulties have also militated against the use of a single coder in common to a number of channels in a multichannel system, because such a coder is in continuous operation and has no idle periods during which it can cool.

The object of the present invention is to modify and improve the coding arrangement of the parent specification so that the effect of the "sneak" pulses is greatly reduced, thus enabling smaller control currents to be used with the coder.

The invention will be described with reference to the accompanying drawing, in which:

FIG. 1 shows a schematic circuit diagram of part of a coder illustrating the features of the invention; and

FIG. 2 shows a schematic circuit diagram to illustrate the manner in which the digit windings are applied to the cores of FIG. 1.

The codes commonly used in pulse code modulation systems are binary codes in which each combination comprises a fixed number of code element periods. Digit pulses are present in some of these element periods and absent in others. Accordingly each coding core has hitherto been provided with only such digit output windings as correspond to the digit pulses which have to be present in the corresponding code combination. According to the present invention, each core is further provided with reverse digit output windings corresponding to the digit pulses which are absent so that the coder effectively produces code combinations of positive and negative digit pulses, instead of combinations of digit pulses and blanks. In order to produce the code combinations in the usual form, all the digit pulses of one sign may be eliminated by conventional means. This arrangement causes substantial cancellation of the "sneak" pulses for the following reason. If one particular digit position be considered in the case of the ordinary or cyclic permutation binary code, half the code combinations have a digit pulse in the digit position considered, and the other half have no digit pulse. Thus in the case of the arrangement according to the invention in which all the output digit windings are in series, approximately half the "sneak" pulses will be in one direction and the other half will be in the opposite direction, and on the assumption that all the "sneak" pulses are of equal amplitude, the "sneak," output will be practically zero. In practice, of course, the amplitude of the "sneak" pulse from any core depends on the total effective bias of that core, but on the whole, there will be very substantial cancellation of the "sneak" output.

This advantage is not limited to the particular codes just mentioned, but is obtained with any form of the binary code which is such that for any digit position, the number of combinations having a digit pulse in that position is substantially equal to the number having a blank.

In FIG. 1 there are shown three pairs of magnetic cores, which for clearness will be assumed to form part of a coder for producing a 7-digit unit-disparity cyclic permutation binary code, such as is described in the specification of British application No. 11905/58 of H. Grayson, K. W. Cattermole, and W. Neu which matured into British Patent No. 849,891 on January 18, 1961. The code described therein is an improved form of cyclic permutation binary code for use in code systems employing extremely high pulse repetition frequencies. The code is so arranged that the code group representing the sampled amplitude of a signal to be transmitted always consists of an equal number of marks and spaces. The coder may be assumed to be arranged on the lines of that illustrated in FIGS. 7 and 8 of the specification of above cited co-pending application, Serial No. 819,089, except that two coding cores are

provided for each amplitude level, instead of only one. Thus the coder will have 67 pairs of cores additional to those shown in FIG. 1.

FIG. 1 is drawn similarly to FIG. 1 of the parent specification, except that an additional pair of cores is shown. The three pairs of cores, which are of ferrite or other suitable ferromagnetic material, define three adjacent amplitude levels. Cores 1 and 2 will be assumed to define the mth amplitude level, cores 3 and 4 to define the $(m+1)$th amplitude level, and cores 5 and 6 to define the $(m+2)$th amplitude level. These cores are represented diagrammatically as horizontal straight rods, though in practice they will preferably be toroids, or other closed magnetic circuits. The conventions used in the parent specification will be adopted. Thus a short line sloping upwards to the left indicates a winding wound "straight" on a core, while one which slopes to the right indicates a winding wound "reverse." A vertical line drawn through the intersection of a winding line with the core indicates a conductor with which the winding is in series. A current flowing downwards through a straight winding on a core will be assumed to produce a flux from left to right in the core.

Core No. 1 is provided with a sampling winding 7, a signal winding 8, a bias winding 9, and an output digit winding 10. Windings 7, 8 and 10 are wound straight, while winding 9 is wound reverse. Similar windings are provided on core No. 2 except that the sampling and digit windings are wound reverse instead of straight. Cores 3 and 4 have windings similar to cores 1 and 2 respectively, cores 5 and 6 have windings similar to cores 1 and 2 respectively, except that the digit windings are oppositely wound, respectively, to those on cores 1 and 2.

All the sampling windings 7 have the same number of turns as do all the signal windings 8 and all the output windings 10. The bias windings 9 on the cores 1 and 2 have m turns, those on cores 3 and 4 have $m+1$ turns and those on cores 5 and 6 have $m+2$ turns. The bias windings could have some integral multiple of the number of turns given so long as the same multiple is used in each case.

The signal windings 8 are connected in series to a source 11 of a signal wave, while all the bias windings 9 are connected to a direct current bias source 12 which produces a bias flux from left to right in all the cores. The output digit windings 10 are connected in series with a digit conductor 13 which is connected through a rectifier 14 and a normally blocked gating amplifier 15 to a digit output terminal 16.

It will be understood that there will actually be six digit output conductors (not shown) additional to conductor 13, passing through corresponding digit windings (not shown) on the cores 1 to 6. The arrangement of the digit windings will be explained later with reference to FIG. 2.

A source of sampling pulses of defined volt-time product comprises a sinewave source 17 of high impedance connected to an input winding 18 wound straight on a sampling core 19 similar to cores 1 to 6. This core has an output winding 20 connected to all the sampling windings 7 on all the cores 1 to 6 in a series loop circuit of negligible resistance. The output winding 20 has the same number of turns as the sampling windings 7.

The meaning of a "pulse of defined volt-time product" is explained in the parent specification.

It will be understod that the windings of all the other 67 pairs of cores (not shown) are connected in series respectively with the corresponding windings of the cores 1 to 6.

The sinewaves from the source 17 are also supplied to a gate pulse generator 21 which generates one gating pulse per cycle of the sinewave. The gating pulses are supplied to unblock the amplifier 15 during the periods when output digit pulses are due from the cores 1 to 6, as will be explained later.

The manner in which the pairs of cores operate to prevent unwanted outputs due to variations in the signal amplitude is explained in the parent specification and the explanation will not be repeated here. It will be sufficient to mention that the sinewave source 17 triggers the sampling core 19 in the forward direction just after the sinewave has passed through zero in the positive direction, and a sampling pulse of defined volt-time product is then generated by the output winding 20, which reverses the condition of saturation of one of the coding cores in which the flux due to the signal wave from the source 11 substantially neutralises the bias flux due to the bias source 12, and a corresponding output digit pulse is delivered from winding 10 to the digit output condutor 13.

In the case of FIG. 1, it will be assumed that a digit pulse is required on conductor 13 when the signal level is m or $m+1$, but no digit pulse if the signal level is $m+2$. The output windings 10 on the cores 1 to 4 are wound in such direction that if any one of these cores is switched, then a positive output pulse is supplied to the digit conductor 13, and is able to pass through the rectifier 14 to the amplifier 15, which is unblocked at this time by a pulse from the generator 21. However, if the signal level is $m+2$, one of the cores 5 or 6 will be switched, but since the digit output windings 10 of these cores are wound oppositely to the corresponding windings on cores 1 and 2, the output pulse delivered to conductor 13 when either one of the cores 5 or 6 is switched will be negative and will be blocked by the rectifier 14. Thus a digit pulse is delivered to terminal 16 if the signal level is m or $m+1$, but no digit pulse is delivered if the signal level is $m+2$.

When the sampling sinewave from the source 17 changes sign from positive to negative half a cycle later, the sampling core 19 will be switched back to its original condition, and a reverse sampling pulse will be supplied to all the windings 7 of the cores 1 to 6, which will reset the core which had previously been switched. If this had been one of the cores 5 or 6, an unwanted positive output pulse would be supplied to conductor 13 and this pulse would be passed by the rectifier 14. The gating amplifier 15 is, however, blocked at this time, and so the unwanted pulse is eliminated.

It will be evident to those skilled in the art, that if the amplifier 15 is designed to respond only to positive input pulses, the rectifier 14 may be omitted. Clearly any other suitable gating arrangement could be used.

While in general the code will comprise code element periods during some of which digit pulses are present, and during other digit pulses are absent, it may sometimes be required that all code element periods should contain pulses, some of which are positive and others negative. In that case, a rectifier 14 will be omitted, and the amplifier 15 will be designed to respond to both positive and negative pulses.

The arrangement of FIG. 1 differs from the arrangement of the above cited co-pending application, Serial No. 819,089, whether or not incorporating the features of the parent specification, in that every coding core has an output digit winding, instead of only those cores which are to produce output digit pulses according to the code. As already pointed out, in the coders of the type concerned, it is assumed that no output is obtained from any core except the one which is switched. This requirement is not met because the hysteresis characteristic of the magnetic core material departs appreciably from the ideal rectangular form, and so a change of applied magnetic field always produces a small but not negligible change in flux in a core which is not switched. In the arrangement of FIG. 1, however, in which there are for example, a total of 70 pairs of cores, the "sneak" pulses due to approximately half the cores will be in the opposite direction to those due to the remainder, because, for a given digit position, approximately half the code combinations have a pulse in that digit position. The "sneak" pulses due to cores which are not switched

therefore substantially cancel out, and the coder operates very nearly as if the hysteresis wave of the core material were rectangular.

The arrangement according to the invention is not restricted to any particular form of the binary code, but it should be pointed out that if any relatively large number of the code combinations are not used, the condition for substantial cancellation of the "sneak" pulses may not be met unless the combinations to be omitted are suitably selected so that, for any digit, approximately as many digit pulses are present as are absent in the combinations retained. This condition is met by the 70-level code for which FIG. 1 is designed.

In order to show more clearly the manner in which the digit windings are applied, FIG. 2 shows the coding cores for four successive signal levels **26** to **29** according to the code employed for the coder illustrated in the above cited co-pending application, Serial No. 819,089. The seven digit conductors corresponding to conductor **13** are shown and also the corresponding digit windings **10** on each core. The windings **7**, **8** and **9** of FIG. 1 are not shown, but it will be understood that they are arranged on the cores in the manner indicated in FIG. 1. Opposite each pair of cores is given the level number followed by the corresponding code combination in which "1" indicates a digit pulse and "0" no digit pulse. It will be seen that each "A" core has a straight digit winding where the code combination has "1" and each "B" core has a straight digit winding where the code combination has "0." The other 66 pairs of cores (not shown) are provided with windings in like manner. It will be understood that each of the seven digit conductors in FIG. 2 is connected to a gating amplifier similar to **15** (FIG. 1), all these amplifiers being simultaneously unblocked by pulses from the gate pulse generator **21**. If necessary, also, a rectifier similar to **14** is provided for each digit conductor.

It should be mentioned that each pair of cores shown in FIGS. 1 or 2 could alternatively be provided by a toroid of ferrite material having a small hole through the material of the ring, through which hole the windings **7** and **10** are threaded, as illustrated in FIGS. 3 and 4 of the parent specification.

It may be pointed out that it has been found in a practical case that by adopting the features of the present invention, the currents which must be supplied to the cores could be reduced to about one tenth of the currents which previously had to be used. This means that the total power dissipation is reduced to 1% of its previous value. From this it follows that smaller cores can be used, smaller gauge wires for the windings, and more favourable magnetic material, so that more quickly acting cores can be obtained. In the case of a 70-level coder made according to the present invention, each of the cores had an inside diameter of 0.07 inch, an outside diameter of 0.1 inch and a thickness of 0.03 inch. The windings **7**, **8** and **10** (FIG. 1) all had one turn and the diameters of copper wire used for the windings were as follows:

	Wire diameter, inches
Trigger winding **7**	0.012
Signal winding **8**	0.018
Bias winding **9**	0.0032
Digit winding **10**	0.0032

While the principles of the invention have been described above in connection with specific embodiments, and particular modifications thereof, it is to be clearly understood that this description is made only by way of example and not as a limitation on the scope of the invention.

What we claim is:

1. A triggering arrangement comprising ferromagnetic material forming a plurality of pairs of similar saturable magnetic circuits, first, second and third electric circuits linking all the magnetic circuits, means for supplying to the first electric circuit a first conditioning current in such manner as to produce a flux in a given direction in each magnetic circuit, means for supplying to the second electric circuit a triggering pulse of defined volt-time product in such manner as to produce a flux in the given direction in one magnetic circuit of each pair and in the opposite direction in the other magnetic circuit of each pair, and a common output circuit connected to the third electric circuit, the arrangement being such that, in the case of each pair of magnetic circuits, an output pulse of the same polarity is produced in the output circuit when the condition of magnetic saturation of either magnetic circuit is reversed in response to the said triggering pulse, and also such that the polarity of the output pulse corresponding to each of one or more pairs of saturable magnetic circuits is opposite to that of the output pulse corresponding to each of the remainder of the pairs of saturable magnetic circuits.

2. A triggering arrangement according to claim 1, comprising a fourth electric circuit linking all the said magnetic circuits, and means for supplying to the fourth magnetic circuit a second conditioning current in such a manner as to produce a flux in the direction opposite to the given direction in each core.

3. A triggering arrangement according to claim 1, in which the means for supplying the said triggering pulse comprises a core of ferromagnetic material having an input winding connected to an alternating current source, and an output winding connected to the said second electric circuit.

4. An electric pulse coder for generating combinations of digit pulses representing samples of a signal wave according to a binary code of *m* digits, with reference to an amplitude scale having N steps, comprising N pairs of similar cores of saturable ferromagnetic material, a bias winding linking each core, means for passing a unidirectional bias current through each bias winding in such manner as to produce a bias flux in a given direction in the corresponding core, the bias flux being the same for the two cores of each pair but different for every pair of cores, a signal winding linking each core, means for supplying to all the signal windings in series a signal wave to be coded in such manner as to produce in each core a flux in the direction opposite to the given direction, a triggering winding linking each core, means for supplying to all the triggering windings in series a triggering pulse of defined volt-time product in such manner as to produce a triggering flux in the given direction in one core of each pair and in the opposite direction in the other core of each pair, *m* separate digit output conductors, and *m* digit windings linking each core and connected in series with the output conductors in such manner that each output conductor has connected in series therewith one winding from each core, the arrangement being such that when the condition of magnetic saturation of either core of a pair of cores is reversed in response to a triggering pulse, an output pulse of the same polarity is delivered to each of the output conductors, the polarity of the output pulse being of one sign when derived from certain pairs of cores, and of the opposite sign when derived from the other pairs of cores.

5. A coder according to claim 4, comprising means connected to each output conductor for suppressing all the output pulses of one particular polarity.

6. A coder according to claim 4, in which triggering pulses of alternately opposite polarities are periodically supplied to all the said triggering windings, and in which gating means connected to each output conductor is provided for suppressing all output pulses delivered to that output conductor in response to triggering pulses of one given polarity.

7. A coder according to claim 6, in which the means for supplying the triggering pulses to the triggering windings comprises an additional core of saturable ferromagnetic material having an input winding connected to

an alternating current source, and an output winding connected to all the said triggering windings in series, and in which the output signal of said alternating source controls the said gating means connected to each output conductor.

8. A trigger arrangement according to claim 2, in which the means for supplying said triggering pulse comprises a core of ferromagnetic material having an input winding connected to an alternating current source, and an output winding connected to said second electric circuit.

9. A coder according to claim 3, in which said triggering pulses having alternately opposite polarities are periodically supplied to said second circuit, and in which

gating means is connected to said output circuit for suppressing all output pulses delivered to said output circuit in response to triggering pulses of one given polarity.

10. A coder according to claim 9, further including means responsive to the output signal of said alternating signal source to control said gating means.

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