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(54) Title: DIMMING CONTROLLING CIRCUIT FOR LED

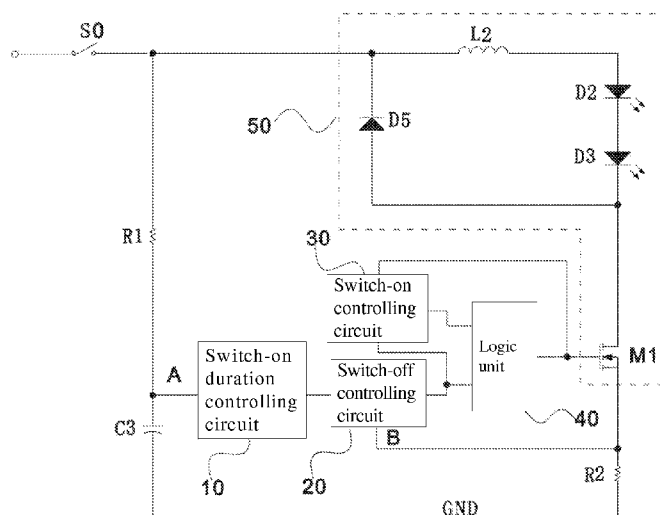


Fig.1

(57) Abstract: A dimming controlling circuit for LED comprises: a switch (S0) configured to connect a main circuit (50) and a power grid; a switch-on duration controlling circuit (10) configured to output a switch-on duration controlling signals according to action times of the switch (S0); a switch-off controlling circuit (20) configured to output a switch-off controlling signal according to a comparison result of the voltages of the switch-on duration controlling signal and of a signal from a terminal of a switch transistor (M1) in the main circuit (50); a switch-on controlling circuit (30) configured to generate a switch-on controlling signal after a first preset duration since receiving the switch-off controlling signal; and a logic unit (40) configured to output a switch transistor controlling signal. The dimming controlling circuit for LED of the present disclosure is simple in structure and a manufacturing cost is low.

DIMMING CONTROLLING CIRCUIT FOR LED

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority and benefits of Chinese Patent Application Serial No.
5 201010274894.5, filed with the State Intellectual Property Office of P. R. China on August 31,
2010, the entire content of which is incorporated herein by reference.

FIELD

The present disclosure relates to a field of LED controlling circuit, and more particularly, to
10 a dimming controlling circuit for LED.

BACKGROUND

LED lamp has gradually become a new generation of illuminations because of advantages
such as low energy consumption, energy-saving, fast response and longer service life etc.
15 However, dimming controlling for LED lamp is still a realistic problem.

The current dimming technology for LED lamp includes linear dimming, PMW(Pulse Width
Modulation) dimming and silicon controlled dimming, all of which are realized by adding some
circuits inside driving chips of the LED and adding peripheral components cooperating with the
circuits. For example, the linear dimming may be realized by adjusting an adjustable resistances
20 and the PMW dimming may be realized by adding some PMW chips, both of which need adding
some extra components. Although the silicon controlled dimming may replace incandescent lamps
or halogen lamps by LED lamps, it works under a chopped wave mode and an output voltage may
not be a sine wave and thus a lot of harmonic waves may be created and may cause serious
damages to a power grid.

25 Since the above-mentioned methods of dimming need adding extra components outside chips,
structures of the lamps may be complicated, manufacture costs may be high, and operations of
the lamps may be inconvenient.

SUMMARY

30 The present disclosure is directed to solve at least one of the problems. Accordingly, a
dimming controlling circuit for LED is provided to control on or off of a switch transistor in a
main circuit and to supply stable electrical current for LED lamp.

According to an embodiment of the present disclosure, a dimming controlling circuit for LED is provided, comprising: a switch configured to connect a main circuit and a power grid; a switch-on duration controlling circuit configured to output a switch-on duration controlling signal according to action times of the switch; a switch-off controlling circuit configured to compare a voltage of the switch-on duration controlling signal and a voltage of a signal from a terminal of a switch transistor in the main circuit to obtain a comparison result and to output a switch-off controlling signal according to the comparison result; a switch-on controlling circuit configured to generate a switch-on controlling signal after a first preset duration since receiving the switch-off controlling signal; and a logic unit configured to output a switch transistor controlling signal according to the switch-off controlling signal and the switch-on controlling signal.

The dimming controlling circuit for LED according to embodiments of the present disclosure may realize a graded dimming of the LED by fast actions of the switch, and the circuit provided by the present disclosure is simple in structure and a manufacturing cost is low.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other features and advantages of the disclosure will become apparent and more readily appreciated from the following descriptions taken in conjunction with the drawings in which:

Fig. 1 is a schematic diagram of a dimming controlling circuit for LED according to a first embodiment of the present disclosure;

Fig. 2 is a schematic diagram of a switch-on duration controlling circuit and a switch-off controlling circuit according to the first embodiment of the present disclosure shown in Fig.1;

Fig.3 is a schematic diagram of a dimming controlling circuit for LED according to a second embodiment of the present disclosure;

Fig. 4 is a schematic diagram of a switch-on duration controlling circuit and a switch-off controlling circuit according to the second embodiment of the present disclosure shown in Fig.3; and

Fig. 5 is an input and output waveform diagram of a detecting circuit according to the second embodiment of the present disclosure shown in Fig.3.

DETAILED DESCRIPTION

Reference will be made in detail to embodiments of the present disclosure. The embodiments

described herein with reference to drawings are explanatory, illustrative, and used to generally understand the present disclosure. The embodiments shall not be construed to limit the present disclosure. The same or similar elements and the elements having same or similar functions are denoted by like reference numerals throughout the descriptions.

5 An embodiment of the dimming controlling circuit for LED according to the present disclosure will be described with reference to Fig.1 and Fig.2. Fig. 1 is a schematic diagram of a dimming controlling circuit for LED according to a first embodiment of the present disclosure. As shown in Fig.1, the dimming controlling circuit for LED comprises: a switch S0, a switch-on duration controlling circuit 10, a switch-off controlling circuit 20, a switch-on controlling circuit 30 and a logic unit 40.

The switch S0 is configured to connect a main circuit 50 and a power grid (not shown in Figs). The switch-on duration controlling circuit 10 is configured to output a switch-on duration controlling signal according to action times of the switch S0. The switch-off controlling circuit 20 is configured to compare a voltage of the switch-on duration controlling signal and a voltage of a signal from a terminal of a switch transistor M1 in the main circuit 50 to obtain a comparison result and to output a switch-off controlling signal according to the comparison result. The switch-on controlling circuit 30 is configured to generate a switch-on controlling signal after a first preset duration T1 since receiving the switch-off controlling signal. The logic unit 40 is configured to output a switch transistor controlling signal according to the switch-off controlling signal and the switch-on controlling signal so as to control the switch transistor M1.

The dimming controlling circuit for LED according to the embodiment of the present disclosure may realize a graded dimming of the LED by fast actions of the switch, and the circuit provided by the present disclosure is simple in structure and a manufacturing cost is low.

Furthermore, a first terminal of a first resistance R1 is connected with a first terminal of a third capacitance C3; a second terminal of the first resistance R1 is connected with the switch S0; and a second terminal of the third capacitance C3 is grounded. A node A between the first resistance R1 and the third capacitance C3 shown in Fig.1 is connected with the switch-on duration controlling circuit 10 to provide an input voltage for the switch-on duration controlling circuit 10. The main circuit 50 is connected to ground via a second resistance R2, and a node B between the second resistance R2 and the main circuit 50 shown in Fig.1 may lead the signal from the terminal of the switch transistor M1 in the main circuit 50 to the switch-off controlling circuit 20.

Fig. 2 is a schematic diagram of a switch-on duration controlling circuit and a switch-off controlling circuit according to the first embodiment of the present disclosure shown in Fig.1. As shown in Fig.2, the switch-on duration controlling circuit 10 comprises: a power generating circuit 101, a detecting circuit 102, a shift register 103, a resetting circuit 104 and a decoding circuit 105. The power generating circuit 101 is configured to generate a first voltage according to the input voltage. The detecting circuit 102 is configured to detect the input voltage, to output an invalid shift controlling signal when determining the input voltage reaches a first threshold voltage and to output a valid shift controlling signal when determining the input voltage descends below a second threshold voltage and above a third threshold voltage. The shift register 103 is configured to output a shift result according to the shift controlling signal. The resetting circuit 104 is configured to reset the shift register 103 to zero, such as by providing a power to the shift register 103. The decoding circuit 105 is configured to decode according to the shift result outputted by the shift register 103 to obtain a decoding result. The selecting circuit 106 configured to select a voltage corresponding to the switch-on duration controlling signal according to the decoding result of the decoding circuit 105. The first threshold voltage is higher than the second threshold voltage and the second voltage is higher than the third threshold voltage.

The switch-off controlling circuit 20 comprises a comparator 201. A first input terminal of the comparator 201 is connected with the voltage of the signal from the terminal of the switch transistor M1 in the main circuit 50 and a second input terminal of the comparator 201 is connected with the voltage selected by the selecting circuit 106. The first input terminal of the comparator 201 is a positive input terminal and the second input terminal of the comparator is a negative input terminal.

As shown in Fig.1, the main circuit 50 comprises a second inductor L2, a LED group (D2 and D3), a switch transistor M1 and a flywheel diode D5. The second inductor L2, the LED group and the flywheel diode D5 are connected in series to form a loop, a negative terminal of the flywheel diode D5 is connected with the power grid and a positive terminal of the flywheel diode D5 is connected with a drain of the switch transistor M1. In one embodiment, the switch transistor M1 is a NMOS transistor.

In one embodiment, the logic unit 40 may be a R-S trigger, a R terminal of the R-S trigger is configured to receive the output switch-off controlling signal sent by the switch-off controlling circuit 20, a S terminal of the R-S trigger is configured to receive the switch-on controlling signal sent by the switch-on controlling circuit 30, and an output terminal of the R-S trigger is connected

with an input of the driving circuit 70 and outputs the switch transistor M1 controlling signal.

Another embodiment of the dimming controlling circuit for LED according to the present disclosure will be described with reference to Fig.3 and Fig.4.

Fig.3 is a schematic diagram of a dimming controlling circuit for LED according to a second
5 embodiment of the present disclosure. As shown in Fig.3, the difference between the first
embodiment and the second embodiment is that the dimming controlling circuit for LED further
comprises a rectifying circuit D1, a driving circuit 70 and a filtering circuit 60. The rectifying
circuit D1 is connected with the main circuit 50. The rectifying circuit D1 may be a rectifying
bridge formed by four diodes in one embodiment of the present disclosure. The driving circuit 70
10 is set at a controlling terminal of the switch transistor M1 to drive the switch transistor M1. The
filtering circuit 60 is arranged between the main circuit 50 and the rectifying circuit D1. The
filtering circuit 60 comprises a first inductor L1, a first capacitor C1 and a second capacitor C2.
The first capacitor C1 and the second capacitor C2 are connected with each other in series, the
first inductor L1 is connected with the capacitor C1 and the second capacitor C2 in parallel, and
15 two terminals of the first inductor L1 are connected with the rectifying circuit D1 and the main
circuit 50 respectively.

The logic unit 40 comprises a R-S trigger, a R terminal of the R-S trigger is configured to
receive the output switch-off controlling signal sent by the switch-off controlling circuit 20, a S
terminal of the R-S trigger is configured to receive the switch-on controlling signal sent by the
20 switch-on controlling circuit 30, and an output terminal of the R-S trigger is connected with an
input of the driving circuit 70 and outputs the switch transistor M1 controlling signal.

Fig. 4 is a schematic diagram of a switch-on duration controlling circuit and a switch-off
controlling circuit according to the second embodiment of the present disclosure shown in Fig.3.
As shown in Fig. 4, the difference between the first embodiment and the second embodiment is
25 that there are two shift registers U11 and U12, output terminals of the U11 and U12 are connected
with an input terminal of the decoding circuit 105, and four decoding signals output by the
decoding circuit 105 are connected with an input terminal of the selecting circuit 106 to select
voltages corresponding to four switch-on duration controlling signals.

Next, a working principle of the dimming controlling circuit for LED in the second
30 embodiment will be described in detail with reference to Fig.3 to Fig.5. In this embodiment, there
are four dimming grades, and the LED group comprises two LED lamps.

Fig. 5 is an input and output waveform diagram of the detecting circuit according to the

second embodiment of the present disclosure.

Three voltages are preset for node A, which are V_{TH1} , V_{TH2} and V_{TH3} (V_{TH3} is not shown in Fig. 5) and $V_{TH3} < V_{TH2} < V_{TH1}$. When the switch S0 is ON, the voltage of node A begins to rise. When the voltage of node A is smaller than V_{TH3} , the power generating circuit 101 doesn't generate a voltage. When the voltage of node A reaches V_{TH3} , the power generating circuit 101 generates a voltage VC1. The voltage of the power grid continues to rise and reach V_{TH1} and the NMOS transistor M1 is still OFF, the switch-on controlling circuit 30 starts timing and when the time gets to a first preset time T1, the switch-on controlling circuit 30 outputs a switch-on controlling signal to conduct the NMOS transistor M1. If the switch-on controlling signal is high level 1, the output voltage of the R-S trigger is also high level 1 since the switch-on controlling signal is input to the S terminal of the R-S trigger 10, meanwhile the NMOS transistor M1 is conducted and a current through the second resistance R2 increases.

Meanwhile, the voltage VC1 makes the resetting circuit 103 output a resetting signal to reset the shift register 104. Both the outputs of the two shift registers U11 and U12 (Q1 and Q0) are reset to be zero. After the decoding circuit 105 processes the outputs of U11 and U12, the selecting circuit 106 selects a voltage corresponding to the switch-on controlling signal, and the voltage is defined as a first grade voltage V1, provided that V1 is 0.25V, meanwhile the voltage of the signal from the terminal of the switch transistor M1 in the main circuit 50 is the voltage of node B shown in Fig.3.

The voltage of node B begins to rise when the NMOS transistor M1 is conducted, and when the voltage of node B is larger than the first grade voltage 0.25V, the output voltage of the comparator 201 is high level 1 and the output voltage of the R-S trigger 40 is low level 0 after the output voltage of the comparator 201 getting through the R terminal of the R-S trigger, and then the low level 0 output by the R-S trigger 40 makes the NMOS transistor M1 OFF. Because of the inductor L2, a current flows continuously in a free-wheeling loop formed by the inductor L2, the LED lamp group D2, D3 and the flywheel diode D5, and thus a stable current may be provided to the LED lamp group and then the LED lamp group is on a first grade brightness. When the NMOS transistor M1 is OFF, the switch-on controlling circuit 30 starts timing and outputs a switch-on controlling signal to conduct M1 when the timing reaches the first preset time T1. If there is no voltage change of the power grid, the detecting circuit 102 does not work and the LED lamp group may work under a stable current.

If the switch-off time of the switch S0 is longer than a second preset time T2, the voltage of

node A descends to below the third threshold voltage V_{TH3} and the switch S0 is considered to be OFF. When the switch S0 is ON again, the shift register is reset to zero again and the working process is the same as the above-mentioned process and such process will not be described.

If the switch-off time of the switch S0 is shorter than the second preset time T_2 and if the
 5 voltage of node A descends to be between V_{TH2} and V_{TH3} , the power generating circuit 101 still outputs the voltage VC1. As shown in Fig.5, when the voltage of node A descends to V_{TH2} , the output CK of the detecting circuit 102 turns from the low level 0 to the high level 1. The shift register 104 is shifted because a waveform of the detecting circuit is during its ascending phase, i.e. the output of Q1 is 1, the output of the Q0 is 0. After the outputs of Q1 and Q0 is decoded by
 10 the decoding circuit 105, the selecting circuit 106 selects a second grade voltage V2 corresponding to the switch-on duration controlling signal, provided V2 is 0.175v.

If the switch-off time of the switch S0 is short, the switch S0 is ON within the preset time T_2 . Since a period between the OFF and ON of the switch S0 is short, the lowest voltage of node A is still higher than V_{TH3} , which makes the power generating circuit 101 continuously generate the
 15 voltage VC1 and the resetting circuit 103 is invalid because the resetting circuit 103 may not work without a power supply. When the switch S0 is ON, the voltage of the power grid begins to rise again. As shown in Fig.5, when the voltage of node A reaches V_{TH1} , the output CK of the detecting circuit 102 switches from high level 1 to low level 0, the shift register 104 keeps its previous output signal and does not shift, and then the selecting circuit 106 selects the second
 20 grade voltage V2. Furthermore, the switch-on controlling circuit 30 starts timing as soon as it receives a switch-off controlling signal, and when the time reaches the preset time T_1 , the NMOS transistor M1 is conducted and the current of the second resistance R2 increases gradually. When the voltage of node B is larger than V2 which is 0.175v, the output of the comparator 201 is high level 1 and the output voltage of the R-S trigger 40 is low level 0 after the output voltage of the
 25 comparator 201 getting through the R terminal of the R-S trigger 40, and then the low level 0 output by the R-S trigger 40 makes the NMOS transistor M1 OFF. Because of the inductor L2, a current flows continuously in a free-wheeling loop formed by the inductor L2, the LED lamp group D2, D3 and the flywheel diode D5, and thus a stable current may be provided to the LED lamp group and then the LED lamp group is on a second grade brightness.

30 The working principle of the switch S0 hereafter is the same as the above. If the switch-off time of the switch S0 is longer than the second preset time T_2 , the switch S0 is considered to be OFF, and when S0 is ON again, the working process is the same as the first time. If the switch-off

time of the switch S0 is shorter than the second preset time T2, when the switch S0 is OFF, the shift register 104 is shifted to the next grade; when the switch S0 is ON again, the shift register 104 does not shift and the LED lamp lights according to the brightness grade selected by the selecting circuit 106 when the switch S0 is OFF. If every switch-off time of the switch S0 is shorter than the second preset time T2, then before the switch-off time is longer than the second preset time T2, the brightness grade of the LED lamp group is adjusted each time when the switch S0 is ON or OFF.

In one embodiment of the present disclosure, the number of the shift register 104 is two, the number of selecting signals outputted by the decoding circuit 105 is four, the number of voltage grades of the selecting circuit 106 is four, and the number of brightness grades of the LED lamp group is also four. It should be understood that the number of shift registers may be changed, the number of brightness grades of the LED lamp group may be accordingly determined by users and designers and the number of the LED lamps may also be plural in some embodiments of the present disclosure. It should also be understood that the more the shift registers are, the more the voltage grades of the selecting circuit 106 are and the more the brightness grades of the LED lamp group are. For example, if the number of shift registers is three, then the number of selecting signals outputted by the decoding circuit 105 is eight, the number of voltage grades of the selecting circuit 106 is eight, and the number of brightness grades of the LED light group is also eight

Although explanatory embodiments have been shown and described, it would be appreciated by those skilled in the art that changes, alternatives, and modifications may be made in the embodiments without departing from spirit and principles of the disclosure. Such changes, alternatives, and modifications all fall into the scope of the claims and their equivalents.

WHAT IS CLAIMED IS:

1. A dimming controlling circuit for LED, comprising:

a switch configured to connect a main circuit and a power grid;

5 a switch-on duration controlling circuit configured to output a switch-on duration controlling signal according to action times of the switch;

a switch-off controlling circuit configured to compare a voltage of the switch-on duration controlling signal and a voltage of a signal from a terminal of a switch transistor in the main circuit to obtain a comparison result and to output a switch-off controlling signal according to the
10 comparison result;

a switch-on controlling circuit configured to generate a switch-on controlling signal after a first preset duration since receiving the switch-off controlling signal; and

a logic unit configured to output a switch transistor controlling signal according to the switch-off controlling signal and the switch-on controlling signal.

15

2. The dimming controlling circuit for LED according to claim 1, wherein the switch-on duration controlling circuit comprises:

a power generating circuit configured to generate a first voltage according to an input voltage;

20 a detecting circuit configured to detect the input voltage, to output an invalid shift controlling signal when determining the input voltage reaches a first threshold voltage and to output a valid shift controlling signal when determining the input voltage descends below a second threshold voltage and above the third threshold voltage;

a shift register configured to output a shift result according to the invalid or valid shift
25 controlling signal;

a resetting circuit configured to reset the shift register to zero;

a decoding circuit configured to decode according to the shift result to obtain a decoding result; and

a selecting circuit configured to select a voltage corresponding to the switch-on duration
30 controlling signal according to the decoding result.

3. The dimming controlling circuit for LED according to claim 2, wherein the first threshold

voltage is higher than the second threshold voltage and the second threshold voltage is higher than the third threshold voltage.

4. The dimming controlling circuit for LED according to claim 1, wherein the switch-off
5 controlling circuit comprises:

a comparator, wherein a first input terminal of the comparator is connected with the voltage of the signal from the terminal of the switch transistor in the main circuit and a second input terminal of the comparator is connected with the voltage selected by the selecting circuit.

10 5. The dimming controlling circuit for LED according to claim 4, wherein the first input terminal of the comparator is a positive input terminal and the second input terminal of the comparator is a negative input terminal.

6. The dimming controlling circuit for LED according to claim 1, wherein the logic unit
15 comprises a R-S trigger, a R terminal of the R-S trigger is configured to receive the output switch-off controlling signal sent by the switch-off controlling circuit, a S terminal of the R-S trigger is configured to receive the switch-on controlling signal sent by the switch-on controlling circuit and an output terminal of the R-S trigger is configured to output the switch transistor controlling signal.

20 7. The dimming controlling circuit for LED according to claim 1, wherein the main circuit comprises a second inductor, a LED group, a flywheel diode and a switch transistor, in which the second inductor, the LED group and the flywheel diode are connected in series to form a loop and the flywheel diode has a negative terminal connected with the power grid and a positive terminal
25 connected with the switch transistor.

8. The dimming controlling circuit for LED according to claim 7, wherein the switch transistor is a NMOS transistor.

30 9. The dimming controlling circuit for LED according to claim 7, wherein a driving circuit is set at a controlling terminal of the switch transistor to drive the switch transistor.

10. The dimming controlling circuit for LED according to any one of claims 1-9, wherein the main circuit is also connected with a rectifying circuit.

11. The dimming controlling circuit for LED according to claim 10, wherein the rectifying
5 circuit is a rectifying bridge formed by four diodes.

12. The dimming controlling circuit for LED according to claim 10 or 11, wherein a filtering circuit is arranged between the main circuit and the rectifying circuit.

10 13. The dimming controlling circuit for LED according to claim 12, wherein the filtering circuit comprises a first inductor, a first capacitor and a second capacitor, in which the first capacitor and the second capacitor are connected in series, the first inductor is connected with the first capacitor and the second capacitor in parallel, and two terminals of the first inductor are connected with the rectifying circuit and the main circuit respectively.

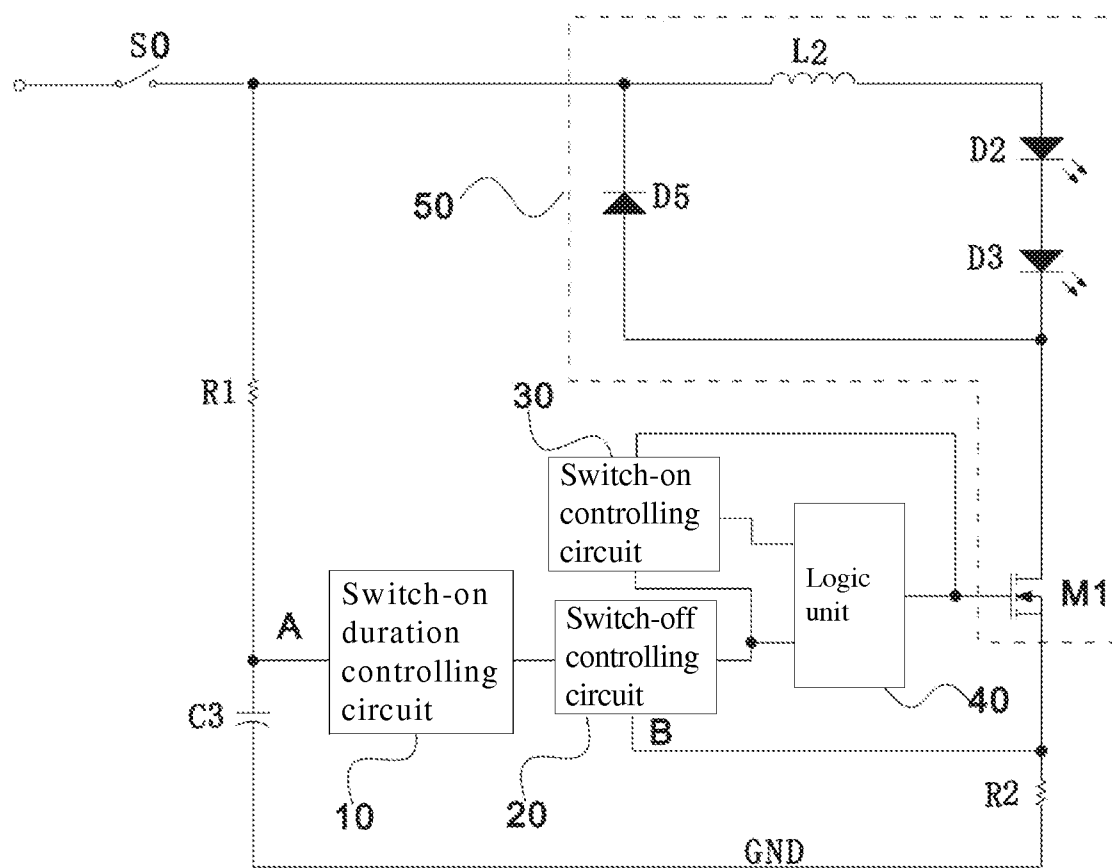


Fig.1

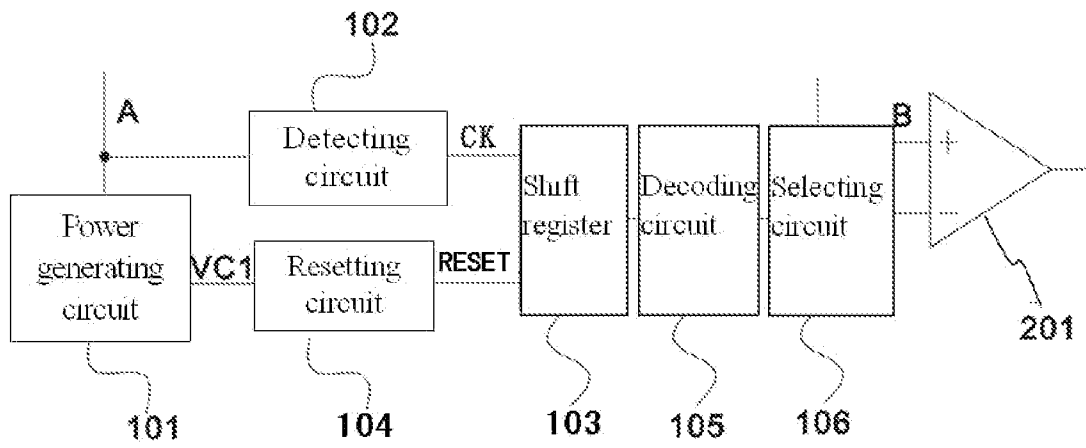


Fig.2

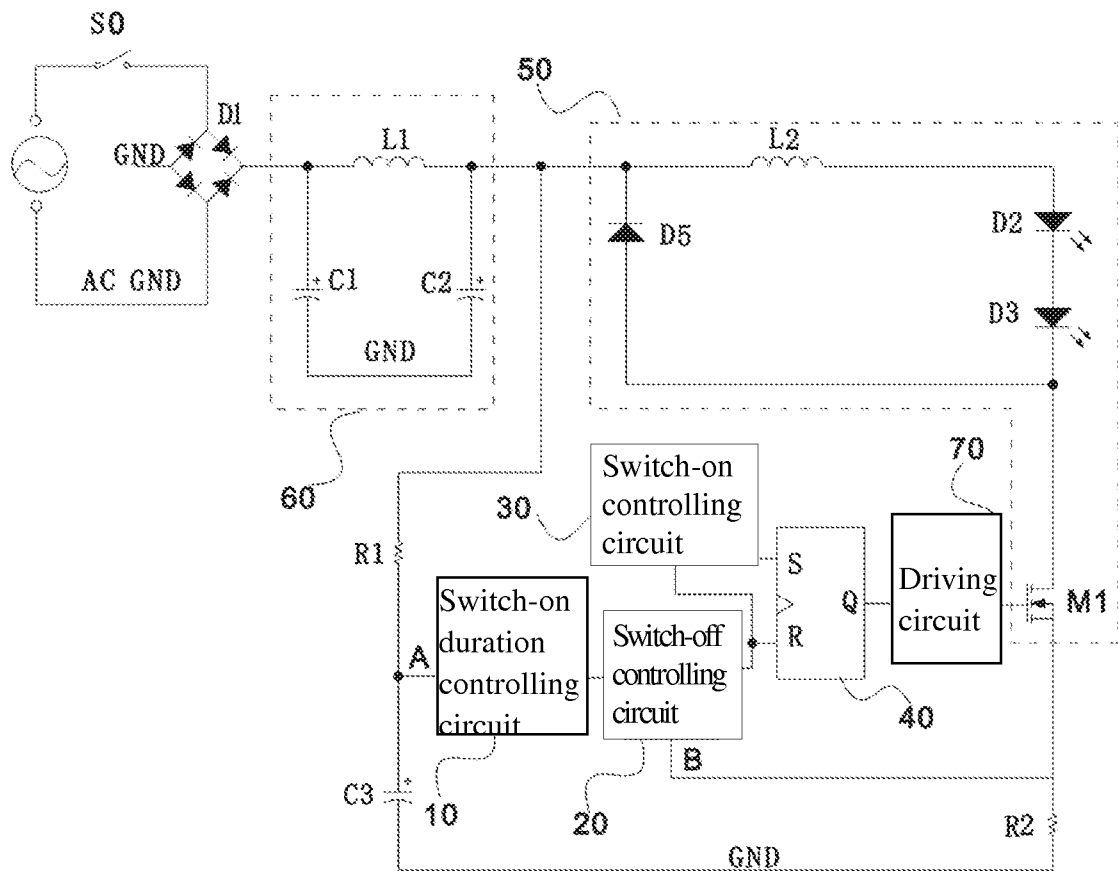


Fig.3

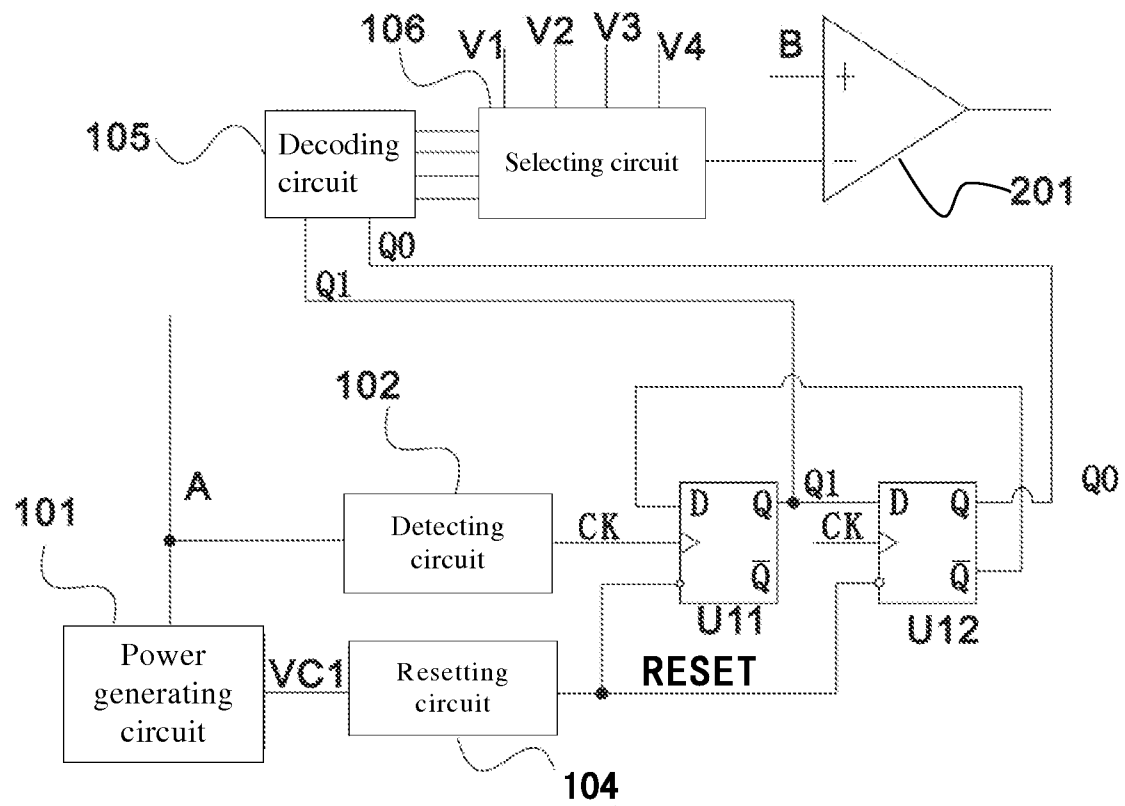


Fig.4

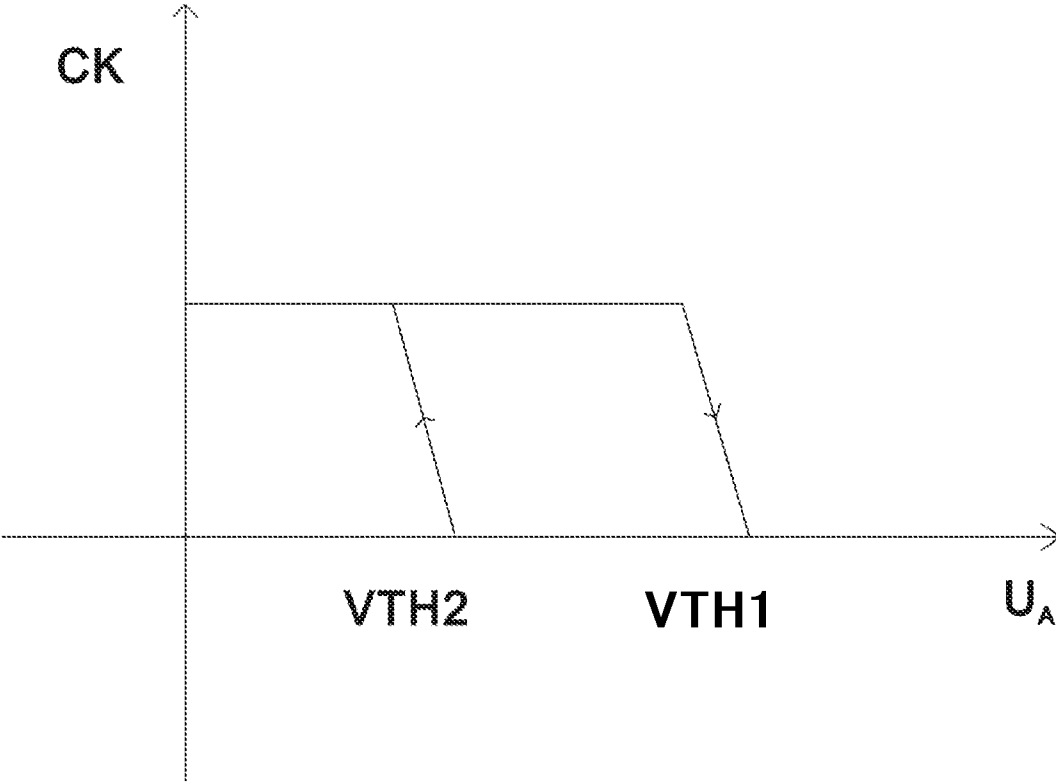


Fig.5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2011/079138

A. CLASSIFICATION OF SUBJECT MATTER

H05B37/02(2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC:H05B37/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS;CNTXT;VEN;CNKI: LED,LIGHT EMITTING DIODE, DIMMING, SWITCH, ON-OFF, COMPAR+, TIMES, DURATION, VOLTAGE, BRIGHTNESS, LIGHT,CONTROL,TIMING

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	CN102052592A(NEW GREEN TECH CO LTD) 11 May 2011 (11.05.2011) Paragraphs 22-23,69-80 and 84-86 of the description, figs.7,8,10	1,4-13
A	KR20090056567A(SAMSUNG ELECTRO-MECHANICS CO) 03 Jun. 2009 (03.06.2009) Paragraphs 15-38 of the description, fig. 2	1-13
A	CN101039540A(SAMSUNG ELECTRONICS CO LTD) 19 Sep. 2007 (19.09.2007) The whole document	1-13
A	CN101754530A(O2 MICRO CO LTD) 23 Jun. 2010 (23.06.2010) The whole document	1-13
A	US2008316781A1(GREEN MARK TECHNOLOGY INC) 25 Dec. 2008 (25.12.2008) The whole document	1-13

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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Date of the actual completion of the international search 24 Nov. 2011(24.11.2011)	Date of mailing of the international search report 08 Dec. 2011 (08.12.2011)
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
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