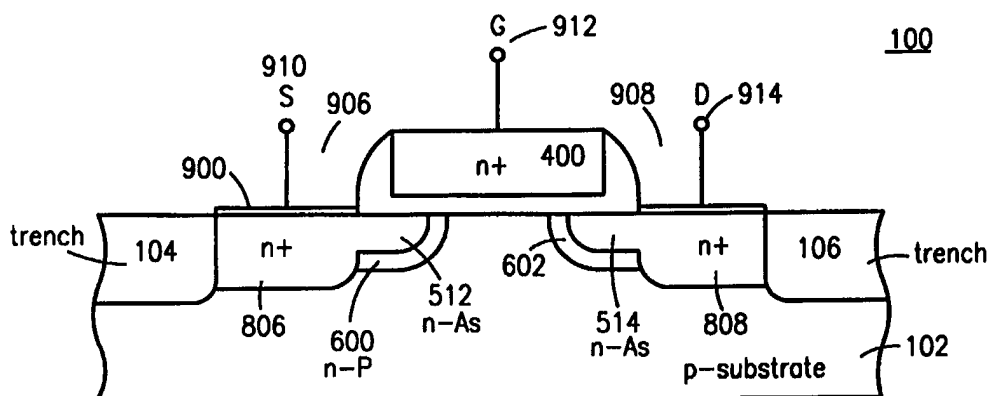




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(21) International Application Number: PCT/US98/01153 (22) International Filing Date: 21 January 1998 (21.01.98) (30) Priority Data: 08/786,821 21 January 1997 (21.01.97) US (71) Applicant: ADVANCED MICRO DEVICES, INC. [US/US]; One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US). (72) Inventors: NAYAK, Deepak, Kumar; 3702 Poinciana Drive #93, Santa Clara, CA 95051 (US). RAKKHIT, Rajat; 662 Troon Court, Milpitas, CA 95035 (US). HAO, Ming-Yin; 964 Mangrove Avenue, Sunnyvale, CA 90486 (US). (74) Agent: RODDY, Richard, J.; Advanced Micro Devices, Inc., One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).		(81) Designated States: JP, KR, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i> <i>Before the expiration of the time limit for amending the</i> <i>claims and to be republished in the event of the receipt of</i> <i>amendments.</i>

(54) Title: As/P HYBRID nLDD JUNCTION AND MEDIUM V_{dd} OPERATION FOR HIGH SPEED MICROPROCESSORS

**(57) Abstract**

A method of manufacturing a semiconductor device wherein hybrid nLDD regions are formed by implanting arsenic ions and phosphorous ions in source and drain regions of a substrate. The source and drain regions are formed by implanting either arsenic or phosphorous ions.

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As/P HYBRID nLDD JUNCTION AND MEDIUM V_{dd}
OPERATION FOR HIGH SPEED MICROPROCESSORS

BACKGROUND OF THE INVENTION

5 1. Field of the Invention

This invention relates generally to the manufacture of high performance semiconductor devices and, more particularly, to the manufacture of submicron semiconductor devices, and even more particularly, to the manufacture of submicron semiconductor devices
10 having hybrid nLDD regions doped with arsenic and phosphorous.

2. Discussion of the Related Art

The semiconductor industry is increasingly characterized by a growing trend toward fabricating more complex circuits on a given semiconductor chip. This is being achieved by reducing the size of
15 individual devices within the circuits and spacing the devices closer together. The reduction of the size of individual devices and the closer spacing has the potential to bring about improved electrical performance.

As the integrated circuit technology approaches the sub-0.5
20 micron regime, the electric field inside the device tends to increase which decreases the long-term device reliability. Devices having such small dimensions suffer from certain problems that are not of serious concern when the gate dimensions are greater than about 1 micron. Aggressive scaling of gate dimensions to deep submicron regime demands
25 very shallow and sharp junctions in order to maintain good short channel characteristics and current drive. Using arsenic doped nLDD regions, high performance CMOS logic technology operating at 2.5 V has been achieved. However, due to the sharp arsenic junction, the power supply voltage, V_{dd}, must be reduced below 2.5 V in order to maintain
30 a sufficient hot carrier reliability margin. Although lower V_{dd} voltage is attractive in terms of power dissipation considerations, it compromises speed and current drive in microprocessor computer systems. As shown in **Figure 11**, the gate delay is increased by 22%

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when the Vdd is reduced from 3.3 to 2.5 V. In addition, at low Vdd, the threshold voltage must be lowered in order to maintain high current drive, which results in high off-stage leakage. The experimental results show that the arsenic only junctions limit the performance due to low hot carrier life time.

Hence, what is needed is a high performance semiconductor device that is not performance limited due to low hot carrier life time.

SUMMARY OF THE INVENTION

The present invention is directed to a method of manufacturing a semiconductor device having hybrid nLDD regions doped with arsenic and phosphorus.

The drain and source regions are formed by implanting either arsenic or phosphorus ions.

The hybrid nLDD regions are implanted with arsenic ions in a concentration of $1-10E14$ ions per cm^2 .

The hybrid nLDD regions are implanted with phosphorus ions in a concentration of $1-10E13$ ions per cm^2 .

The present invention is further directed to a semiconductor device having hybrid nLDD regions.

The hybrid nLDD regions are doped with arsenic ions in a concentration of $1-10E14$ ions per cm^2 and with phosphorus ions in a concentration of $1-10E13$ ions per cm^2 .

The semiconductor device has source and drain regions doped with either phosphorous ions or arsenic ions.

The semiconductor device has a layer of silicide formed on the surface of the substrate over the source and drain regions.

The present invention is better understood upon consideration of the detailed description below, in conjunction with the accompanying drawings. As will become readily apparent to those skilled in this art from the following description there is shown and described embodiments of this invention simply by way of illustration of the best mode to carry out the invention. As will be realized, the

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invention is capable of other embodiments and its several details are capable of modifications in various obvious aspects, all without departing from the scope of the invention. Accordingly, the drawings and detailed description will be regarded as illustrative in nature
5 and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings incorporated in and forming a part of the specification, illustrate the present invention, and together with the detailed description below serve to explain the principles of the
10 invention. In the drawings:

Figure 1 shows a portion of a wafer substrate with an active region in the substrate defined by isolation trench regions and a layer of gate oxide formed in the substrate between the isolation trench regions.

15 **Figure 2** shows the portion of the wafer shown in **Figure 1** with a layer of polysilicon on the wafer and a layer of photoresist on the layer of polysilicon.

Figure 3 shows the portion of the wafer shown in **Figure 2** with the photoresist layer selectively removed by photolithography to
20 define the gate region.

Figure 4 shows the portion of the wafer shown in **Figure 3** with a polysilicon gate and a gate oxide region formed by etching the polysilicon layer and removing the remaining photoresist layer.

Figure 5 shows protective layers formed on selected portions of
25 the portion of the wafer shown in **Figure 4** and shows the implantation of arsenic ions to form the nLDD regions.

Figure 6 shows the implantation of phosphorus ions to form the hybrid nLDD regions.

Figure 7 shows the formation of sidewall spacers around the gate
30 and the protective layers removed.

Figure 8 shows the implantation of P or As ions to form the source and drain regions.

Figure 9 shows the semiconductor device with the source and drain regions formed, the hybrid nLDD regions formed, a silicide layer formed over the source and drain regions, and electrical contacts made to the source, drain, and gate regions.

5 **Figure 10** is a graphical representation of the experimental results of the I_{dsat} life time as a function of $1/V_{dd}$ for a device having phosphorous only junctions, a device having arsenic/phosphorous hybrid junctions, and a device having arsenic only junctions.

10 **Figure 11** is a graphical representation of the experimental results showing the ring oscillator delay/stage for a device having phosphorous only junctions, a device having arsenic/phosphorous hybrid junctions, and a device having arsenic junctions with all three having an L_{eff} of 0.20 microns.

15 **Figure 12** is a graphical representation of the experimental results showing the ring oscillator delay/stage for expected nominal L_{eff} for three different junctions; phosphorous only junctions, arsenic/phosphorous hybrid junctions, and arsenic only junctions.

20 **Figure 13** is a graphical representation of the experimental results of the ring oscillator delay/stage for expected subnominal L_{eff} for three different junction; phosphorous only junctions, arsenic/phosphorous hybrid junctions, and arsenic only junctions.

Figure 14 is a graphical representation of the experimental results showing the comparison of off-state leakage for arsenic/phosphorous hybrid junctions and for arsenic only junctions.

25 **Figure 15** is a graphical representation of the experimental results of the effect of arsenic/phosphorous junction doping on substrate current.

DETAILED DESCRIPTION

30 Reference is now made in detail to a specific embodiment of the present invention, which illustrates the best mode presently contemplated by the inventors for practicing the invention. Alternate embodiments may also be described as applicable. However, the present

invention is not limited to the following outlined process, but is so chosen so that the key aspects can be easily visualized.

It is assumed that the incoming wafers are properly fabricated and the latest production techniques are used.

5 Referring to **Figure 1** there is shown a portion of a semiconductor device 100. The device 100 is made up of a substrate material 102 selectively doped. In this case, the substrate is doped with a p type dopant to provide a p-doped substrate. The method of obtaining a p-doped substrate is well known in the semiconductor art and will not be
10 discussed. The substrate 102 has trench isolation regions, indicated at 104 and 106, formed to define an active region, indicated at 108, and to isolate the active area 108 from other parts of the wafer. The isolation regions 104 and 106 are shown as being trench oxide regions.

Any method of forming trench oxide regions can be used to form the
15 isolation regions. An alternate method is to form oxide regions, known in the art as field oxide (FOX) regions. The device 100 is shown with a layer of oxide 110 formed on the surface of the active region 108 between the isolation regions 104 and 106. As can be appreciated, there are at least two methods of obtaining a gate oxide
20 region. One method, as discussed here, is to form a layer of oxide and then selectively remove the portions of the oxide that will not be needed. Another method is to mask the device with a protective layer (to form a protective layer over the portions of the device for which an oxide layer is not wanted) and to grow or form an oxide layer on
25 the portions of the device that are not masked. Either method could be used and would be the choice of the process designer.

Referring to **Figure 2** there is shown the device 100 with a layer of polysilicon 200 formed on the surface of the wafer 100 shown in
30 **Figure 1** and a layer of photoresist 202 formed on the layer of polysilicon 200. In this figure and in subsequent figures, like numeral designations will be used for like elements.

Figure 3 shows the device 100 with the photoresist layer 202

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selectively removed to define a gate region which will be subsequently formed on the surface of the substrate 102.

Figure 4 shows the device 100 shown in Figure 3 with a gate 400 formed on the gate oxide region 402. The method of forming the gate 400 is well known in the art and can be accomplished by conventional methods. The gate 400 is typically formed of polysilicon and selectively doped to make it conductive.

Figure 5 shows the device 100 with protective photoresist layers 500 and 504 formed on portions of the device 100 to protect the device where nLDD is not required. Arrows, indicated at 506, represent the implantation of arsenic ions (As ions) into and beneath the surface 508 of the substrate 102. The implantation of the arsenic ions is at a concentration of $1-10E14$ ($1-10 \times 10^{14}$) and forms regions known as nLDD regions, indicated at 510 and 512. The term nLDD means a Lightly Doped Drain_region doped with an n type dopant. It is conventional in the semiconductor art to designate a region as an LDD region even if the region is or will be doped with medium or high doses. These regions are also referred to as source/drain extensions.

Figure 6 shows the device as shown in Figure 5 with the protective layers 500 and 502 still in place and arrows, indicated at 600, representing the implantation of phosphorous (P) ions into and beneath the surface 510 of the substrate 102 to form the hybrid nLDD regions 600 and 602. The phosphorous ions penetrate further into the substrate as indicated at 600 and 602. As is known in the semiconductor processing art, the implantation of ions into the surface of a substrate causes the surface to be damaged. At some point in the processing an annealing process is done to cure the surface damage and also to drive the ions to a selected depth in the substrate. This annealing process can be done at any point subsequent to the implantation of the ions.

Figure 7 shows the device shown in Figure 6 with the protective layers 500 and 502 removed and sidewall spacers 700 and 702 formed

around the gate 400.

Figure 8 shows the device 100 with protective layers 800 and 802 formed on selected surfaces of the device 100. It is noted that some surfaces may not require a protective surface for some processes. For example, a trench oxide surface such as those at 104 and 106 may not require a protective surface. However, this would be known by a person of ordinary skill in the semiconductor processing art and will not be further addressed. Also shown in Figure 8 is the implantation of ions, indicated by arrows 804. The ion implantation at this point in the manufacturing process is to form the source region 806 and drain region 808. The ion implantation can be either phosphorous ions or arsenic ions at a sufficient concentration to form the source and drain regions. The required concentration would be dependent upon the particular process and application and would be determinable by a person of ordinary skill in the semiconductor processing art and the determination of the required concentration is not considered to constitute undue experimentation.

Figure 9 shows the device 100 with the source and drain regions formed at 806 and 808, respectively and the protective layers 800 and 802 removed. In addition, silicide layers which are optional are indicated at 902 and 904 and are shown formed on the source and drain regions 906 and 908, respectively. Electrical connections to the source region 906, the gate 400, and the drain region 908 are indicated at 910, 912, and 914, respectively.

Figure 10 is a graphical representation of the experimental results of the I_{dsat} life time as a function of $1/V_{dd}$ for a device having phosphorous only junctions 1000, a device having arsenic/phosphorous hybrid junctions in accordance with the present invention 1002, and a device having arsenic only junctions 1004.

Figure 11 is a graphical representation of the experimental results showing the ring oscillator delay/stage for a device having phosphorous only junctions 1100, a device having arsenic/phosphorous

hybrid junctions in accordance with the present invention 1102, and a device having arsenic junctions 1104 with all three devices having an L_{eff} of 0.20 microns.

Figure 12 is a graphical representation of the experimental results showing the ring oscillator delay/stage for expected nominal L_{eff} for three different junctions; a device having phosphorous only junctions 1200, a device having arsenic/phosphorous hybrid junctions in accordance with the present invention 1202, and a device having arsenic junctions 1202.

Figure 13 is a graphical representation of the experimental results of the ring oscillator delay/state for expected subnominal L_{eff} for three different junctions; a device having phosphorous only junctions 1300, a device having arsenic/phosphorous hybrid junctions in accordance with the present invention 1302, and a device having arsenic junctions 1304.

Figure 14 is a graphical representation of the experimental results showing the comparison of off-state leakage for arsenic/phosphorous hybrid junctions in accordance with the present invention 1400 and for arsenic only junctions 1402. I_{doff} for nominal devices at 1404 and subnominal devices at 1406 are given. In the case of the subnominal devices, I_{doff} for the arsenic only junction 1408 is more than 10 times higher than that of the arsenic/phosphorous hybrid junctions 1410 in accordance of the present invention.

Figure 15 is a graphical representation of the experimental results of the effect of arsenic/phosphorous junction doping on substrate current. The experimental results indicates that substrate current is a strong function of the light phosphorous dose in the hybrid junction in accordance with the present invention, whereas substrate current is a weak function of arsenic dose in the hybrid junction. Open squares and circles at 1500 compare the effect of tripling arsenic dose. Open squares and closed triangles at 1502 compare the effect of doubling the phosphorous dose.

It is anticipated that any appropriate process technology can be adapted for the present invention. One example of a process technology is a technology that uses a p-epi/p+substrate, LOCOS isolation, dual-gate poly, 7 nanometer gate oxide, and DUV lithography to define 0.30 micron Ldrawn poly lines. After the hybrid arsenic/phosphorous implants, the implant is driven to obtain the required channel length. Gate poly and S/D regions are doped simultaneously, and RTA (rapid thermal anneal) processes are used for n+ and p+ dopant activation. Self-aligned Ti silicide is formed over the gate and S/D regions.

Figure 10 shows the experimental I_{dsat} DC life time for three different junctions. In order to maintain 10 years of life time, the highest operating voltages for arsenic only devices **1004**, the hybrid arsenic/ phosphorous junctions **1002** in the devices of the present invention, and the phosphorous junctions **1000** devices are 2.4, 3.1, and 3.7 V respectively. In order to compare the performance of these junctions, the inverter delays were compared at a constant L_{eff} of 0.20 microns. **Figure 11** shows that the delay/stage at a given Vdd are approximately the same for all junctions. A slightly higher propagation delay/stage, especially at lower Vdd, found for the arsenic only junction. This is attributed to the higher gate capacitance resulting from the larger Lpoly used for the arsenic only junction device. However, from the hot-carrier DC life time requirement of 10 years, arsenic only junctions can not be used above 2.4 volts, whereas hybrid arsenic/phosphorous junctions, and phosphorous only junctions can be used up to 3.1 and 3.7 volts, respectively. Alternately, for a DC life time of 10 years the phosphorous, hybrid, and arsenic junctions produce delay/stage of 32, 38 and 49 picoseconds, respectively as shown by the dotted lines **1106** in **Figure 11** which clearly demonstrates that hot-carrier reliability limits the performance of arsenic only junctions.

Due to the low diffusivity of arsenic, it is the preferred dopant

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for shallow junctions, providing better roll-off for short-channel devices. In **Figure 12**, inverter delay performance is given for different channel lengths. Three different channel lengths were used corresponding approximately to the expected nominal regime of operation for these junctions. At 3.1 volts and an L_{eff} of 0.215 microns, the hybrid junction delivers 37 picoseconds delay/stage, as shown by the dotted lines 1206 in **Figure 12**. For the arsenic only junction, the same gate delay is achieved with a smaller L_{eff} of 0.164 microns at only 1.9 volts. The reliability constraint of 10-year life time can still be sustained at this voltage for the arsenic only junction as shown in **Figure 10**. In a manufacturing process the L_{eff} variations due to poly gate lithography, etch, and other process parameters must be considered. For example, a 25 nanometer manufacturing variation in L_{eff} causes the delay/stage for the hybrid junction is reduced to 31 picoseconds at 3.1 volts for L_{eff} of 0.19 microns as shown by the dotted lines 1306 in **Figure 13**. This 31 picoseconds delay can be achieved by the arsenic only junctions at 1.8 volts, as shown in **Figure 13**, at an L_{eff} of 0.14 microns. Although the 10 year life time is still achieved at the subnominal L_{eff} of 0.14 microns for the arsenic only junction, off-stage leakage (I_{doff}) becomes unacceptably high at this short channel length. **Figure 14** shows that for the subnominal devices, I_{doff} for arsenic only junctions is more than 10 times higher than that for the hybrid arsenic/phosphorous junctions.

Adding light phosphorous to medium arsenic in the hybrid nLDD dramatically improves hot carrier reliability. For a constant saturation current, I_{dsat} , maximum substrate current, I_{sub} decreases significantly when the phosphorous dose is doubled (compare the open squares with the closed triangles in **Figure 15**), whereas tripling the arsenic doses increases I_{sub} only marginally (compare open squares with open circles in **Figure 15**). The light phosphorous dose in the hybrid junctions helps in grading the nLDD junction profile, thereby reducing

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the peak electric field at this junction. No degradation of the universal $I_{\text{doff}}-I_{\text{dsat}}$ characteristics is found when the phosphorous dose in hybrid junctions is doubled. Increasing the arsenic or phosphorous dose in the hybrid junction decreased the inverter propagation delay.

5 Increasing Vdd from 2.9 to 3.1 volts, the inverter gate delay was reduced from 32 to 31 picoseconds for an L_{eff} of 0.19 microns.

 The foregoing description of the embodiment of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise
10 form disclosed. Obvious modifications or variations are possible in light of the above teachings. The embodiment was chosen and described to provide the best illustration of the principles of the invention and its practical application to thereby enable one of ordinary skill in the art to utilize the invention in various embodiments and with
15 various modifications as are suited to the particular use contemplated. All such modifications and variations are within the scope of the invention as determined by the appended claims when interpreted in accordance with the breadth to which they are fairly, legally, and equitably entitled.

CLAIMS

What we claim is:

1. A method of manufacturing a semiconductor device, the method comprising:
 - 5 defining an active area in a substrate; and
 - forming hybrid nLDD regions by implanting arsenic ions and phosphorous ions in a source region of the substrate and in a drain region of the substrate, wherein the source region and the drain region are in the active region of the substrate.
- 10 2. The method of Claim 1, further comprising: forming a gate oxide region on a surface of the substrate over the active region; forming a gate on the gate oxide region; and forming gate oxide spacers around the gate.
3. The method of Claim 2, further comprising forming source
15 and drain regions by implanting a selected dopant ion.
4. The method of Claim 3, wherein the selected dopant ion is selected from the group consisting of As and P.
5. The method of Claim 4, wherein forming the hybrid nLDD regions is accomplished by implanting As ions in a concentration of 1-
20 $10E14$ per cm^2 .
6. The method of Claim 5, wherein forming the hybrid nLDD region is accomplished by implanting P ions in a concentration of 1-
 $10E13$ per cm^2 .
7. The method of Claim 6, wherein the active region is defined
25 by forming isolation regions in the substrate wherein the active regions are between the isolation regions.
8. The method of Claim 7, further comprising forming a layer of silicide on the surface of the substrate over the source, drain, and gate regions.
- 30 9. A semiconductor device, comprising:
 - a substrate having an active area; and
 - a hybrid nLDD region in a drain region of the active area.

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10. A semiconductor device of Claim 9, further comprising a hybrid nLDD region in a source region of the active area.

11. The device of Claim 10, wherein the hybrid nLDD region in the drain region and the hybrid nLDD region in the source region are
5 doped with arsenic ions and phosphorous ions.

12. The device of Claim 11, wherein the hybrid nLDD region in the drain region and the hybrid nLDD region in the source region are doped with arsenic ions in a concentration of $1-10E14$ per cm^2 .

13. The device of Claim 12, wherein the hybrid nLDD in the
10 drain region and the hybrid nLDD in the source region are doped with phosphorus ions in a concentration of $1-10E13$ per cm^2 .

14. The device of Claim 13, wherein the source and drain regions comprise regions implanted with a selected dopant ion.

15. The device of Claim 14, wherein the selected dopant ion is
15 selected from the group consisting of phosphorus ions and arsenic ions.

16. The device of Claim 15, further comprising a gate oxide region formed on surface of the substrate in the active region and a gate formed on the gate oxide region.

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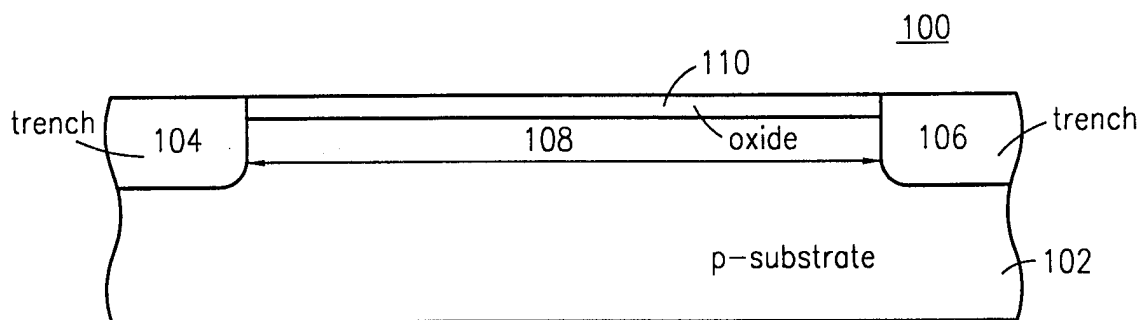


FIG. 1

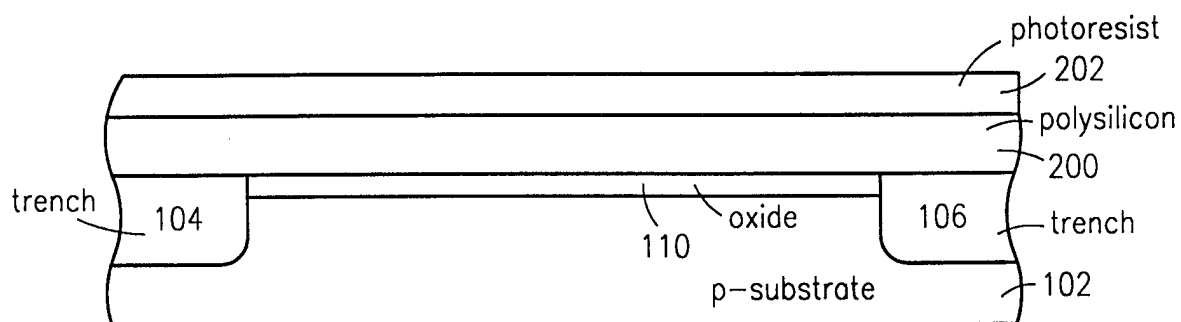


FIG. 2

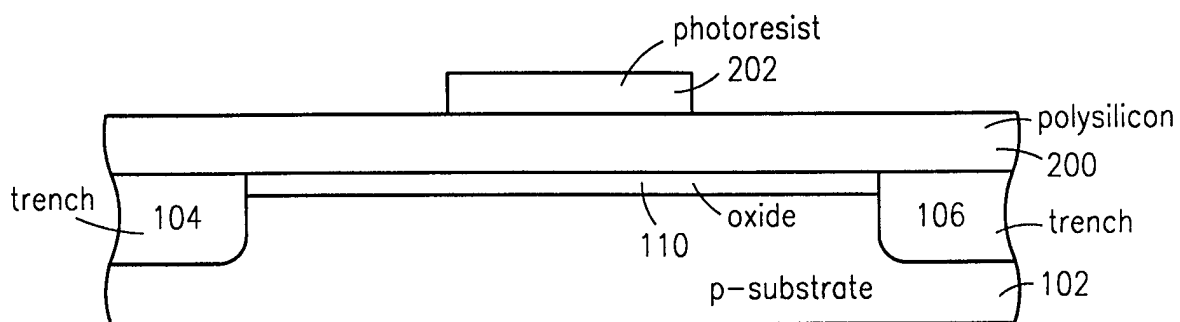


FIG. 3

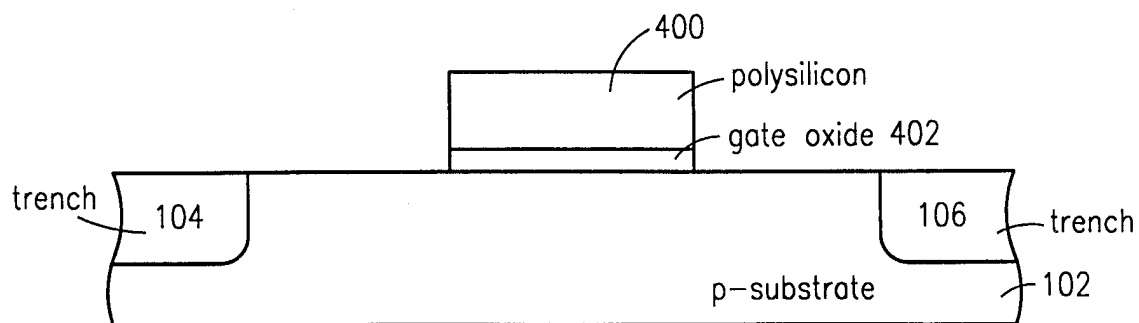


FIG. 4

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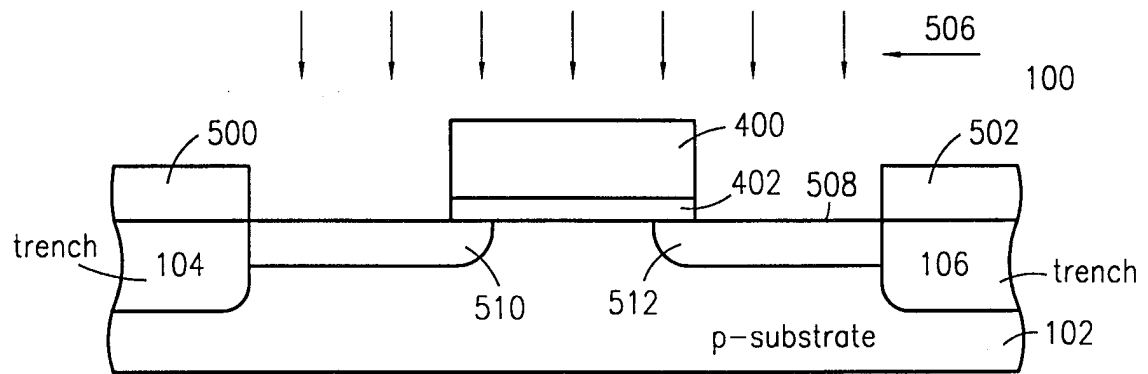


FIG. 5

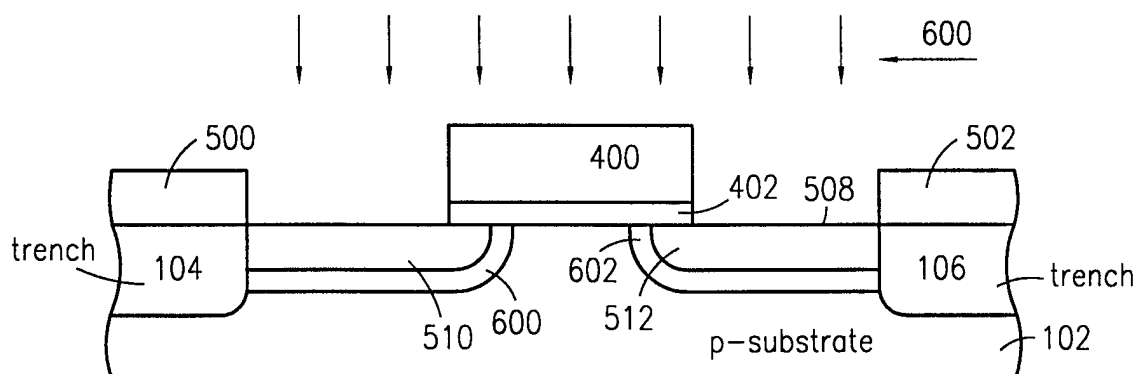


FIG. 6

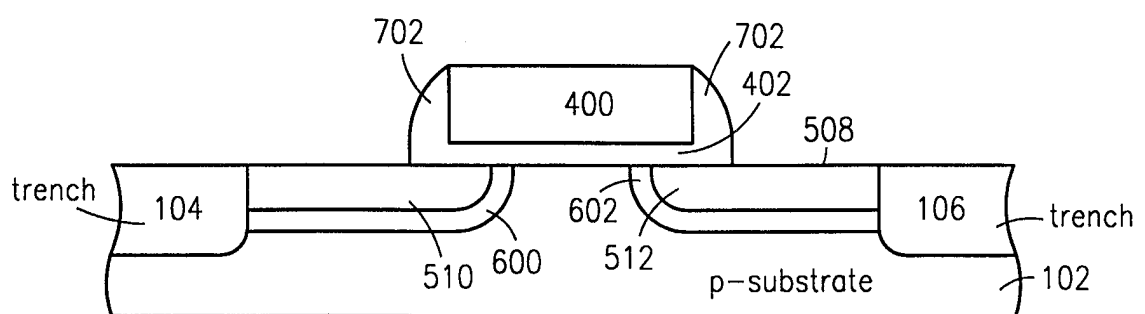


FIG. 7

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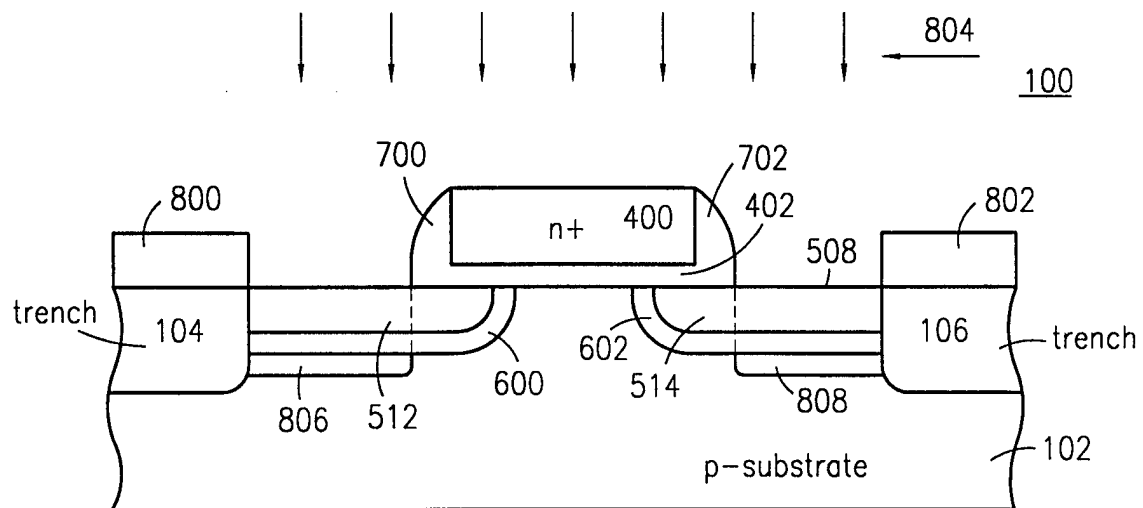


FIG. 8

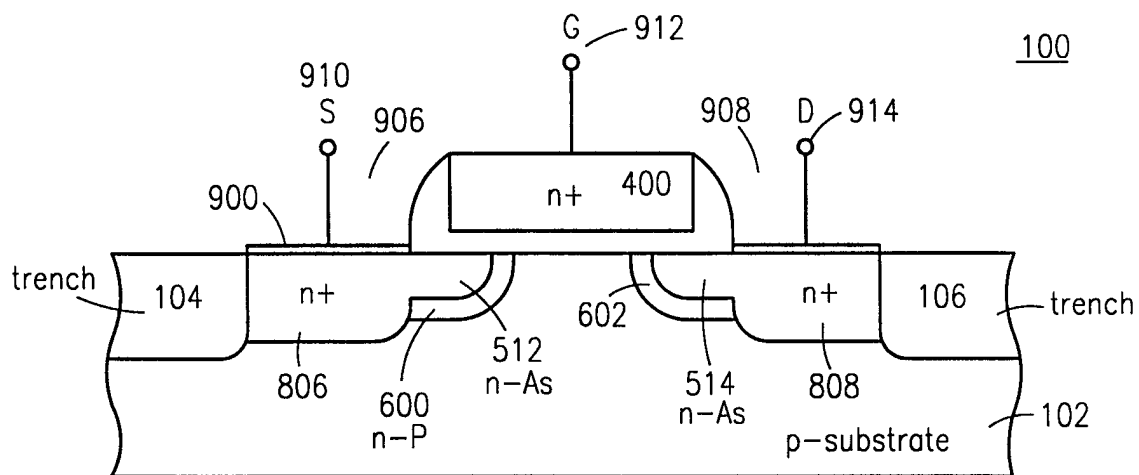


FIG. 9

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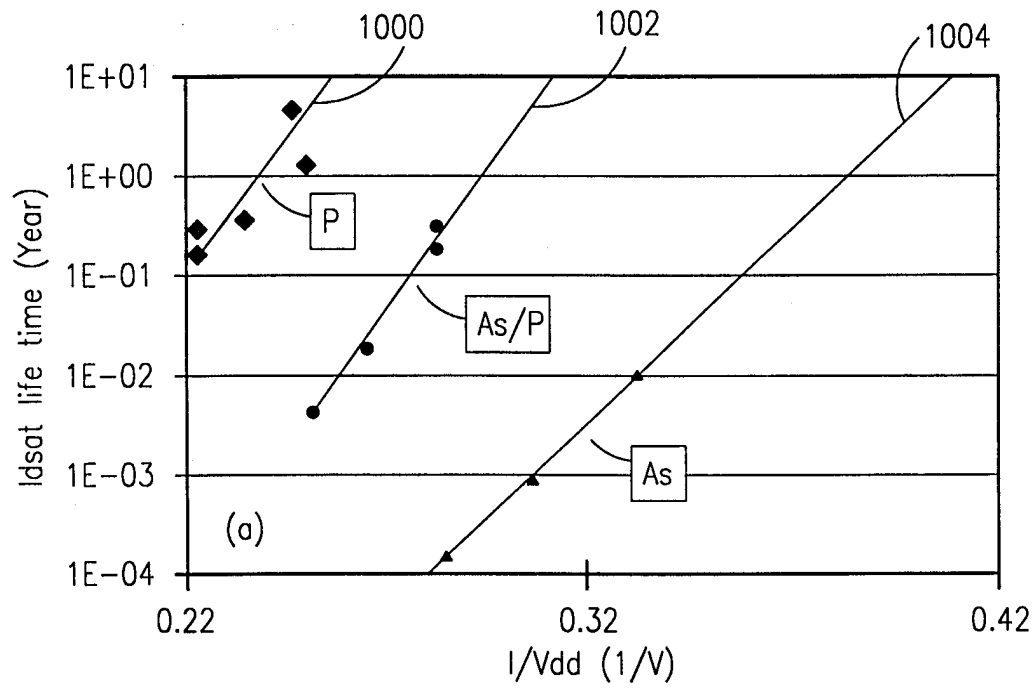


FIG. 10

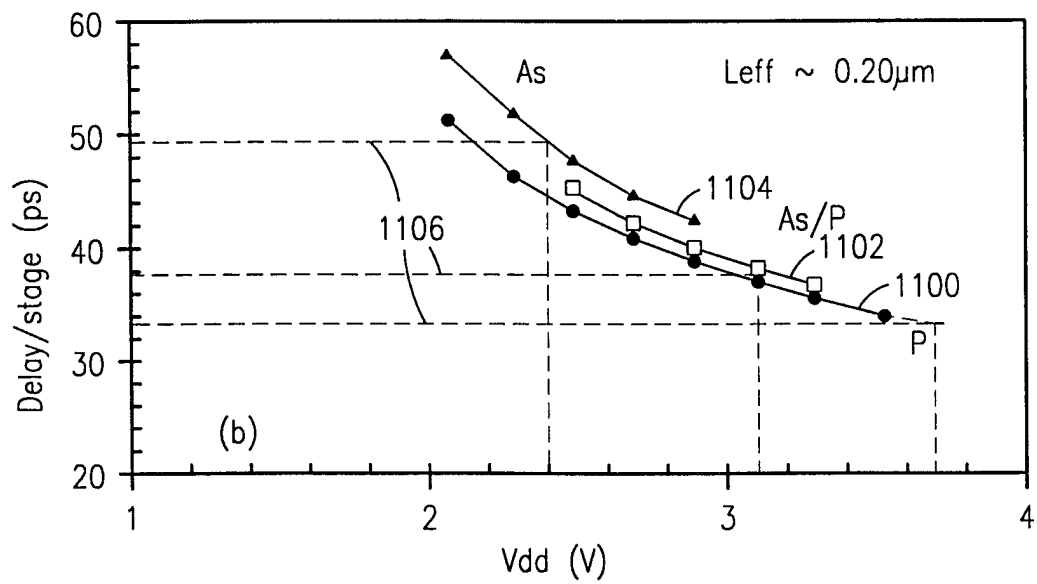


FIG. 11

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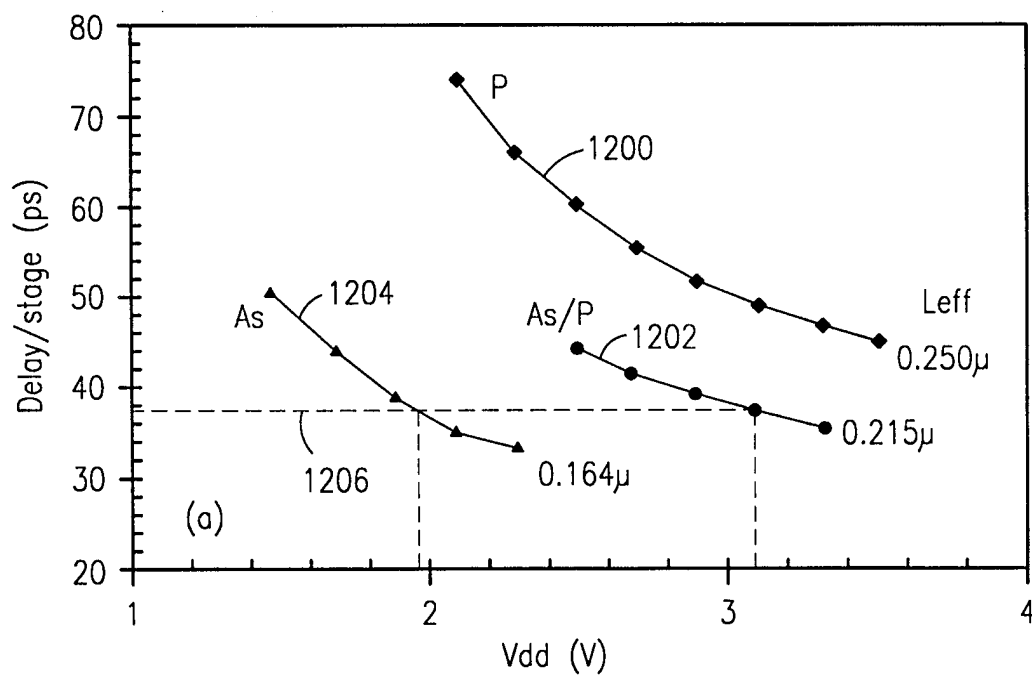


FIG. 12

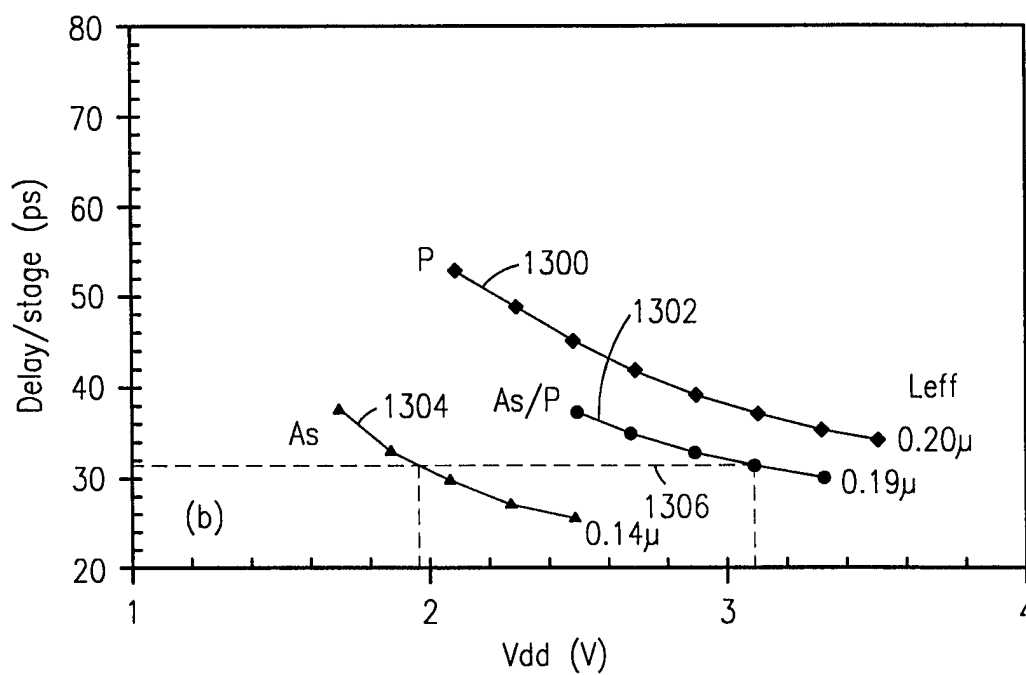


FIG. 13

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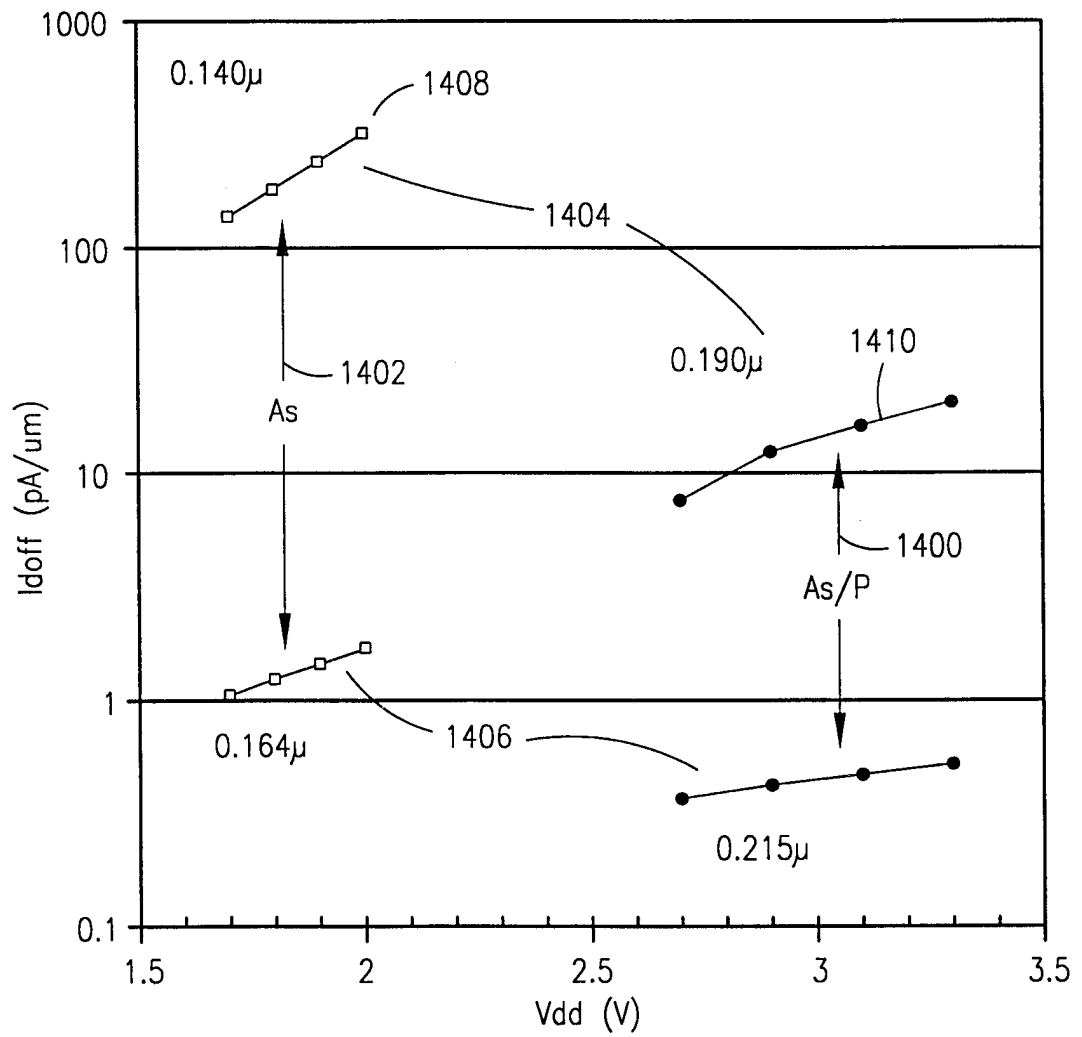


FIG. 14

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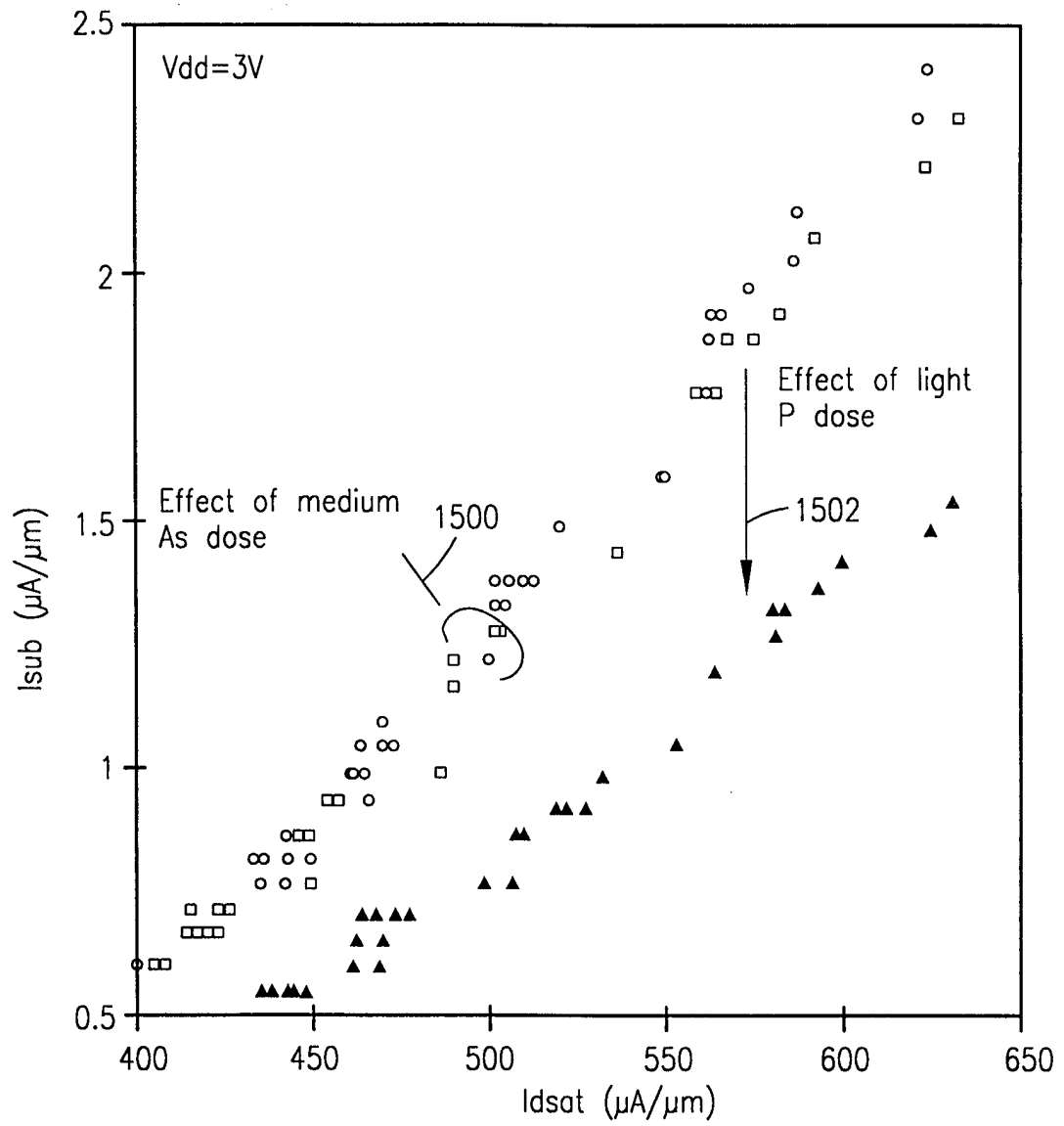


FIG. 15

INTERNATIONAL SEARCH REPORT

Inter. nal Application No

PCT/US 98/01153

A. CLASSIFICATION OF SUBJECT MATTER

IPC 6 H01L29/78 H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 187 016 A (TOKYO SHIBAURA ELECTRIC CO) 9 July 1986	1-7, 9-16
Y	see page 6, line 6 - page 7, line 11; figures 1-4, 6-9 see page 9, line 9 - page 11, line 2 ---	8
X	EP 0 195 607 A (FUJITSU LTD) 24 September 1986 see page 3, column 4, line 37 - line 68; figures 6A-6D ---	1-7, 9-16
X	US 5 376 566 A (GONZALEZ FERNANDO) 27 December 1994 see column 3, line 53 - line 68 --- -/--	1-7, 9-16



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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INTERNATIONAL SEARCH REPORT

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