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ATM CELL SWITCHING NETWORK
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- (71) Applicant(s)
ALCATEL N.V.
- (72) Inventor(s)
MARC DIEUDONNE; PROF. DR. ING LOTHAR KATZSCHNER
- (74) Attorney or Agent
ALCATEL AUSTRALIA LIMITED , BOX 525 G.P.O., SYDNEY N.S.W. 2001
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1. A switching network for switching information in the form of cells transmitted using the ATM technique, the switching network being of the multi-path, cell self-routing and directed sub-switching type, characterised in that detection means are provided at each output access of the switching network in order to detect the absence of a "missing" cell, in the context of a call using this output, and failure registering means for then recording a failure indication specifying that a cell is missing and indicating, from path information derived from another cell in the same call, the path that should have been taken by the missing cell.

AUSTRALIA

Patents Act 1990

ORIGINAL
COMPLETE SPECIFICATION
STANDARD PATENT

Invention Title:

"ATM CELL SWITCHING NETWORK"

The following statement is a full description of
this invention, including the best method of
performing it known to us:-

This invention relates to a switching network for switching information in the form of cells transmitted using the ATM (Asynchronous Transfer Mode) technique, also called asynchronous time multiplexing, the network being of the multi-path, cell self-routing type.

In such switching networks, at the time of a call, cells separated by generally variable intervals have to be routed from an input access to an output access, which permits data transfer between a transmitting terminal connected to the input access and a receiving terminal connected to the output terminal. At any time, the network establishes a multiplicity of such calls. For this purpose, the switching network includes switches which are usually arranged in several stages. The input accesses are connected to the input ports of switches in an input stage, and the output accesses to the output ports of switches in an output stage, while the output ports of switches in the input stage are connected to the input ports of switches in the output stage by switches in one or more intermediate stages. Such a switching network is called a multi-path switching network when it is arranged so that there are several possible paths between any input access and any output access. Such a switching network is called a cell self-routing switching network when it automatically routes each of the cells in the same connection by using path information contained in the cell and which defines by itself, in each stage of the switching network, the address of the cell.

With the cells in the same call being equally distributed over the possible paths, the advantage of switching networks of the latter type is that the overall cell traffic can be distributed in the network homogeneously and that blockage through congestion of cells in one part of the switching network can thus be substantially reduced, or even completely eliminated.

However, one shortcoming of such a type of switching network is that, in the event of a malfunction in the network, which affects only certain cells using the malfunctioning element of the switching network, the malfunctioning element cannot be easily localised. Maintenance is difficult and requires specific, and therefore expensive, measures.

Furthermore, from French Patent Application N° 9414451 (not yet published), a switching network is known of the type which allows the cells in the same call to be

equally distributed over the possible paths and arranged to that effect so that, in the transmission of successive cells in the same call via N possible paths, provision is made for:

- 5 - a census of N possible paths for the cells in the call,
- establishing N sub-connections corresponding to the N possible paths,
- systematically equal distribution of the cells in the call over the established N sub-connections,
- the assembly afterwards of the cells routed by the N sub-connections.

10 In what follows, such a switching network will be described as a "directed sub-switching network".

Such a network also suffers the disadvantage mentioned above.

15 The invention thus has as an objective a switching network of the latter type which has just been mentioned, i.e. a switching network for switching information in the form of cells transmitted using the ATM technique, the network being of the multi-path, cell self-routing and directed sub-switching type which is arranged to facilitate the localisation of defects.

20 According to the invention, there is provided a switching network for switching information in the form of cells transmitted using the ATM technique, the switching network being of the multi-path, cell self-routing and directed sub-switching type, characterised in that detection means are provided at each output access of the switching network in order to detect the absence of a "missing" cell, in the context of a call using this output, and failure registering means for then recording a failure indication specifying that a cell is missing and indicating, from path information derived from another cell in the same call, the path that should have been taken by the missing cell.

25 Advantageously this path information is made up of path data supplied by a cell in the same call, prior to determining that a cell in the call is missing, the said detection means including storage means arranged to record the said path data on transmitting the said prior cell and to play back the said data on transmitting a failure

30 cell so that the said data constitute the said path information in the said failure indication.

According to one variant, the path information is made up of path data supplied by a cell in the same call, which data are available at the time when a cell in the call is determined to be missing and which constitute the said path information in the said failure indication.

When the switching network is organised to maintain the sequence of the cells, i.e. to supply at an output access the cells in a call in the order in which the cells arrived at an input access, whether the connection network preserves the sequence by a controlled routing of the cells in the switches in the various stages of the network or whether it restores the sequence, at each output access, by using sequencing means, application of the foregoing consists quite simply in comparing the sequence number of a failure cell with that of the preceding cell in the call in question. The sequence number must have increased by one unit in relation to the previous one. If not, a cell is assumed missing.

According to one form of implementation, the said detection means include storage means arranged to record the said sequence number on transmission of a previous cell in a call in question and to play it back on transmission of a failure cell in the call in question, and means for comparing the said previous cell sequence number and the said failure cell sequence number, assuming that a cell is missing when the sequence number of the failure cell is different to that of the said previous cell increased by a constant.

According to one form of implementation, each input access includes sequencing means which distribute a sequence number to each cell in the same call and insert it in the path data of the cell, as well as path processing means which in particular write into each cell a path choice value indicating which path the cell has to take from a plurality of possible paths.

Additionally, each switch in the switching network includes means which act when, in the context of a broadcast call, the routing to be given by the switch to a failure cell requires use of a broadcast path memory supplying routing information in order to have the said routing information entered into the said path indication.

The invention thus applies both to broadcast communications and point-to-point communications.

In order that the invention may be readily carried into effect, embodiments thereof will now be described in relation to the accompanying drawings, in which:

Figure 1 is the connection diagram of a switching network in which this invention can be applied,

Figure 2 shows a routed cell in the switching network in Figure 1,

Figure 3 shows the means provided in an access unit (uae) mentioned in Figure 1 to prepare cells in accordance with Figure 2,

Figure 4 shows the means of path marking, provided in each of the switching network switches in Figure 1, to write into each cell routing data indicating which path the cell has taken in the case of a broadcast connection,

Figure 5 shows the means provided in an output unit mentioned in Figure 1 (uas) to utilise cells according to Figure 2 and to record a failure indication in the case of detecting a missing cell.

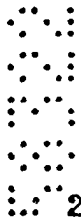
Figure 6 shows a variant of the means in Figure 5.

Figure 1 represents a switching network 1 for switching information in the form of cells transmitted using the ATM technique, the network being a multi-path, cell self-routing and directed sub-switching type.

It includes input accesses such as ace, switches in a stage A such as ma, switches in a stage B such as mb, switches in a stage C such as mc, switches in a stage D such as md, switches in a stage E such as me, and output access such as acs.

Each switch is represented by a rectangle containing a number, 1, N, 32. In the vertical direction, the consecutive switches with numbers 1, N, 32 illustrate a group of 32 similar switches. In this way, the figure represents, in stage A, groups of 32 switches, such as ga, laid out in tiers vertically. At the input ports of these switches, on the left of the figure, which at the same time constitute the input accesses of the switching network 1, input links are connected, such as le, equipped with access units, such as uae, each one connected to the input access port which belongs to it by an input access link lae. Each switch has for example 32 input ports and 32 output ports.

The figure also shows, in stage B, just as in stage A, groups of 32 switches, such as gb, laid out in tiers vertically. The linkages such as lab between stage A and stage



B are arranged separately, in each case between a group of 32 switches in stage A and a group of 32 switches in stage B, such as ga and gb. More precisely, each of the outputs in each switch in stage A is coupled by a linkage to a different switch in stage B and, similarly, each of the inputs in each switch in stage B is coupled by a linkage to a different switch in stage A, and this within two associated groups, such as ga and gb.

The same layout is found within stages E and D, through symmetry, where groups such as ge and gd are equivalent to groups ga and gb.

The interconnection between the groups of switches thus defined in stages B and D is achieved through stage C in which the switches are distributed in sets such as gc, each set having as many switches, for example 32, as each switch in stage B has output ports. The switches in one set all have the same number, which is 1 for the switches in the set gc. Also illustrated are sets of switches with numbers N and 32 to indicate that there are 32 sets. The 32 switches "1" in stage C interconnect the set, which is constituted by the 32 switches "1" in stage B, with those which form the 32 switches "1" in stage D. More precisely, each of the outputs of each switch "1" in stage B is coupled by a linkage such as lbc to a different switch "1" in stage C and, likewise, each of the inputs of each switch in stage C is coupled by a linkage similar to a different switch "1" in stage B. And similar linkages such as lcd are provided between the switches "1" in stage C and the switches "1" in stage D. The same applies to the other sets.

Thus it is clear that a cell reaching the input access ace of the switch ma in stage A can be routed as far as the output access acs of the switch me in stage E through any one of the 32 switches in group gb, through any one of 32 x 32 switches in stage C and through one of the switches in group gd. It will be observed that the identity of the latter is specified as soon as that of the switch in stage C is itself specified. This means no less clearly that each cell thus has the use of $32 \times 32 = 1024$ paths.

In accordance with the patent application mentioned at the beginning of this text, 1024 sub-connections will correspond to these 1024 paths and the 1024 sub-connections will be cyclically used to route the successive cells of the call in question.

The same applies to all calls at the same time, which results in the throughput of the cells in all calls underway being mixed in the switching network and the throughput of cells passing through each switch is a fraction of the overall throughput routed by the switching network, the same for each of them, which avoids complete blocking.

Additionally, it will be mentioned again that the output accesses of the switching network are each provided with an output access unit such as uas, leading to an output linkage ls.

Of course, Figure 1 provides a very specific example of a switching network, just to clarify the concepts, and it is well known in this technology that numerous variants are possible, for example providing switches with more or less inputs and outputs, rectangular switches to reduce the loads of linkages and switches situated at the centre of the switching network, several linkages between two given switches rather than a single one, etc.

Routing of cells in a call is determined from the access unit, such as uae, of the access input through which the call is established. The means employed with this end in view will be those of the previously-mentioned patent application.

These means, contained in the input access unit uae, will allow, from the information received over the linkage le, whatever the format containing it, successive cells to be formed corresponding for example to the format illustrated in Figure 2.

The cell illustrated in Figure 2 thus includes a header ENT followed by a data segment CU containing the call information itself. The header ENT includes in particular (among other data not represented) a path indication ITR, a sequence number NS and a reference indicator NCV.

The path indication ITR corresponds, for each cell in the same call, to one of the available sub-connections. In effect it fully defines the sub-connection by specifying, with the values aa, ab, ac, ad, ae, each reserved for a switch in each of the stages A, B, ..., E, the identity of the output over which the cell reaching the switch has to be transmitted. In the case indicated, where the switches have 32 outputs, each of the values is a binary number of 5 bits.

The sequence number NS is a binary number of several bits (5, for example) which takes the various possible values of the number, cyclically, in the successive cells

of the same call. It readily allows checking of the order of arrival of cells at the output access of the switching network and detecting if one is missing.

The reference indicator NCV identifies the call. It is allocated by a call controller which will not be described in this patent application, because it lies outside the scope of this invention. It is used, among other things, in the case of a broadcast call from one point to several points, from one input access to several output accesses. By using path information previously distributed to these switches, it is then used in certain switches in the switching network to supply the identity of the output(s) of the switch over which the cell has to be retransmitted. We will return later to this aspect of switching within the switching network

We are now going to turn to Figure 3 which represents one mode of design of the access unit uae in Figure 1 which receives input cells and prepares cells conforming to the one in Figure 2.

The input linkage le is connected to an input register RE . For each input cell, this input linkage le supplies at least one data segment CU and a call reference indicator RCV . The data segment is located in the part RCU of the register RE . The reference indicator is located in the part $RNCV$ of the register RE . At the same time, the reference indicator is used as an address to read a call memory MT having one recording location for each call. A sequence number NS which is located in a location RNS of the register RE , and a path indication ITR which is located in a location $RITR$ of the register RE , are read from the addressed location. Furthermore, the sequence number NS is supplied to a sequencing processing unit BC which supplies a new sequence number NNS according to a sequencing algorithm. The sequence algorithm can be simply typified in the addition of a unit modulo 2^s , s being the number of bits in the number NS . Further still, the path indication ITR is sent to a path processing unit BB which supplies a new path indication $NITR$ according to a path algorithm. This algorithm can be typified by repeating the previous example, in the addition of a unit modulo NT to a path choice value formed by putting together the values aa and bb of the cell in Figure 2, in which it may be recalled that they each have 5 bits and each identifies the output port to be used, in the switch of stage A for the first, and in the switch of stage B for the second. In fact, these two combined values really represent

the identity of one of the matrices in stage C, i.e. the identity of one of the 1024 possible paths for any point-to-point call in the switching network in Figure 1. In this case, certainly, NT is precisely $2^{10} = 1024$. The other values of the indication ITR, which identify the output for which the cell is intended, obviously remain unchanged.

The new sequence number NNS and the new path indication NITR are supplied to an input of the memory MT and the reading operation which has just been mentioned is followed by a writing operation by which both these data are written into the same memory location, the address NCV remaining unchanged, to become the corresponding data NS and ITR to be used for the following cell in the same call.

At this time, the content of the register RE is transferred into the register RAE via a linkage It, to be then provided over the input access linkage lae (see also Figure 1). The register RE thus becomes available to receive the following cell, of the same or another call.

The input access unit in Figure 3 further includes a control unit IC which receives data defining the calls to be established from a call controller (not shown, since it is not part of the invention) as previously indicated. These data are transmitted to it via a control linkage lcc and essentially include information to be written into the memory MT, via the linkage cmt, at an address corresponding to a call reference indicator (NCV), this information constituting a path indication ITR and including (see also Figure 2) predetermined values aa and ob, and a set of values ac, ad, ae identifying an output of the switching network to which the cells of the call in question have to be addressed.

Furthermore, the control unit IC controls the rate of operation of the memory MT and the units BC and BB, via the linkages cmt, cbc and cbb.

The foregoing has implicitly dealt with the case of a point-to-point call.

As has already been indicated, in the case of a point-to-multipoint call, the path indication ITR is partially missing in the cells of a broadcast call routed within the network at the time the cells are inserted into an input port in stage A. The reference indicator NCV, translated in certain switches receiving such a cell, defines on which output port(s) of the switch the cell has to be retransmitted. The role of the unit in Figure 3 can now be exactly the same as the one which has just been described,

except that the control unit IC writes a conventional value into the memory MT for the part of the indication ITR (see Figure 2) which corresponds to the values ac, ad, ae.

We will now turn to Figure 4 which represents schematically path marking means, provided in each of the switches in the switching network in Figure 1, to write routing data into each cell indicating which path the cell has taken.

Figure 4 represents for this purpose a switch comprising a cell switching device cm to which are connected input linkages such as lec and output linkages such as lsc, and its control device ccm. Represented in the latter are a path processing register rtt as well as a routing control device dtt, a broadcast path memory mtt and a path indication processing unit utt.

With a cell arriving over the linkage lec, the routing data NCV and ITR in its header (see Figure 2) are provided to the register rtt, via a linkage ett, and from there to the routing control device dtt. The latter, in the case of a point-to-point call, selects the value in the indication ITR corresponding to the stage in which the switch in question is found, aa for example. It transmits this information over the linkage ach to the cell switching device cm. Simultaneously, the device dtt actuates the unit utt whose role is, for example in accordance with a well-known method, to transpose the values aa to ae in the indication ITR which the register rtt holds, so that the value ab takes the place of the value aa which itself takes the place of the value ae, and so on. This allows each switch, without knowing in which stage it is situated, to always take the value, which is intended for it, at the same place in the indication ITR. The cell switching device cm, receiving thus modified routing data over the linkage ett and routing information over the linkage ach, consequently modifies the received cell, then records and writes it in order to be retransmitted over an output linkage such as lsc designated by this routing information. When this is possible, i.e. after other possibly ready and priority cells, the cell in question modified in this way will be retransmitted over the designated output of the switch in Figure 4. It will be remembered from the foregoing that the complete path indication ITR remains in the cell, which will make it possible to ascertain which path the cell has taken in the switching network and even, to be more precise, which of the possible paths it has taken.

In the case of a broadcast call, the device dtt activates the broadcast path memory which receives the reference indicator NCV and consequently supplies routing information which is transmitted over the linkage ach, in place of the value derived from the path indication ITR. This information is transmitted at the same time to the unit utt which enters this information into the values of the path indication ITR in place of that which would have been used if it had been a matter of a point-to-point call. Apart from this difference, the routing of a cell over an output is the same as that described above. If the cell has to be retransmitted over a second output, the device dtt receives the information from the memory mtt and repeats the operation. Of course, in order to save time, certain parts of these repeated operations can be performed in parallel and shared in accordance with known techniques. Apart from this, the result is that the indication ITR of a duplicate of the cell in question is thus going to receive a value corresponding to the routing carried out in the switch and that such a duplicate will arrive over an output of the switching network while having received a sequence of values which will complete its path indication ITR so that the latter will define the path taken by the cell within the switching network.

Thus all cells arriving at the outputs of the switching network contain such a whole or completed path indication ITR characterising the route which they have taken in the switching network.

While referring to Figure 5, we now turn towards the means which are provided in an output unit mentioned in Figure 1 to make use of the cells in accordance with Figure 2 and to record a failure indication in the event of detecting a missing cell.

The means illustrated by Figure 5 include:

- a cell arrival register RCC receiving header data from each cell transmitted as output from the switching network to the output linkage ls,
- a cell path memory MCA storing data related to the various calls established over the linkage ls,
- a preceding cell register RCL in which will be written the information previously recorded in the memory MCA on the occasion of a preceding cell in a call, when a cell in the call is transmitted over the linkage ls,
- a comparator CP being used to detect a missing cell,

- a memory MIC constituting a failure register,
- a linkage clock HG.

Each cell appearing over the linkage acs', which is one of the output linkages in the switching network in Figure 1, is transmitted to the transmission device FE which will not be further described here, since it goes beyond the scope of the invention.

A resequencer can be inserted between the output of the switching network such as that in Figure 1 and the linkage acs'. Such a device is described in European Patent Applications N° 0602281 and 0602282, both having the title of "Resequencing device for a cell switching system node". Since the throughput time of the switching network is different according to the cells in the same call because of variable holding times in the switches passed through, as indicated above, the resequencer has the function of putting the cells into sequence number order.

In each of the cells transmitted over the linkage acs', the linkage clock HG monitors an operating cycle of the device in Figure 5. First it activates the operation of the register RCC so that it records the header of the cell containing the routing reference indicator NCV, the sequence number NS and the path indicator ITR. As soon as the header is present in the register RCC, it is recorded in the cell path memory MCA, in an appropriate location for the call to which the cell in question belongs, designated by an address which is supplied by the indicator NCV.

First, however, the information written into the same location on transmission of the previous cell in the same call and retained there until transmission of the cell in question, is read in order to be written into the register RCL. The sequence numbers of the cell in question, NS, and the previous cell NS' are compared in a comparator CP which constitutes a detection device allowing the lack of a cell to be detected. If the two numbers are in the right order ($NS' = NS + 1$), everything is normal and no further operations take place.

If the two numbers are not in the right order, a cell is said to be missing. In that case, the comparator CP supplies a signal si which simply starts recording into the failure memory MIC the contents of the register RCL, to which the sequence number NS of the cell in question is optionally added. The recorded information concerns essentially a cell correctly routed in the switching network in Figure 1 before the cell in

question. It makes it possible to ascertain which way the cell has gone. Since it has been seen that successive cells in the same call successively take, in a given order, the different paths available, it is easy to deduce which path the following cell in the same call should have followed. The accumulation of such information and their statistical analysis makes it possible to establish that all the missing cells had to take a given circuit in the switching network, which can be assumed to be defective. This may give rise to corrective action.

If subsequently a missing cell arrives over the linkage acs', the comparator CP will also detect it. The information recorded in the failure memory MIC actually contains the sequence number of this cell transmitted out of sequence. Interpretation of the information recorded in the failure memory MIC will make it possible to establish the particular circumstances and, for example, to remove this cell from the missing cell category.

With reference to Figure 6, a variant of the means in Figure 5 will now be briefly described. The elements retained from the device in Figure 5 have the same references, while those which have been modified have an asterisk.

Therefore, unchanged are the linkage acs', transmission device FE, linkage ls, clock HG and the cell arrival register RCC. The memory MCA* is similar to the memory MCA, except that it records only the sequence number NS of the failure cell. In the same way, the previous cell register RCL* reads only the previous sequence number NS'. The comparator CP is unchanged. The memory MCI is not modified but, in the event of a missing cell, it records the sequence number NS and the path indication ITR of the failure cell, instead of path data derived from the memory MCA. Operation is the same as previously, with this exception which signifies that, in the missing cell case, the path indication of the failure cell is recorded, the missing cell assumed to be the one which preceded it, whereas in the case of Figure 5 the path indication of a previously transmitted cell is recorded, the missing cell assumed to be the cell which immediately followed this previous cell. In all cases where a single cell is missing, the two solutions are equivalent.

The failure indications written into the memory MCI can be used in quite a few ways. The simplest, when the switching network has a high reliability, merely consists

in supervising the filling level of the memory MCI. As long as this level rises only at a slow and random rate, one is presented only with sporadic failures which can be neglected. On the other hand, if the level starts to suddenly rise at a sustained rate, an alarm must be given and the contents of the memory MCI must be subjected to statistical processing which aims to determine the path which each missing cell ought to have taken. In the case of the device in Figure 5, the hypothesis is made that the missing cell was the one which immediately followed the cell whose path data have been recorded. Knowing the algorithm applied by the unit BB in the input access units of the network such as uae (Figure 3), it is easy to establish the path allocated to the missing cell. In the case of the variant in Figure 6, the hypothesis is made that the missing cell was the one which immediately preceded the cell whose path data have been recorded. Its path will be quite easily determined as well. The missing cell paths can be expressed in the form of a sequence of 5 switch numbers, one per stage of the switching network, which is sufficient for comparison. If it seems that the same number reappears continually, in one of the stages, the switch which it identifies is probably at fault. Before replacing the switch, one automatic maintenance step will consist in modifying the algorithm applied in the units BB of the input access units (Figure 3) so that, of the possible paths, at least all those which pass through this matrix are removed.

It is quite obvious that the preceding descriptions have only been given by way of example only and that numerous variants can be devised despite that without departing from the scope of the invention as defined in the claims. The numerical values in particular will vary with each application. Moreover, mention will be made that it is not necessary that the cells transmitted through the switching network have a sequence number (NS), an abnormally long period between successive cells can also indicate that a cell is missing. Likewise, the comparative test of the cell path indications which are in the right order can indicate that the sequence defined by the sequencing algorithm is no longer complied with, which also is characteristic of a cell being missing.

The claims defining the invention are as follows:

1. A switching network for switching information in the form of cells transmitted using the ATM technique, the switching network being of the multi-path, cell self-routing and directed sub-switching type, characterised in that detection means are provided at each output access of the switching network in order to detect the absence of a "missing" cell, in the context of a call using this output, and failure registering means for then recording a failure indication specifying that a cell is missing and indicating, from path information derived from another cell in the same call, the path that should have been taken by the missing cell.

2. A switching network as claimed in Claim 1, wherein the path information is made up of path data supplied by a cell in the same call, prior to determining that a cell in the call is missing, the said detection means including storage means arranged to record the said path data on transmitting the said prior cell and to play back the said data on transmitting a failure cell so that the said data constitute the said path information in the said failure indication.

3. A switching network as claimed in Claim 1, wherein the path information is made up of path data supplied by a cell in the same call, which data are available at the time when a cell in the call is determined to be missing and which constitute the said path information in the said failure indication.

4. A switching network as claimed in Claim 2 or 3, wherein the said detection means include storage means arranged to record the said sequence number on transmission of a previous cell in a call in question and to play it back on transmission of a failure cell in the call in question, and comparator means for comparing the said previous cell sequence number and the said failure cell sequence number, assuming that a cell is missing when the sequence number of the failure cell is different to that of the said previous cell increased by a constant.

5. A switching network as claimed in Claim 4, wherein the said constant is 1.

6. A switching network as claimed in any one of the preceding claims, wherein each input access includes sequencing means which allocate a sequence number to each cell in the same call and insert it into the path data, and path processing means writing in particular into each cell a path choice value indicating which path the cell

has to take from a plurality of possible paths.

7. A switching network as claimed in any one of the preceding claims, wherein each switch in the switching network includes means acting when, in the context of a broadcast call, the routing to be given by the switch to a failure cell requires use of a broadcast path memory supplying routing information, in order to enter the said routing information into the said path indication.
8. A switching network substantially as herein described with reference to Figures 1 - 6 of the accompanying drawings.

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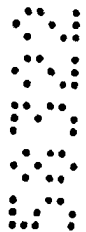
DATED THIS SEVENTH DAY OF JUNE 1996
ALCATEL N.V

ABSTRACT

A switching network of the "multi-path, cell self-routing and directed sub-switching" type including detection means (RCC, MCA, RCL, CP; RCC, MCA*, RCL*, CP) provided at each output access of the switching network in order to detect the absence of a "missing" cell, in the context of a call using this output.

Incident registering means (MCI) then are provided to record a failure indication specifying that a cell is missing and indicating, from path information derived from another cell in the same call, the path that should have been taken by the missing cell.

Figure to be published: 5



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FIG. 2

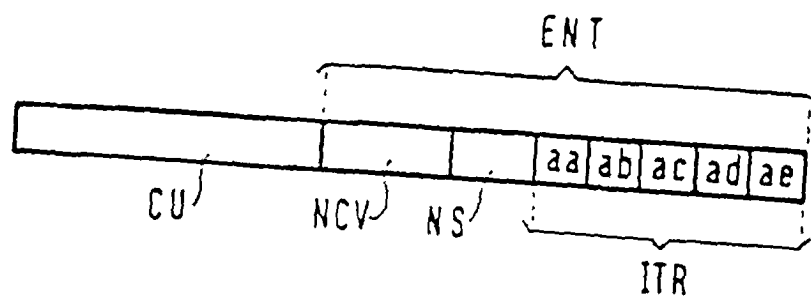


FIG. 3

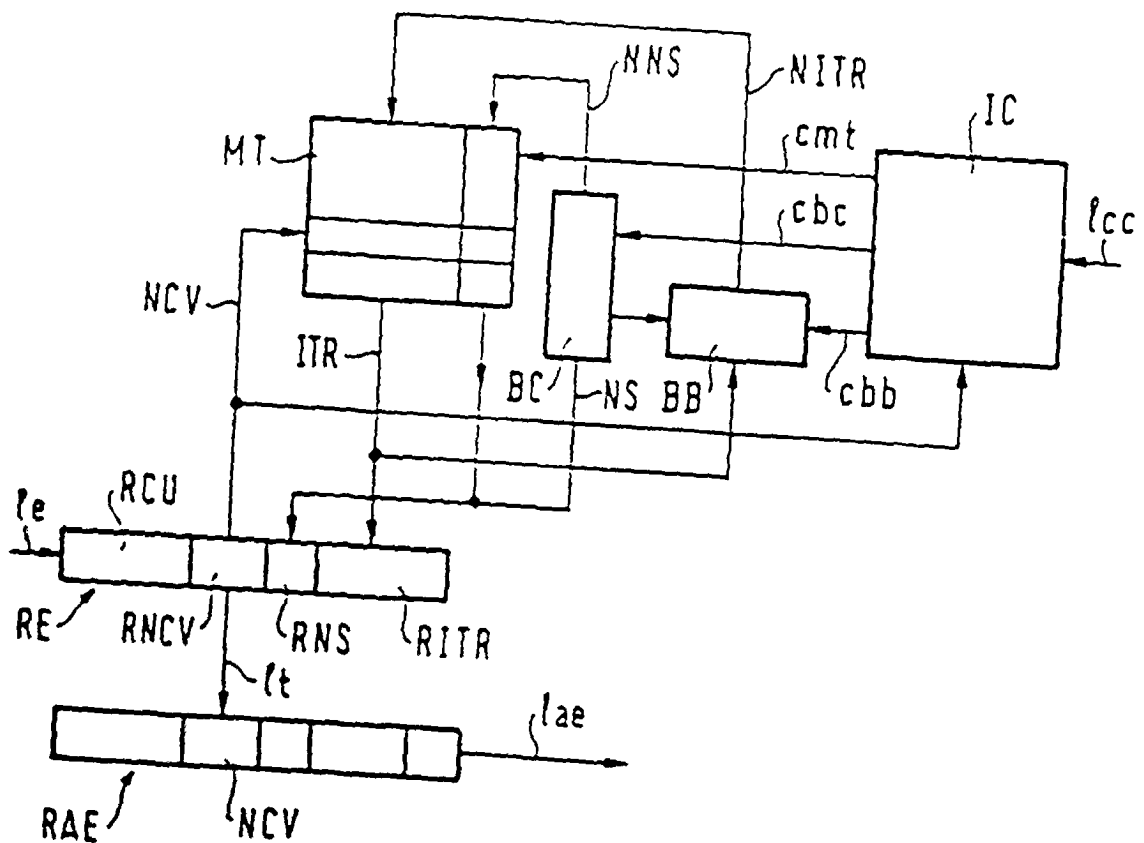


FIG. 4

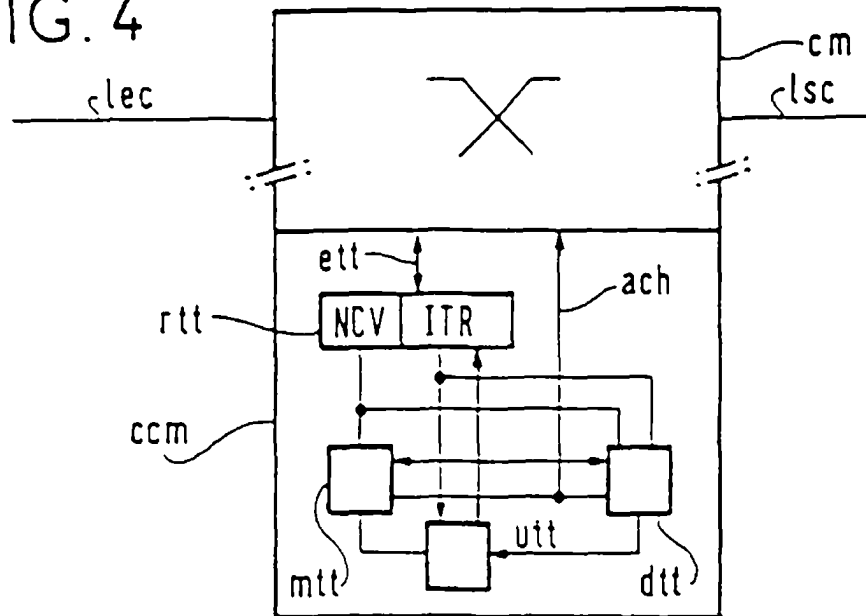


FIG. 5

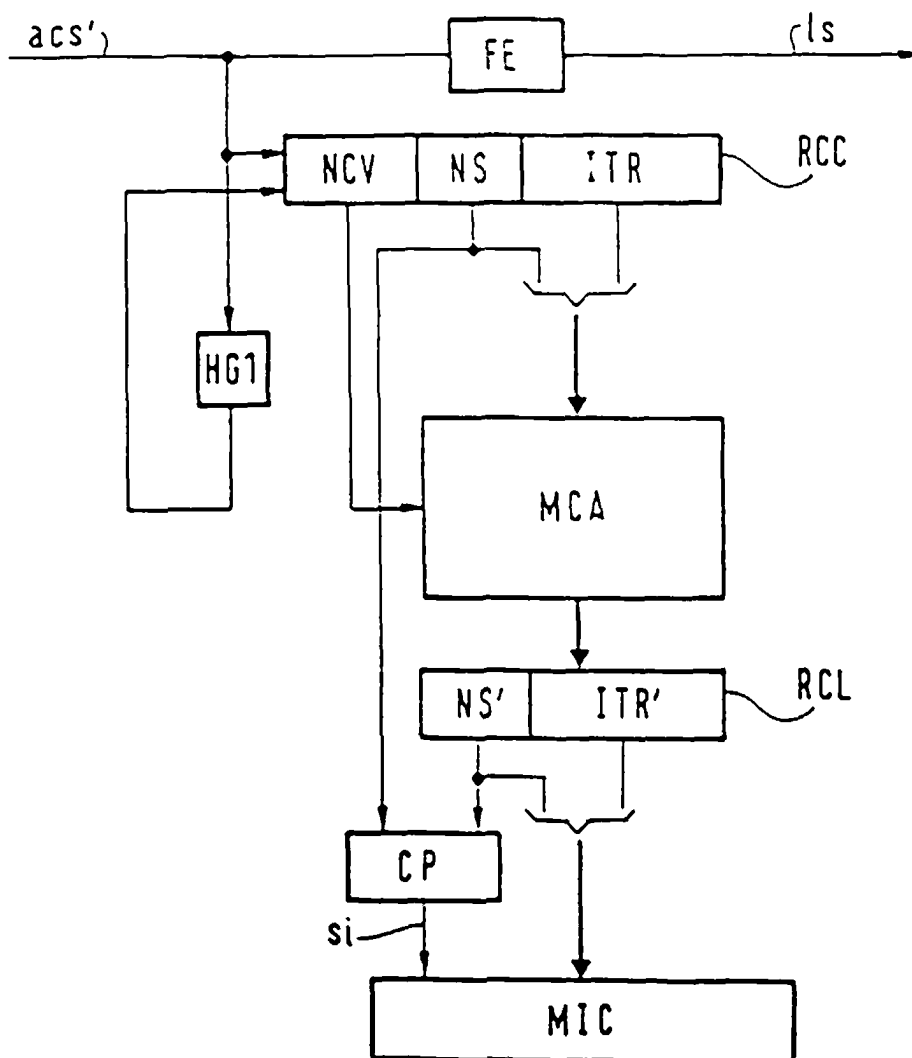


FIG. 6

