

[54] **SOLID STATE TIMER**

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[51] Int. Cl. **H03k 17/28**

[58] Field of Search 102/70.2; 307/220, 223, 293, 307/304; 328/129, 130, 131, 39, 41, 43, 48, 63, 72, 74, 75, 77; 331/113; 340/174 SR

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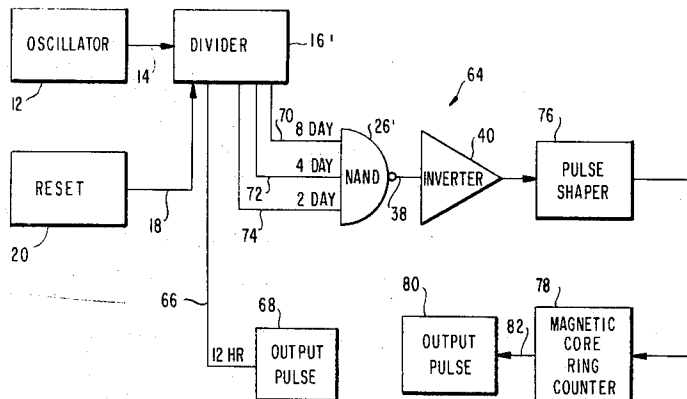
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Assistant Examiner—R. C. Woodbridge
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[57] **ABSTRACT**

Disclosed is a timer of all solid state components and primarily formed from integrated circuits. The timer comprises a very low frequency oscillator coupled through a divider to an output circuit. In one embodiment, the timer is used to self-destruct a land mine after about twelve hours. In another, it produces an output from a magnetic core ring counter after about a year. Complementary MOSFET's are used for the circuit components to minimize power consumption in both embodiments.

8 Claims, 6 Drawing Figures



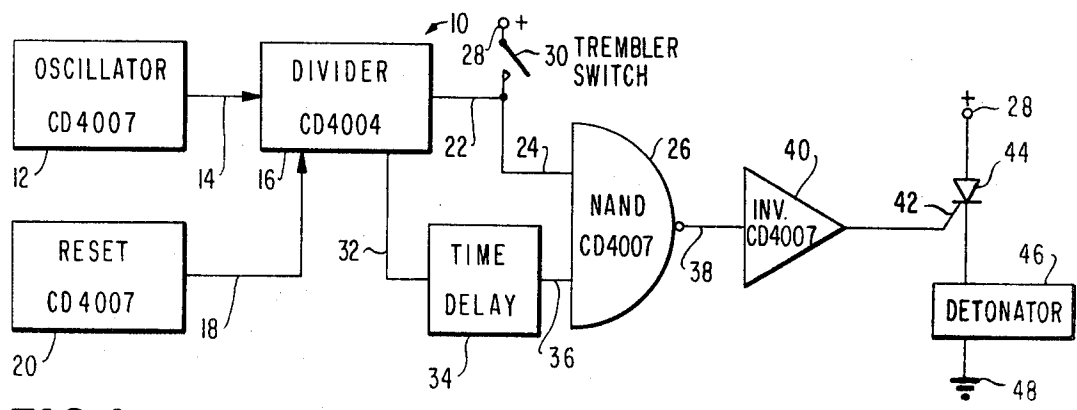


FIG. 1

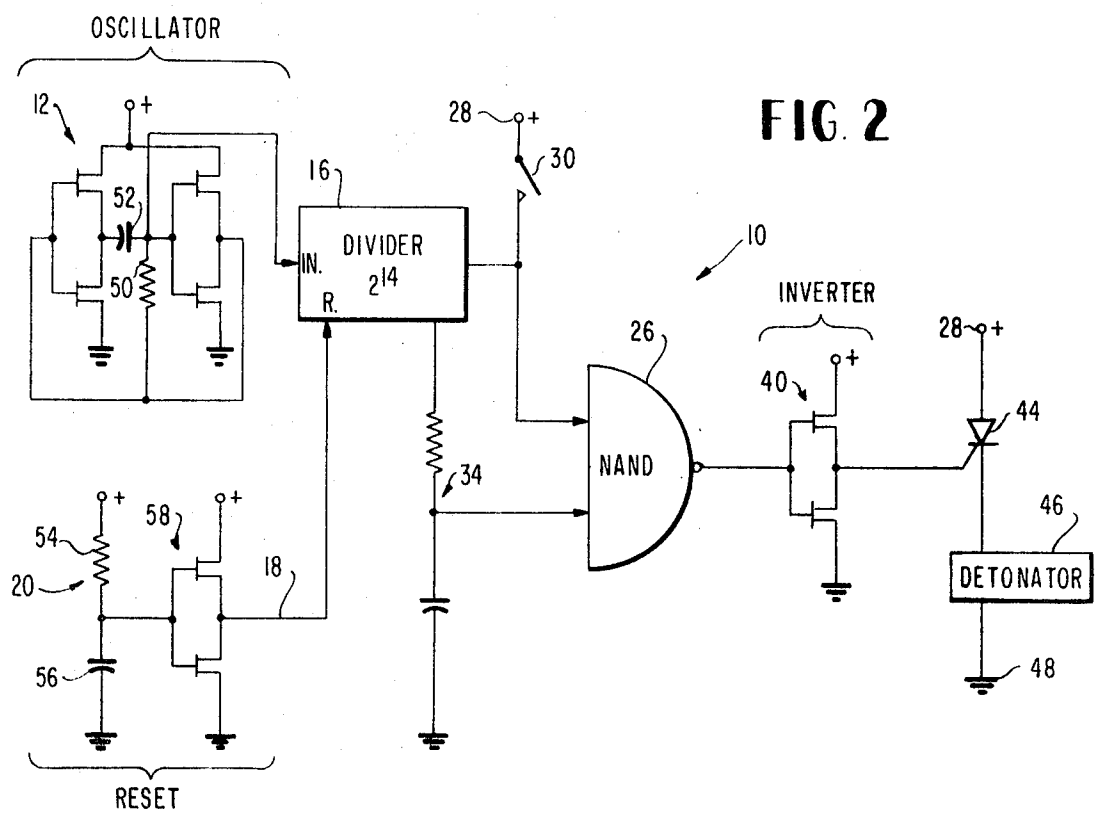


FIG. 2

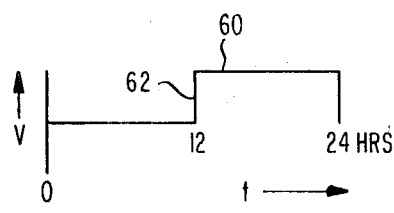
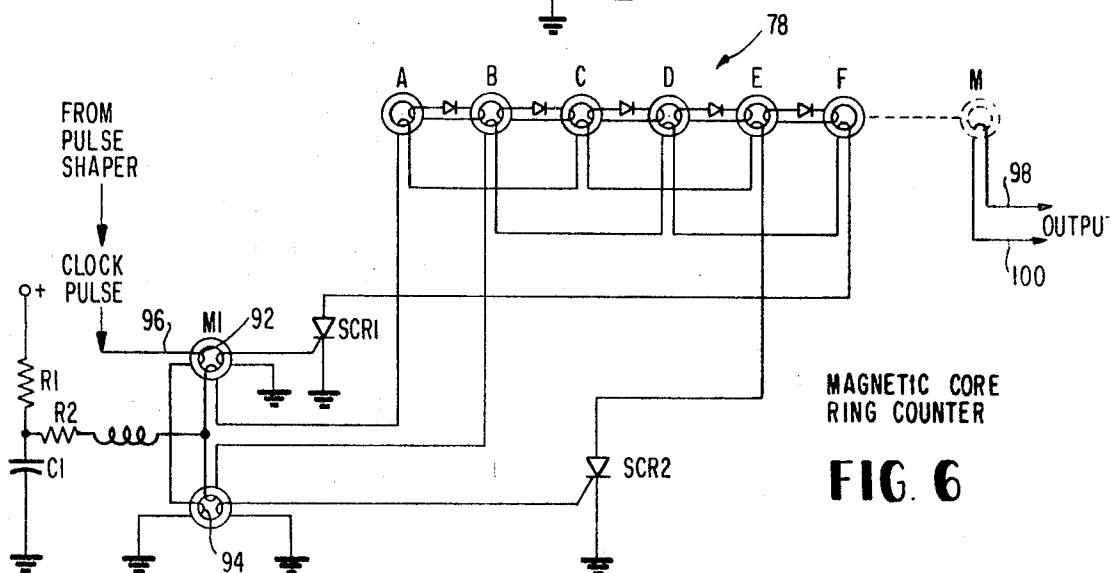
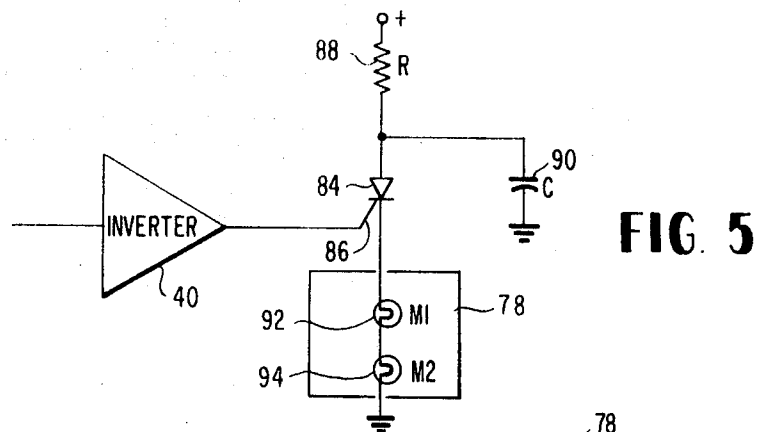
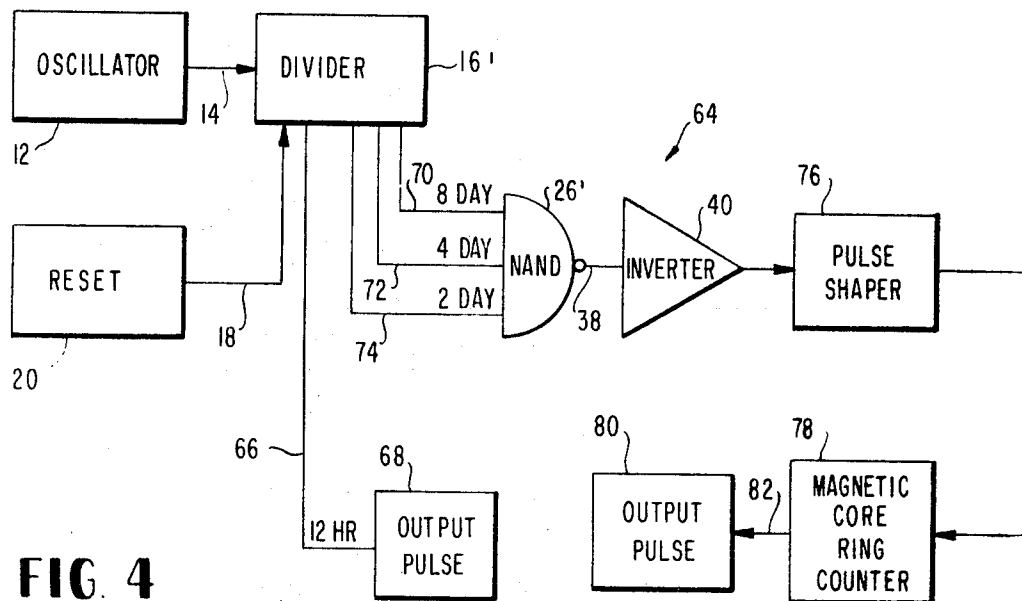


FIG. 3

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SOLID STATE TIMER

This invention relates to solid state timing devices and more particularly to an integrated circuit digital timer capable of initiating functions over a substantial period of time. Important features of the invention include the provision of a timing device which requires little power, is of small physical size and weight, and which will operate reliably in severe environments.

The timer of the present invention is particularly adapted for military and related applications where detonator circuits or signal or control circuits must be closed after a predetermined time of substantial duration. In one embodiment of the present invention, the timer is particularly adapted to cause a land mine or similar explosive charge to detonate or self-destruct after a period of as much as twelve hours. In a second embodiment, the timer of the present invention is adapted to provide an electrical output in a lunar surface environment after a period of as much as one year.

Timing devices for producing an electrical output after a substantial length of time are well known. In many instances these take the form of mechanical devices which are quite bulky and which in many instances will not withstand the severe environments to which they may be exposed. Previous electrical devices for producing extended delays have likewise usually been excessively large and have required large power supplies to supply the required energy for the electrical components of the system.

The present invention provides an electrical timer which overcomes these and other disadvantages through the utilization of integrated circuit components which are of relatively small size and weight and which will operate on a minimum of power for extended periods of time. The basic timer construction takes the form of an integrated circuit low frequency oscillator which supplies pulses to a utilization device through a frequency divider in the form of a solid state counting chain of integrated circuit flip-flops. In one embodiment, the divider output is passed through a logic circuit to actuate the detonator of an explosive charge, such as a land mine. In a second embodiment, the output of the divider is supplied to a ring counter to produce extended periods of delay with a minimum of energy drain.

It is therefore one object of the present invention to provide an improved electronic timing device.

Another object of the present invention is to provide an improved solid state timer for initiating events after a substantial predetermined period of time.

Another object of the present invention is to provide a solid state timer in which the solid state components require a minimum of energy to operate.

Another object of the present invention is to provide a solid state timer made up primarily of integrated circuit components.

Another object of the present invention is to provide a timer comprising an oscillator and counting chain connected to a magnetic core ring counter.

Another object of the present invention is to provide a self-destruct delay circuit for explosive charges, such as are used in land mines.

These and further objects and advantages of the invention will be more apparent upon reference to the following specification, claims, and appended drawings, wherein:

FIG. 1 is a block diagram of a timer circuit particularly adapted for use in energizing the explosive charge of a land mine;

FIG. 2 is a more detailed diagram of the circuit of FIG. 1;

FIG. 3 shows a waveform of the voltage output for the circuit of FIGS. 1 and 2;

FIG. 4 is an overall block diagram of a counter constructed in accordance with the present invention and particularly adapted to operate on the moon;

FIG. 5 is a circuit diagram of the pulse shaper forming a part of the timer of FIG. 4; and

FIG. 6 is a detailed circuit diagram of the magnetic core ring counter forming a part of the timer of FIG. 4.

Referring to the drawings, FIG. 1 is a block diagram of a timer, generally indicated at 10 in that FIG., particularly adapted for use in a land mine. The timer comprises an integrated circuit oscillator 12 feeding an output signal by way of lead 14 to an integrated circuit divider 16. Also applied to divider 16 by way of a second lead 18 is a reset pulse or signal from reset pulse source 20.

The divider output is connected by way of lead 22 to one input 24 of an integrated circuit NAND-gate 26. This input of NAND-gate 26 is connected to the positive side of a power supply (not shown), i.e., power supply terminal 28, by way of a trembler switch 30. The other input of NAND-gate 26 is connected to the positive side of the power supply through the divider 16 and by way of lead 32 and arming time delay 34 to the other gate input 36.

NAND-gate 26 supplies an output at lead 38 through an inverter 40 to the gate 42 of a silicon controlled rectifier 44. SCR 44 acts as a switch connecting a land mine detonator 46 between the positive side 28 and grounded side 48 of the power supply.

FIG. 2 shows the timer 10 of FIG. 1 with certain components disclosed in more detail. Oscillator 12 forms a time base which supplies clock pulses to the divider 16. In the preferred embodiment, oscillator 12 operates at a rate of one pulse every 5.625 seconds. That is, its pulse repetition rate is 1/5.625 per second. The oscillator in the preferred embodiment is of the type shown and described in assignee's copending application Ser. No. 802,571, filed Feb. 26, 1969, the disclosure of which is incorporated herein by reference. It is an RC or multivibrator type oscillator utilizing complementary metal oxide silicon field effect transistors (COM/MOSFET). It is a relatively stable oscillator which employs two complementary sections of RCA's COM/MOSFET CD4007, plus a resistor 50 and a capacitor 52.

Reset circuit 20 in FIG. 2 comprises a time delay circuit made up of resistor 54 and capacitor 56 connected to the input of a single complementary section 58 of RCA's COM/MOSFET CD4007. The reset pulse is supplied by lead 18 to the reset terminal of divider 16. Divider 16 is in the form of a flip-flop counting chain and preferably comprises sufficient stages to divide the output of the oscillator 12 by 2^{14} . The divider is preferably formed of two RCA COM/MOSFET integrated circuit CD4004. The logic two NAND-gate 26 employs an RCA COM/MOSFET CD4007 and inverter 40 is a single complementary section of RCA CD4007.

The circuit of FIG. 2 is designed to perform the following functions: (a) Become operative upon the inception of power to the various components, (b) introduce a 90-second delay period for arming the mine (sterile period), (c) after 90 seconds the mine is in the "armed" position such that when trembler switch 30 within the mine is disturbed, the mine detonates, (d) the mine self-destructs if it has not been disturbed within a 12 hour period. These features are all provided in an electrical circuit construction which has small physical size and weight since most of the circuit components, including the oscillator, the reset, the divider, the NAND gate, and the inverter, are made of integrated circuits and because of the complementary MOSFET construction, the timer requires little power and consumes it at a very low and slow rate.

In operation, when the mine has been installed, the timer is activated by closure of a suitable manual switch (not shown) connecting the components shown in FIGS. 1 and 2 across the mine power supply, i.e., a small battery. When the circuit is energized, the reset pulse generator 20 acts to provide a high level pulse to set all the stages of the divider 16 to the same level to insure the proper count of a pulse each time the circuit is activated. After the reset generator 20 injects the short high level pulse, it grounds the reset input of divider 16 to allow proper functioning of the divider.

Divider 16 acts as an accumulator to collect pulses from oscillator 12 and, depending upon the number of stages, can give very long time delays. In one circuit constructed in accordance with the present invention, divider 16 was provided

with 14 stages and was capable of producing one complete cycle in 24 hours as illustrated by the voltage waveform 60 in FIG. 3 with a 5.625 second pulse input rate. In the actual device constructed, only one-half of the period of the last divider stage was used in order to minimize circuitry and parts and improve reliability. In the circuit, after 12 hours, the positive going signal at 62 in FIG. 3 appears at the input to the logic circuit 26 and since the signal on the other input 36 from the arming time delay (ATD) 34 is also a high level signal at the same time, logic circuit 26 shifts from a high level to a low level state at its output. It is apparent that the circuitry becomes more involved if the total period of 24 hours is used since there is a negative going signal at the end of the period.

An arming time delay (ATD) of 90 seconds is introduced by connecting the power supply through one of the stages of divider 16 to an RC circuit 34 whose output is fed to one input 36 of logic circuit 26. By connecting the power supply signal through the divider, i.e., tapping off the divider, it is possible to use smaller values of resistor and capacitor for time delay circuit 34 than possible if this circuit were to be connected directly to the power supply battery. That is, by connecting through the divider, it is possible to use physically smaller components for time delay circuit 34 with a corresponding reduction in size and weight.

When the timing circuit is first energized, reset generator 20 supplies a reset pulse to the divider resetting the stages of the divider to a zero state. After 90 seconds, the power supply signal passes through the divider and the time delay circuit 34 and appears at the input 36 of logic circuit 26. This 90 second delay period affords the person who sets the mine an opportunity to get away from it before it becomes armed. Once the mine is armed, actuation, i.e., closing of trembler switch 30, causes the power supply voltage to also appear on input lead 24 to the NAND or logic circuit 26. Conversely, if the trembler switch is not energized, divider 16 counts the pulses from oscillator 12 and at the end of 12 hours switches to a high voltage level at output 22 which is applied to input 24 of the NAND gate. The logic circuit (negative AND gate) notes all intermediate functions, arm time delay and either the trembler switch or the divider output, by their level shifts before it produces an output level change to turn "on" the load switching circuit (SCR) 44. Inverter 40 is required at the output of the logic circuit to give a high level signal needed to turn "on" the silicon controlled rectifier. Thus, if the trembler switch 30 is activated at any time which is more than 90 seconds after the timer is energized but less than 12 hours after energization, the mine will detonate since a positive or high level signal is applied through switch 30 to one input of the NAND gate and a second positive or high level signal from the same battery or power supply is applied by way of the divider and 90 second time delay 34 to the other input of the NAND gate. If the trembler switch is not activated during this period of time, at the end of 12 hours, a positive or high level output signal appears at the output lead 22 of divider 16 and this is applied through the NAND gate to cause the detonator 46 to be activated and the mine to self-destruct at the end of 12 hours. An embodiment incorporating a 14-stage divider was constructed in accordance with the present invention and was tested and operated satisfactorily with a power consumption rate under 100 microwatts.

FIG. 4 is an overall block diagram of a modified timer constructed in accordance with the present invention and adapted to provide extremely long delay times and capable of operation in a moon environment such as on the lunar surface. Specifically, the timer of FIG. 4 is constructed to withstand the extremes of temperature on the lunar surface and to produce an output pulse one year after energization. In FIG. 4, like parts bear like reference numerals.

The timer generally indicated at 64 in FIG. 4 again comprises the low frequency oscillator 12 and the reset pulse generator 20 in all respects identical to the oscillator and reset pulse generator illustrated in FIG. 1. Again, these signal sources apply pulses by way of their respective output leads 14

and 18 to the divider 16' which is identical to the divider previously described in conjunction with FIG. 1 but which includes more counting stages. Specifically, divider 16' is provided with sufficient stages so that its last stage will not change state until after 8 days from initiation of timer operation.

In the same manner as previously described, after a period of 12 hours, an output pulse appears on 12 hour output lead 66 and this is applied to a pulse output device 68. Divider 16' is also provided with 8 day output lead 70, 4 day output lead 72, and 2 day output lead 74. These leads are all connected to the respective inputs of a 3-input logic NAND-gate 26' and its output at lead 38 passes through inverter 40 to a pulse shaper 76. From the pulse shaper a signal is fed to a magnetic core ring counter 78 which, at the end of one year, applies an output pulse to output device 80 by way of output lead 82.

FIG. 5 is a more detailed showing of the pulse shaper 76 of FIG. 4. The pulse shaper comprises a silicon controlled rectifier 84 having a gate 86 receiving the output from inverter 40. Connected in series across the power supply with the SCR 84 is a resistor 88 and capacitor 90 is connected across the SCR. Also in series with the silicon controlled rectifier are windings 92 and 94 of cores M1 and M2 respectively forming a part of the magnetic core ring counter 78.

FIG. 6 is a detailed showing of the magnetic core ring counter 78 of FIG. 4. The counter is of conventional construction and comprises an input lead 96 which receives a signal from the pulse shaper and applies to the windings 92 and 94 of the magnetic cores M1 and M2. The cores change state in a well known manner in accordance with the number of input pulses until an output is developed on leads 98 and 100 connected to the last core M and forming the output signal delayed for one year from the initiation of the timer. While a ring counter incorporating only 7 stages is illustrated, it is understood that in the preferred embodiment the magnetic core ring counter comprises stages A through M constituting thirteen in number.

With the long time counter 64 of FIG. 4 combining a magnetic core ring counter with a flip-flop counting stage or divider, the magnetic core counter acts to keep the power consumption to a lower level than that required by the addition of divider stages. In addition, the magnetic core ring counter 78 has the properties of a permanent memory characteristic such that when power is removed, the core remembers its last state.

Timer 64 is specifically designed to perform the following functions: (a) Operate in a lunar environment, such as on the lunar surface, (b) it will operate for 14 earth days during a lunar day, (c) it is turned "off" for 14 earth days during the lunar night (no power is available during this period), (d) it supplies an output pulse after one year, (e) it is automatically self-starting with energization of the battery or other power supply, (f) will operate under 1-milliampere current consumption with a 12-volt supply, and (g) supplies a pulse every 12 hours during the lunar day. All of this is provided in a physical package of small size and weight, namely, having a 1.25 inch diameter with an overall length of 2.25 inches.

As previously mentioned, the oscillator and reset circuits are the same as those previously described. Divider 16' is formed of three RCA integrated circuits CD4004. The logic triple gate NAND circuit 26' employs an RCA CD4004. Pulse shaper 76 comprises a silicon controlled rectifier and associated resistor and capacitor as shown in FIG. 5.

The 12 hour pulse is obtained in the same manner as described in conjunction with the embodiment of FIGS. 1-3. Triple NAND-gate 26' is used to obtain an output at the end of 14 days, which output pulse drives the magnetic core ring counter. That is, an output appears at output lead 68 when outputs simultaneously appear on leads 70, 72, and 74 at the end of 14 days from initiation, i.e., activation of the power supply or closure of a suitable start switch. When these three signals are present, a high level signal is fed to the gate of the silicon controlled rectifier in the pulse shaper. The load circuit of the pulse shaper is represented by the two cores M1 and M2 of the magnetic core ring counter. The ring counter has 13

cores in the memory circuit and the output is taken off of the last core M.

It is apparent from the above that the present invention provides an improved timer and particularly a timer construction which is of small size and weight, is very rugged to withstand severe temperature and other environmental conditions, and which gives an accurately timed output over relatively long periods of time. This is brought about by incorporating digital counting devices which require a minimum of energy for operation and which may be formed from integrated circuit components. In one embodiment, the timer is particularly adapted for use in causing an explosive charge, such as a land mine, to self-destruct after a predetermined period of time, and, in a second embodiment, the timer is adapted to produce an output pulse at the lunar surface after a period of as much as one year or more. By combining a divider formed of several stages of complementary MOS circuits with a magnetic core ring counter, long periods of time may be digitally measured with very low power consumption.

The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiments are therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

What is claimed and desired to be secured by United States Letters Patent is:

1. A timer comprising an integrated circuit oscillator operating at a frequency below 1 Hz, and an integrated circuit divider coupled to the output of said oscillator, said oscillator

and divider being formed of complementary MOSFET's whereby said timer requires a minimum of energy, a logic circuit coupled to the output of said divider, said logic circuit comprising a multiple input NAND gate, each input of said gate being coupled to a different stage of said divider, and a magnetic core ring counter coupled to the output of said gate.

2. A timer according to claim 1 including a pulse shaper coupling said NAND gate to said ring counter.

3. A timer according to claim 2 wherein said pulse shaper includes a silicon controlled rectifier.

4. A timer comprising an oscillator operating at a frequency below 1 Hz., a divider coupled to said oscillator to divide the oscillator output, a switch coupled to receive an output from said divider, and including a trembler switch coupled to the output of said divider.

5. A timer comprising an integrated circuit oscillator operating at a frequency below 1 Hz., an integrated circuit divider coupled to the output of said oscillator, said oscillator and divider being formed of complementary MOSFET's whereby said timer requires a minimum of energy, a logic circuit coupled to the output of said divider, said logic circuit comprising a 2-input NAND gate, the output of said divider being coupled to one gate input, and a time delay circuit coupled to the other input of said gate.

6. A timer according to claim 5 including a trembler switch coupled to said one gate input.

7. A timer according to claim 6 wherein said time delay circuit comprises an arming delay circuit for a land mine.

8. A timer according to claim 7 wherein said arming delay circuit comprises a resistor and a capacitor coupled between said other gate input and said divider.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,657,571 Dated April 18, 1972

Inventor(s) Vincent W. Martin and Bruce G. Steiner

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In Column 4, line 28, "applies" should read --applies it--;
line 61, "RCA CD4004" should read --RCA CD4007--.

Signed and sealed this 19th day of September 1972.

(SEAL)
Attest:

EDWARD M. FLETCHER, JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents

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