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(54) **ESD PROTECTION DEVICES**

ESD-SCHUTZEINRICHTUNGEN

DISPOSITIFS DE PROTECTION CONTRE LES DECHARGES ELECTROSTATIQUES

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Description

BACKGROUND OF THE INVENTION

[0001] The invention generally relates to electronic protection devices, and more particularly to electrostatic discharge (ESD) protection devices.

[0002] Integrated circuits are susceptible to a variety of reliability problems. One of these issues is the possible vulnerability to ESD events. ESD occurs when a charged object, e.g., a piece of equipment used to install integrated circuits into a printed circuit board, is brought into close proximity to a pin of an integrated circuit that is at a different potential compared to the charged object. The discharge consists, typically, of current levels exceeding an ampere during a time period less than 200 nanoseconds. The magnitude of the peak current and the waveshape of the discharge depend on the effective resistance, capacitance and inductance of the system and the amount of charge present before the discharge. The result of ESD on unprotected integrated circuits is often destruction characterized by melting and/or explosion of part of the circuit. It is common practice for the designer to include extra components in an integrated circuit that are intended to provide protection against ESD damage by providing paths for the ESD events that bypass the components used for the normal circuit functions and are not destroyed by the ESD events.

[0003] In BiCMOS integrated circuits, a frequently used circuit configuration is a differential pair 10 of bipolar transistors, as shown in Fig. 1. When this configuration is used as an input with the bases of the transistors connected to external bonding pads, it is very difficult to protect these transistors from ESD events.

[0004] US-A-4206418 describes a circuit including means for limiting the potential difference that can exist between corresponding electrodes of two input transistors interconnected to form a differential amplifier stage. The control electrode of each input transistor is coupled via a normally conducting gating transistor to its respective input terminal and via a normally non-conducting clamping transistor to a common point to which is connected one end (source or emitter) of the main conduction paths of the two input transistors. In response to an input signal at an input terminal having a polarity and a first value to turn off an input transistor, the gating transistor is turned off and decouples the control electrode of the input transistor from its corresponding input terminal. Then, as the input signal increases beyond the first value in a direction to further reverse bias the input transistor, the clamping transistor is turned on and clamps the control electrode of the input transistor to the common point. The circuit may also include means connected to the output (drain or collector) electrodes of the two input transistor to prevent excessive voltage differentials between their output electrodes.

[0005] WO92/07402 describes a circuit protection arrangement comprises a series switching circuit that is

intended to be connected in a line of the circuit and will switch to an open state when subjected to an over current, and a shunt switching circuit that is open under normal operating conditions but will shunt the over current across the load of the circuit or to ground when triggered by the series switching circuit. Preferably the series switching circuit comprises a switching transistor (4) that is controlled by a control transistor (6), and the shunt switching circuit comprises a shunt-switching transistor (9) that is controlled by a shunt control transistor (11), which is itself controlled by the series switching circuit. The shunt switching circuit may be connected to ground or it may be connected to a back-up load or voltage fold-back device such as a triac.

[0006] A typical ESD protection scheme is shown in Fig. 2. If pad A is stressed positive with respect to pad B, one of the likely paths for the ESD current is through a resistor R1, the forward biased base-emitter junction BE-1, the reverse biased base-emitter junction BE-2, and a resistor R2. In high frequency integrated circuits, transistors Q 1 and Q2 are small in area, significantly limiting the ability of the base-emitter junction to carry current in the forward direction before the internal power dissipation is sufficient to cause damage. The base-emitter junction is very weak in the reverse direction, with a typical breakdown voltage of 4 V or less. Resistors R1 and R2 are often low-valued resistors to improve performance. The result of this configuration is that it is very difficult to protect the differential pair against the effects of ESD events.

[0007] The ESD protection scheme shown in FIG. 2 is required to limit the voltage between points C and D to a safe value during a typical ESD event, where the discharge current may exceed 2 A. For high forward currents, the internal series resistance of the diode results in a larger forward drop (typically 2 to 3 V) than the typical low current diode drop (0.7 V). The preferred current path would be through diode D1, a power supply clamp 12, and diode D2. If it is assumed that the voltage drop across power supply clamp 12 is 5 V, and the voltage across each of the two diodes in forward bias under the ESD event is 3 V, then 11 V appears from pad A to pad B. Also, if it is assumed that the current through the reverse biased BE-2 is limited to 10 mA with a voltage drop of 4 V and that the voltage drop across the forward biased BE-1 is 0.6 V at 10 mA, then the voltage drop across resistor R1 plus resistor R2 must be 6.4 V at 10 mA. The result is that R1 and R2, which are equal, must be at least 320 k Ω to protect the device. For high performance, it may be necessary to limit R1 and R2 to less than 100 Ω each. Note that it may be necessary to limit the current through the reverse biased base-emitter junctions to 1 mA or less for very small devices. An alternative is to increase the physical size of the transistors, which degrades the performance, to improve ESD protection.

[0008] An alternative approach is to divert the current from the input pads A and B directly. One such approach is shown in FIG. 3, where anti-parallel diodes, D5 and D6, are connected between pads A and B. This approach

limits the voltage across the differential pair to one high current diode drop (approximately 3 V), if the same assumptions as in the above for FIG. 2 are used. Note that the other diodes are also necessary to provide protection for ESD stresses from the pads to the power supply and ground. The major difficulty with this approach is that the input signal is also diverted by the diode pair D5 and D6, limiting the input swing to approximately 0.6 V in either polarity. If the input swing is larger than this voltage, the anti-parallel diodes D5 and D6 are no longer a valid solution for ESD protection.

[0009] Therefore, there is a need for an effective ESD protection scheme that allows a larger swing of an input voltage.

SUMMARY OF THE INVENTION

[0010] The invention provides a way of protecting a differential pair of bipolar transistors by diverting the current into an n-channel MOSFET which is driven into conduction during an ESD event and allows a larger swing of input voltage than the anti-parallel diode pair. No extra processing steps are required and the MOSFET is driven on, rather than relying on the parasitic bipolar npn transistor triggering into snap-back as in the grounded gate n-MOS transistor that is commonly used for ESD protection in CMOS integrated circuits.

[0011] According to the present invention, an ESD protection circuit is provided for protecting a differential pair of transistors having two input terminals. The circuit comprises a switching element (such as an NMOS transistor) having first and second terminals and a control terminal; a first resistive element, coupled between the first and control terminals of the switching element; and a second resistive element, coupled between the second and control terminals of the switching element; wherein the first and second terminals of the switching element are for connecting, respectively, to input terminals of the differential pair.

[0012] According to one embodiment of the invention, the first and second resistive elements in the protection circuit are two resistors. The resistance values of the two resistors are preferably equal.

[0013] According to another embodiment of the invention, each of the first and second resistive elements in the protection circuit includes a parallel circuit. Each parallel circuit includes a pair of anti-parallel diodes.

[0014] According to a further embodiment of the invention, each parallel circuit in the protection circuit further includes two resistors each connected in series with one of the diodes of the parallel circuit. The resistance values of the two resistors in each parallel circuit are preferably equal.

[0015] Other objects and attainments together with a fuller understanding of the invention will become apparent and appreciated by referring to the following description and claims taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The invention is explained in further detail, and by way of example, with reference to the accompanying drawings wherein:

FIG. 1 shows a conventional differential pair of bipolar transistors;

FIG. 2 shows a typical conventional ESD protection scheme;

FIG. 3 shows an alternative conventional ESD protection scheme;

FIG. 4 shows an ESD protection circuit according to one embodiment of the invention;

FIG. 5 shows a variation of the ESD protection circuit in FIG. 4; and

FIG. 6 shows a variation of the ESD protection circuit in FIG. 5.

Throughout the drawings, the same reference numerals indicate similar or corresponding features or functions.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] FIG. 4 shows an ESD protection circuit 20 having a MOS transistor Q3 and resistors RC and RD. Transistor Q3 is placed with its source and drain directly in parallel with differential pair Q1 and Q2, between points C and D. In a preferred embodiment of the invention, transistor Q3 is a symmetrical NMOSFET designed using ESD rules (e.g., silicide is blocked on both sides of the gate to improve the reliability of the transistor under ESD stress). For a symmetrical protection, resistors RC and RD are equal in magnitude and large in value (typically 50k Ω to 100k Ω to limit the current through these resistors during normal operation. The time constant of the parallel combination of RC and RD and the gate to source capacitance of Q3 should typically be less than 1 nanosecond to assure that Q3 turns on fast enough to protect the bipolar transistors. The width of Q3 is determined by how much of the ESD event is to be absorbed in the structure, as discussed below. The length of Q3 may be the minimum value allowed in the process. The triggering voltage of the protection scheme using Q3 is determined by the threshold voltage, VT, of Q3 (typically 0.6 V). When the voltage from C to D reaches approximately twice the magnitude of VT in either polarity, Q3 will turn on to draw current. A voltage drop across resistors R1 and R2 will occur due to the current. The result will be that the pad voltage from A to B will continue to rise until the diode-clamp combination (D1, Clamp 12 and D4) becomes the primary current path, and the voltage across C to D remains clamped to approximately twice VT. The size of resistors R1 and R2 determines the current level that Q3 must be able to absorb during an ESD event. In general, the larger R1 and R2, the smaller the width required for Q3, and vice versa. For example, if R1 and R2 are 1 Ω ,

and clamp 12 requires 5 V to trigger, then the current through R1 and R2 (and Q3) must be approximately 3 A before some of the current will be diverted from Q3. If R1 and R2 are 10 Ω , current in excess of 300 mA will be diverted from Q3. If R1 and R2 are 100 Ω , current in excess of 30 mA will be diverted from Q3. The width of Q3 can be adjusted accordingly. Note that if R1 and R2 are zero, the entire ESD event will go through Q3. The input voltage swing during normal operation will have to be larger to accommodate larger values of R1 and R2, but the voltage swing between points C and D will remain the same (less than 1.2 V for the situation described above). Fig. 5 illustrates an ESD protection circuit 20, in which resistors RC and RD are replaced with two pairs of anti-parallel diodes. This will provide a similar performance as that in Fig. 4, with a voltage swing limit of approximately 1.4 V.

[0018] If the input voltage swing must exceed twice V_T , it is possible to skew the triggering voltage by adding extra resistors in series with the diodes as shown in another alternative ESD protection circuit 30 in Fig. 6. In this case $R_G/R_H = R_J/R_K$, but R_G is not equal to R_H . For symmetry, $R_G = R_J$ and $R_H = R_K$, but it is only necessary that the ratio be set properly.

[0019] The present invention may also be used in place of the diode D 1 between pad A and power supply and the diode D2 between pad A and ground, and in a similar manner, in place of diodes D3 and D4 connected to pad B. In that case, the entire ESD event must go through the MOSFET, so the width of the device would be similar to that of the grounded gate MOSFET currently used as the primary protection in many CMOS integrated circuits.

[0020] While the invention has been described in conjunction with specific embodiments, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art in light of the foregoing description.

Claims

1. An ESD protection circuit (20) for protecting a differential pair of transistors (Q1, Q2) having two input terminals (A,B), comprising:

- a switching element (Q3) having first and second terminals and a control terminal;
- a first resistive element (RC), coupled between the first and control terminals of the switching element; and
- a second resistive element (RD), coupled between the second and control terminals of the switching element; the first and second terminals of the switching element are for connecting, respectively, to input terminals of the differential pair; the ESD protection circuit being **characterized in that** each of the first and second resistive elements includes a pair of anti-parallel

diodes.

2. The circuit of claim 1, wherein the switching element is an NMOS transistor and the control terminal is its gate terminal.
3. The circuit of claim 1, wherein the first and second resistive elements are two resistors.
4. The circuit of claim 3, wherein the resistance values of the two resistors are equal.
5. The circuit of claim 1, wherein each of the first and second resistive elements includes two resistor (R_G , R_J , R_H , R_K), each connected in series with one of the diodes of the parallel circuit.
6. The circuit of claim 5, wherein the resistance values of the two resistors (R_G , R_J , R_H , R_K) in each parallel circuit are equal.
7. A circuit, comprising:
 - a differential pair of transistors (Q1, Q2) having two input terminals; and
 - an ESD protection circuit (20) as claimed in previous claims coupled between the two input terminals of the differential pair.

Patentansprüche

1. ESD-Schutzschaltung (20) zum Schützen eines Differential-Paares von Transistoren (Q1, Q2), das zwei Eingangsanschlüsse (A, B) aufweist,
 - mit einem Schaltelement (Q3), das erste und zweite Anschlüsse und einen Steueranschluss aufweist,
 - mit einem ersten Widerstandselement (RC), das zwischen dem ersten Anschluss und dem Steueranschluss des Schaltelementes geschaltet ist, und
 - mit einem zweiten Widerstandselement (RD), das zwischen dem zweiten Anschluss und dem Steueranschluss des Schaltelementes geschaltet ist,
 - wobei der erste und zweite Anschluss des Schaltelementes zum Verbinden mit entsprechenden Eingangsanschlüssen des Differential-Paares vorgesehen sind,

dadurch gekennzeichnet, dass in der ESD-Schutzschaltung jedes der ersten und zweiten Widerstandselemente ein Paar antiparallel geschalteter Dioden enthält.

2. Schaltung nach Anspruch 1, **dadurch gekennzeichnet,**

- zeichnet, dass** das Schaltelement ein NMOS-Transistor und der Steueranschluss sein Gate-Anschluss ist.
3. Schaltung nach Anspruch 1, **dadurch gekennzeichnet, dass** die ersten und zweiten Widerstandselemente zwei Widerstände sind.
4. Schaltung nach Anspruch 3, **dadurch gekennzeichnet, dass** die Widerstandswerte der beiden Widerstände gleich sind.
5. Schaltung nach Anspruch 1, **dadurch gekennzeichnet, dass** jedes der ersten und zweiten Widerstandselemente zwei Widerstände (RG, RJ, RH, RK) enthält, von denen jeder in Serie mit einer der Dioden der Parallelschaltung geschaltet ist.
6. Schaltung nach Anspruch 5, **dadurch gekennzeichnet, dass** die Widerstandswerte der beiden Widerstände (RG, RJ, RH, RK) in jeder Parallelschaltung gleich sind.
7. Schaltungsanordnung
- mit einem Differential-Paar von Transistoren (Q1, Q2), das zwei Eingangsanschlüsse aufweist, und
 - mit einer ESD-Schutzschaltung (20) nach den vorhergehenden Ansprüchen, die zwischen die beiden Eingangsanschlüsse des Differential-Paares geschaltet ist.
- Revendications**
1. Circuit de protection contre les ESD (20) pour la protection d'une paire différentielle de transistors (Q1, Q2) comprenant deux bornes d'entrée (A, B), comprenant :
- un élément de commutation (Q3) comprenant des première et deuxième bornes et une borne de commande ;
 - un premier élément résistant (RC), couplé entre la première borne et la borne de commande de l'élément de commutation; et
 - un deuxième élément résistant (RD), couplé entre la deuxième borne et la borne de commande de l'élément de commutation; les première et deuxième bornes de l'élément de commutation étant respectivement destinées à être connectées aux bornes d'entrée de la paire différentielle ; le circuit de protection contre les ESD étant **caractérisé en ce que** chacun des premier et deuxième éléments résistants comprend une paire de diodes montées tête-bêche.
2. Circuit selon la revendication 1, dans lequel l'élément de commutation est un transistor NMOS et la borne de commande est sa borne de grille.
3. Circuit selon la revendication 1, dans lequel les premier et deuxième éléments résistants sont deux résistances.
4. Circuit selon la revendication 3, dans lequel les valeurs ohmiques des deux résistances sont égales.
5. Circuit selon la revendication 1, dans lequel chacun des premier et deuxième éléments résistants comprend deux résistances (RG, RJ, RH, RK), chacune montée en série avec l'une des diodes du circuit en parallèle.
6. Circuit selon la revendication 5, dans lequel les valeurs ohmiques des deux résistances (RG, RJ, RH, RK) de chaque circuit en parallèle sont égales.
7. Circuit, comprenant :
- une paire différentielle de transistors (Q1, Q2) comprenant deux bornes d'entrée ; et
 - un circuit de protection contre les ESD (20) selon les revendications précédentes, couplé entre les deux bornes d'entrée de la paire différentielle.

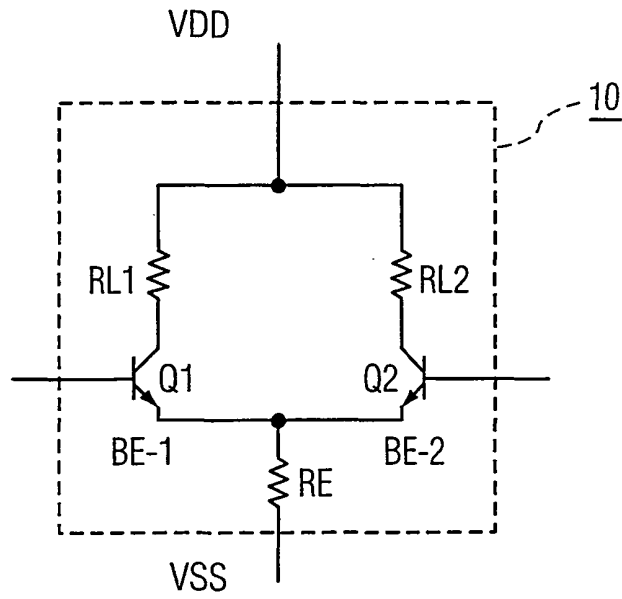


FIG. 1
PRIOR ART

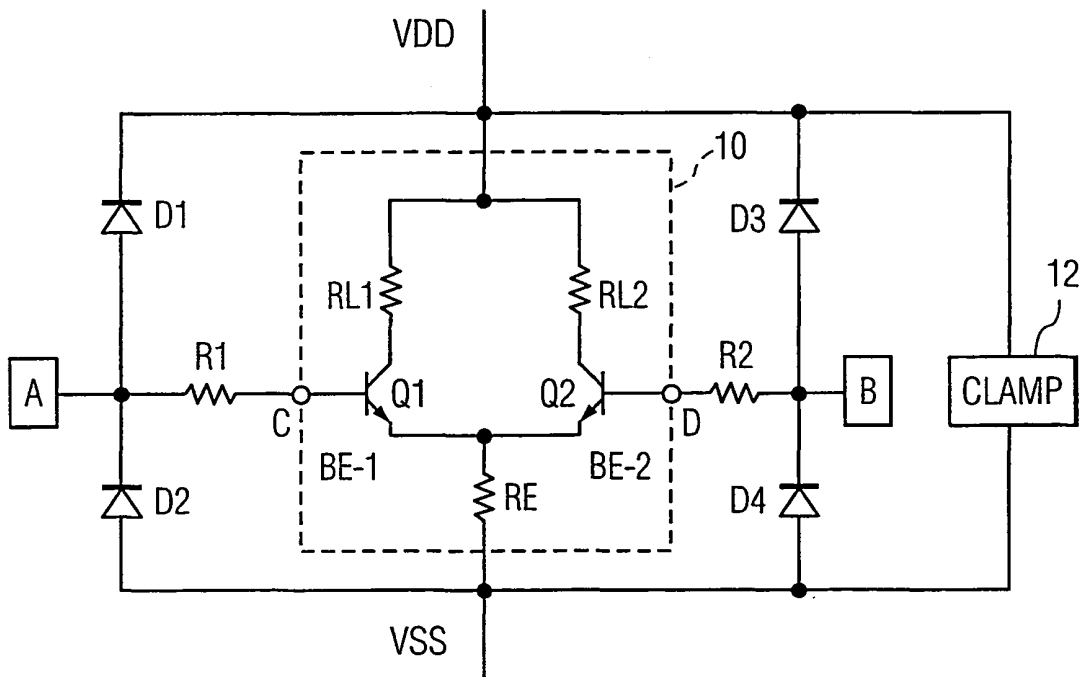
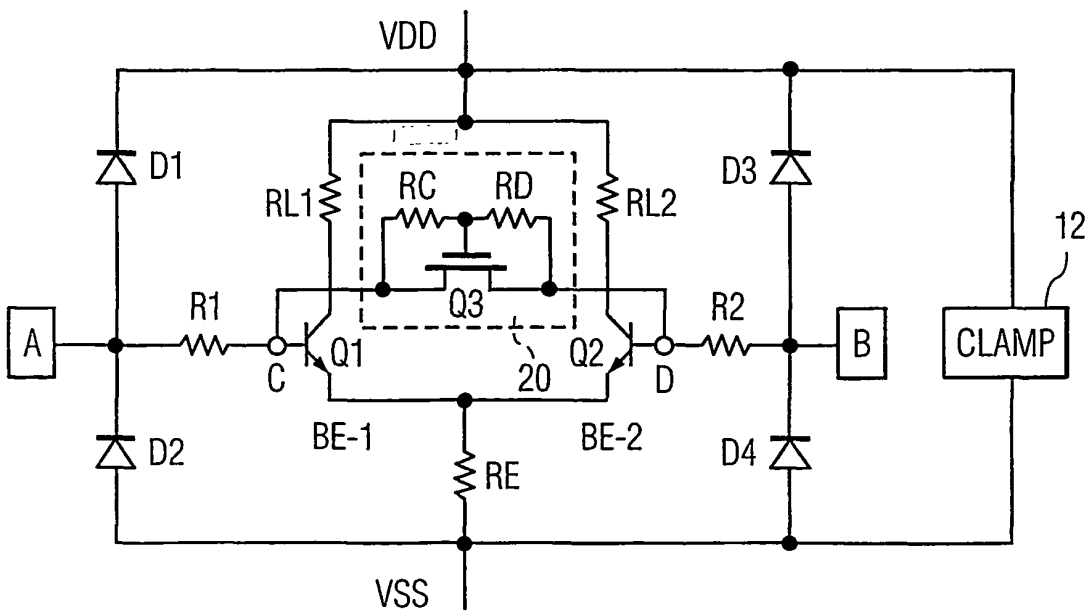
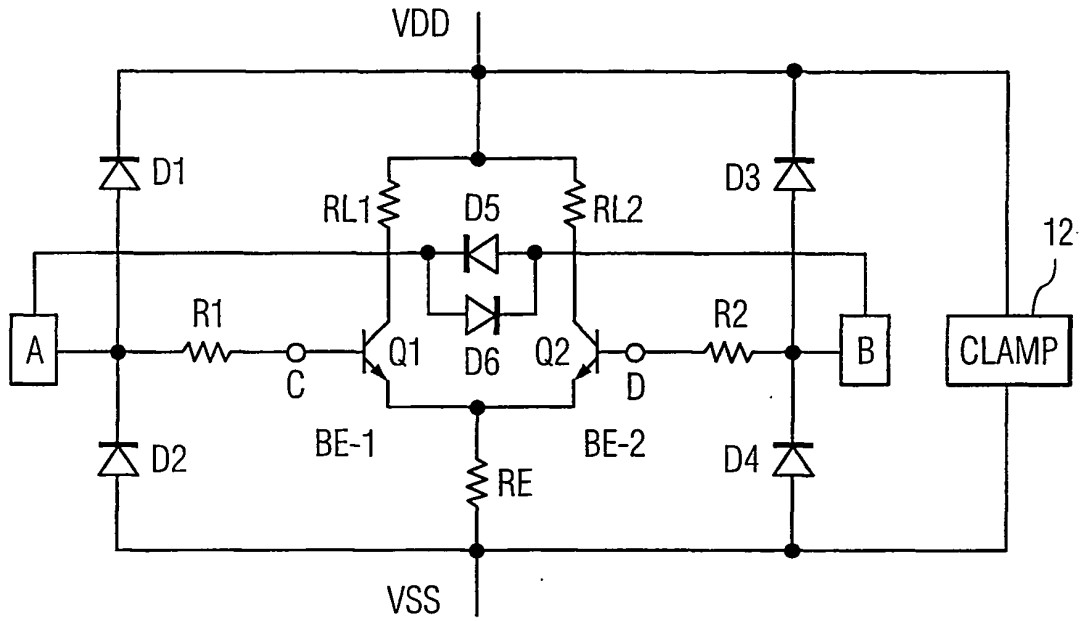


FIG. 2
PRIOR ART



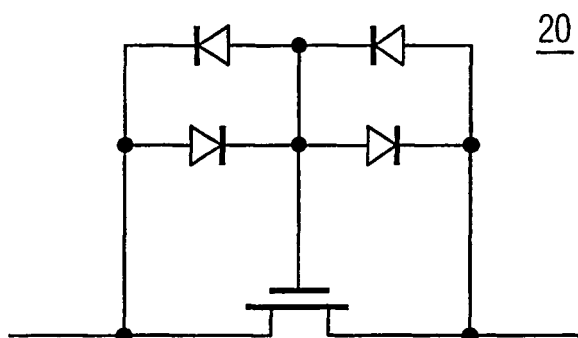


FIG. 5

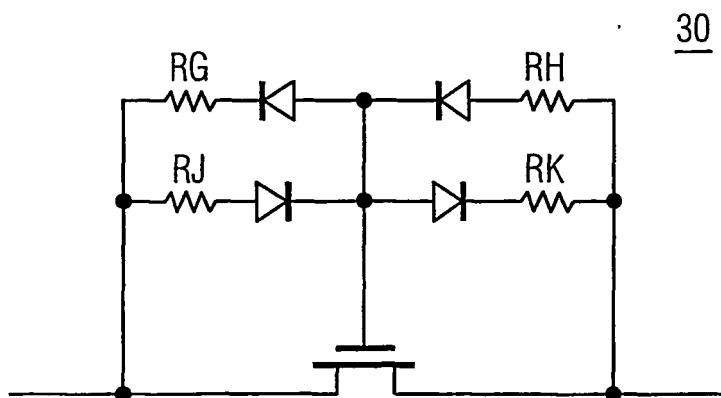


FIG. 6

REFERENCES CITED IN THE DESCRIPTION

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