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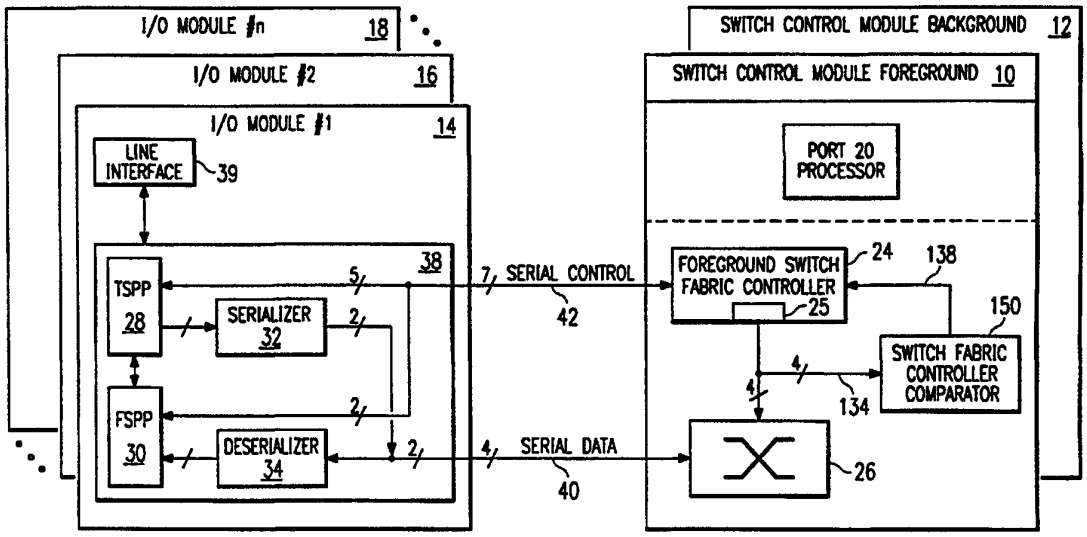

(57) Abstract

A switch fabric controller comparator system (200) is provided for comparing the contents of a foreground port mapping memory (25) and a background port mapping memory (125). The switch fabric controller comparator system (200) includes the foreground port mapping memory (25), the background port mapping memory (125), and a switch fabric controller comparator (150). Routinely, the switch fabric controller comparator (150) compares the contents of the foreground port mapping memory (25) and the background port mapping memory (125) to determine if any discrepancy exists between the two memories as to which input ports are mapped to which output ports. If a discrepancy or error is found, an error signal is generated by the switch fabric controller comparator (150). The foreground switch fabric controller (24) may log the error signal and enable another signal in response.

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SWITCH FABRIC CONTROLLER COMPARATOR SYSTEM AND METHOD

RELATED APPLICATIONS

This application claims benefit of U.S. Provisional Application Serial No. 60/001,498, filed July 19, 1995.

TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to communication switching systems, and more specifically to a switch fabric controller comparator system and method.

BACKGROUND OF THE INVENTION

Usage and demand for modern communication systems continues to soar as users demand more and more sophisticated communication services and bandwidth while relying on the instant availability of these communication systems. Users are demanding that communication systems provide almost instant access to all types of information including voice, video, and data.

Modern communication systems include a collection of components, such as digital switching systems, that communicate, manipulate, and process information in a variety of ways. Digital switching systems are integral components of today's modern communication systems. The availability of communication systems is directly related to the availability of the digital switching systems used in these communication systems. As reliance and the importance of communication systems continues to increase, the availability of the digital switching systems used in these communication systems becomes critically important.

Problems arise when attempting to increase the availability of a digital switching system. The digital switching system may provide redundant capability so that if a circuit or module of the digital switching system fails, a backup circuit or module may be used. Problems arise when transitioning from a system or circuit operating in the foreground to a system or circuit operating in the background or in hot-standby. Performance suffers greatly when the transition causes delays, interruptions in service, and errors. Delays, interruptions in service, and errors often occur because the backup circuit or module is not properly initialized. It is also critical that a hot-standby circuit or module can be relied upon to operate correctly if needed. Overall system performance suffers

when system resources are consumed when attempting to verify that a backup circuit or module is operating correctly so that the backup circuit or module may be relied upon in the event of a failure.

SUMMARY OF THE INVENTION

In accordance with the present invention, a switch fabric controller comparator system and method are provided which substantially eliminate or reduce the disadvantages and problems associated with increasing the availability and reliability of the switch fabric of a digital switching system. The present invention verifies that a foreground and a background switch fabric controller are identically mapping the input ports to the output ports of a switch fabric while minimizing or eliminating any adverse effects on actual switching operation.

According to an embodiment of the present invention, a switch fabric controller comparator system is provided that includes a foreground port mapping memory, a background port mapping memory and a switch fabric controller comparator. The foreground port mapping memory stores foreground port mapping data identifying the mapping of an input port of a foreground switch fabric to an output port of the foreground switch fabric, and the background port mapping memory stores background port mapping data identifying the mapping of an input port of a background switch fabric to an output port of the background switch fabric. The switch fabric controller comparator compares the foreground port mapping data to the background port mapping data for every output port.

The switch fabric controller comparator system and method provide various technical advantages. A technical advantage of the present invention includes increased switch availability. Another technical advantage includes the ability to systematically and routinely verify the operation of a background switch fabric controller during actual switch operation to ensure that the background switch fabric controller is operating identically to the

foreground switch fabric controller while minimizing or eliminating any adverse effect on overall switch performance. Other technical advantages are readily apparent to one skilled in the art from the following figures, descriptions, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following brief description, taken in connection with the accompanying drawings and detailed description, wherein like reference numerals represent like parts, in which:

FIGURE 1 is an overview block diagram illustrating a control and a data interconnection between a first I/O module and a foreground switch control module and a background switch control module;

FIGURE 2 is a block diagram illustrating a switch fabric controller comparator and the data interconnection between the first I/O module and the foreground switch control module and the background switch control module;

FIGURE 3 is a block diagram illustrating a switch fabric controller comparator system including the switch fabric controller comparator; and

FIGURE 4 is a flowchart illustrating a method for operating the switch fabric controller comparator system.

DETAILED DESCRIPTION OF THE INVENTION

FIGURE 1 is an overview block diagram illustrating a control and a data interconnection between a first I/O module 14, a foreground switch control module 10, and a background switch control module 12 all used in a digital communication switch. Also shown in FIGURE 1 are a plurality of additional I/O modules represented by a second I/O module 16 and an n^{th} I/O module 18. Each of the plurality of I/O modules interconnect with foreground switch control module 10 in the same manner that first I/O module 14 couples to foreground switch control module 10. Background switch control module 12 also interconnects to each of the plurality of I/O modules in the same manner that foreground switch control module 10 interconnects to each of these plurality of I/O modules. Background switch control module 12 operates in the background and serves as a redundant module in the event that foreground switch control module 10 fails or is taken out of service.

In operation, the plurality of I/O modules receive information, such as voice, video, and data, from a corresponding communications link using a variety of access technologies. Each I/O module provide this information to the inputs of a foreground switch fabric 26 of foreground switch control module 10 and background switch control module 12. Foreground switch control module 10, using a foreground switch fabric controller 24 and any available switching scheme, controls the switching of foreground switch fabric 26 so that the communication information provided by each I/O module is properly routed or mapped to the appropriate destination I/O module. Foreground switch control module 10 receives control information from the various I/O modules to assist with carrying out the switching scheme.

First I/O module 14 is representative of the plurality of I/O modules and includes a line interface 39 and a cell flow processor 38. In one embodiment, line interface 39 includes a connectivity engine, a network interworking, and a physical interface to exchange information with a particular type of access technology provided by the communication link or network that is coupled to line interface 39. This coupling is not shown in FIGURE 1.

Each of the plurality of I/O modules occupies a particular port in the digital communication switch. Each of the plurality of I/O modules are similar, except for the line interface which allows a particular I/O module to interface with a particular access technology. The access technology may include virtually any communications format or protocol such as asynchronous transfer mode (ATM), cell relay, frame relay, circuit emulation, LAN emulation, internetworking, and the like, and using virtually any physical medium or transmission hierarchy. Line interface 39 may support any suitable communication technique, whether connection-based or connection less. Thus, first I/O module 14 may interface, through line interface 39, with a communication link that supports a particular access technology, while the line interfaces of other I/O modules may support different access technologies. In this manner, information may be received by an I/O module in a particular format, converted to a common or core cell format used in foreground switch control module 10 by the line interface, routed to a destination I/O module through foreground switch control module 10, and finally provided to the communication link coupled to the destination I/O module that uses a completely different access technology than the source communication link.

Cell flow processor 38 provides an interface between line interface 39 and foreground switch control module 10. Cell flow processor 38 interconnects with foreground switch control module 10 using a first I/O serial data signal 40 and a first I/O serial control signal 42. In one embodiment, these may be provided as eleven unidirectional lines. The reference to "lines" may include conductors, couplings, connectors, matings, connections, and the like. Cell flow processor 38 also provides these same signals to background switch control module 12 through similar interconnections. Unlike line interface 39, which may vary from one I/O module to another, cell flow processor 38 has the same structure and performs the same function in all I/O modules. In a particular embodiment, cell flow processor 38 implements a core cell transfer function using ATM with virtual channel (VC) buffer and bandwidth control.

Cell flow processor 38 includes a to-switch port processor (TSPP) 28, a from-switch port processor (FSPP) 30, a serializer 32, and a deserializer 34. In a particular implementation, TSPP 28 and FSPP 30 may be implemented using an application specific integrated circuit (ASIC). Cell flow processor 38 uses TSPP 28 to receive information from line interface 39, to process the information, to provide communication signals to and from foreground switch control module 10, which exchange control information with foreground switch control module 10. TSPP 28 controls access to input buffers and to the bandwidth of foreground switch fabric controller 24 on a per connection basis. TSPP 28 requests and receives grants for switch bandwidth from foreground switch fabric controller 24. TSPP 28 also receives flow control information. FSPP 30 may also be an ASIC. The FSPP 30 controls access to output

buffers and linked bandwidth on a per connection basis. FSPP 30 also sends and receives flow control information.

Serializer 32 receives the information from TSPP 28 in parallel format and converts the information to serial format and provides the information as either first I/O serial data signal 40. TSPP 28 may also receive control information from foreground switch fabric controller 24. FSPP 30 receives information from foreground switch control module 10 through first I/O serial data signal 40 and first I/O serial control signal 42. Deserializer 34 receives these data signals where they are converted from serial format to parallel format and then provided to FSPP 30. TSPP 28 and FSPP 30 are in communication with one another.

In one embodiment, foreground switch control module 10 and background switch control module 12 are essentially interchangeable modules with one operating in the foreground and the other operating in the background to provide a redundant system to increase overall system availability. Thus, the following discussion of foreground switch control module 10 may apply equally as well to background switch control module 12.

Foreground switch control module 10 includes a port processor 20, a foreground switch fabric controller 24, a foreground switch fabric 26 having input ports and output ports corresponding to each of the plurality of I/O modules, and a switch fabric controller comparator 150. Port processor 20 is used to communicate with the TSPPs 28 and FSPPs 30 on the I/O modules in the system.

Foreground switch fabric controller 24 controls the operation of foreground switch fabric 26 by determining how the data signals provided from the plurality of I/O modules, such as first I/O serial data signal 40, are interconnected (switched) by foreground switch fabric 26.

Foreground switch fabric controller 24 accumulates and arbitrates transfer requests from each I/O module. Foreground switch fabric controller 24 may also maintain and access a topology state for each connection. This topology information controls the fan-in and the fan-out of multipoint connections. In one embodiment, foreground switch fabric controller 24 may include a bandwidth arbiter (BA) ASIC to decide which I/O modules or ports have access to foreground switch fabric 26, and a multipoint topology controller (MTC) ASIC to maintain and access topology states for each connection in the digital communication switch. Foreground switch fabric controller 24 receives control signals from each of the I/O modules, such as first I/O serial control signal 42 from first I/O module 14. Foreground switch fabric controller 24 uses this information in its switching scheme to determine which data signal from all of the I/O modules should be provided at a particular input of foreground switch fabric 26 and routed to a particular output of foreground switch fabric 26.

Once foreground switch fabric controller 24 determines which connection should be made within foreground switch fabric 26, a control signal is provided to the TSPP of the appropriate I/O module so that the correct data signal may be provided to the input port of foreground switch fabric 26 corresponding to that I/O module. For example, first I/O module 14, through TSPP 28, provides first I/O serial control signal 42 to foreground switch fabric controller 24 indicating a request for communication from first I/O module 14. Eventually, foreground switch fabric controller 24 grants the request and communicates the grant to TSPP 28 through first I/O serial control signal 42. At this time, the cell may be transferred from TSPP 28 through

first I/O serial data signal 40 to foreground switch fabric 26.

Foreground switch fabric 26, under the control of foreground switch fabric controller 24, maps or switches first I/O serial data signal 40 to the designated output port for receipt by the FSPP of the receiving I/O module. The data signals provided from the various I/O modules, such as first I/O serial data signal 40, may be provided as communication cells having a header portion and a data portion. These communication cells may be provided in asynchronous transfer mode (ATM) format, or the like. The information may then be processed by the line interface of the receiving I/O module and provided in the communication format of the interfacing access technology.

Switch fabric controller comparator 150, described more fully below and shown in FIGURE 3, receives a foreground port mapping signal 134 from foreground switch fabric controller 24, and a background port mapping signal 136 from a background switch fabric controller 124, not shown in FIGURE 1. Each of these signals are provided from a port mapping memory, such as foreground port mapping memory 25 of foreground switch fabric controller 24. Foreground port mapping signal 134 is the same control signal used to control foreground switch fabric 26 and may be a four bit signal. Background port mapping signal 136 is the same control signal used in background switch control module 12.

Switch fabric controller comparator 150 compares foreground port mapping signal 134 and background port mapping signal 136 to see if foreground switch fabric controller 24 and background switch fabric controller 124, not shown in FIGURE 1, are generating the same switching signals. As a result of this comparison, switch fabric controller comparator 150 generates a port error

signal 138. Port error signal 138 may be provided to a port error table provided in a memory. For example, foreground switch fabric controller 24 may implement a port error table in memory and receive port error signal 138. Foreground switch fabric controller 24 may perform other actions as a result of the status of the port error table.

Background switch control module 12 receives the same signals from the I/O modules, such as I/O first module 14, that are provided to foreground switch control module 10. Background switch control module 12 operates in the same manner as foreground switch control module 10. In the event that foreground switch control module 10 fails or is taken out of service, background switch control module 12 may operate in the foreground with minimal disruption of service. In one embodiment, port processor 20 switches between foreground control module 10 to background control module 12 in response to external control. However, before taking foreground switch control module 10 out of service or before foreground switch control module 10 fails, it is important to ensure that background switch control module 12 is operating correctly so that service will not be disrupted.

FIGURE 2 is a block diagram illustrating switch fabric controller comparator 150 and the data interconnection between the first I/O module 14, the foreground switch control module 10, and the background switch control module 12. FIGURE 2 illustrates a switch fabric controller comparator 150 for both the foreground switch fabric 26 and background switch fabric 126. The operation of both comparators 150 is the same. As discussed above, when first I/O module 14 provides information to foreground switch control module 10, the information is correspondingly also provided to background switch control

module 12. Background switch control module 12 includes the same or similar components as that provided in foreground switch control module 10. These same or similar components may include a background switch fabric controller 124, and a background switch fabric 126 as shown in FIGURE 2. Before both foreground switch control module 10 and background switch control module 12 may both receive the same information, background switch fabric controller 124 and foreground switch fabric controller 24 must be synchronized so that these controllers stay in lock-step. This may include identically configuring control registers, and updating tables and entries. When a communication cell is provided from TSPP 28, it is provided to serializer 32 in parallel format and converted to serial format and provided to processor interface 36. In one embodiment, processor interface 36 then provides the communication cell to background switch fabric 126 through a background first I/O serial data signal 41. This same communication cell is also provided to foreground switch fabric 26 through first I/O serial data signal 40. At this time, both background switch fabric 126 and foreground switch fabric 26, under the control of their respective switch fabric controllers and utilizing the same switching scheme, map or switch the communication cell to a designated output port where the cell may then be provided to that port's I/O module for further processing. In normal operation, first I/O serial data signal 40, as provided at the output of foreground switch fabric 26, is a communication cell that is provided to the designated I/O module. However, if foreground switch control module 10 fails or is taken out of service, then background first I/O serial data signal 41, as provided at the output of background switch fabric 126, may be provided to the designated I/O module.

It is critical that the components of background switch control module 12 are operating correctly so that in the event of a failure, background switch control module 12 may be relied upon for continued operation with minimal interruption of service. Thus, it is desirous to routinely verify the operation of background switch control module 12 to ensure that it is operating correctly while minimizing or eliminating any adverse effect on overall system performance caused by the verification of the background operation. The present invention accomplishes all of this as discussed above and as illustrated below.

This is accomplished using switch fabric controller comparator 150. Switch fabric controller comparator 150 is used to compare foreground port mapping signal 134 and background port mapping signal 136, to determine if foreground switch fabric controller 24 and background switch fabric controller 124 are generating the same mapping or switching signals. As a result of this comparison, switch fabric controller comparator 150 generates port error signal 138. In one implementation port error signal 138 is provided to foreground switch fabric controller 24 which implements a port error table in memory. Foreground switch fabric controller 24 receives port error signal 138 and stores the result in the port error table. Foreground switch fabric controller 24 may enable other signals when the port error table indicates that a predefined number of errors have occurred.

FIGURE 3 is a block diagram illustrating a switch fabric controller comparator system 200 that includes switch fabric controller comparator 150 coupled to foreground port mapping memory 25 and background port mapping memory 125. As shown in FIGURE 2, foreground port mapping memory 25 may be implemented in one embodiment as

a memory area included in foreground switch fabric controller 24 while background port mapping memory 125 may be included as a memory area in background switch fabric controller 124. However, foreground port mapping memory 25 and background port mapping memory 125 may be implemented independently from their corresponding switch fabric controller.

Switch fabric controller comparator system 200 uses switch fabric controller comparator 150 to compare the contents of foreground port mapping memory 25 and background port mapping memory 125 to determine if a discrepancy or difference exists. If a discrepancy or difference exists, this indicates, generally, that either foreground switch control module 10 or background switch control module 12 are not operating properly.

Foreground port mapping memory 25 and background port mapping memory 125 each contain the input port mappings to each output port of their respective switch fabric. Referring now to foreground port mapping memory 25, in one implementation, the underlying foreground switch fabric 26 contains n output ports and n input ports. The input port mapping for each output port is shown in the column entitled "Input Ports." For example, foreground port mapping memory element 130 corresponds to foreground output port 3 and indicates that foreground input port B has been mapped to foreground output port 3. Background port mapping memory 125 is structured in the same manner and operates in the same manner as just described for foreground port mapping memory 25. For example, background port mapping memory element 132 corresponds to background output port 3 and indicates that background input port D has been mapped to output port 3. A comparison of foreground port mapping memory element 130 of foreground

port mapping memory 25 to background port mapping memory element 132 of background port mapping memory 125 indicates that foreground port mapping 25 and background port mapping memory 125 do not correspond identically at output port 3.

Switch fabric controller comparator 150 compares each memory element to determine if the data provided in foreground port mapping memory 25 and background port mapping memory 125 contain equivalent input port mappings for each output port. This may be accomplished using a foreground port mapping signal 134 which provides the contents of foreground port mapping memory 25 on an output-port by output-port basis. Foreground port mapping signal 134 is compared to a background port mapping signal 136 to determine if discrepancies exist. Background port mapping signal 136 is identical to foreground port mapping signal 134 except that it provides the contents of background port mapping memory 125.

Switch fabric controller comparator 150 may include any of a variety of known circuitry such as digital logical circuitry, comparator circuitry, microprocessor circuitry, and the like. For example, a series of digital logic gates, such as AND gates, may be provided in switch fabric controller comparator 150 so that all of the output ports may be compared at one time. The resulting error signal would be a digital signal that indicates which output ports are not identically mapped.

Switch fabric controller comparator 150 provides a port error signal 138 as a result of the comparisons performed on foreground port mapping signal 134 and background port mapping signal 136. Port error signal 138 may be provided to any memory element such as a port error memory. The port error memory may include a port error table that logs or records each time, on an output-port by

output-port basis, that foreground port mapping signal 134 differed from background port mapping signal 136. The port error memory may be provided in foreground switch fabric controller 24. If a particular element of the port error table reaches a predefined value, a signal may be enabled indicating that a particular action should be taken. For example, an alarm may be enabled as a result.

FIGURE 4 is a flow chart illustrating a method for operating switch fabric controller comparator system 200. The method starts at step 300 and proceeds to step 302 where the foreground switch fabric controller is synchronized to the background switch fabric controller. This may involve any number of steps to insure that the foreground switch fabric controller and the background fabric controller are receiving the identical signals after being provided in an identical state.

The method proceeds next to step 304 where the foreground port mapping memory is compared to the background port mapping memory. The foreground port mapping memory includes foreground port mapping data and the background port mapping memory includes background port mapping data indicating for each output port which input port is mapped to that output port, for a foreground switch fabric and a background switch fabric respectively. Foreground port mapping memory includes the foreground port mapping data for the foreground switch fabric, such as an n x n cross-point switch fabric. Similarly, the background port mapping memory includes the background port mapping data for the background switch fabric. Step 304 involves comparing each output port memory location of the foreground port mapping memory to the corresponding output port memory location of the background port mapping memory

to insure that the input ports mapped to these output ports are the same.

The method proceeds next to step 306 where an error signal is generated if the contents of the foreground port mapping memory and the background port mapping memory differ. For example, the foreground port mapping memory may indicate that input port A is mapped to output port 2 of the foreground switch fabric, while the background port mapping memory may indicate that input port C is mapped to output port 2 of the background switch fabric. In such a case, an error signal will be generated indicating that the foreground switch fabric controller and the background switch fabric controller differ in their switch port mappings.

Proceeding next to step 308, as a result of the error signal being generated, a particular action may be taken if the error signal reaches a predefined state. For example, after a predefined number of errors have been detected, a foreground switch fabric controller may enable a signal indicating that a problem exists between the operation of the foreground switch fabric controller and the background switch fabric controller. The method then concludes at step 310.

Thus, it is apparent that there has been provided, in accordance with the present invention, a switch fabric controller comparator system and method that satisfies the advantages set forth above. The present invention improves overall system availability while eliminating or minimizing any adverse effect on overall system operation. Although the preferred embodiment of the present invention has been described in detail, it should be understood that various changes, substitutions, and alterations may be made to the described embodiment without departing from the spirit and

scope of the present invention. The direct connections illustrated herein could be altered by one skilled in the art such that two devices are merely coupled to one another through an intermediate device or devices without being directly connected while still achieving the desired results demonstrated by the present invention. Other examples of changes, substitutions, and alterations are readily ascertainable by one skilled in the art and could be made without departing from the spirit and scope of the present invention as defined by the following claims.

WHAT IS CLAIMED IS:

1. A switch fabric controller comparator system comprising:

a foreground port mapping memory including foreground port mapping data identifying the mapping of an input port of a foreground switch fabric to an output port of the foreground switch fabric;

a background port mapping memory including background port mapping data identifying the mapping of an input port of a background switch fabric to an output port of the background switch fabric; and

a switch fabric controller comparator operable to compare the foreground port mapping data to the background port mapping data for every output port.

2. The switch fabric controller comparator system of Claim 1, wherein the switch fabric controller comparator is operable to generate an error signal if the foreground port data does not correspond to the background port mapping data for every output port.

3. The switch fabric controller comparator system of Claim 2, further comprising:

a port error memory operable to receive the error signal and to store the error signal.

4. The switch fabric controller comparator system of Claim 3, wherein the port error memory is included in a foreground switch fabric controller.

5. The switch fabric controller comparator system of Claim 4, wherein a signal is enabled by the foreground switch fabric controller when the contents of the port error memory are in a predefined state.

6. The switch fabric controller comparator system of Claim 1, wherein the switch fabric controller comparator performs a comparison of all output ports each clock cycle.

7. The switch fabric controller comparator system of Claim 1, wherein the switch fabric controller comparator includes digital logic circuitry to perform comparisons.

8. The switch fabric controller comparator system of Claim 7, wherein the digital logic circuity includes an AND gate.

9. The switch fabric controller comparator system of Claim 1, wherein the foreground switch fabric and the background switch fabric receive communication cells.

10. The switch fabric controller comparator system of Claim 9 wherein the communication cells include a header portion and a data portion.

11. The switch fabric controller comparator system of Claim 10 wherein the communication cells are asynchronous transfer mode formatted cells.

12. A method for operating a switch fabric controller comparator system, the method comprising the steps of:

synchronizing the operation of a foreground switch fabric controller and a background switch fabric controller;

comparing a foreground port mapping memory to a background port mapping memory after synchronizing; and

generating an error signal if the contents of the foreground port mapping memory differ from the background port mapping memory.

13. The method of Claim 12, wherein the foreground switch fabric controller is a foreground bandwidth arbiter, and the background switch fabric controller is a background bandwidth arbiter.

14. The method of Claim 12, further comprising the steps of:

generating a foreground port mapping data scheme and storing the foreground port mapping data scheme in the foreground port mapping memory, and generating a background port mapping data scheme and storing the background port mapping data scheme in the background port mapping memory all before the comparing a foreground port mapping memory to a background port mapping memory step.

15. The method of Claim 12, further comprising the step of:

storing the error signal in port error memory.

16. The method of Claim 15, wherein the port error signal is provided in a switch fabric controller.

17. The method of Claim 15, further comprising the step of:

enabling a signal if the contents of the port error memory reaches a predefined level.

FIG. 1

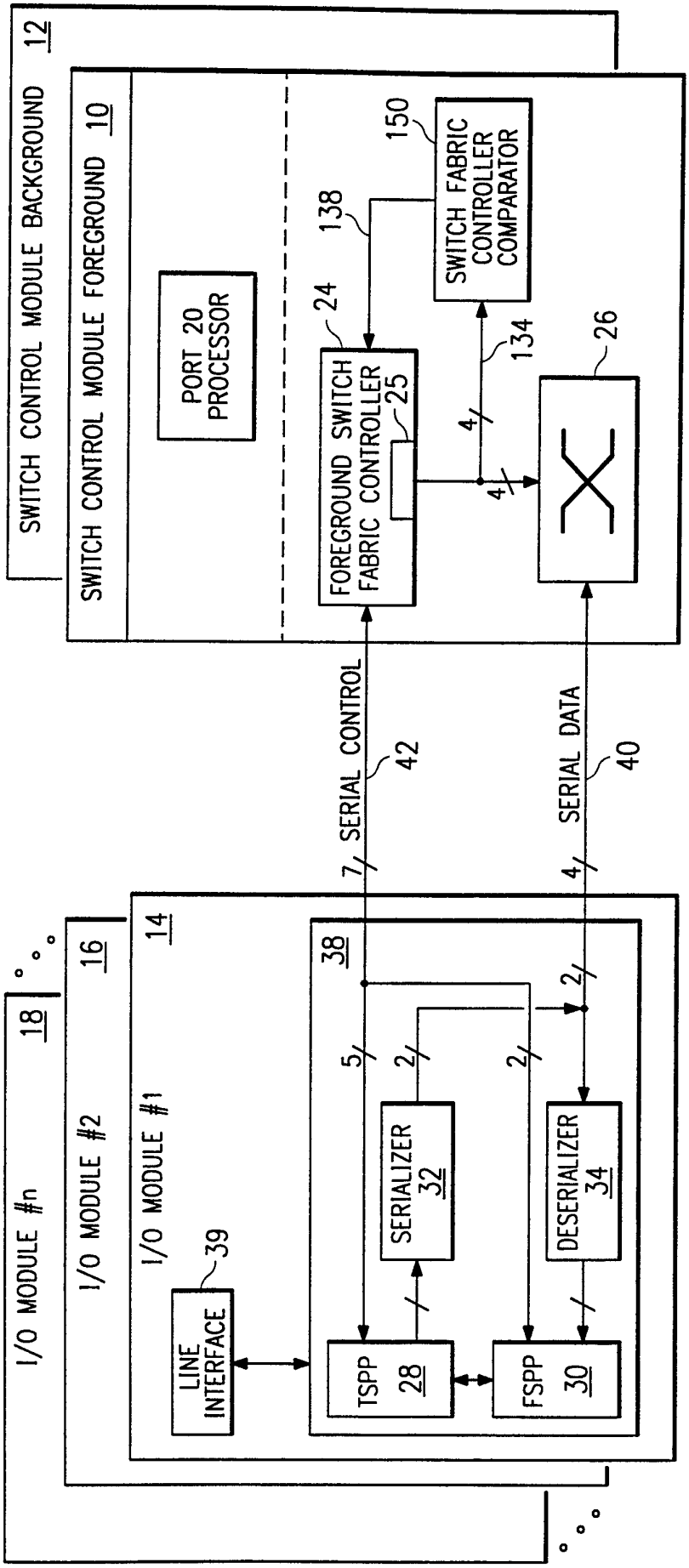

SWITCH CONTROL MODULE BACKGROUND 12
SWITCH CONTROL MODULE FOREGROUND 10
PORT 20 PROCESSOR
FOREGROUND SWITCH FABRIC CONTROLLER 25
24
138
SWITCH FABRIC CONTROLLER COMPARATOR
150
134
26
4
4
7 SERIAL CONTROL
42
4 SERIAL DATA
40
I/O MODULE #n 18
I/O MODULE #2 16
I/O MODULE #1 14
38
5
2
2
2
SERIALIZER 32
DESERIALIZER 34
LINE INTERFACE
39
TSPP 28
FSPP 30

FIG. 2

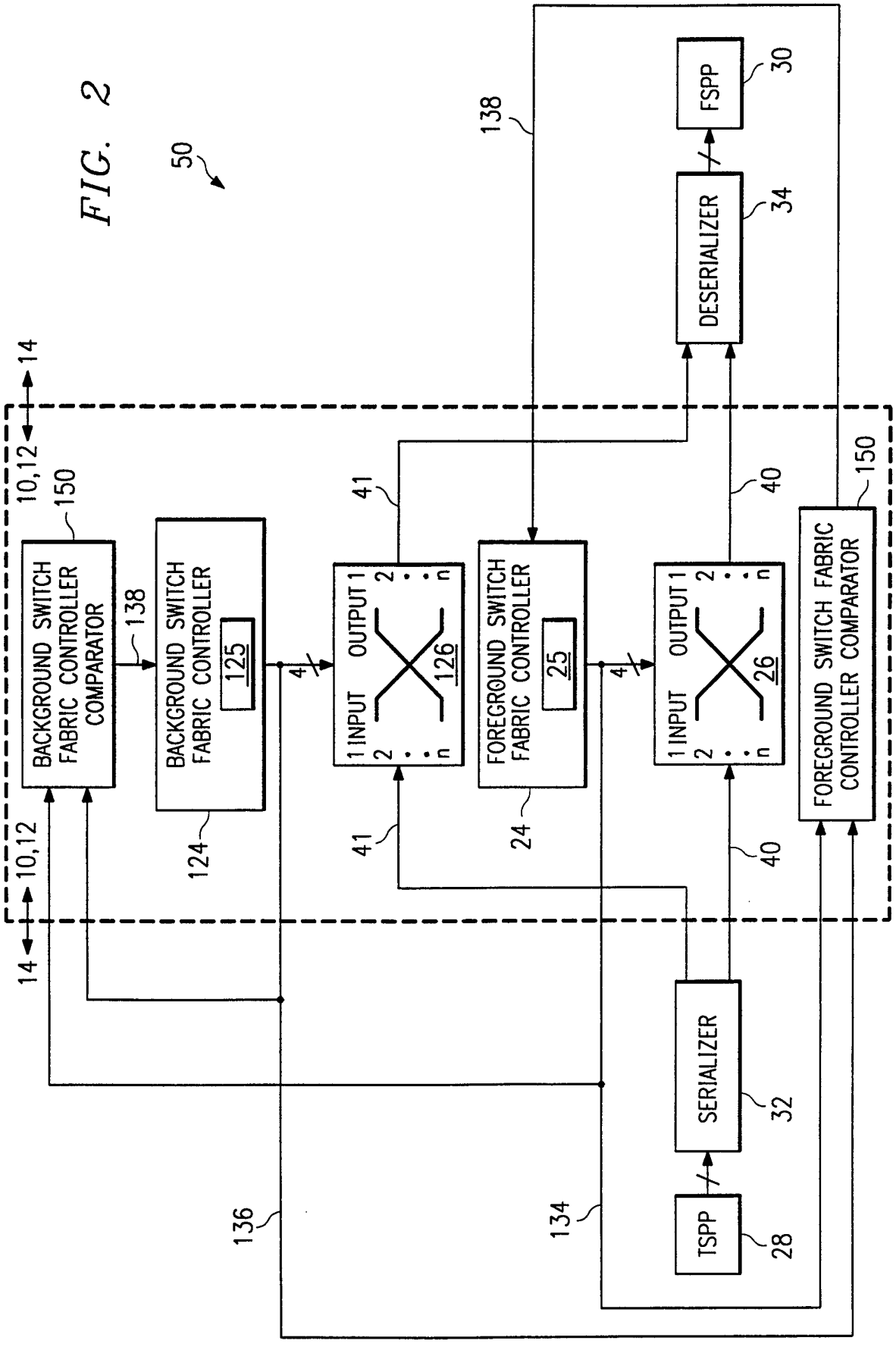

50
14
10,12
150
BACKGROUND SWITCH FABRIC CONTROLLER COMPARATOR
138
BACKGROUND SWITCH FABRIC CONTROLLER
125
124
4
1 INPUT OUTPUT 1
2
n
126
41
FOREGROUND SWITCH FABRIC CONTROLLER
25
24
26
40
FOREGROUND SWITCH FABRIC CONTROLLER COMPARATOR
DESERIALIZER
34
FSPP
30
SERIALIZER
32
TSPP
28
136
134

FIG. 3

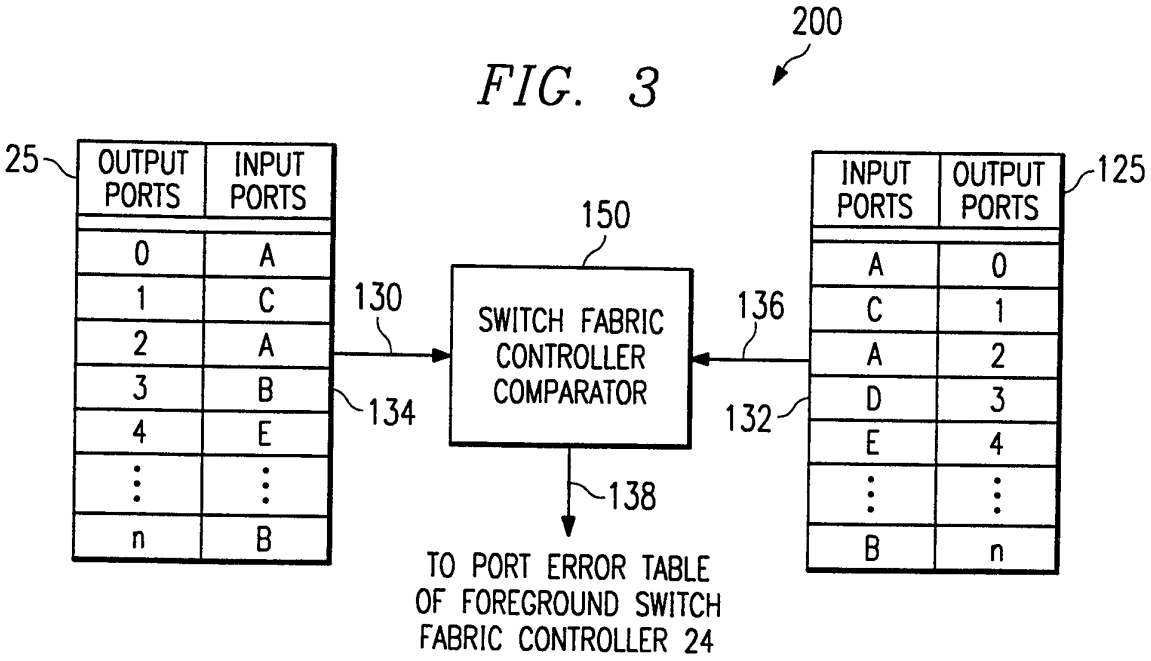
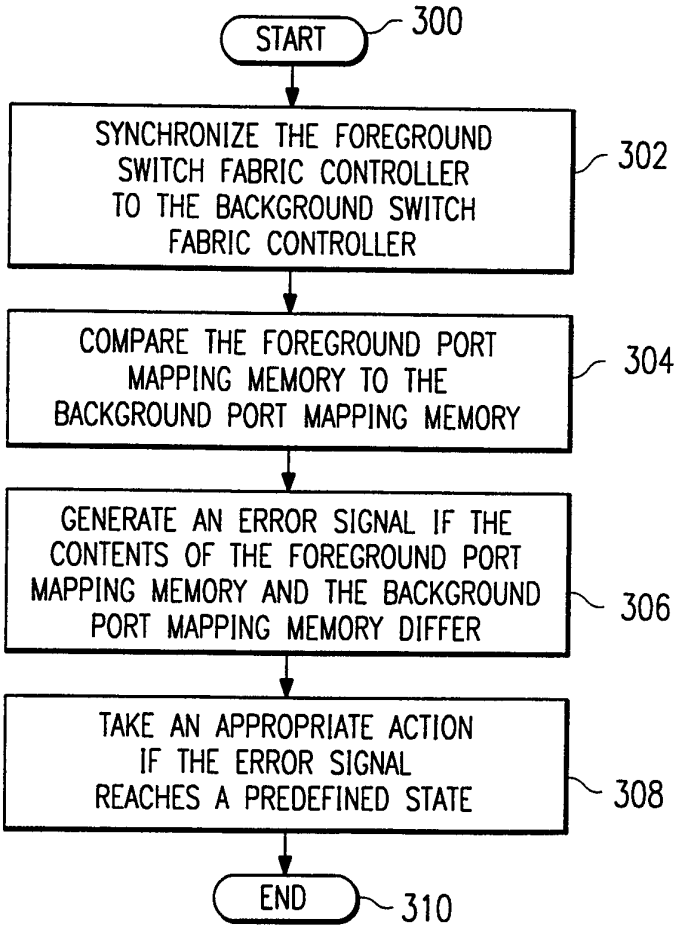

200
25
OUTPUT PORTS
INPUT PORTS
0 A
1 C
2 A
3 B
4 E
n B
130
134
150
SWITCH FABRIC CONTROLLER COMPARATOR
136
132
138
TO PORT ERROR TABLE OF FOREGROUND SWITCH FABRIC CONTROLLER 24
INPUT PORTS
OUTPUT PORTS
A 0
C 1
A 2
D 3
E 4
B n
125

FIG. 4


START
300
SYNCHRONIZE THE FOREGROUND SWITCH FABRIC CONTROLLER TO THE BACKGROUND SWITCH FABRIC CONTROLLER
302
COMPARE THE FOREGROUND PORT MAPPING MEMORY TO THE BACKGROUND PORT MAPPING MEMORY
304
GENERATE AN ERROR SIGNAL IF THE CONTENTS OF THE FOREGROUND PORT MAPPING MEMORY AND THE BACKGROUND PORT MAPPING MEMORY DIFFER
306
TAKE AN APPROPRIATE ACTION IF THE ERROR SIGNAL REACHES A PREDEFINED STATE
308
END
310

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/11916

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : H04L 12/56
US CL : 370/16, 58.1, 58.2, 60, 60.1; 395/182.4
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 370/16, 58.1, 58.2, 60, 60.1; 395/182.4, 182.02, 182.03, 182.05

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	US, A, 5,485,453 (WAHLMAN) 16 January 1996, col. 9, line 42 through col. 10, line 40.	1-17
A	US, A, 5,379,418 (SHIMAZAKI et al.) 03 January 1995, see entire document.	1-17
A	US, A, 5,301,184 (URIU et al.) 05 April 1994, see entire document.	1-17
A,P	US, A, 5,488,606 (KAKUMA et al.) 30 January 1996, see entire document.	1-17
A,P	US, A, 5,436,886 (MCGILL) 25 July 1995, see entire document.	1-17
A	EP, A, 0,484,943 (CHUJO et al.) 13 May 1992, see entire document	1-17

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
27 SEPTEMBER 1996	16 OCT 1996
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer MIN JUNG Telephone No. (703) 305-4363

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