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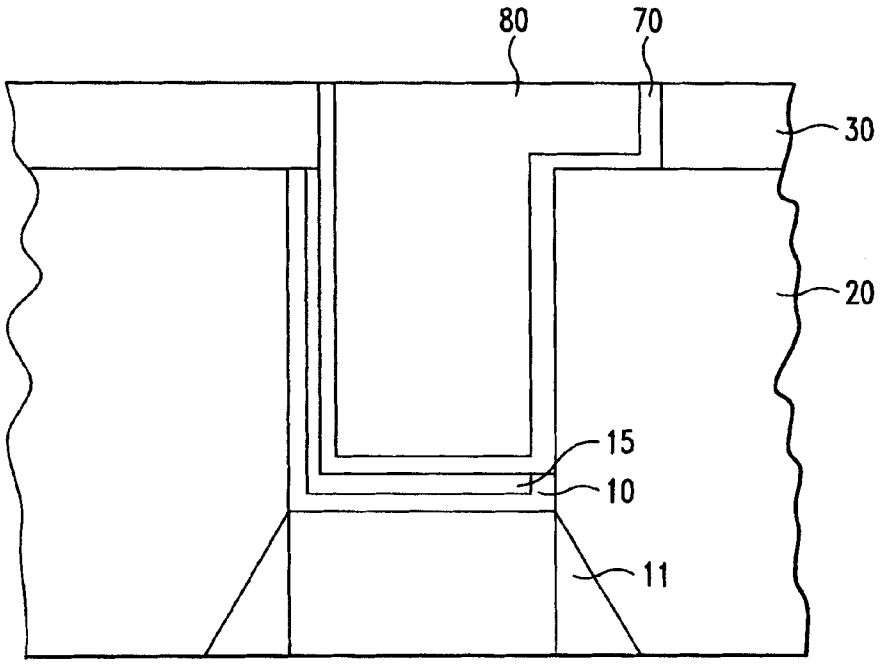
(54) Title: DRY ETCHBACK OF INTERCONNECT CONTACTS



(57) Abstract: A method and structure for a composite stud contact interface with a decreased contact resistance and improved reliability. A selective dry etch is used which comprises a fluorine containing gas. The contact resistance is reduced by partially dry-etching back the tungsten contact after or during the M1 RIE process. The recessed contact is then subsequently metalized during the M1 liner/plating process. The tungsten contact height is reduced after it has been fully formed.

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DRY ETCHBACK OF INTERCONNECT CONTACTS

FIELD OF THE INVENTION

The present invention is directed to the manufacture of semiconductor devices and particularly to the manufacture of metallurgy for integrated circuit devices.

BACKGROUND

This invention relates to the formation of metallurgical interconnects for semiconductor devices, and particularly to the formation of contacts formed at the semiconductor surface which interface with metallurgy formed of copper-based metals. In the currently practiced process local interconnect trenches are etched into a first insulating layer deposited on top of a substrate having active devices. The etched trenches are filled with a liner/tungsten core to make contact with some portions of the substrate devices and polished to be coplanar with the first insulating layer to form the local interconnect (MC).

A second insulating layer is deposited and stud contact holes etched into it. The etched stud contact holes are filled with a liner/tungsten core and polished to be coplanar with a second insulating layer forming the stud contacts (CA) imbedded in the insulating layer which make contact with the local interconnect (MC) and also with additional portions of the devices. The first wiring level (M1) is then formed by either a deposition and subtractive etch or by a damascene process requiring a third layer. This M1 wiring level makes contact with the stud contacts (CA).

SUMMARY

A first aspect of the present invention provides a method of making an electronic device comprising the steps of providing a substrate on which contacts are to be formed; providing a conductive via comprised of a first conductive material formed in an oxide on the substrate; providing a dielectric layer on the conductive via; providing an oxide layer on the dielectric layer; providing a photoresist layer on the oxide layer; forming openings in the photoresist layer; removing the photoresist layer and removing in the openings the dielectric layer and the oxide layer and at least a portion of the first conductive material with a fluorine

containing gas; and depositing a second conductive material in the openings to form a composite conductive via comprising the first conductive material and the second conductive material.

The present invention can ameliorate the problem of increasing CA (stud contact) contact resistance, which is increasing as the technology moves from a 90nm node size to 65nm and 45nm node size. The invention can also provide a more reliable contact than in some known devices.

The fluorine containing gas is preferably NF_3, F_2 or SF_6. In a preferred embodiment the dielectric layer is a low-K SiCOH material. The low-K SiCOH material may be a porous ultra low-K material. In a preferred embodiment the first conductive material is Tungsten and the second conductive material is Copper. However, the invention is not limited to using a tungsten local interconnect. In a preferred embodiment the fluorine containing gas comprises approximately 500 sccm of Argon and approximately 50 sccm of NF_3. The fluorine containing gas may further comprise approximately 10 sccm O_2 and 50 sccm of CH_2F_2 or CH_3F at a pressure of approximately 100 mTorr to approximately 200 mTorr.

A second aspect of the invention provides a method of making an electronic device comprising the steps of: providing a substrate on which contacts are to be formed; providing a conductive via comprised of a first conductive material formed in an oxide on the substrate; providing a dielectric layer on the conductive via; providing an oxide layer on the dielectric layer; providing a photoresist layer on the oxide layer; forming openings in the photoresist layer; removing in the openings the dielectric layer and the oxide layer with a fluorocarbon containing gas; removing the photoresist layer; removing at least a portion of the first conductive material in the openings with a fluorine containing gas; and depositing a second conductive material in the openings to form a composite conductive via comprising the first conductive material and the second conductive material.

Another aspect of the invention provides a method of making an electronic device comprising the steps of: providing a substrate on which contacts are to be formed; providing a conductive via comprised of a first conductive material formed in an oxide on the substrate; providing a dielectric layer on the conductive via; providing an oxide layer on the dielectric layer; providing a photoresist layer on the oxide layer; forming openings in the photoresist layer; removing in the openings the dielectric layer and the oxide layer with a fluorocarbon containing gas;

removing the photoresist layer and removing in the openings a portion of the first conductive material with a fluorine containing gas; depositing a second conductive material in the openings to form a composite conductive via comprising the first conductive material and the second conductive material.

The invention further provides, in another aspect, an electronic device comprising: a poly-silicon gate formed on a substrate; a composite stud via structure in contact with the poly-silicon gate, the composite stud via structure having a first portion and a second portion. In a preferred embodiment the first portion is comprised of Tungsten and the second portion is comprised of Copper. In a preferred embodiment only the first portion is in contact with the poly-silicon gate. In a preferred embodiment the composite stud via structure is approximately 100 nanometers in width and approximately 2,000 angstroms in height. The first portion is approximately 500 angstroms in height.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention are described below in more detail, by way of example, with reference to the accompanying drawings in which:

Figures 1 – 5 illustrate a conventional process for forming a stud contact interconnect; and

Figures 6 – 9 illustrate a method for forming a stud contact interconnect according to the present invention.

The Figures are for illustration purposes only and are not drawn to scale.

DESCRIPTION OF EMBODIMENTS

The present invention reduces the CA contact resistance by partially dry-etching back the tungsten CA contact after or during the M1 RIE process. The recessed CA contact is then subsequently metalized during the M1 liner/plating process. The present invention reduces the tungsten CA height after it has been fully formed. Reducing the CA height will have a significant impact on the CA contact resistance.

For example, consider M1 in a SiCOH material with a TEOS (Tetraethyl Orthosilicate, $Si(OC_2H_5)_4$) hard mask (HM). There is a selective SiCOH etch chemistry which does not (or at a much lower rate) etch TEOS (both HM and

CA TEOS). This SiCOH etch chemistry is NF3 based which is expected to readily etch W.

The present invention discloses the etchback in the dielectric etch of M1 in order to lower the resistance of the tungsten contact. The recess of the tungsten is not a problem for subsequent metallization since the invention uses conventional liner/seed/plating processes that can reliably fill high aspect ratio features.

Referring to the Figures in more detail, and particularly referring to Figure 1, there is shown a conductive via (CA) **15** in an oxide **20**. In a preferred embodiment the conductive material will be Tungsten (W). Referring now to Figure 2, the next level metal wires can now be created by a conventional damascene process which starts out with the deposition of a low-k dielectric film (M1 dielectric) **30** followed by the deposition of an oxide hardmask (M1 Hardmask) **40** and M1 photoresist **50**.

Referring now to Figure 3 there is shown the transfer of the M1 line pattern **60** into the dielectric **30** by Reactive Ion Etching (RIE) including a resist strip. Referring now to Figure 4 there is shown the conventional processing step of liner/seed/plating to form liner **70** and M1 wiring metal **80**. Referring now to Figure 5 there is shown the last conventional processing step of CMP to form the M1 wiring **90**.

The present invention can be used with the same dielectric deposition steps of the low-k material **30** and oxide hardmask **40**, followed by the same lithography step as illustrated in Figure 2. The present invention deviates from the known art either during or after the RIE step.

Referring to Figure 6, a first embodiment of the present invention is to use a fluorine containing gas (but not a fluorocarbon based gas) such as NF3, F2 or SF6 to selectively etch the low-k dielectric **30** to oxide **20**. In a preferred embodiment the low-k dielectric **30** is a SiCOH-like material, and could be a porous-ULK material. The resist selectivity during this RIE step will be low and the critical dimension (CD) control in this case is provided by the oxide hardmask **40** which exhibits a low etch rate in these fluorine-based chemistries. Once the low-k material **30** above the CA tungsten **15** clears, the fluorine based chemistry can also etch the CA tungsten **15** as well as the CA liner **10**. Therefore, the low-k over etch can be used to recess the CA tungsten via

to the desired depth. Since the etch rate of resist is high in these chemistries, it can be completely consumed before or during the low-k over etch and no additional resist strip is required.

This selective M1 RIE process is compatible with conventional etch tools such as parallel plate and medium density plasma RIE tools. In a preferred embodiment the etch gases comprise approximately 500 sccm of Ar and approximately 50 sccm of NF_3. In addition, small amounts of O_2 and CH_2F_2 or CH_3F may be added. For example, approximately 10 sccm of O_2 and approximately 50 sccm of CH_2F_2 or CH_3F. The latter additions can help maintain the critical dimensions or increase the selectivity to the oxide hardmask or resist. In a preferred embodiment the pressure is approximately 100 to 200 mTorr with a power of about 500W for both 27 and 2 MHz frequencies.

Another embodiment of the present invention is to follow known art after the lithography step. In other words, use a fluorocarbon based chemistry to define the trench and a resist strip to remove the photoresist materials. At this point, one can switch to the fluorine-based chemistry (NF3, F2, SF6) to recess the CA tungsten **15 and** liner **10** selectively to the oxide hardmask **20** and CA TEOS.

In another embodiment of the present invention, the known art is followed after the lithography step. In this case, one can use a fluorocarbon based chemistry to define the trench into the low-k dielectric **30** but omit the resist strip. The next step would be to recess the CA tungsten **15** and liner **10** which also strips the remaining photoresist materials **50**.

Figure 6 shows the final results in cross section. Figure 7 shows a top-down view for these three embodiments illustrating the partially exposed CA tungsten **15** and liner **10** in the recessed trench formed in the low-k dielectric **30** and oxide hardmask **40**. The metallization of this structure is achieved by the known art discussed above.

Referring to Figure 8 the structure is shown following liner/seed/plating of liner 70 and M1 wiring metal **80**. Referring to Figure 9 the structure is shown after CMP.

The novel features of the invention can be appreciated by comparing Figures 5 and Figures 9. The CA has been recessed directly below the M1

line and a significant portion of the Tungsten volume **15** in the CA stud has been replaced by Copper **80**. The lower resistivity of Copper **80** results in a lower stud resistance. In addition, the contact area between the CA stud **15** and the M1 line **80** is significantly higher with the new structure and will yield a more reliable interface. This offers the significant reliability advantage that the interface to the devices remains unaltered and the material is the same (barrier and W).

As illustrated in Figure 9 the CA stud interconnect is now a composite structure of two conductive materials. In the preferred embodiment the conductive materials are Tungsten and Copper. In a preferred embodiment the composite stud structure is approximately 100 nanometers in width and approximately 2,000 angstroms in height and the Tungsten portion is approximately 500 angstroms in height.

This composite CA stud contact will have a lower contact resistance than a conventional contact. For example, a 2,000 angstrom high and 95nm wide conventional Tungsten CA stud has an estimated contact resistance of 19 ohms. Approximately a third of this resistance is from W conductivity. If the Tungsten CA is etch backed to a 500 angstrom height, the contact resistance will drop from 19 to 13 ohms. Another advantage is that the contact area between any misaligned (and recessed) CA stud and the M1 line is increased. Besides a lower contact resistance between the copper line and the CA stud, this also provides a more reliable contact.

It will be apparent to those skilled in the art having regard to this disclosure that other modifications of this invention, beyond those embodiments specifically described herein, may be made without departing from the spirit of the invention. Accordingly, such modifications are considered within the scope of the invention as set out in the appended claims.

CLAIMS

1. A method of making an electronic device comprising the steps of:
providing a substrate on which contacts are to be formed;
providing a conductive via comprised of a first conductive material formed in an oxide on said substrate;
providing a dielectric layer on said conductive via;
providing an oxide layer on said dielectric layer;
providing a photoresist layer on said oxide layer;
forming openings in said photoresist layer;
removing said photoresist layer and removing in said openings said dielectric layer and said oxide layer and a portion of said first conductive material with a fluorine containing gas;
depositing a second conductive material in said openings to form a composite conductive via comprising said first conductive material and said second conductive material.

2. The method of claim 1 wherein said fluorine containing gas is selected from the group consisting of NF_3, F_2 and SF_6.

3. The method of claim 1 wherein said dielectric layer is a low-K SiCOH material.

4. The method of claim 3 wherein said low-K SiCOH material is a porous ultra low-K material.

5. The method of claim 1 wherein said first conductive material in Tungsten and said second conductive material is Copper.

6. The method of claim 2 wherein said fluorine containing gas removal comprises approximately 500 sccm of Argon and approximately 50 sccm of NF_3.

7. The method of claim 6 wherein said fluorine containing gas removal further comprises approximately 10 sccm O_2 and 50 sccm of CH_2F_2 or CH_3F.

8. The method of claim 6 wherein said fluorine containing gas removal pressure is approximately 100 mTorr to approximately 200 mTorr.

9. A method of making an electronic device comprising the steps of:
providing a substrate on which contacts are to be formed;
providing a conductive via comprised of a first conductive material formed in an oxide on said substrate;

providing a dielectric layer on said conductive via;
providing an oxide layer on said dielectric layer;
providing a photoresist layer on said oxide layer;
forming openings in said photoresist layer;
removing in said openings said dielectric layer and said oxide layer with a fluorocarbon containing gas;
removing said photoresist layer;
removing a portion of said first conductive material in said openings with a fluorine containing gas;
depositing a second conductive material in said openings to form a composite conductive via comprising said first conductive material and said second conductive material.

10. The method of claim 9 wherein said fluorine containing gas is selected from the group consisting of NF_3, F_2 and SF_6.

11. The method of claim 9 wherein said dielectric layer is a low-K SiCOH material.

12. The method of claim 11 wherein said low-K SiCOH material is a porous ultra low-K material.

13. The method of claim 9 wherein said first conductive material in Tungsten and said second conductive material is Copper.

14. The method of claim 10 wherein said fluorine containing gas removal comprises approximately 500 sccm of Argon and approximately 50 sccm of NF_3.

15. The method of claim 14 wherein said fluorine containing gas removal further comprises approximately 10 sccm O_2 and 50 sccm of CH_2F_2 or CH_3F.

16. The method of claim 14 wherein said fluorine containing gas removal pressure is approximately 100 mTorr to approximately 200 mTorr.

17. A method of making an electronic device comprising the steps of:
providing a substrate on which contacts are to be formed;
providing a conductive via comprised of a first conductive material formed in an oxide on said substrate;
providing a dielectric layer on said conductive via;
providing an oxide layer on said dielectric layer;
providing a photoresist layer on said oxide layer;
forming openings in said photoresist layer;

removing in said openings said dielectric layer and said oxide layer with a fluorocarbon containing gas;

removing said photoresist layer and removing in said openings a portion of said first conductive material with a fluorine containing gas;

depositing a second conductive material in said openings to form a composite conductive via comprising said first conductive material and said second conductive material.

18. The method of claim 17 wherein said fluorine containing gas is selected from the group consisting of NF_3, F_2 and SF_6.

19. The method of claim 17 wherein said dielectric layer is a low-K SiCOH material.

20. The method of claim 19 wherein said low-K SiCOH material is a porous ultra low-K material.

21. The method of claim 17 wherein said first conductive material in Tungsten and said second conductive material is Copper.

22. The method of claim 18 wherein said fluorine containing gas removal comprises approximately 500 sccm of Argon and approximately 50 sccm of NF_3.

23. The method of claim 22 wherein said fluorine containing gas removal further comprises approximately 10 sccm O_2 and 50 sccm of CH_2F_2 or CH_3F.

24. The method of claim 22 wherein said fluorine containing gas removal pressure is approximately 100 mTorr to approximately 200 mTorr.

25. An electronic device, comprising:

a poly-silicon gate formed on a substrate;

a composite stud via structure in contact with said poly-silicon gate, said composite stud via structure having a first portion and a second portion.

26. The electronic device of claim 25 wherein said first portion is comprised of Tungsten and said second portion is comprised of Copper.

27. The electronic device of claim 26 wherein only said first portion is in contact with said poly-silicon gate.

28. The electronic device of claim 27 wherein said composite stud via structure is approximately 100 nanometers in width and approximately 2,000 angstroms in height.

29. The electronic device of claim 27 wherein said first portion is approximately 500 angstroms in height.

30. The electronic device of claim 26 wherein said first portion is in contact with said poly-silicon gate and a conductive metal interconnect.

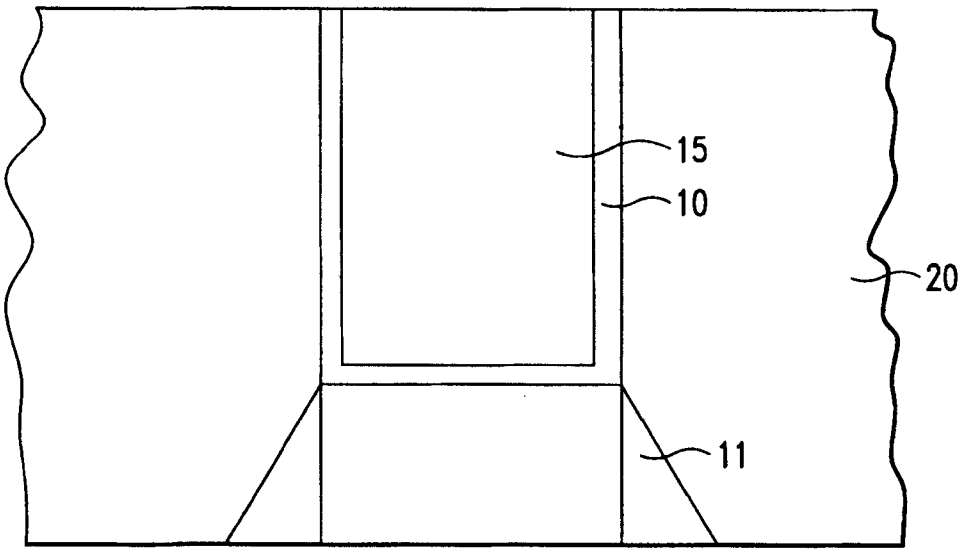

FIG. 1

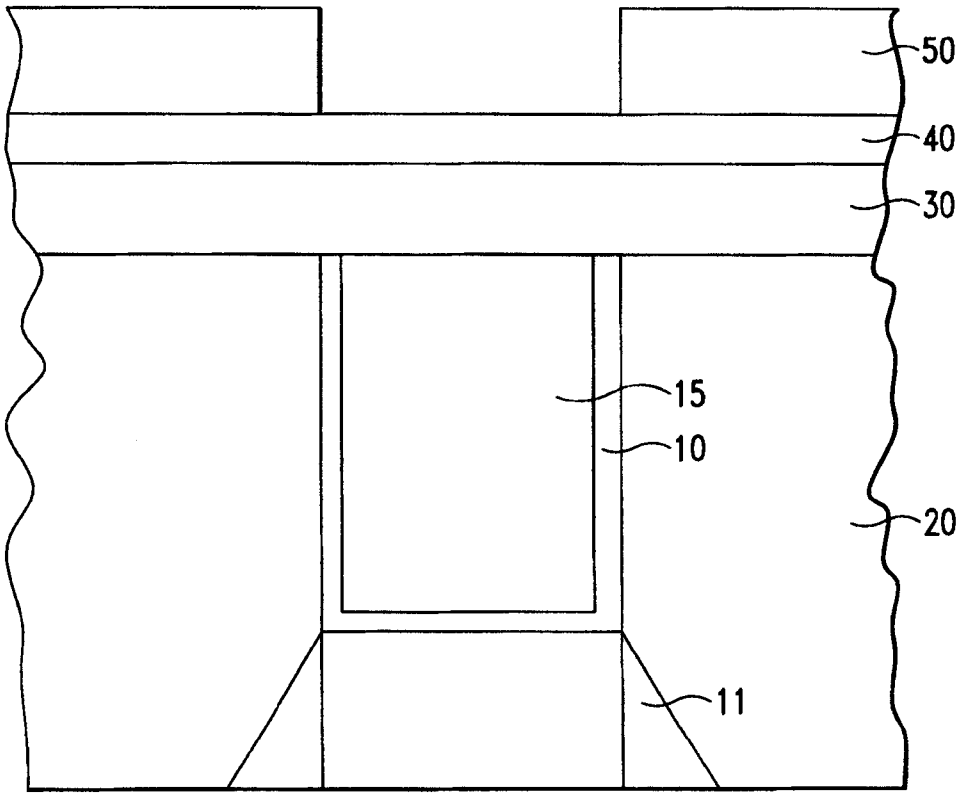

FIG. 2

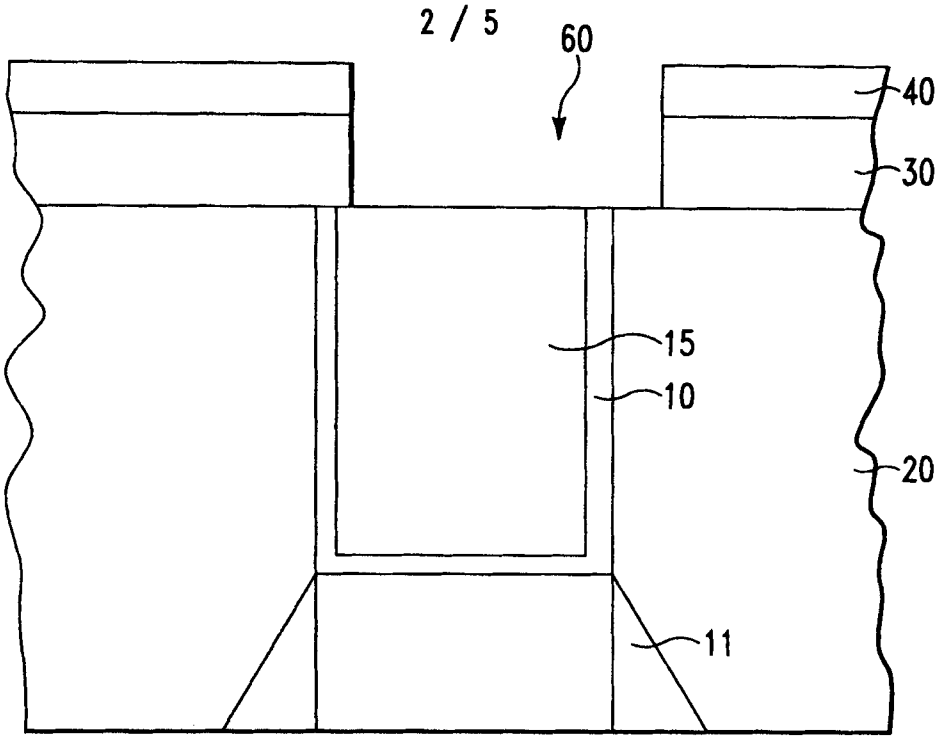

FIG. 3

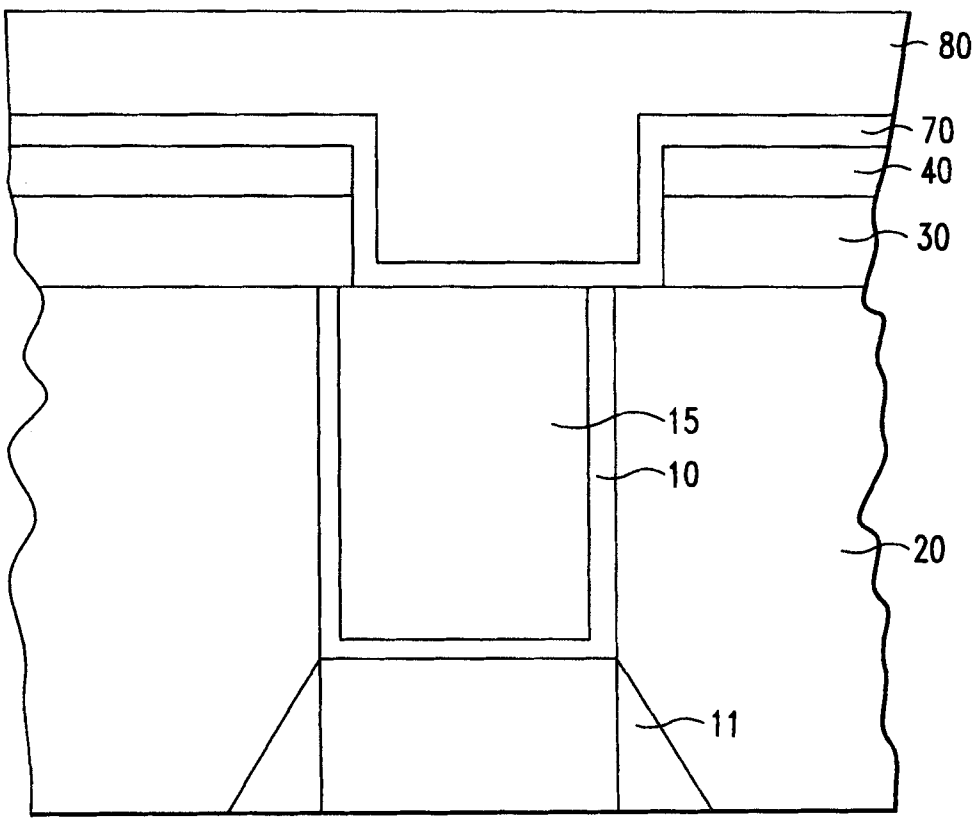

FIG. 4

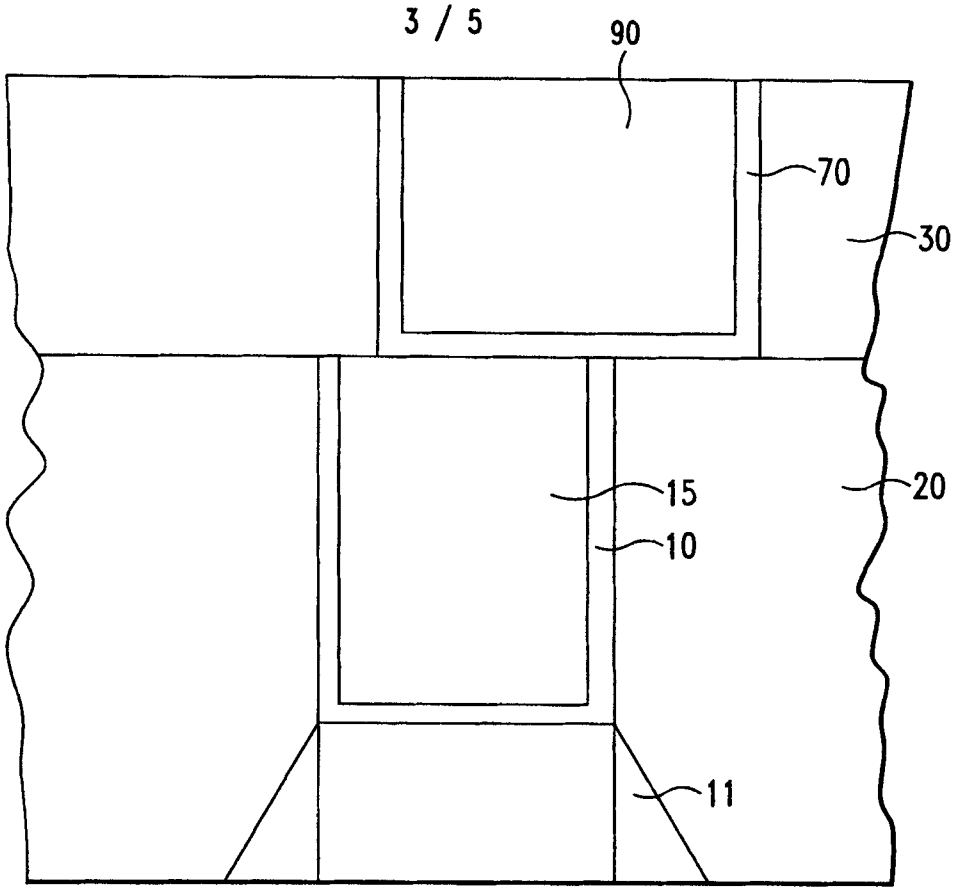

FIG. 5

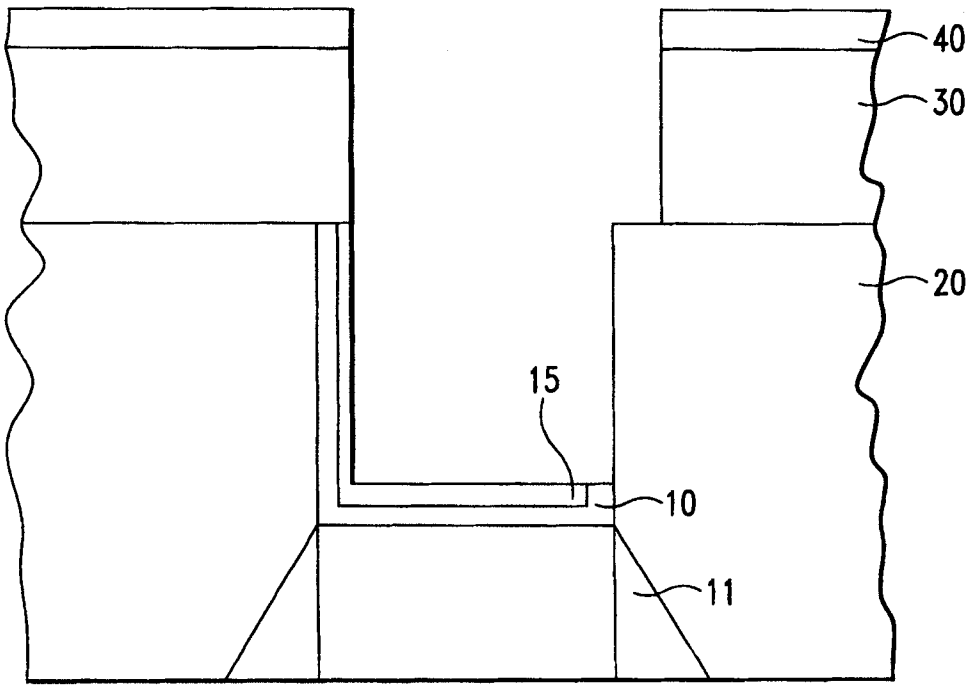

FIG. 6

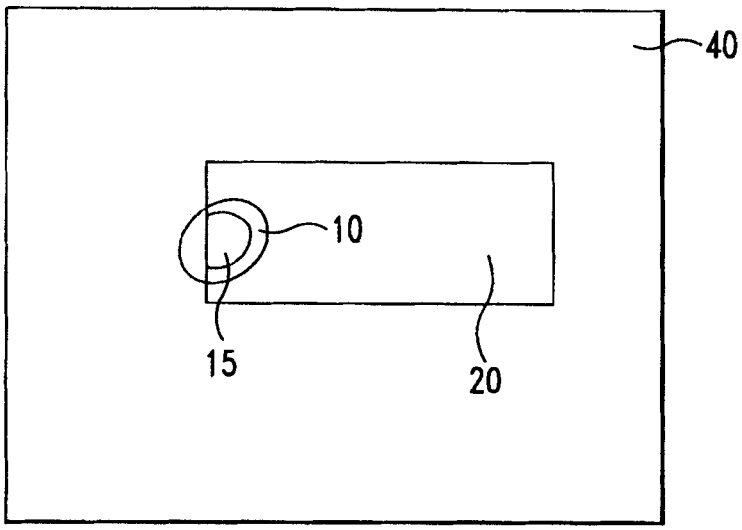

FIG. 7

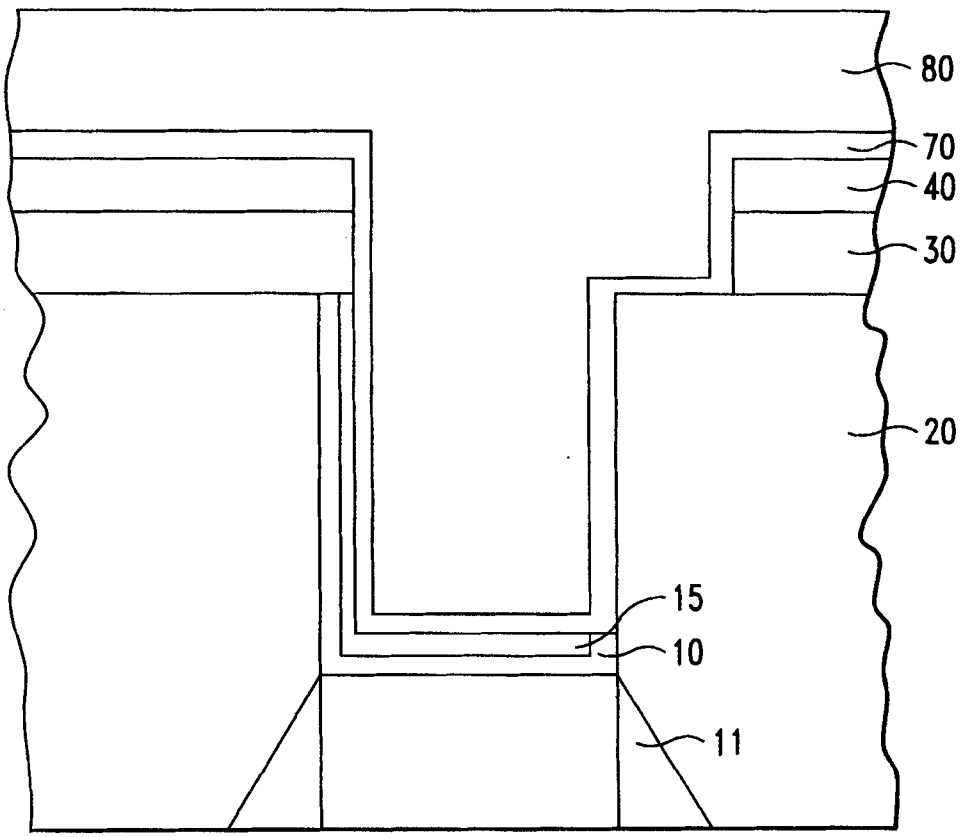

FIG. 8

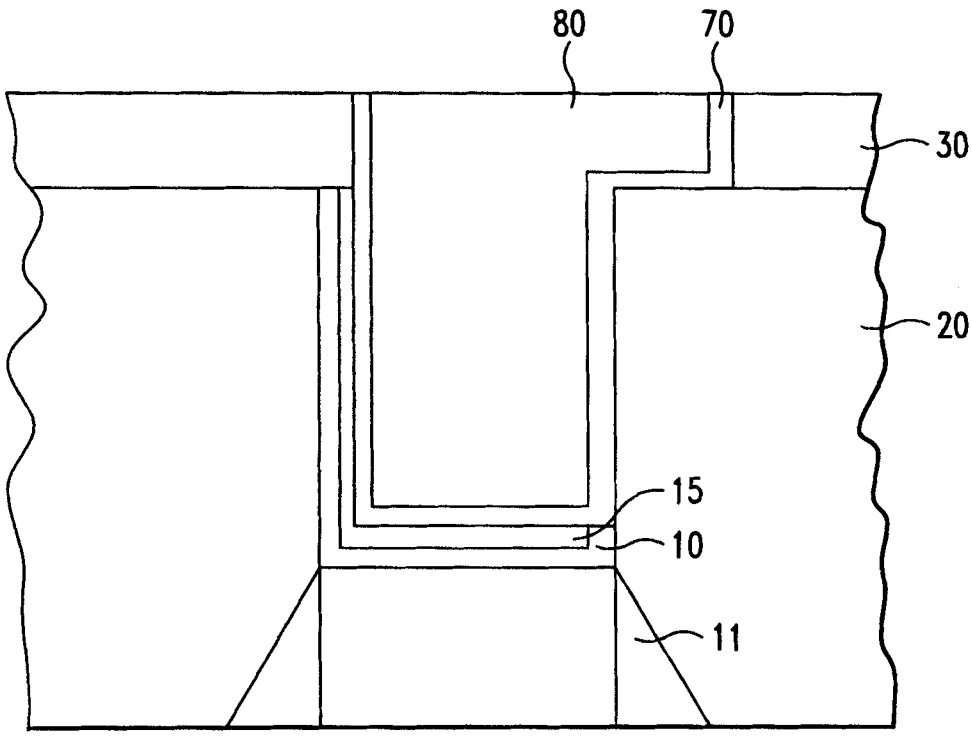

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2006/064757

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/768 H01L23/522 H01L23/532

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	page 17, paragraph 258-268 figures 14a-15d	1-8,10, 14-24
X	EP 0 966 037 A2 (IBM [US]) 22 December 1999 (1999-12-22) page 8, paragraph 41 page 11, paragraph 45 figures 7A,7B,8	25-30
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X	US 5 970 374 A (TEO YEOW MENG [SG]) 19 October 1999 (1999-10-19) column 6, line 62 - column 7, line 67 figures 5A-5E	25-30
A		1-24

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search	Date of mailing of the international search report
18 October 2006	26/10/2006

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Ekoué, Adamah

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2006/064757

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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Information on patent family members

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