(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
16 December 2004 (16.12.2004)

PCT

(10) International Publication Number
WO 2004/109595 A2

(51) International Patent Classification[7]: G06T

(21) International Application Number:
PCT/IB2004/001876

(22) International Filing Date: 26 April 2004 (26.04.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/472,426 22 May 2003 (22.05.2003) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 60/472,426 (CON)
Filed on 22 May 2003 (22.05.2003)

(71) Applicants: **LEE, Jin, H.** [KR/CA]; Canada Interworld Telecommunications Inc., 303-1281 W. Georgia St., Vancouver, British Columbia V6E 3J5 (CA). **CANADA INTERWORLD TELECOMMUNICATIONS INC.** [CA/CA]; 303-1281 W. Georgia St., Vancouver, British Columbia V6E 3J5 (CA).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

WO 2004/109595 A2

(54) Title: METHOD FOR DOUBLING RESOLUTION LCD DISPLAY USING LINE DOUBLING AND NON-LINEAR INTERPOLATION CURVE

(57) Abstract: The most portable devices have a small size LCD display pannel. It is caused form the portable device has some restricted working environment, such as power and computing performance. But these small size LCD display are very hard to read and view. To solve these problems, we need a CPU independent and low-power consumsion hardware architecture. Most desktop and laptop computer system used a VGA card for that purpose. But in portable devices, VGA system is too big to use. So, this proposed system should have very small size hardware and simple image processing algorithm. The proposed architecture use the YCbCr color system and modified image processing algorithms for enlargement, and the new pixel formating method for effiency of frame buffer useage. These methods make available of independent and low-power LCD controller without decreasing of the CPU performance and increasing of the frame buffer memory.

Title: Method for doubling resolution LCD display using line doubling and non-linear interpolation curve.

Introduction

The PDA and cellular phone's LCD displays are used a RGB color system. In the RGB color system, each color component's value is very important for pixel presentation. This means that each color component can not overlook and decimate. In digital image processing, RGB color format is not suitable because of computational complexity and performance. The LCD controller module has the RGB input specifications. So, the most LCD controller's output format is RGB format.

The conventional LCD controller's functions consist with data processing and data transfer function. Input data of LCD controller handled by data processing unit which can enlarge the image size and adjust the contrast, hue, and saturation. The adjustment of contrast, hue, and saturation is performed in same resolution of input data size, so its processing performance depends on the hardware architecture and color format. The enlargement of display size is more complex than the adjustment processing.

The enlargement function is very useful for small systems with large LCD display. The small systems, such as cellular phone, PDA, and embedded systems have some constraints of CPU usages. The enlargement of display size needs computational overheads and memory traffic; even though use the simplest algorithm. So, some LCD controller support the hardware enlargement processing that means enlargement processing needs many computation and memory traffics. The most interpolation methods use the FIR filter structures. The common implementation of FIR filter used multipliers and adders. In the simple liner interpolation algorithm, filter coefficient is very easy to implement because the coefficient value is 2^n. So, the hardware is implemented with simple shifter. The simple algorithm results in bad quality. There is trade-off between quality and complexity. And like Fig.1, when enlarge the original display image, pixel clock(PCLK) and frame buffer memory size also increase for transfer the pixel data to LCD driver module.

Therefore the proposed architecture uses the YCbCr color format for computing like Fig. 2. This color format is very useful for improving the computational complexity, enlargement quality, and memory traffic. After color format changed, each pixel doesn't need all value of Cb, and Cr component. And for image quality and computational complexity, using the new interpolation method base on the look-up table which has a feedback loop. The frame buffer size is very critical for total chip size and external interface pin configuration because memory access need many data and address pins. That kind of external pins effect the total power consuming. And if it uses the MMIC technology, memory size is increase the total die size of chip. So, using smaller memory size is better. For memory buffer size and memory transfer traffic, this architecture proposed the interpolated pixel compression and decompression method. It could reduce the total frame buffer size and traffic.

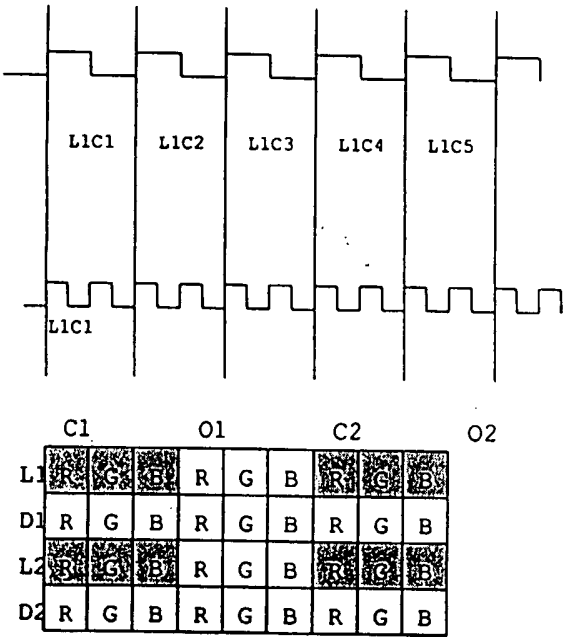


Fig. 1. The relationship between PCLK(Pixel Clock) and resolution.

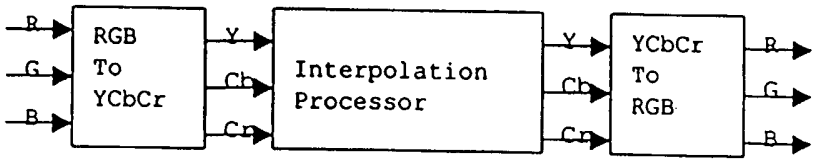


Fig.2. The block diagram of color format useage.

Technical objective

The present invention is improved the interpolation complexity, the frame buffer memory size, a cost effective hardware architecture, and the power consuming for LCD display controller. And also, it support the intellectual property (IP) characterization features.

System architecture

The display data have a temporal and spatial redundancy. In this system, spatial redundancy is key point. An adjacent pixel is very closely related. So, these pixels difference of value is very small or zero. The amount of differences could decide that pixel is on the edge or the background. When pixel is on the background, that pixel's information could be decimated. This method could reduce the total computation amount. The background area is not critical in the enlargement of display size because of background interpolated pixel value is very similar to original pixel values. But, the edge area is very important for image clearance. The common interpolation filter is reduced the high frequency components. So, the edge is looked smooth by interpolation pixels.

Proposed system maximizes the preserving of edge information and the reducing of computational complexity, and also reducing the memory usage by pixel data compression method.

SYSTEM ARCHITECTURE

The overall enlargement system is like Fig. 3. The first step of enlargement is simple motion detection module. It detects the pixel values difference between current pixel and previous pixel. After the motion detection, controller decides interpolation flow. The interpolator & quantizer generate the new pixel data for interpolation position. It is larger than original pixel resolution. So, the next step is compression of the pixel data with encoder module.

Fig. 4 shows the interpolator module block diagram. The most interpolators are consisted with multiplier and adder. The new interpolator module is consisted with Look-up Table (LUT) of quantize step, controller, and interpolation decision unit.

The controller decides the LUT index value and makes control signals. The LUT is contained step size of interpolation value. It is add or subtracted to original values. This step sizes are determined that kept the edge property. And decision unit check the error value and updated the LUT values.

Fig. 9(a) is non-linear interpolation curve. This curve is non-linear but it has symmetric characteristics. So, if display mode is set to 2x mode, the result is almost same as linear interpolation. In fig.9 (a), center line is conventional interpolation deciding line which is center of two pixel values. It is very easy to decide but we loose high frequency component form original signal. So, this system uses $I_{n,n+1}$ line for 2x mode. Fig. 9 (a) shows two $I_{n,n+1}$ lines, in 2x mode use only one line which is decided by relation of 2 pixels(P_n, P_{n+1}). Fig. 9 (b) ~(c) shows the decision line of interpolation. This method can support the varieties of interpolation step as the input situation.

Fig. 5 describes the relation of RGB and YCbCr color format. The digital video and image processing use the YCbCr color format. Because YCbCr color format is more efficient to store the pixel data. The YCbCr format could decimate to 4:1:1(Y:Cb:Cr) for every 4 pixels.

The interpolation value is decimating with Fig 5. And then, Y component value is encoded with differential pulse coded modulation (DPCM) method. Fig.6 shows that the DPCM encoder's block diagram. The delay is one or three pixels for prediction. The performance of encoder depends on the predictor's accuracy. Because the encoder's output is difference between predicted value and current value. So, if predictor makes good prediction value, the output variable length coder result is very good. It means that compression rate is very high. This compression could reduce the frame buffer memory usage. As the enlargement rate is bigger than 2, the frame buffer memory usage increase with 2^n. So, compression is very important for the efficiency of frame buffer memory.

The encoded data is decoded with decoder. Fig. 7 shows the decoder block diagram. It is inverse process of encoder modules.

As like Fig. 8, the input data is interpolated with new LUT methods that only output the LUT index data. This data is compressed with Fig. 6, and then stored frame buffer memory. Finally output date is decoded with Fig. 7; its data is real pixel data that include the interpolated pixel data. So, Fig. 7 will have the calculation modules that will be simple adder. This separation of decoder and encoder function is very efficient for parallel processing and it could be reduce the image processing overload.

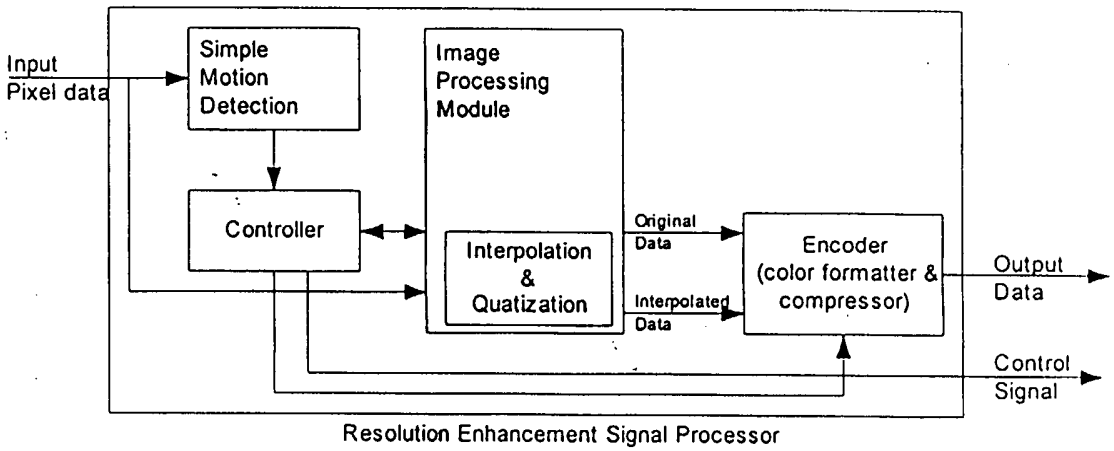


Fig. 3. The block diagram of the resolution enhancement signal processor

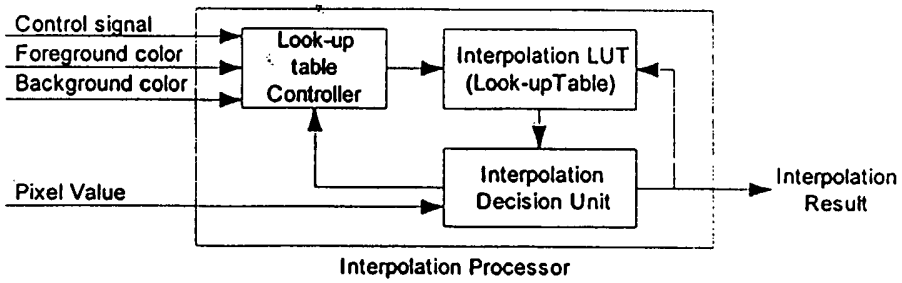


Fig. 4. The signal flow diagram of interpolation processor which is based on look-up table method

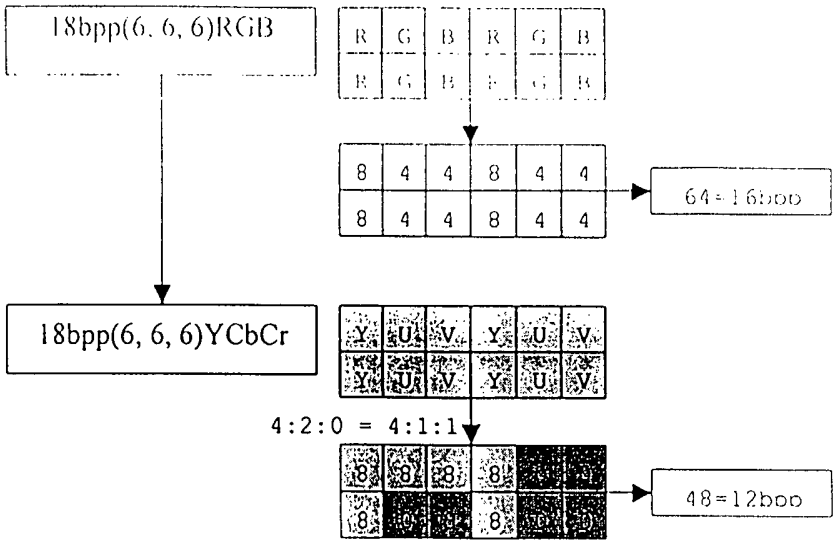


Fig. 5 The relation of RGB and YCbCr

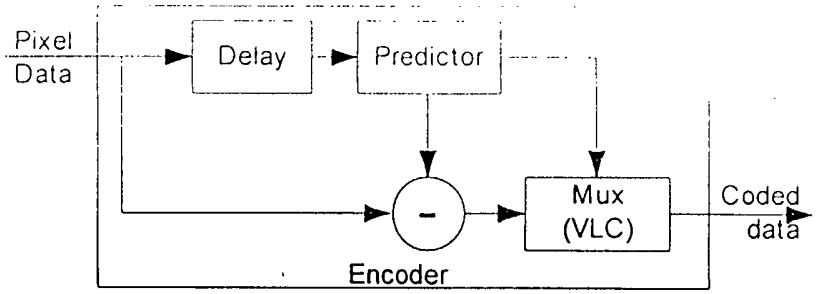


Fig. 6 The block diagram of encoder module

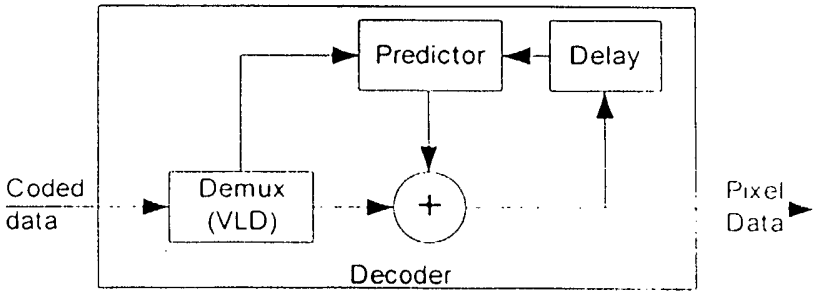


Fig. 7 The block diagram of decoder module

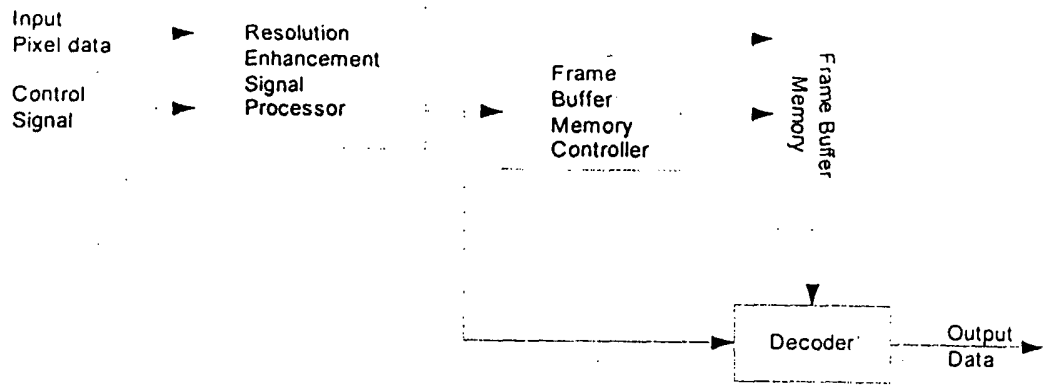


Fig. 8 The data flow of the overall processing

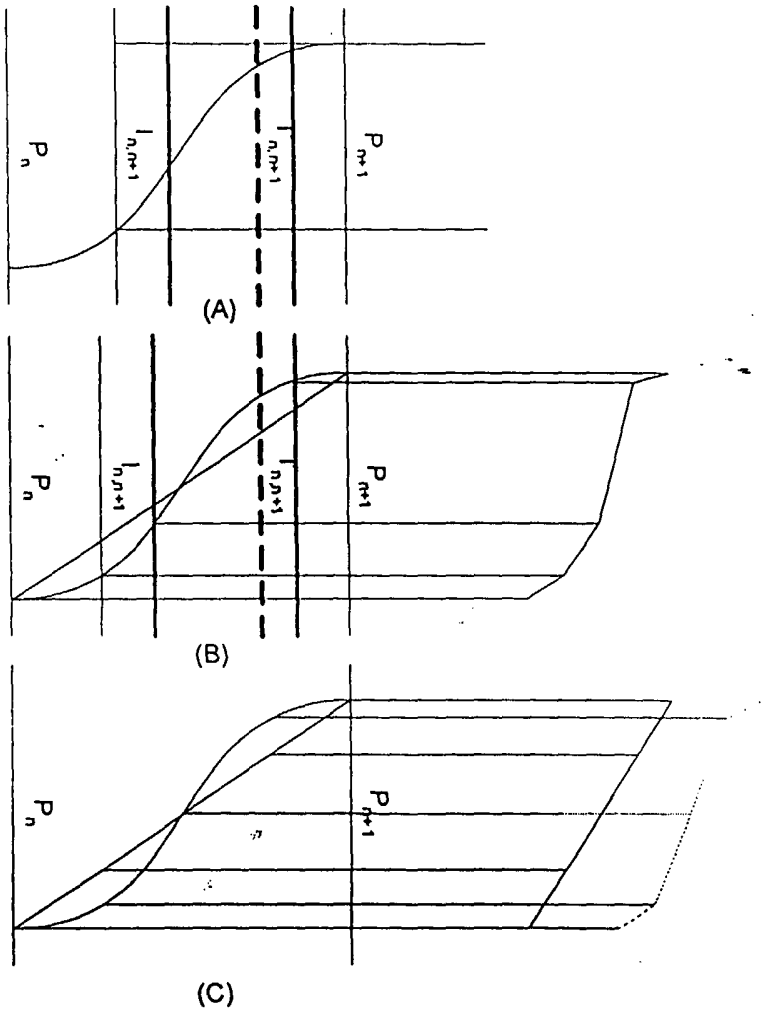


Fig. 9 The method of interpolation table decision.
(a) non-linear interpolation curve
(b) non-linear and linear interpolation curve
(c) an comparison of linear and non-linear results.

Claims :

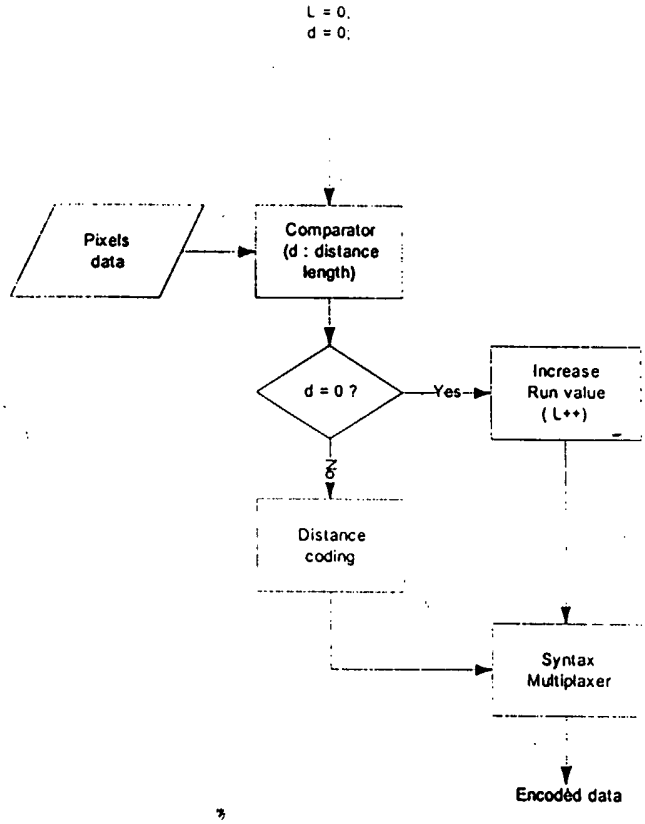
1. A method for scaling a low resolution display size to multiple of 2. It includes the simple motion detector, controller, image processing module, and data compression codec.

2. A method for interpolating a pixel data. And look-up table based interpolation step decision method. It includes look-up table, step size decision controller, and decision unit that have table update function.

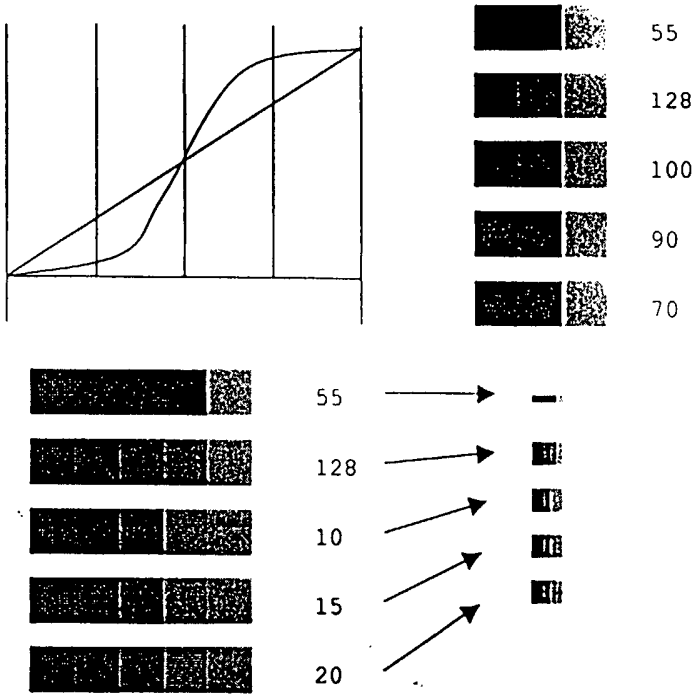
3. A method for compressing an interpolated pixel data. It receives the index data from claim 2, and predicted the current value with predictor. And it includes the LUT base variable length code book.

4. A method for decompressing a compressed data as claim 3. It includes a syntax parser, index predictor, and adder.

5. A method for making and deciding an interpolation step size table as claim 2. It reserves the edge characteristics and can implement with adaptive architecture.



The flow chart of pixel compression (reference figure)



The example of interpolation pixel value decision method (reference figure)

Many efforts have been made to find a way to view full HTML web pages on mobile devices over the wireless Internet. In order to that, there are two approaches, one thing is to increase the display panel size and the other is to increase the resolutions of display. As it reveals, the large panel is not adequate for mobile terminal and thus, small LCD that has more pixels in the unit area is required, which has technical limitation to enhance resolution to an some extent. The method to increase the resolutions without increasing number of pixels has been developed and called Smart Display Technology (SDT). SDT is implemented by hardware logic only. With this SDT, you can get mobile Web access to real Web pages that maintain full text legibility.

Smart Display Technology

Smart Display Technology (SDT) is a new method for increasing horizontal and/or vertical resolution in TFT LCD. We describe the method for doubling vertical resolution as well as horizontal resolution for digital color TFT LCDs, which are used for mobile terminal such as cell phone, PDA, and HPC. As the digital LCD has a different array of pixels from that of analog type LCD, we applied an method to attain doubling horizontal and vertical resolutions simultaneously. With this method, horizontal and vertical resolutions are doubled, that is to say, the resolution is increased by 4 times comparing to the conventional method. This technology is implemented using hardware logic only, less than 2k gates are used; therefore, this is independent to the OS, or applications. In addition, this hardware logic size is small enough to merged into graphic controller as a sub-function.

Key Solutions for Doubling Resolutions in TFT color LCD

Digital TFT are arrayed in in-line and square pixels as depicted in Figure 1.

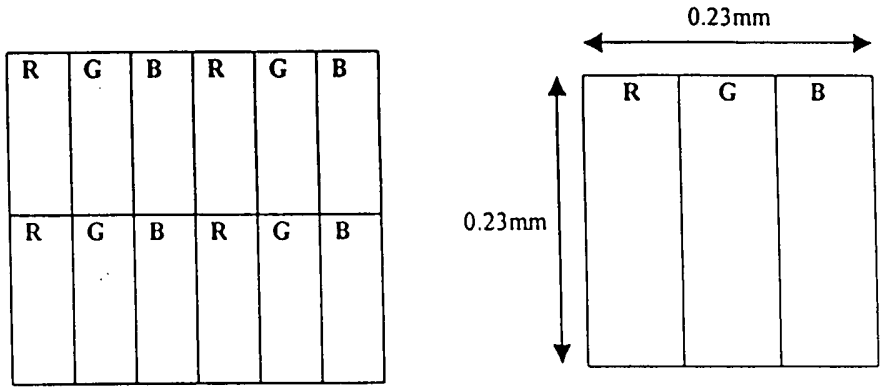
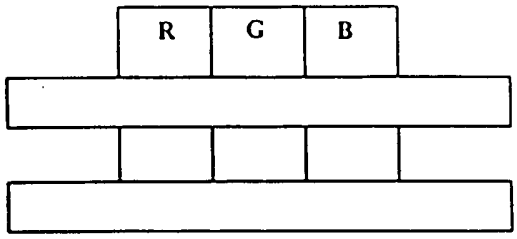
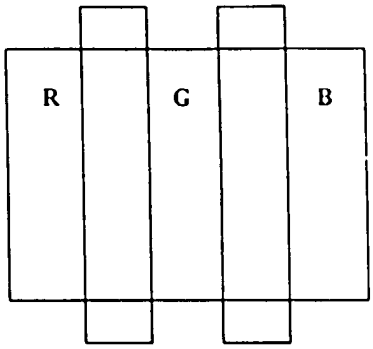


Figure 1. Pixel Architecture

The digital TFT has different array and aspect ratio of pixels from those of analog type TFT. In order to increase resolution with this digital one, we have to increase it to same ratios in horizontal and vertical because original picture was made based on that the pixels are square and aspect ratio is 1 to 1. We invented the new method displaying without loss of any information, which is not conventional averaging or sampling.



a) Doubling Vertical Resolution



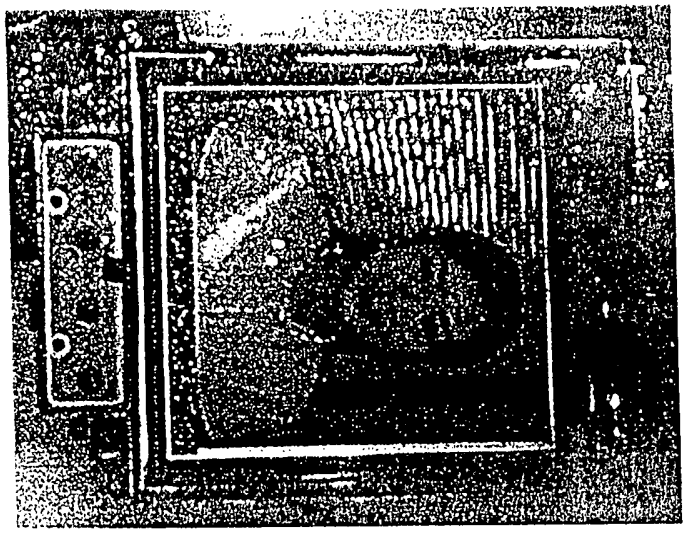
b) Doubling Horizontal Resolutions

Figure 2. Method of doubling the resolutions

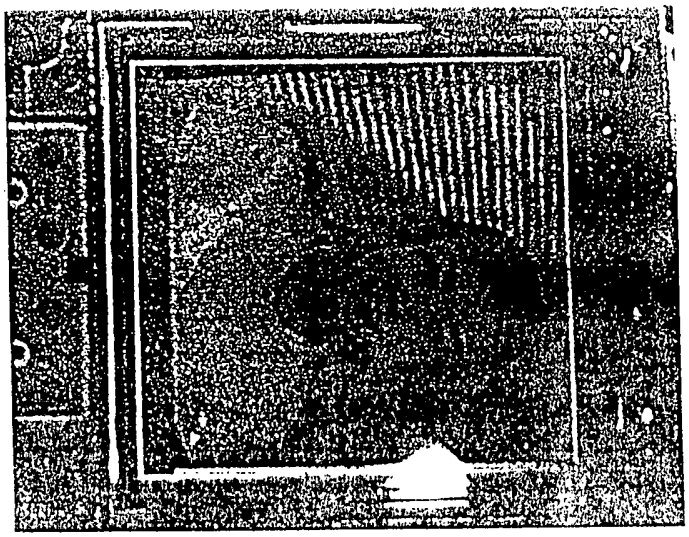
As shown in Figure 2, our method is to display 2 lines in vertical and/or horizontal on one RGB pixel. Conventionally, it can be displayed only one horizontal and vertical line.

Implementation results in TFT color LCD

To implement and test SDT, Samsung 2.32 Inch TFT LCD, 162 x 174 pixels, was used. Followings (Figure. 3 and Figure. 4) are comparison pictures between 160x160 (original picture) and 320 x 320 (enhanced resolution).

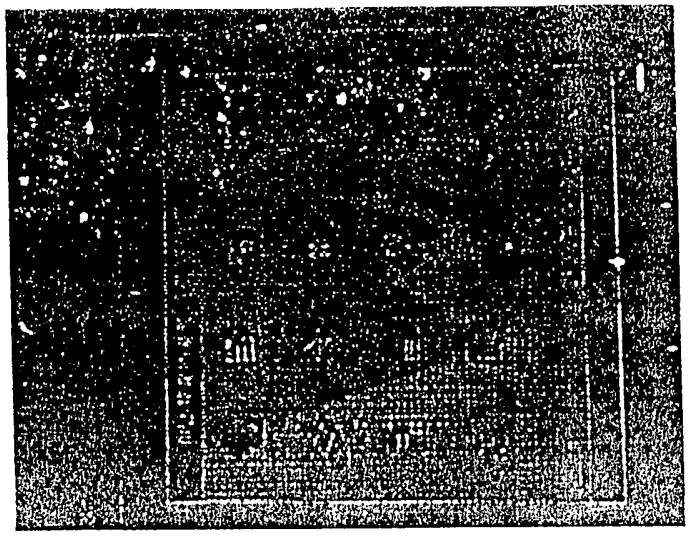


a) 160 by 160 image displayed on 162 by 174 TFT LCD using conventional method

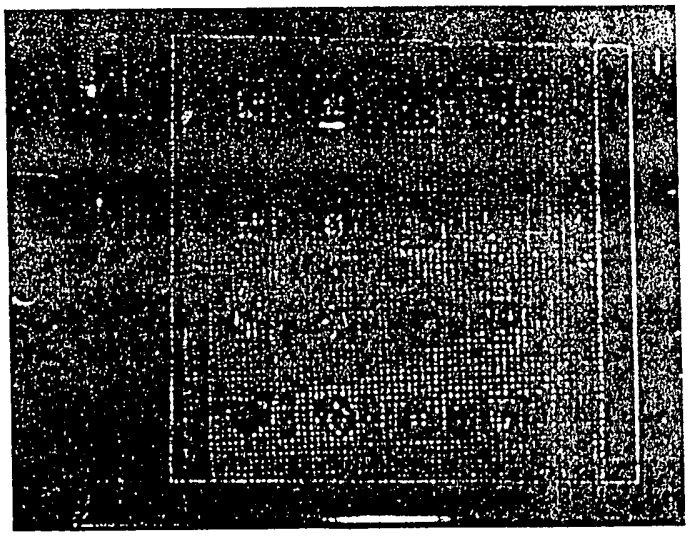


b) 320 by 320 image displayed on 162 by 174 TFT LCD using SDT

Figure 3. Test Result 1



a) 160 by 160 image displayed on 162 by 174 TFT LCD using averaging method



b) 320 by 320 image displayed on 162 by 174 TFT LCD using SDT

Figure 4. Test Result 2

Application 1. Embedded in MSM Chip

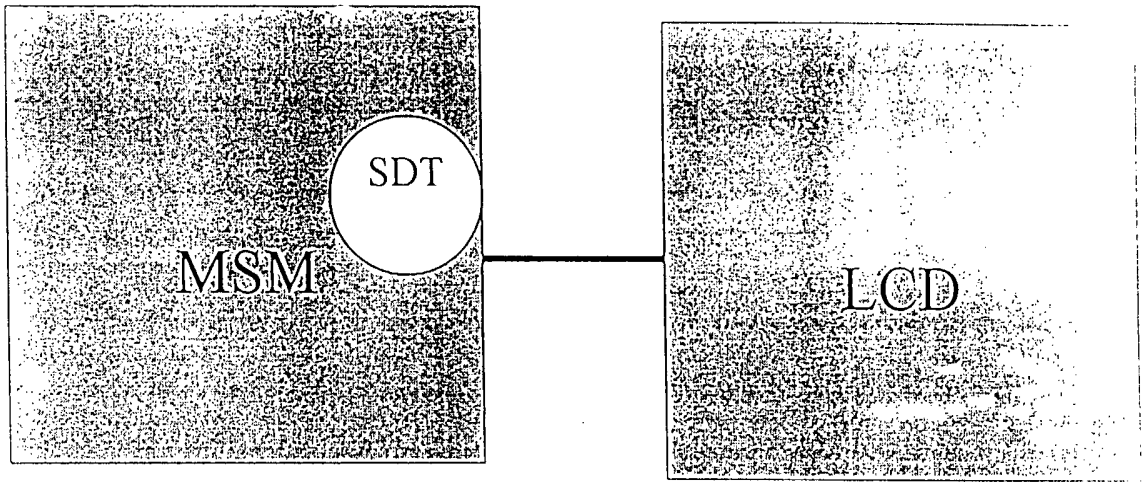


Figure 5. Embedded SDT

SDT function is implemented using around 2000 gates hardware logic so it can be embedded any chip as a sub function.

SDT can be embedded in MSM chip so that users can enable/disable the function or change from normal mode to enhanced mode, or vice versa.

It will be very useful for phone manufacturers to use the SDT function without any PCB modification or additional space to mount it. It will save the cost and keep the phones still small size.

Phone developers can change the parameter by setting MSM register, which will increase the flexibility of the application.

Application 2. Interface with Cellular

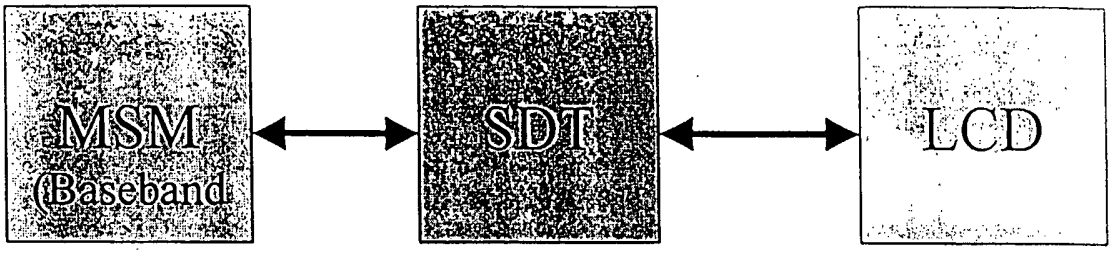


Figure 6. Block Diagram for Phone Application

MSM Chip provides LCD pins to interface LCD. To increase the LCD resolution 2 or 4 times, SDT can be connected between MSM and LCD. SDT processes data from MSM to display them in LCD with increased resolution.

System Configuration for Cell phone

The SDT 1909 application exemplary configuration is as follow.

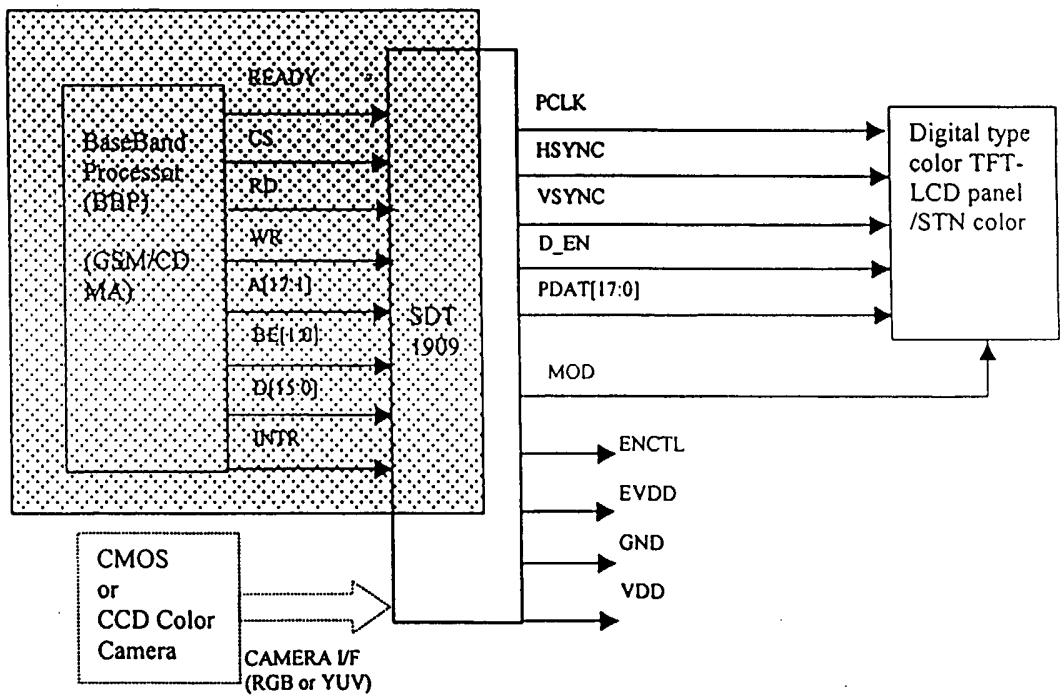


Figure 7. Configuration of SDT1909 application for Cell Phone

SDT1909 Specifications

Introduction

Smart Display Chip (SDT1909) is to enhance the graphic resolution performance on the existing TFT/STN LCD panel resulting twice horizontal and vertical resolution respectively. This chip can be applicable to both analog and digital type TFT/STN LCD panel. With this solution, we can replace expensive TFT color LCD in mobile terminals such as cellular phones, smart phones, and PDAs to low cost analog TFT LCD. In addition, it can achieve product competency in cost and power consumption by using the half sized TFT LCD for the same required performance.

The SDT1909 is suitable for low-power, embedded applications, where high-resolution color displays is required at a low cost and without redesigning the system. These applications include:

.-. Wireless Handsets including smart-phones
.-. PDAs.
.-. Handheld game machine.
.-. MPEG players with audio.

The SDT1909 allows handset to support for color displays with high-resolution graphics and for camera interface (as needed in wireless gaming or other mobile applications) without redesigning of the entire handset.

Key Features

- Doubling the horizontal and/or vertical resolution on existing color LCD by signal processing. No software involved, but graphic size modification is required.
- SDT can be enabled/disabled depend upon the applications.
- Camera module interface function.
- Frame buffering for power saving.
- Advanced Power Management function

Specifications

- Resolution control range: 160*160~ 640*640.
- Applicable LCD pixels: 80*80 ~ 320*320.
- Horizontal and vertical resolutions are controlled by inner register settings independently.
- Frame buffer memory: 512k bytes.
- Panels: Stripe type TFT color, STN color LCD
- Camera interface
- Support 260K colors (18-bpp)
- 2-D graphic acceleration
- Power down mode
- High and Normal resolution mode
- Picture rotations: 0, 90, 270 Deg.
- Color space conversion
- Camera overlay
- Video interface: CCIR656 or CPU Host
- Image scaling
- LCD interface (H-sync, V-sync, clock, 8bit data).
- 3.0 V single power supply.
- Package: 144 pin BGA (88 pins are used).

System Configuration

Example of SDT 1909 application

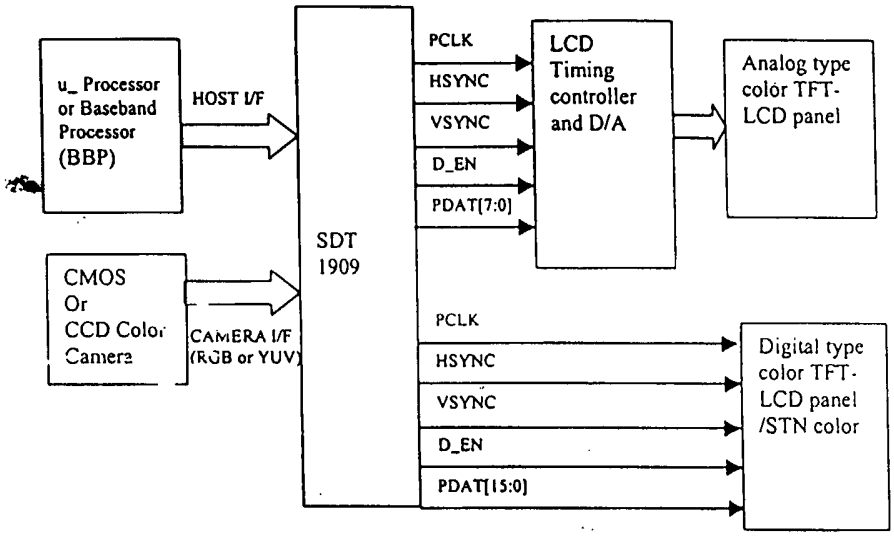


Figure 1. System configuration for SDT 1909

The SDT graphics controller is designed to connect to the TFT-LCD controller such that it can drive the color TFT-LCD panel. The pin interface of SDT1909 is shown in the following table.

Table 1) Pin Descriptions

SDT1909 pin symbol	Description
PCLK	Data clock input
HSYNC	Horizontal sync. signal
VSYNC	Vertical sync. signal
PDAT0	Digital data input bit 0, LSB.
PDAT1	Digital data input bit 1
PDAT2	Digital data input bit 2
PDAT3	Digital data input bit 3
PDAT4	Digital data input bit 4
PDAT5	Digital data input bit 5
PDAT6	Digital data input bit 6
PDAT7	Digital data input bit 7, analog MSB
PDAT8	Digital data input bit 8.
PDAT9	Digital data input bit 9
PDAT10	Digital data input bit 10
PDAT11	Digital data input bit 11
PDAT12	Digital data input bit 12
PDAT13	Digital data input bit 13
PDAT14	Digital data input bit 14
PDAT15	Digital data input bit 15, Digital MSB
D_EN	Data enable and control
Host I/F	16 bit asynchronous bus (ARM based)
Camera I/F	CCIR656 compliant(YUV or RGB)

Block Diagram of SDT 1909

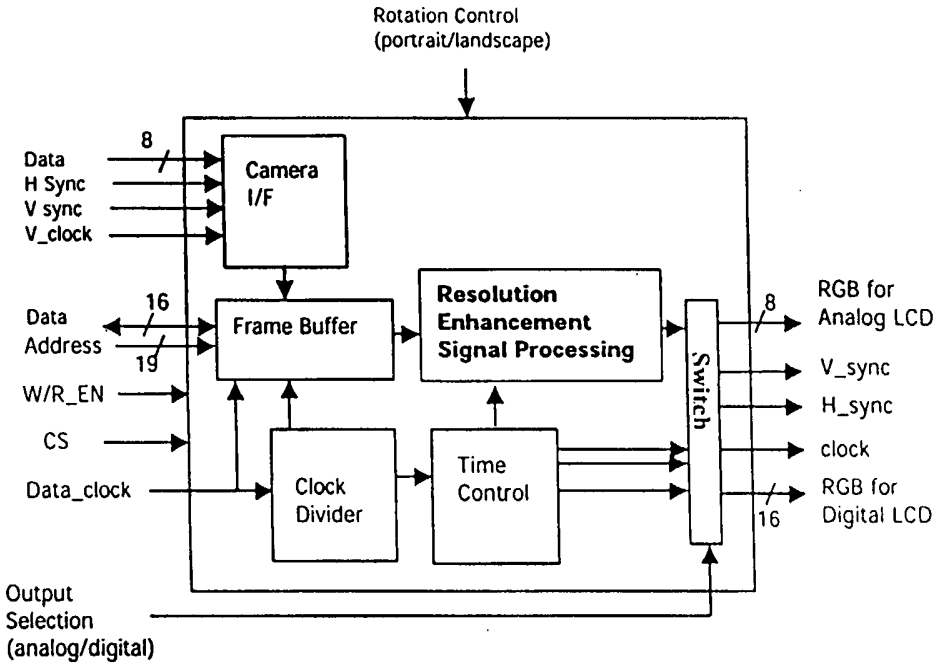


Figure 2. Block diagram of SDT 1909

The functions of each block in figure 2 are;

(i) Camera I/F: camera data can be YUV or RGB. Color space conversion is performed in this block and data will be written in the frame buffer memory.

(ii) Frame buffer: memory for R,G,B data of a page of picture, which is a frame. In case of 320x240 picture that is composed of 16 bits pixel data (5,6,5 in R,G,B format), the required memory size is 230.4k bytes. This memory can be replaced to system memory, but for less power consumption to access memory, this architecture is preferred.

(iii) Clock Divider: this block is for making four-times-clock synchronized to the data clock from video processor (or system processor)

(iv) Time control: this block is for generating horizontal and vertical sync that is required to LCD. This timing is dependent to the LCD specifications.

(v) High resolution display control: depend upon the fields and lines, the order of R,G,B is controlled in this block. Using the external "display selection" signal, the displayed picture can be rotated just rearranging the sequence of reading data from frame memory.

(vi) Switch: this is for switching the output data according to the used LCD, analog or digital.

Package Specifications

- Mechanical Drawings

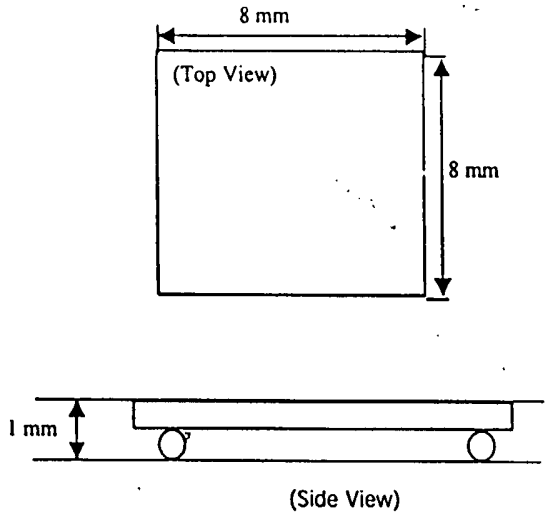


Figure 3. Mechanical Drawing of SDT 1909