



- | | |
|--|---|
| (51) International Patent Classification:
<i>G01R 31/3193</i> (2006.01) <i>H04L 9/32</i> (2006.01)
<i>H03K 5/24</i> (2006.01) | (72) Inventor: ZOU, Zhi-Yuan; 1355 Carlson Drive, Colorado Springs, Colorado 80919 (US). |
| (21) International Application Number:
PCT/US2019/057960 | (74) Agent: BACA, Andrew J. et al.; P.O. Box 2550, Salt Lake City, Utah 84110 (US). |
| (22) International Filing Date:
24 October 2019 (24.10.2019) | (81) Designated States (<i>unless otherwise indicated, for every kind of national protection available</i>): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW. |
| (25) Filing Language: English | |
| (26) Publication Language: English | |
| (30) Priority Data:
62/786,016 28 December 2018 (28.12.2018) US
16/294,467 06 March 2019 (06.03.2019) US | |
| (71) Applicant: MICROCHIP TECHNOLOGY INCORPORATED [US/US]; 2355 West Chandler Boulevard, Chandler, Arizona 85224 (US). | (84) Designated States (<i>unless otherwise indicated, for every kind of regional protection available</i>): ARIPO (BW, GH |

(54) Title: CLASSIFYING COMPARATORS BASED ON COMPARATOR OFFSETS

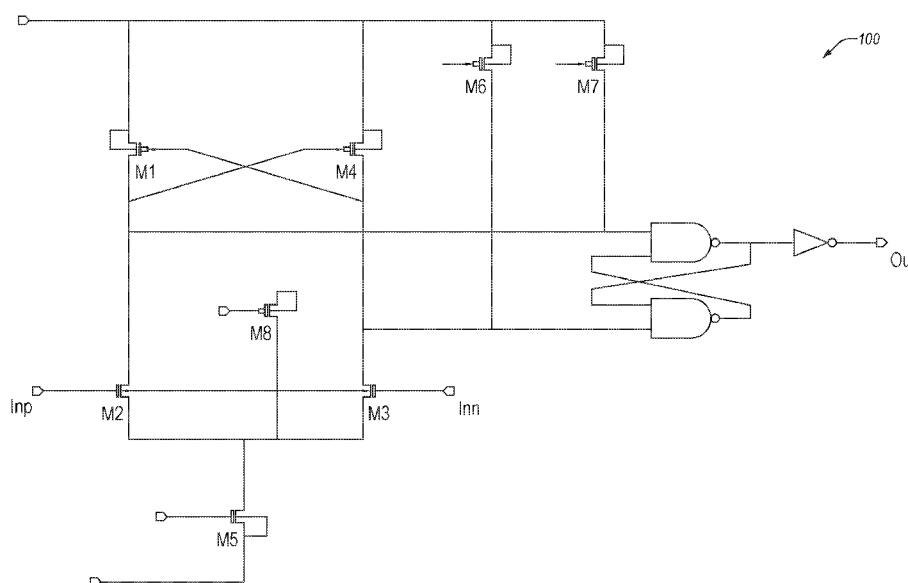


FIG. 1

(57) Abstract: Various embodiments relate to classifying comparators (100) based on comparator offsets. A method may include applying, via a strobe (M5 gate), a first voltage to each of a first input (Inp) and a second input (Inn) of a comparator to generate a number of output signals (Out) from the comparator, wherein each output signal has one of a first polarity and a second polarity. The method may further include in response to each of the number of output signals being the first polarity, applying, via a strobe, an external offset voltage (Vinp at Inp, Vinn at Inn) having the second polarity to the comparator to generate a second number of output signals. Further, the method may include in response to each of the second number of output signals being the same polarity, identifying the comparator as a reliable comparator.

GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

- *with international search report (Art. 21(3))*
- *with amended claims and statement (Art. 19(1))*

- 1 -

CLASSIFYING COMPARATORS BASED ON COMPARATOR OFFSETS**PRIORITY CLAIM**

This application claims the benefit of the filing date of United States Provisional
5 Patent Application No. 62/786,015, filed December 28, 2018, for “METHODS OF
CLASSIFYING COMPARATORS BASED ON COMPARATOR OFFSETS” (the ‘015
Provisional Application), and claims the benefit of the filing date of United States Patent
Application Serial No. 16/294,467, filed March 6, 2019, for “CLASSIFYING
COMPARATORS BASED ON COMPARATOR OFFSETS,” pending, the disclosure of
10 each of which is hereby incorporated herein in its entirety by this reference.

TECHNICAL FIELD

The present disclosure relates generally to classifying comparators based on
comparator offsets, and more specifically, to identifying comparators with suitable offsets
15 for reliable key generation.

BACKGROUND

A physical unclonable function (PUF) may serve as a unique physical identity in a
physical structure (e.g., a semiconductor device such as a microprocessor). A PUF, which
20 is based on a physical variation that may occur naturally during a semiconductor
manufacturing process, may allow for differentiation between otherwise identical
semiconductor devices. Because semiconductor devices may be slightly different,
operation of the semiconductor devices (e.g., outputs generated by the semiconductor
devices) may vary.

25

BRIEF DESCRIPTION OF THE DRAWINGS

While this disclosure concludes with claims particularly pointing out and distinctly
claiming specific embodiments, various features and advantages of embodiments within the
scope of this disclosure may be more readily ascertained from the following description when
30 read in conjunction with the accompanying drawings, in which:

FIG. 1 depicts a comparator circuit, according to one or more embodiments of the
disclosure;

- 2 -

FIGS. 2 and 3 are plots for depicting comparator input offset statistical distribution, according to one or more embodiments of the disclosure;

FIG. 4 is a flowchart of an example method of identifying a comparator with a suitable input offset for key generation;

5 FIG. 5 is an example circuit for generating an external offset voltage, in accordance with various embodiments of the disclosure;

FIG. 6 is an example circuit diagram including a comparator coupled to a resistor string, according to one or more embodiments of the disclosure;

FIG. 7 is a block diagram of an example system, according to one or more embodiments
10 of the disclosure; and

FIG. 8 is a block diagram of an example computing system.

MODE(S) FOR CARRYING OUT THE INVENTION

In the following detailed description, reference is made to the accompanying
15 drawings, which form a part hereof, and in which are shown, by way of illustration, specific examples of embodiments in which the present disclosure may be practiced. These embodiments are described in sufficient detail to enable a person of ordinary skill in the art to practice the present disclosure. However, other embodiments may be utilized, and structural, material, and process changes may be made without departing from the scope of
20 the disclosure.

The illustrations presented herein are not meant to be actual views of any particular method, system, device, or structure, but are merely idealized representations that are employed to describe the embodiments of the present disclosure. The drawings presented herein are not necessarily drawn to scale. Similar structures or components in the various
25 drawings may retain the same or similar numbering for the convenience of the reader; however, the similarity in numbering does not mean that the structures or components are necessarily identical in size, composition, configuration, or any other property.

The following description may include examples to help enable one of ordinary skill in the art to practice the disclosed embodiments. The use of the terms “exemplary,” “by
30 example,” and “for example,” means that the related description is explanatory, and though the scope of the disclosure is intended to encompass the examples and legal equivalents, the use of such terms is not intended to limit the scope of an embodiment or this disclosure to the specified components, steps, features, functions, or the like.

- 3 -

It will be readily understood that the components of the embodiments as generally described herein and illustrated in the drawing could be arranged and designed in a wide variety of different configurations. Thus, the following description of various embodiments is not intended to limit the scope of the present disclosure, but is merely representative of
5 various embodiments. While the various aspects of the embodiments may be presented in drawings, the drawings are not necessarily drawn to scale unless specifically indicated.

Furthermore, specific implementations shown and described are only examples and should not be construed as the only way to implement the present disclosure unless specified otherwise herein. Elements, circuits, and functions may be shown in block diagram form in
10 order not to obscure the present disclosure in unnecessary detail. Conversely, specific implementations shown and described are exemplary only and should not be construed as the only way to implement the present disclosure unless specified otherwise herein. Additionally, block definitions and partitioning of logic between various blocks is exemplary of a specific implementation. It will be readily apparent to one of ordinary skill
15 in the art that the present disclosure may be practiced by numerous other partitioning solutions. For the most part, details concerning timing considerations and the like have been omitted where such details are not necessary to obtain a complete understanding of the present disclosure and are within the abilities of persons of ordinary skill in the relevant art.

Those of ordinary skill in the art would understand that information and signals may
20 be represented using any of a variety of different technologies and techniques. Some drawings may illustrate signals as a single signal for clarity of presentation and description. It will be understood by a person of ordinary skill in the art that the signal may represent a bus of signals, wherein the bus may have a variety of bit widths and the present disclosure may be implemented on any number of data signals including a single data signal.

25 The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein may be implemented or performed with a general purpose processor, a special purpose processor, a Digital Signal Processor (DSP), an Integrated Circuit (IC), an Application Specific Integrated Circuit (ASIC), a Field Programmable Gate Array (FPGA) or other programmable logic device, discrete gate or
30 transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general-purpose processor (may also be referred to herein as a host processor or simply a host) may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or

- 4 -

state machine. A processor may also be implemented as a combination of computing devices, such as a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. A general-purpose computer including a processor is considered a
5 special-purpose computer while the general-purpose computer is configured to execute computing instructions (e.g., software code) related to embodiments of the present disclosure.

The embodiments may be described in terms of a process that is depicted as a flowchart, a flow diagram, a structure diagram, or a block diagram. Although a flowchart
10 may describe operational acts as a sequential process, many of these acts can be performed in another sequence, in parallel, or substantially concurrently. In addition, the order of the acts may be re-arranged. A process may correspond to a method, a thread, a function, a procedure, a subroutine, a subprogram, etc. Furthermore, the methods disclosed herein may be implemented in hardware, software, or both. If implemented in software, the functions
15 may be stored or transmitted as one or more instructions or code on computer-readable media. Computer-readable media includes both computer storage media and communication media including any medium that facilitates transfer of a computer program from one place to another.

Any reference to an element herein using a designation such as “first,” “second,” and
20 so forth does not limit the quantity or order of those elements, unless such limitation is explicitly stated. Rather, these designations may be used herein as a convenient method of distinguishing between two or more elements or instances of an element. Thus, a reference to first and second elements does not mean that only two elements may be employed there or that the first element must precede the second element in some manner. In addition, unless
25 stated otherwise, a set of elements may comprise one or more elements.

As used herein, the term “substantially” in reference to a given parameter, property, or condition means and includes to a degree that one of ordinary skill in the art would understand that the given parameter, property, or condition is met with a small degree of variance, such as, for example, within acceptable manufacturing tolerances. By way of
30 example, depending on the particular parameter, property, or condition that is substantially met, the parameter, property, or condition may be at least 90% met, at least 95% met, or even at least 99% met.

- 5 -

Although a manufacturing process may be the same for a number of devices (e.g., integrated circuits (ICs)), each device may be slightly different due to normal manufacturing variabilities. More specifically, one or more physical properties of the devices may vary from device to device due to the manufacturing process. One or more distinct physical properties of a device (e.g., an IC) that vary from device to device due to the manufacturing process may be considered a physical unclonable function (PUF) of the device (e.g., if it can be used to generate an electrical function reflecting the variation). Because devices may be slightly different, operation of the devices (e.g., outputs generated by the devices) may be different. More specifically, for example, outputs (e.g., output values for a given output) of various comparator ICs may vary based on PUFs of the comparator ICs. For example, some comparators may have relatively large input offsets and some comparators may have relatively small input offsets. Comparators with relatively small offsets may have outputs that change polarity due to, for example, noise and/or offset drift (e.g., due to changes in temperature and/or supply voltages). Comparators with relatively large offsets may be more tolerable to noise and offset drift. In other words, comparators with relatively large offsets may have more stable outputs (e.g., the outputs may not change due to noise and offset drift).

Various embodiments described herein relate to classifying comparators based on comparator offsets, and more specifically, to methods for identifying comparators including suitable offsets (e.g., for reliable key generation). Yet more specifically, some embodiments may relate to sorting and identifying comparators for reliable key generation (e.g., PUF key generation) based on offset values of the comparators, and the use of the identified comparators to generate a reliable key.

To utilize comparators for key generation (e.g., wherein each comparator generates one or more bits for multi-bit key), it may be advantageous that each comparator cell on each integrated circuit be repeatable. Thus, in some embodiments utilizing comparators for key generation, a comparator output should be the same over the lifetime of the comparator and under all operating conditions (e.g., variations in noise, temperature, and/or supply voltage). Accordingly, for key generation, it may be advantageous to utilize comparators with relatively large offsets.

Rather than measuring actual exact offset values of each comparator (e.g., via detecting when a comparator output switches), various embodiments as disclosed herein identify comparators with sufficient offsets via one or more tests. Measuring actual exact

- 6 -

offset values for comparators may not be required. According to some embodiments, during one testing phase (e.g., a first testing phase) a comparator may be tested via strobing the comparator multiple times with the two identical inputs (e.g., two inputs tied together). If a polarity of an output of the comparator does not remain the same for each strobe, it may
5 be determined that an offset of the comparator is too small, and thus the output of the comparator may be affected by noise. In these embodiments, comparators with offsets that are too small may be rejected, and other remaining comparators may be divided into groups (e.g., two groups) depending on comparator outputs (e.g., comparators outputting a positive offset (e.g., an output having a positive polarity) may be in one group (e.g., “group 1”) and
10 comparators outputting a negative offset (e.g., an output having a negative polarity) may be in another group (e.g., “group 2”).

Further, the remaining comparators may be tested. More specifically, during another testing phase (e.g., a second testing phase), each of the remaining comparator may be supplied an external offset voltage. According to some embodiments, the external offset
15 voltage applied to a comparator (i.e., at the inputs of the comparator) may have a known absolute value and a polarity that is opposite of a polarity of the offset of the comparator. For example, if a comparator has positive offset (e.g., in group “1”), a negative external offset voltage may be supplied to the comparator. If a comparator has negative offset (e.g., in group “2”), a positive external offset voltage may be supplied to the comparator. The
20 external offset voltage may be determined based on one or more factors. For example, according to some embodiments, the external offset voltage may be selected based on comparator noise, offset drift with temperature, supply voltage, and/or time. More specifically, for example, the sum of these parameters may be used to determine the external test voltage.

25 In some embodiments, a comparator may be strobed multiple times with the external offset voltage. If a polarity of the comparator output does not remain the same as before, or does not remain the same for each strobe, the comparator may be rejected. Otherwise, comparators having outputs that remain the same as before and for each strobe, may be identified as reliable comparators and may be used as PUF comparator cells (e.g., in key
30 generation).

In some embodiments, an absolute value of an offset of the remaining comparators may be equal to or greater than the predefined external offset voltage. Further, in some embodiments, if the comparator noise and offset drift (e.g., with temperature, supply voltage

- 7 -

and time) may be determined empirically, the sum of these parameters may be used as the external test voltage for comparator sorting, which may ensure the comparator repeatability.

According to various embodiments, one or more testing phases may be used to classify a comparator. For example, in some embodiments, a comparator may be classified
5 as either reliable or unreliable based either the first testing phase (e.g., wherein inputs of the comparator receive the same signal (e.g., the inputs are tied together) or a second testing phase (e.g., wherein inputs of the comparator receive an offset voltage). In other embodiments, a comparator may be classified as either reliable or unreliable based on more than one testing phase (e.g., the first testing phase and the second testing phase).

10 Various embodiments disclosed herein may improve comparator classification. Further, comparators with relatively high repeatability may be used in generating a reliable bit in key generation, thus improving key generation (e.g., for encryption and decryption). For at least these reasons, various embodiments of the present disclosure, as described more fully herein, provide a technical solution to one or more problems that arise from technology
15 that could not reasonably be performed by a person, and various embodiments disclosed herein are rooted in computer technology in order to overcome the problems and/or challenges described above. Further, at least some embodiments disclosed herein may improve computer-related technology by allowing computer performance of a function not previously performable by a computer.

20 Various embodiments of the present disclosure are now explained with reference to the accompanying drawings.

FIG. 1 depicts an example comparator circuit 100, according to one or more embodiments of the disclosure. Comparator circuit 100 includes differential inputs Inp and Inn, a plurality of switches (e.g., transistors M1-M8), cross coupled NAND gates configured
25 as an SR flip-flop, and an output Out. During a contemplated operation, an output signal generated at output Out may be based on a signal received an input Inp and a signal received an input Inn. As will be appreciated by a person having ordinary skill in the art, noise, offset, and/or offset drift may impact the output signal. According to various embodiments, depending on a testing phase, input Inp and input Inn may or may not be configured to
30 receive the same input. More specifically, in one testing phase, input Inp and input Inn may receive the same input (e.g., input Inp and input Inn may be tied together). In another testing phase, input Inp and input Inn may be configured to receive a different signal (e.g., an offset voltage may be applied to the inputs). Comparator circuit 100 is provided as an

- 8 -

example comparator circuit, and the disclosure is not limited to any particular comparator circuit.

FIG. 2 is a plot 200 including an area 202 (i.e., to the right of the Y axis; labeled as “1”) and an area 204 (i.e., to the left of the Y axis; labeled as “0”). According to some
5 embodiments, comparators having a positive input offset may be represented to the right of the Y axis (e.g., in area 202) and comparators having a negative input offset may be represented to the left of the Y axis (e.g., in area 204). Further, the larger the offset of a comparator, the farther the offset may be from the Y axis. For example, the offset of a comparator having an offset of 2x may be farther away from the Y axis than for a comparator
10 having an offset of 1x. Comparators having an offset positioned between dashed lines 206 and 208 have a relatively low offset, and therefore the outputs of these comparators may be susceptible to noise and/or offset drift.

As noted above, according to some embodiments, a comparator may be tested via strobing the comparator multiple times with identical inputs (e.g., two inputs of the
15 comparator are tied together). Stated another way, with reference again to FIG. 1, a number of strobe pulses may be applied to a gate of M5 gate, while an input (e.g., a voltage) may be applied to each of input Inp and input Inn. If a polarity of an output of the comparator does not remain the same for each strobe, it may be determined that an offset of the comparator is too small (e.g., the output is between dashed lines 206 and 208) and thus, the output of the
20 comparator may be affected by noise or other phenomena causing an offset drift. It is noted that, in at least some embodiments, the strobing and the output signal values may happen in sequence. In other words, an output signal value is generated in response to each input strobe.

In these embodiments, comparators with offsets that are too small may be rejected
25 (e.g., as unreliable), and other remaining comparators may be divided into groups (e.g., two groups) depending on comparator outputs. For example, comparators outputting a positive offset may be in one group (e.g., “group 1”) and comparators outputting a negative offset may be in another group (e.g., “group 2”).

Moreover, the remaining comparators (e.g., the comparators in groups 1 and 2) may
30 be further tested. More specifically, each of the remaining comparator may be supplied an external offset voltage. The external offset voltage applied to a comparator (i.e., at its inputs) may have a polarity that is opposite of a polarity of the offset of the comparator. For example, if a comparator has positive offset (e.g., in group “1”), a negative external offset

- 9 -

voltage may be supplied to the comparator (e.g., the potential at the input Inp of the comparator is negative in relation to the potential at input Inn of the comparator). If a comparator has negative offset (e.g., in group “2”), a positive external offset voltage may be supplied to the comparator (e.g., the potential at input Inp of the comparator is positive in relation to the potential at input Inn of the comparator). The absolute value of the applied offset voltages may be selected so as to be within a predetermined range appropriate for PUF generation.

In some embodiments, each comparator may be strobed multiple times with the external offset voltage. Stated another way, with reference again to FIG. 1, a number of strobe pulses may be applied to a gate of transistor M5 gate, while the external voltage may be applied to inputs Inp/Inn. If an output of the comparator changes polarity (e.g., a comparator in group 1 is applied a negative offset or a comparator in group 2 is applied a positive offset), an amplitude of the offset of the comparator is likely less than an amplitude of the external offset voltage, and thus the offset of the comparator is likely too small and the comparator may be rejected (e.g., as unreliable). Stated another way, if a polarity of the comparator output does not remain the same as before (e.g., as determined via the prior test) or does not remain the same for each strobe, the comparator may be rejected. Otherwise, comparators having outputs that remain the same polarity for each strobe may be identified as reliable comparators (e.g., having suitable offsets for reliable key generation). According to some embodiments, reliable comparators may be used as PUF comparator cells (e.g., in key generation).

With reference to FIG. 3, which depicts a plot 300, a polarity of an output of a comparator having an input offset positioned between lines 310 and 312 (e.g., at either point A or point B), after an external offset voltage is applied to the comparator inputs, may not remain the same as before (e.g., as determined via the prior test), or may not remain the same for each strobe, and thus the comparator generating that output may be rejected. On the other hand, a polarity of an output to the left of line 312 (region 304) or to the right of line 310 (region 302, e.g., at point C) may remain the same as before and for each strobe, and thus, the comparator generating that output may be identified as a reliable comparator (e.g., that may be used as a comparator cell in key generation).

FIG. 4 is a flowchart of an example method 400 of identifying a comparator with a suitable offset for key generation. Method 400 may be arranged in accordance with at least one embodiment described in the present disclosure. Method 400 may be performed, in

- 10 -

some embodiments, by a device or system, such as a circuit 100 (see FIG. 1), circuit 500 (see FIG. 5), circuit 600 (see FIG. 6), system 800 (see FIG. 8), one or more of the components thereof, or another system or device. In these and other embodiments, method 400 may be performed based on the execution of instructions stored on one or more non-transitory
5 computer-readable media. Although illustrated as discrete blocks, various blocks may be divided into additional blocks, combined into fewer blocks, or eliminated, depending on the desired implementation.

Method 400 may begin at block 402, wherein a first voltage may be applied to each of a first input and a second input of a comparator (e.g., via strobing a number of times) to
10 generate a number of output signals from the comparator, and method 400 may proceed to block 404. For example, each output signal may have a one of a first polarity (e.g., a positive offset) and a second polarity (e.g., a negative offset).

At block 404, in response to each of the number of output signals being the first polarity, an external offset voltage may be applied to the comparator (e.g., via strobing a
15 number of times) to generate a second number of output signals from the comparator, and method 400 may proceed to block 406. For example, the first voltage may be applied to the first input and a second voltage may be applied to the second input (e.g., a number of times) to generate the second number of output signals from the comparator, wherein a difference between the first voltage and the second voltage may be equal to the external offset voltage
20 having the second polarity.

At block 406, in response to each of the second number of output signals being the same polarity, the comparator may be identified as a reliable comparator.

Modifications, additions, or omissions may be made to method 400 without departing from the scope of the present disclosure. For example, the operations of
25 method 400 may be implemented in differing order. Furthermore, the outlined operations and actions are only provided as examples, and some of the operations and actions may be optional, combined into fewer operations and actions, or expanded into additional operations and actions without detracting from the essence of the disclosed embodiment. For example, a reliable comparator may be used for generating a key, which may be used for data
30 encryption and/or data decryption. More specifically, the reliable comparator may be used as a cell for generating one or more bits of a multi-bit key, as described further below.

FIG. 5 depicts an example circuit 500 for generating an external offset voltage. Circuit 500, which may also be referred to as a “resistor string,” may include a number of

- 11 -

switches (e.g., transistors M10-M13), a number of resistors R1-R3, and outputs out1 and out2. In some embodiments, outputs out1 and out2 may be coupled to inputs of a comparator (e.g., comparator 100 of FIG. 1). For example, output out1 may be coupled to a one input of a comparator, and output out2 may be coupled to another input of the comparator.

5 Further, depending on a configuration of transistors M10-M13, outputs out1 and out2 may or may not be coupled together. Thus, according to at least some embodiments, transistors M10-M13 be configured such that outputs out1 and out2 may be coupled together during one phase of a comparator testing process (e.g., by turning on both transistors M10 and M12, or both transistor M11 and M13), as described herein. In this example, outputs out1 and
10 out2 may output a first voltage (e.g., to be supplied both inputs of a comparator). Further, transistors M10-M13 be configured such that outputs out1 and out2 are not coupled together during another phase of the comparator testing process, as also described herein (e.g., by turning on transistors M10 and M13 while setting transistor M11 and M12 to off or by turning on transistors M11 and M12 while setting transistor M10 and M13 to off). In this example,
15 outputs out1 may output the first voltage (e.g., to be supplied to one input of a comparator), and out2 may output a second voltage (e.g., to be supplied to another input of the comparator). Circuit 500 is provided as an example of a circuit for generating an external offset voltage, and other circuits for generating an offset voltage are within the scope of the present disclosure. According to various embodiments, controller 510 may be configured for controlling a
20 configuration of transistors M10-M13 (e.g., via one or more control signals).

FIG. 6 illustrates an example system 600 including a comparator 602 (e.g., comparator 100 of FIG. 1), a resistor string 604 (e.g., circuit 500 of FIG. 5), and a controller 610 (e.g., controller 510 of FIG. 5), according to one or more embodiments of the disclosure. As depicted, outputs of resistor string 604 are coupled to inputs of comparator 602. System 600 is
25 provided as an example system including a comparator and a resistor string, and other systems and/or devices including a resistor string coupled to a comparator are within the scope of the present disclosure.

FIG. 7 depicts an example system 700, in accordance with various embodiments of the present disclosure. System 700, which may be configured to encrypt and decrypt data (e.g., a
30 secret), includes an encryption module 702, a key generation module 704, and a decryption module 706. For example, key generation module 704 may include one or more comparators for generating a key, which may be used to encrypt and/or decrypt data. More specifically, each comparator of key generation module 704 may be configured to generate one or more bits

- 12 -

of a multi-bit key. Further, the one or more comparators of key generation module 704 may be identified as reliable comparators, in accordance with one or more embodiments disclosed herein.

FIG. 8 illustrates an example system 800, according to at least one embodiment described herein. System 800 may include any suitable system, apparatus, or device configured for classifying comparators. System 800 may include a processor 810, a memory 820, a data storage 830, and a communication device 840, which all may be communicatively coupled. Data storage 830 may include various types of data, such as offset polarities for one or more comparators, testing information (e.g., related to one or more comparators), reliability information (e.g., related to one or more comparators), or any other information related to classifying comparators based on comparator offsets.

Generally, processor 810 may include any suitable special-purpose or general-purpose computer, computing entity, or processing device including various computer hardware or software modules and may be configured to execute instructions stored on any applicable computer-readable storage media. For example, processor 810 may include a microprocessor, a microcontroller, a digital signal processor (DSP), an application-specific integrated circuit (ASIC), a Field-Programmable Gate Array (FPGA), or any other digital or analog circuitry configured to interpret and/or to execute program instructions and/or to process data.

Although illustrated as a single processor in FIG. 8, it is understood that processor 810 may include any number of processors distributed across any number of network or physical locations that are configured to perform individually or collectively any number of operations described herein. In some embodiments, processor 810 may interpret and/or execute program instructions and/or process data stored in memory 820, data storage 830, or memory 820 and data storage 830. In some embodiments, processor 810 may fetch program instructions from data storage 830 and load the program instructions into memory 820. In one embodiment instructions executing method 400 may be stored in memory 820 and executed by processor 810.

After the program instructions are loaded into memory 820, processor 810 may execute the program instructions, such as instructions to perform one or more blocks of method 200 and/or method 300 as described herein. According to various embodiments, processor 810 may perform one or more testing operations. For example, processor 810 may apply a first voltage to each input of a comparator, and process a first output generated by the comparator. Further, processor 810 may identify the comparator as an unreliable comparator based on the

- 13 -

first output. Moreover, processor 810 may apply an offset voltage to the comparator, and process a second output generated by the comparator. Moreover, based on the second output, processor 810 may identify the comparator as either a reliable comparator or an unreliable comparator.

5 Memory 820 and data storage 830 may include computer-readable storage media or one or more computer-readable storage mediums for carrying or having computer-executable instructions or data structures stored thereon. Such computer-readable storage media may be any available media that may be accessed by a general-purpose or special-purpose computer, such as processor 810.

10 By way of example, and not limitation, such computer-readable storage media may include non-transitory computer-readable storage media including Random Access Memory (RAM), Read-Only Memory (ROM), Electrically Erasable Programmable Read-Only Memory (EEPROM), Compact Disc Read-Only Memory (CD-ROM) or other optical disk storage, magnetic disk storage or other magnetic storage devices, flash memory devices (e.g., solid state
15 memory devices), or any other storage medium which may be used to carry or store desired program code in the form of computer-executable instructions or data structures and which may be accessed by a general-purpose or special-purpose computer. Combinations of the above may also be included within the scope of computer-readable storage media. Computer-executable instructions may include, for example, instructions and data configured
20 to cause processor 810 to perform a certain operation or group of operations.

 Communication unit 840 may include any component, device, system, or combination thereof that is configured to transmit or receive information over a network. In some embodiments, communication unit 840 may communicate with other devices at other locations, the same location, or even other components within the same system. For example,
25 communication unit 840 may include a modem, a network card (wireless or wired), an infrared communication device, a wireless communication device (such as an antenna), and/or chipset (such as a Bluetooth device, an 802.6 device (e.g., Metropolitan Area Network (MAN)), a WiFi device, a WiMax device, cellular communication facilities, etc.), and/or the like. Communication unit 840 may permit data to be exchanged with a network and/or any other
30 devices or systems described in the present disclosure. For example, communication unit 840 may allow system 800 to communicate with other systems and/or devices.

 Modifications, additions, or omissions may be made to system 800 without departing from the scope of the present disclosure. For example, data storage 830 may be multiple

- 14 -

different storage mediums located in multiple locations and accessed by processor 810 through a network.

As indicated above, the embodiments described herein may include the use of a special purpose or general purpose computer (e.g., processor 810 of FIG. 8) including various computer hardware or software modules, as discussed in greater detail below. Further, as indicated above, embodiments described herein may be implemented using computer-readable media (e.g., memory 820 or data storage 830 of FIG. 8) for carrying or having computer-executable instructions or data structures stored thereon.

Various embodiments relate to a method of classifying a comparator. For example, a method may include strobing a comparator multiple times with an offset voltage to generate a number of output signals from the comparator. Further, in response to each of the number of output signals having a same polarity, identifying the comparator as a reliable comparator.

According to one or more other embodiments, a method may include applying a first voltage to each of a first input and a second input of a comparator (e.g., via strobing a number of times) to generate a number of output signals from the comparator. Each output signal may include one of a first polarity and a second polarity. Further, the method may include, in response to each of the number of output signals being the first polarity, applying an offset voltage having the second polarity to the comparator (e.g., via strobing a number of times) to generate a second number of output signals. Furthermore, the method may include, response to each of the second number of output signals having the same polarity, identifying the comparator as a reliable comparator.

In yet one or more other embodiments, a method may include, for each comparator of a number of comparators, strobing a comparator with a first voltage at each of a first input and a second input of the comparator to generate a number of output signals from the comparator, each output signal having one of a first polarity and a second polarity. In addition, the method may include, in response to each output signal of the number of output signal having the first polarity, strobing the comparator with an external offset voltage having the second polarity to generate a second number of output signals from the comparator. Further, the method may include, in response to each output signal of the second number of output signals having the first polarity, identifying the comparator as a reliable comparator. The method may also include generating a key via a number of reliable comparators.

As used in the present disclosure, the terms “module” or “component” may refer to specific hardware implementations configured to perform the actions of the module or

- 15 -

component and/or software objects or software routines that may be stored on and/or executed by general purpose hardware (e.g., computer-readable media, processing devices, etc.) of the computing system. In some embodiments, the different components, modules, engines, and services described in the present disclosure may be implemented as objects or processes that execute on the computing system (e.g., as separate threads). While some of the system and methods described in the present disclosure are generally described as being implemented in software (stored on and/or executed by general purpose hardware), specific hardware implementations or a combination of software and specific hardware implementations are also possible and contemplated.

10 Terms used in the present disclosure and especially in the appended claims (e.g., bodies of the appended claims) are generally intended as “open” terms (e.g., the term “including” should be interpreted as “including, but not limited to,” the term “having” should be interpreted as “having at least,” the term “includes” should be interpreted as “includes, but is not limited to,” etc.).

15 Additionally, if a specific number of an introduced claim recitation is intended, such an intent will be explicitly recited in the claim, and in the absence of such recitation no such intent is present. For example, as an aid to understanding, the following appended claims may contain usage of the introductory phrases “at least one” and “one or more” to introduce claim recitations. However, the use of such phrases should not be construed to imply that the introduction of a claim recitation by the indefinite articles “a” or “an” limits any particular claim containing such introduced claim recitation to embodiments containing only one such recitation, even when the same claim includes the introductory phrases “one or more” or “at least one” and indefinite articles such as “a” or “an” (e.g., “a” and/or “an” should be interpreted to mean “at least one” or “one or more”); the same holds true for the use of definite articles used to introduce claim recitations.

25 In addition, even if a specific number of an introduced claim recitation is explicitly recited, those skilled in the art will recognize that such recitation should be interpreted to mean at least the recited number (e.g., the bare recitation of “two recitations,” without other modifiers, means at least two recitations, or two or more recitations). Furthermore, in those instances where a convention analogous to “at least one of A, B, and C, etc.” or “one or more of A, B, and C, etc.” is used, in general such a construction is intended to include A alone, B alone, C alone, A and B together, A and C together, B and C together, or A, B, and C together, etc.

- 16 -

Further, any disjunctive word or phrase presenting two or more alternative terms, whether in the description, claims, or drawings, should be understood to contemplate the possibilities of including one of the terms, either of the terms, or both terms. For example, the phrase “A or B” should be understood to include the possibilities of “A” or “B” or “A and B.”

5 While the present disclosure has been described herein with respect to certain illustrated embodiments, those of ordinary skill in the art will recognize and appreciate that the present invention is not so limited. Rather, many additions, deletions, and modifications to the illustrated and described embodiments may be made without departing from the scope of the invention as hereinafter claimed along with their legal equivalents. In addition,
10 features from one embodiment may be combined with features of another embodiment while still being encompassed within the scope of the invention as contemplated by the inventor.

- 17 -

CLAIMS

What is claimed is:

- 5 1. A method, comprising;
strobing a comparator multiple times with an external offset voltage to generate a number of
output signals from the comparator; and
in response to each of the number of output signals having a same polarity, identifying the
comparator as a reliable comparator.
- 10 2. The method of claim 1, further comprising in response to each of the number
of output signals not being the same polarity, identifying the comparator as an unreliable
comparator.
- 15 3. The method of claim 1, further comprising strobing the comparator with an
input voltage at each of a first input and a second input of the comparator to generate another
number of output signals from the comparator.
- 20 4. The method of claim 3, wherein the strobing of the comparator with the
external offset voltage comprises strobing, in response to the generated another number of
output signals all having the same polarity, the comparator with the external offset voltage,
wherein the external offset voltage has a polarity opposite a polarity of the another number of
output signals.
- 25 5. The method of claim 1, further comprising generating a key via the reliable
comparator.
- 30 6. The method of claim 5, wherein generating the key comprises generating at
least one bit of the key via the reliable comparator.
7. The method of claim 5, further comprising at least one of encrypting and
decrypting data with the key.

- 18 -

8. A method, comprising:
applying, via a strobe, a first voltage to each of a first input and a second input of a
comparator to generate a number of output signals from the comparator, each output
5 signal having one of a first polarity and a second polarity;
in response to each of the number of output signals being the first polarity, applying, via a
strobe, an external offset voltage having the second polarity to the comparator to
generate a second number of output signals; and
in response to each of the second number of output signals having the same polarity,
10 identifying the comparator as a reliable comparator.

9. The method of claim 8, wherein applying the external offset voltage
comprises applying the first voltage to the first input and a second voltage to the second input
of the comparator to generate the second number of output signals from the comparator, a
15 difference between the first voltage and the second voltage comprising a voltage equal to the
external offset voltage.

10. The method of claim 9, further comprising generating each of the first voltage
and the second voltage via a voltage generation circuit including a number of switches, a
20 number of resistors, and a number of outputs.

11. The method of claim 8, further comprising at least one of encrypting and
decrypting data with the reliable comparator.

25 12. The method of claim 8, further comprising generating the first voltage via a
resistor string.

13. The method of claim 12, further comprising generating the external offset
voltage via the resistor string.

30

14. The method of claim 12, wherein generating the external offset voltage
comprises generating a second voltage via the resistor string, a difference between the first
voltage and the second voltage comprising the external offset voltage.

- 19 -

15. The method of claim 14, wherein applying the external offset voltage to the comparator comprises applying the first voltage to the first input of the comparator and the second voltage to the second input of the comparator.

5

16. A method, the method comprising:
for each comparator of a number of comparators:

10 strobing a comparator with a first voltage at each of a first input and a second input of the comparator to generate a number of output signals from the comparator, each output signal having one of a first polarity and a second polarity;

in response to each output signal of the number of output signal having the first polarity, strobing the comparator with an external offset voltage having the second polarity to generate a second number of output signals from the comparator; and

15 in response to each output signal of the second number of output signals having the first polarity, identifying the comparator as a reliable comparator; and
generating a key via a number of reliable comparators.

17. The method of claim 16, wherein generating the key comprises generating the
20 key including a number of bits, each bit of the number of bits generated via a comparator of the number of reliable comparators.

18. The method of claim 16, further comprising at least one of encrypting data
and decrypting the data with the key.

25

- 20 -

19. A method, comprising:
- applying a first voltage to each of a first input and a second input of a comparator a number of times to generate a first number of output signals from the comparator;
- in response to the first number of output signals being either all positive values or all negative values, applying the first voltage to the first input and a second voltage to the second input a number of times to generate a second number of output signals from the comparator, a difference between the first voltage and the second voltage comprising an external offset voltage, the external offset voltage having a negative value if each of the first number of output signals have a positive value, and the external offset voltage having a positive value if each of the first number of output signals have a negative value; and
- in response to each of the second number of output signals being either all positive values or all negative values, identifying the comparator as a reliable comparator.
20. The method of claim 19, further comprising generating, via the reliable comparator, one or more bits of a multi-bit encryption key.

AMENDED CLAIMS**received by the International Bureau on 07 April 2020 (07.04.2020)**

- 5 1. (Currently Amended) A method, comprising;
strobing a comparator with an input voltage at each of a first input and a second input of the
comparator to generate a number of output signals from the comparator;
in response to the generated number of output signals all having the same polarity, strobing
the comparator multiple times with an external offset voltage to generate another
10 number of output signals from the comparator; and
in response to each of the another number of output signals having a same polarity,
identifying the comparator as a reliable comparator.
2. The method of claim 1, further comprising in response to each of the number
15 of output signals not being the same polarity, identifying the comparator as an unreliable
comparator.
3. (Canceled)
- 20 4. (Currently Amended) The method of claim 1, wherein the external offset
voltage has a polarity opposite a polarity of the another number of output signals.
5. (Original) The method of claim 1, further comprising generating a key via the
reliable comparator.
25
6. (Original) The method of claim 5, wherein generating the key comprises
generating at least one bit of the key via the reliable comparator.
7. (Original) The method of claim 5, further comprising at least one of
30 encrypting and decrypting data with the key.

8. (Original) A method, comprising:
applying, via a strobe, a first voltage to each of a first input and a second input of a
comparator to generate a number of output signals from the comparator, each output
signal having one of a first polarity and a second polarity;
5 in response to each of the number of output signals being the first polarity, applying, via a
strobe, an external offset voltage having the second polarity to the comparator to
generate a second number of output signals; and
in response to each of the second number of output signals having the same polarity,
identifying the comparator as a reliable comparator.
10
9. (Original) The method of claim 8, wherein applying the external offset
voltage comprises applying the first voltage to the first input and a second voltage to the
second input of the comparator to generate the second number of output signals from the
comparator, a difference between the first voltage and the second voltage comprising a
15 voltage equal to the external offset voltage.
10. (Original) The method of claim 9, further comprising generating each of the
first voltage and the second voltage via a voltage generation circuit including a number of
switches, a number of resistors, and a number of outputs.
20
11. (Original) The method of claim 8, further comprising at least one of
encrypting and decrypting data with the reliable comparator.
12. (Original) The method of claim 8, further comprising generating the first
25 voltage via a resistor string.
13. (Original) The method of claim 12, further comprising generating the external
offset voltage via the resistor string.
14. (Original) The method of claim 12, wherein generating the external offset
voltage comprises generating a second voltage via the resistor string, a difference between
the first voltage and the second voltage comprising the external offset voltage.
30

15. (Original) The method of claim 14, wherein applying the external offset voltage to the comparator comprises applying the first voltage to the first input of the comparator and the second voltage to the second input of the comparator.

5 16. (Original) A method, the method comprising:

for each comparator of a number of comparators:

strobing a comparator with a first voltage at each of a first input and a second input of the comparator to generate a number of output signals from the comparator, each output signal having one of a first polarity and a second polarity;

10 in response to each output signal of the number of output signal having the first polarity, strobing the comparator with an external offset voltage having the second polarity to generate a second number of output signals from the comparator; and

in response to each output signal of the second number of output signals having the first polarity, identifying the comparator as a reliable comparator; and
15 generating a key via a number of reliable comparators.

17. (Original) The method of claim 16, wherein generating the key comprises generating the key including a number of bits, each bit of the number of bits generated via a
20 comparator of the number of reliable comparators.

18. (Original) The method of claim 16, further comprising at least one of encrypting data and decrypting the data with the key.

19. (Original) A method, comprising:
- applying a first voltage to each of a first input and a second input of a comparator a number of times to generate a first number of output signals from the comparator;
- in response to the first number of output signals being either all positive values or all negative values, applying the first voltage to the first input and a second voltage to the second input a number of times to generate a second number of output signals from the comparator, a difference between the first voltage and the second voltage comprising an external offset voltage, the external offset voltage having a negative value if each of the first number of output signals have a positive value, and the external offset voltage having a positive value if each of the first number of output signals have a negative value; and
- in response to each of the second number of output signals being either all positive values or all negative values, identifying the comparator as a reliable comparator.
20. (Original) The method of claim 19, further comprising generating, via the reliable comparator, one or more bits of a multi-bit encryption key.

STATEMENT UNDER ARTICLE 19(1) (RULE 46.4)

Applicant has submitted an amended claim set under Article 19 of the PCT, in which as-filed claims 1 and 4 are amended. The amendments to the claims are more fully described in the Letter Accompanying Article 19 Amendments, which is also submitted herewith. The amendments have no impact on the description or the drawings.

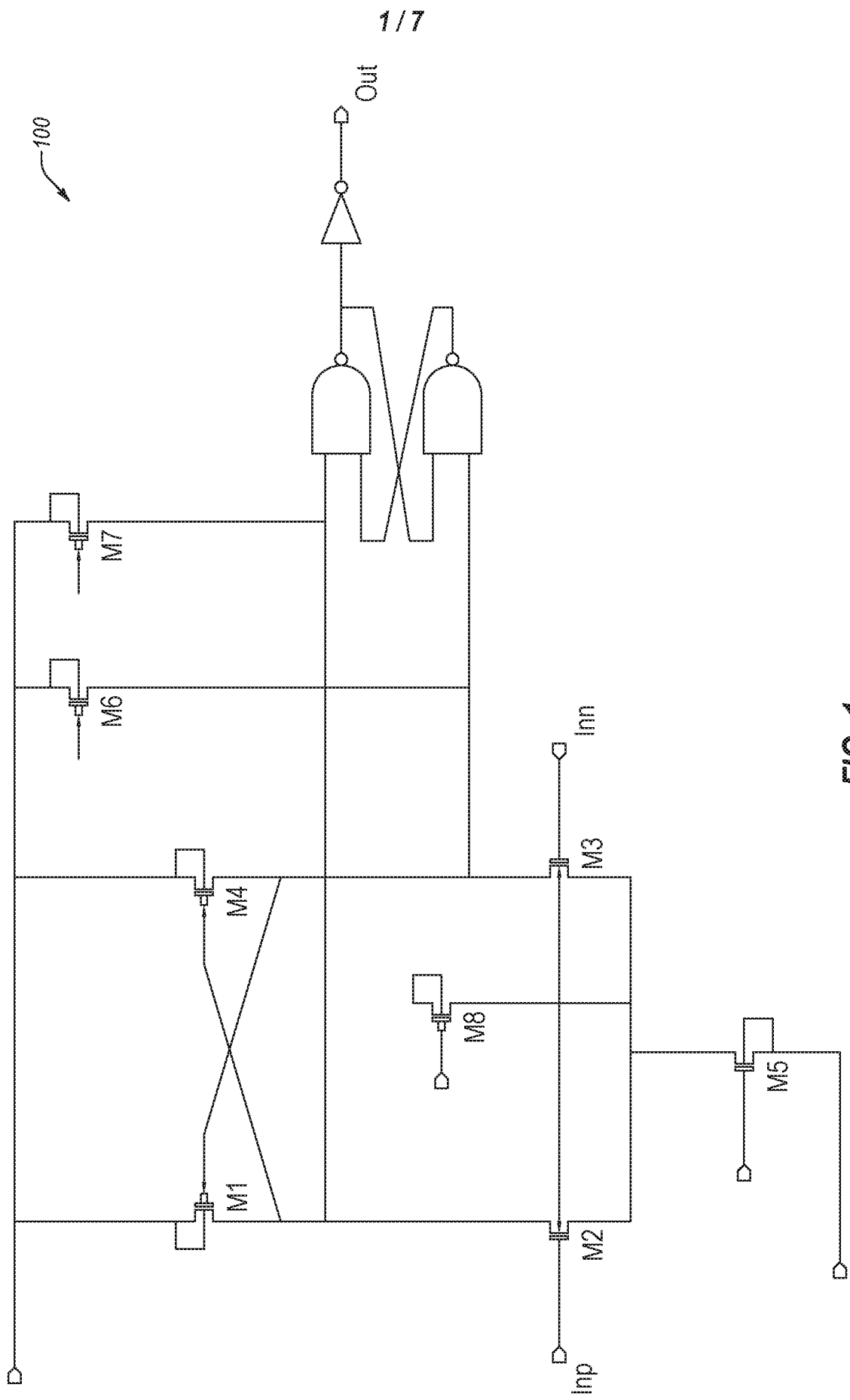


FIG. 1

2 / 7

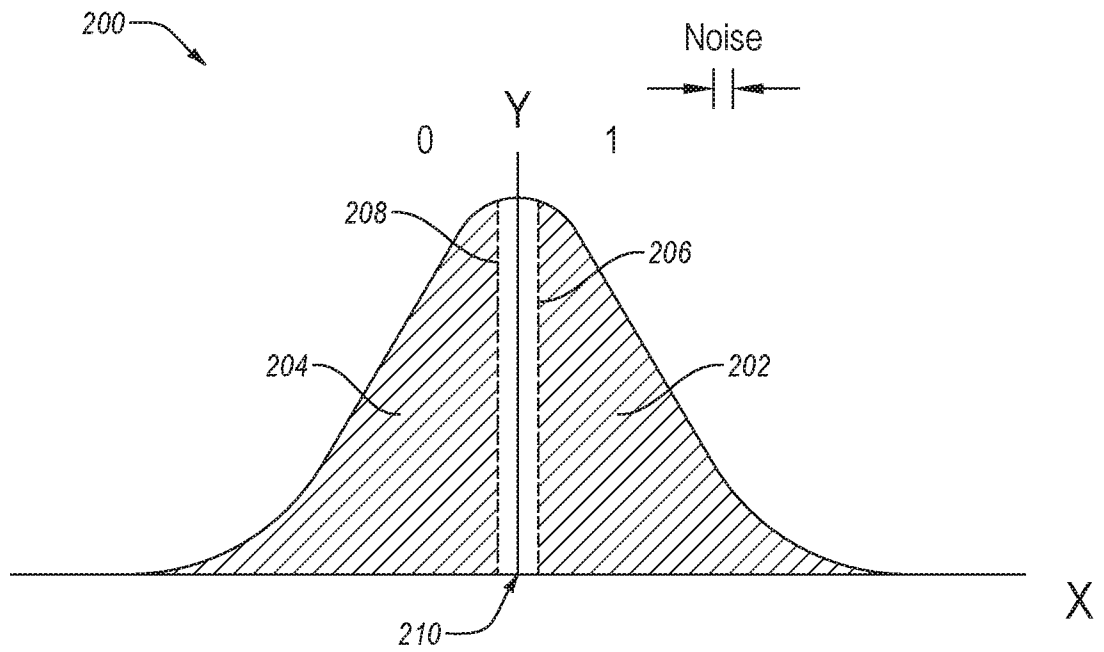


FIG. 2

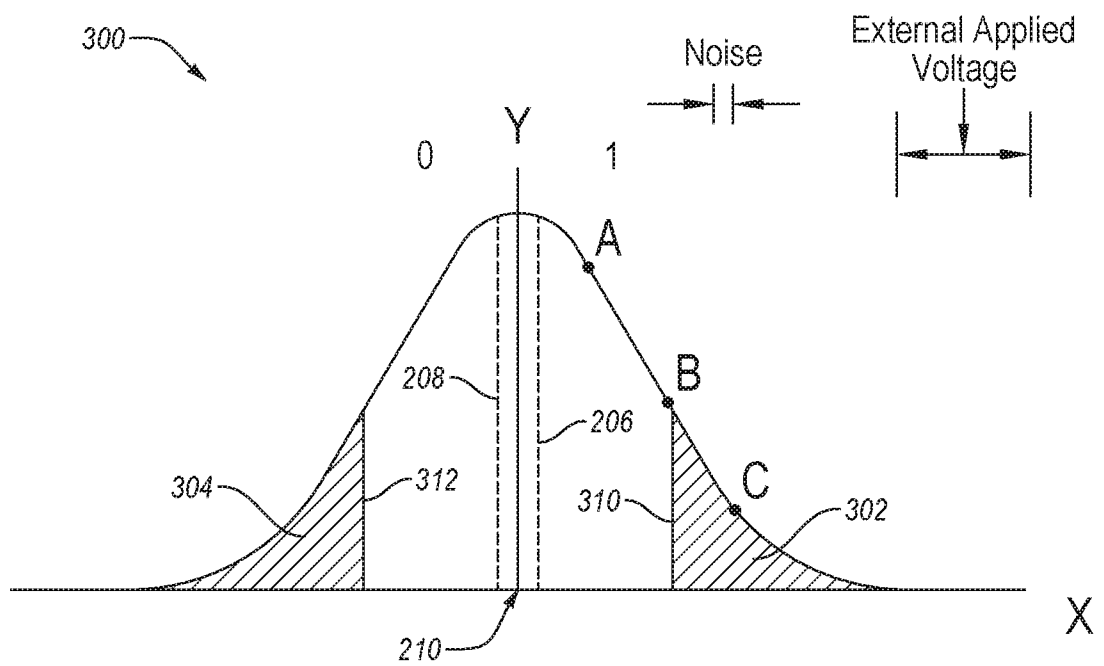
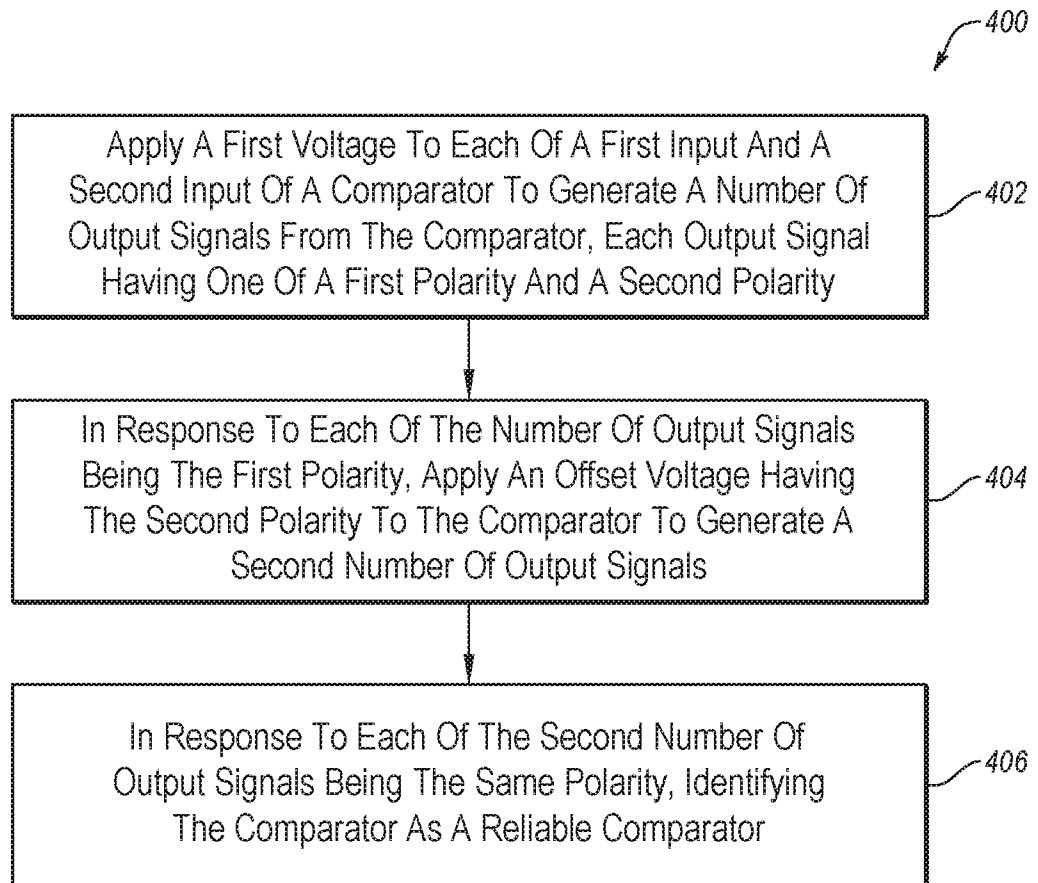
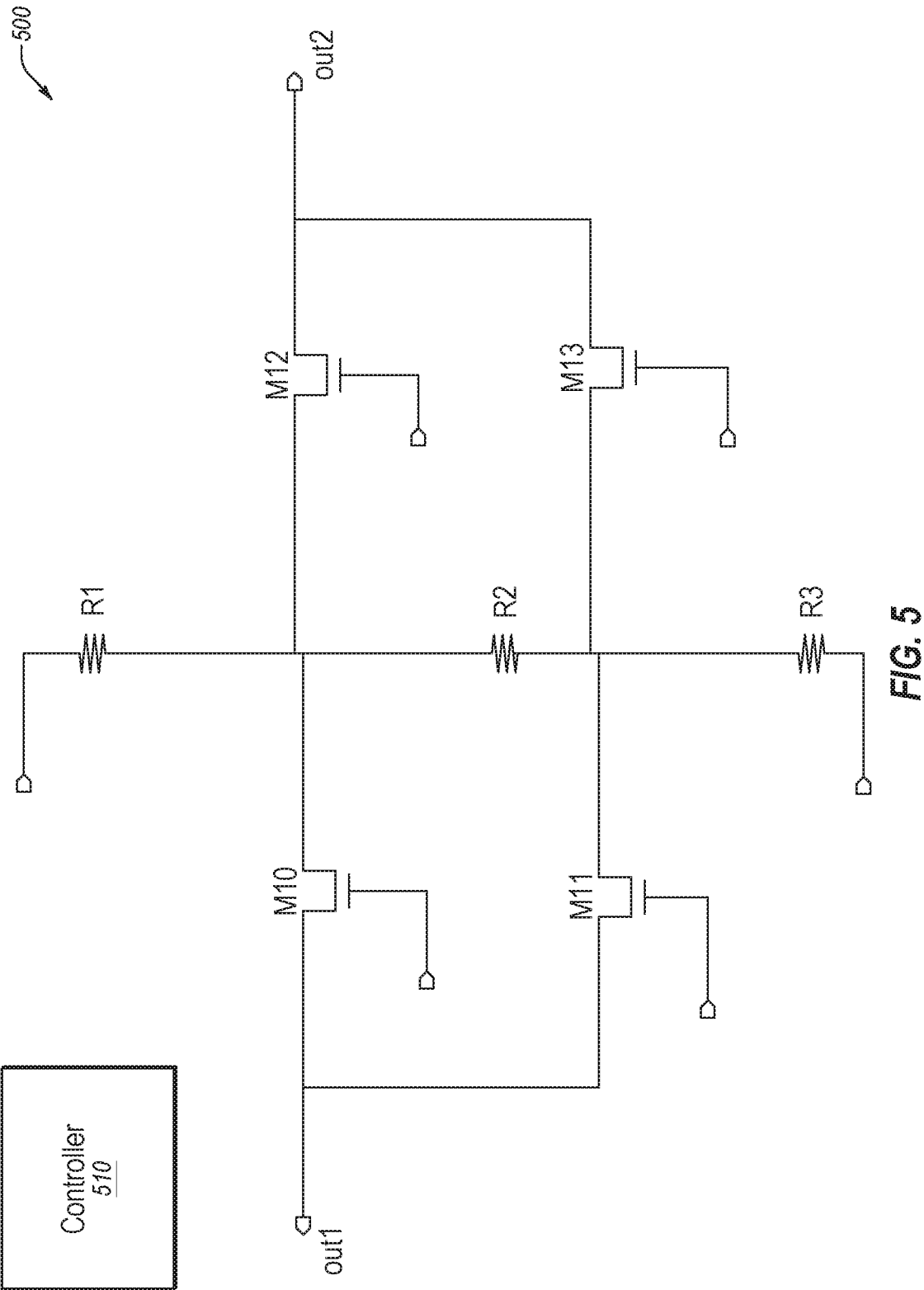


FIG. 3

3 / 7

**FIG. 4**



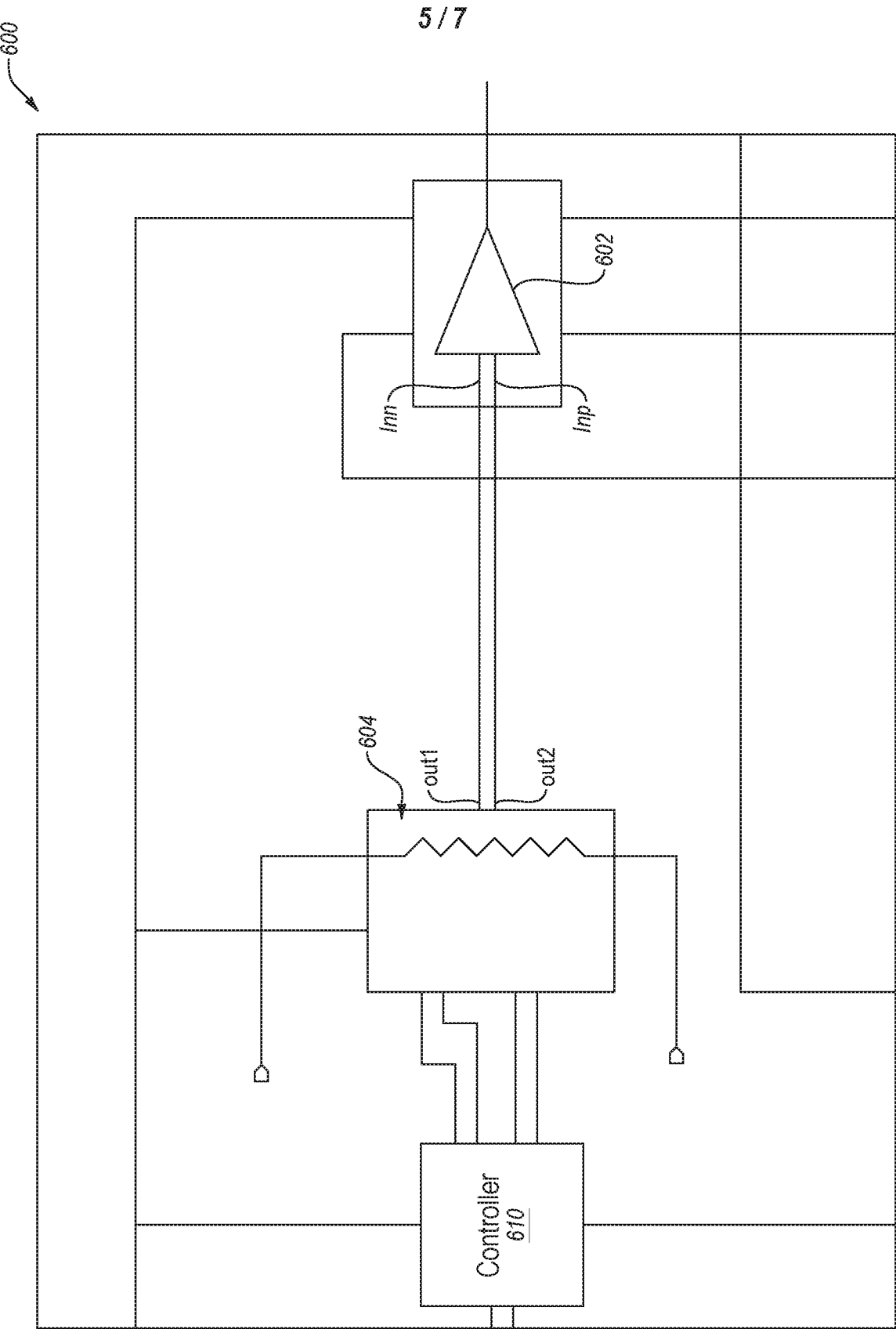


FIG. 6

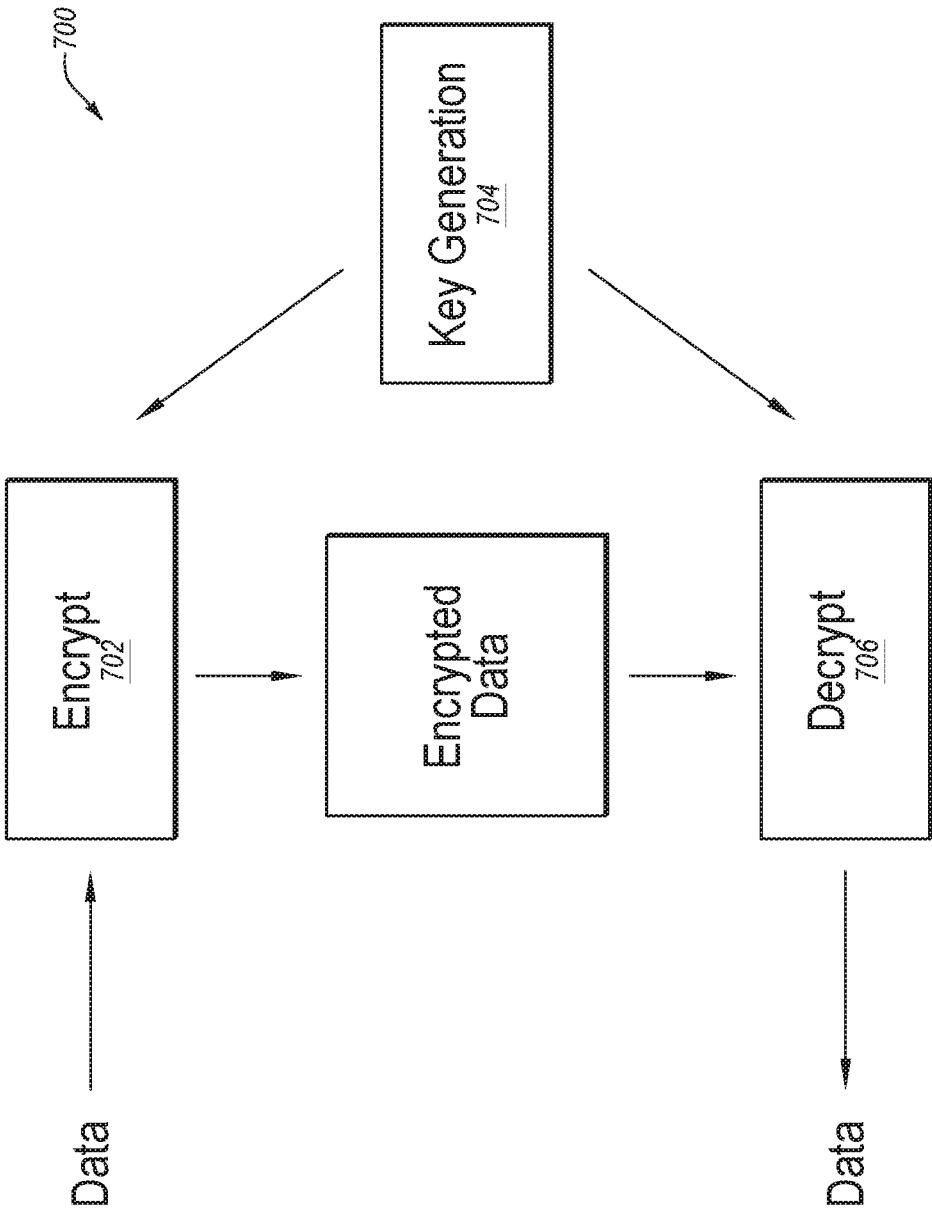


FIG. 7

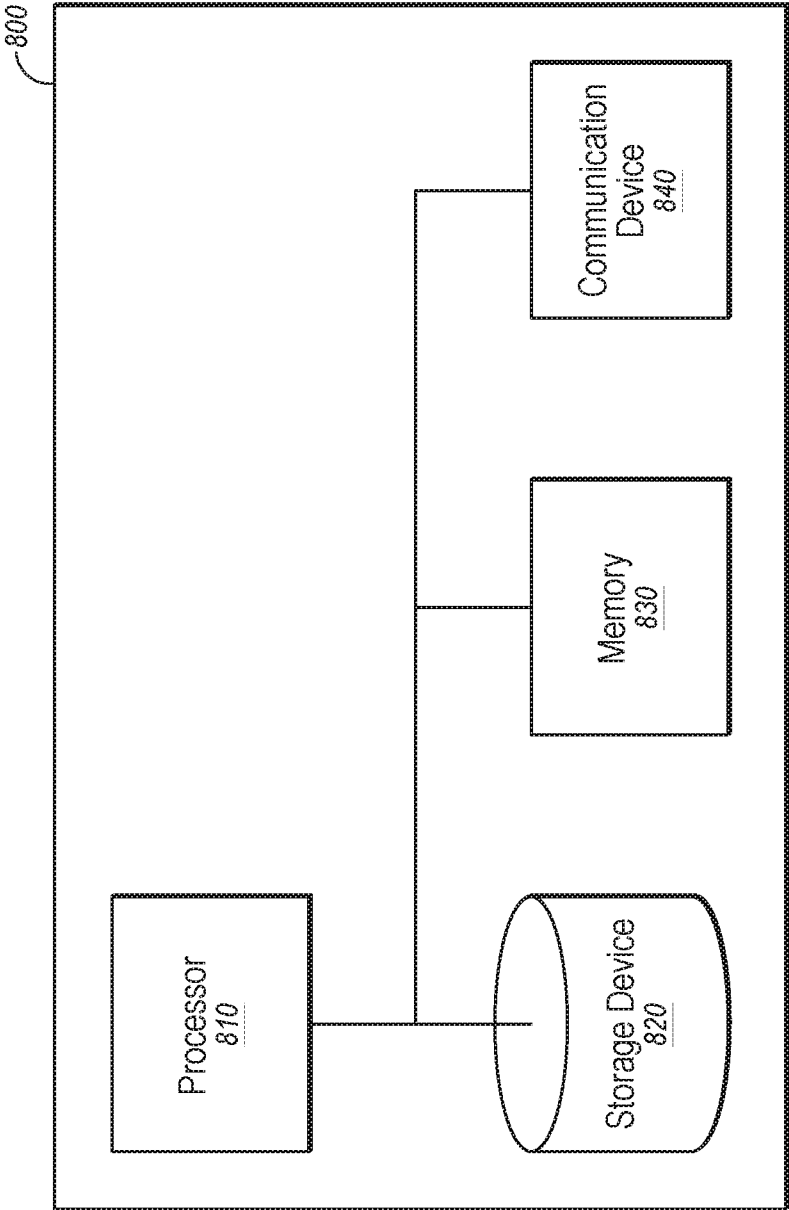


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2019/057960

A. CLASSIFICATION OF SUBJECT MATTER

INV. G01R31/3193 H03K5/24 H04L9/32
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G01R H03K H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2015/148659 A1 (MAI KENNETH WEI-AN [US]) 1 October 2015 (2015-10-01) abstract; figures 1-6 paragraphs [0003], [0004], [0006], [0021], [0024] - [0026], [0028], [0029], [0031], [0032] claims 5,8,13,14,15,21 -----	1-20
X	US 2016/182045 A1 (MAI KENNETH WEI-AN [US] ET AL) 23 June 2016 (2016-06-23) abstract; figures 2,3,4,6 paragraphs [0003], [0004], [0052] - [0056], [0058] - [0060], [0071], [0075], [0076], [0078], [0080] -----	1-9,11, 16-20 10,12-15
Y	US 2013/093467 A1 (KOSIC STEPHEN ROBERT [US] ET AL) 18 April 2013 (2013-04-18) abstract; figure 2 -----	10,12-15
	-/--	



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

28 January 2020

Date of mailing of the international search report

06/02/2020

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Mesic, Maté

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2019/057960

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2012/206281 A1 (BASHIRULLAH RIZWAN [US] ET AL) 16 August 2012 (2012-08-16) abstract; figure 2 paragraphs [0005], [0006], [0015], [0017] -----	1,2 8-10, 12-16,19

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2019/057960

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2015148659 A1	01-10-2015	US 2017180140 A1 WO 2015148659 A1	22-06-2017 01-10-2015
US 2016182045 A1	23-06-2016	US 2016182045 A1 WO 2015027070 A1	23-06-2016 26-02-2015
US 2013093467 A1	18-04-2013	NONE	
US 2012206281 A1	16-08-2012	NONE	