Fig. 1.

DIVIDER OUTPUT

\[ x = \frac{(t - t_0)}{t_1} \] 
DURING FIRST HALF OF "OFF" SEGMENT

\[ x = \frac{(t_2 - t_1)}{t_2} \] 
ON SECOND HALF \((t_2 - t_0)\) OF "OFF" SEGMENT

\[ x = \frac{(t_2 - t_1)}{t_2} \] 
ON "OFF" SEGMENT \((t_2)\) AFTER SEGMENT \((t_1)\)
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FREQUENCY CONVERTING SYSTEM AND METHOD

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2 Sheets—Sheet 2

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Fig. 2.

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FREQUENCY CONVERTING SYSTEM AND METHOD

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The invention relates to a frequency converting system and method, and more particularly to a system and method for converting commutated or continuous information in frequency form to digital and voltage form. Heretofore, apparatus has been provided for converting information in frequency form to digital form. Such apparatus, however, has not provided the performance and accuracy desired for telemetring and other such operations. For example, such equipment has been susceptible to errors caused by drift in the information frequency as well as inaccuracies resulting from wow and flutter when the information is derived from a tape or magnetic record. The converted output signals produced by such prior art apparatus, due to the inherent mode of operation, could only be considered to approximate the desired information.

It is therefore a principal object of the invention to provide a new and improved system and method for converting information in frequency form to digital form.

Another object of the invention is to provide a system and method for converting information in frequency form to voltage form.

Another object of the invention is to provide a new and improved system and method for converting information in frequency form to digital and voltage form.

Another object of the invention is to provide a new and improved system and method for converting commutated information to decommutated form.

Another object of the invention is to provide a new and improved system and method for converting commutated information in frequency form to decommutated information in digital form.

Another object of the invention is to provide a new and improved system and method for converting information from one form to another which is highly accurate allowing modification for the degree of precision required for a particular application.

Another object of the invention is to provide a new and improved frequency converting system and method affording accuracies greater than that now available in existing telemetring and related equipment.

Another object of the invention is to provide a new and improved frequency converting system and method in which each information output reading is independent of the previous information output reading for its accuracy.

Another object of the invention is to provide a new and improved frequency converting system and method delivering normalized output data without restriction to any particular information subcarrier channel.

Another object of the invention is to provide a new and improved frequency converting system and method providing full scale output readings of information irrespective of the particular information channel.

Another object of the invention is to provide a new and improved frequency converting system and method which automatically compensates for frequency drift or variations in the zero percent or hundred percent information signal levels.

Another object of the invention is to provide a new and improved frequency converting system and method furnishing error detecting signals for absence of information signals, and for information output signals outside of the zero to hundred percent information range.

Another object of the invention is to provide a new and improved frequency converting system and method which does not require calibration adjustments.

Another object of the invention is to provide a new and improved frequency converting system and method adapted for obtaining information from a record or otherwise.

Another object of the invention is to provide a new and improved frequency converting system and method compensating for wow and flutter variations which may be produced in an information signal derived from a record or magnetic tape.

Another object of the invention is to provide a new and improved frequency converting system and method having good signal to noise discrimination.

Another object of the invention is to provide a new and improved frequency converting system and method which is operative at very high speeds.

Another object of the invention is to provide a new and improved frequency converting system and method delivering output information in digital form suitable for conversion to voltage form, for actuating printed out equipment, for intermediate storage, or for algebraic interpolation.

Another object of the invention is to provide a new and improved frequency converting system and method particularly well suited for use with existing air-borne transmitting, multiplexing and transmitting equipment as well as magnetic tape transports, and which is compatible with improved and advanced techniques.

Another object of the invention is to provide a new and improved frequency converting system and method adapted for plug-in chassis design.

Another object of the invention is to provide a new and improved frequency converting system and method which minimizes equipment and uses standardized components.

Another object of the invention is to provide a new and improved frequency converting system and method which uses substantially the same equipment for sequential frequency conversion and computation operations.

Another object of the invention is to provide a new and improved frequency converting system and method which is highly reliable and utilizes a minimum number of vacuum tubes.

Another object of the invention is to provide a new and improved frequency converting system and method which is compact and relatively inexpensive to manufacture and maintain in operation.

Another object of the invention is to provide a new and improved frequency converting system and method having simplified circuits which are highly serviceable.

Another object of the invention is to provide a new and improved frequency converting system and method particularly well suited for use with existing air-borne transmitting, multiplexing and transmitting equipment as well as magnetic tape transports, and which is compatible with improved and advanced techniques.

The above objects as well as many other objects of the invention are achieved by providing a frequency converting system for converting a frequency modulated information signal having a frequency $f$ variable within the range between an upper frequency $f_1$ with a period $t_1$ and a lower
frequency $f_2$ with a period $t_2$ which comprises a cycle counting device set to count a predetermined number of cycles of an information signal to determine a control period related to the reciprocal of the frequency $f$ of the information signal.

A first counting unit is adapted for counting clock signals during the control period of the cycle counting device, while a comparison network is provided for delivering an output signal when the first counting unit has a count corresponding to the period $t_1$ of the upper frequency $f_1$.

A second counting unit which counts clock signals concurrently with the first counting unit upon the occurrence of an output signal from the comparator network produces a count directly related to the difference between the period $t$ of the information signal and the period $t_1$ of the upper frequency $f_1$.

An output circuit which is controlled by the count of the first and second counting units delivers a digital output signal representing the quotient of the count of the second unit divided by the count of the first unit. The output signal delivered by the output circuit may be represented by

$$\frac{(t-t_1)/t}{(t_2-t_1)/t_2}$$

where $t_1$ is the period of the frequency $f_2$.

The output circuit by a further operation produces in digital form a normalized information signal which is the quotient of an output signal produced by an information signal having a frequency $f$ divided by the output signal produced by the second reference signal having the frequency $f_2$ which may be represented by

$$\frac{(t-t_1)/t}{(t_2-t_1)/t_2}$$

which is equivalent to

$$\frac{(t-t_1)/t}{(t_2-t_1)/t_2}$$

where

$$t_1 = 1/f$$
$$t_2 = 1/f_2$$

and

$$t_2 = 1/f_2$$

The normalized output information which is delivered in digital form may be readily converted to voltage form by a digital to voltage converter.

The method for converting a frequency modulated information signal having a frequency $f$ variable within the range between an upper limit frequency $f_1$ and a lower limit frequency $f_2$ with a period $t_1$ and a period $t_2$ comprises detecting the information signal and producing a corresponding digital signal represented by

$$\frac{(t-t_1)/t}{(t_2-t_1)/t_2}$$

where $t$ is the period of the information signal. This output signal is then modified by the limit frequencies $f_1$ and $f_2$ forming the divisor represented by

$$\frac{(t_2-t_1)/t_2}{(t_2-t_1)/t_2}$$

producing a normalized digital output signal. The normalized digital output signal may be represented by

$$\frac{(t-t_1)/t}{(t_2-t_1)/t_2}$$

which reduces to

$$\frac{(t-t_1)/t}{(t_2-t_1)/t_2}$$

where

$$t = 1/f$$
$$t_1 = 1/f_1$$

and

$$t_2 = 1/f_2$$

The method of the invention for converting commutated frequency modulated information signals which include data signals each having a frequency $f$ variable within a range between an upper limit frequency $f_1$ with a period $t_1$ and a lower limit frequency $f_2$ with a period $t_2$, and first and second reference signals with respective frequencies $f_1$ and $f_2$ comprises: detecting the first reference signal and producing a first digital reference signal corresponding to the period $t_1$. The first digital reference signal $f_1$ is stored. The second reference signal is detected to produce a second digital reference signal with the utilization of the stored first digital reference signal which may be represented by

$$\frac{(t-t_1)/t}{(t_2-t_1)/t_2}$$

where $t_1$ is the period of the data signal. The digital data signals are modified by the stored second digital reference signal to produce respective normalized digital output data signals represented by

$$\frac{(t-t_1)/t}{(t_2-t_1)/t_2}$$

where $t_1 = 1/f_1$, $t_2 = 1/f_2$, and $t_2 = 1/f_2$.

With the foregoing discussion in mind, the invention will be most readily understood from the following detailed description of a representative embodiment thereof, reference for this purpose being had to the accompanying drawings, in which:

FIGURE 1 schematically illustrates in block form a frequency converting system embodying the invention, and

FIGURE 2 schematically illustrates in block form and in greater detail the frequency converting and computing portion of the system shown in FIGURE 1.

Like reference numerals designate like parts throughout the several views.

Refer to the figures which schematically illustrate in block form a frequency converting system and method embodying the invention. The frequency converting system comprises a detecting and computing portion and an information storage. The frequency converting system includes a number of telemetering apparatus and related systems. Thus, the frequency converting system shown is adapted to receive commutated information in frequency form and in predetermined frequency bands.

For example, information may be provided in this form by a rotary commutating switch having 60 segments. In this manner, information may be sequentially delivered by 27 active or "on" segments each of which is separated by one of 28 "off" or shorted segments, while the remaining five segments of the switch may each be synchronized with signals which appear prior to the information in the "on" channels. Information signals derived during respective active or "on" segments are frequency modulated data signals each having a frequency $f$ which is variable between an
upper limit frequency $f_1$ having a period $t_1$ and a lower limit frequency $f_2$ having a period $t_2$, and first and second reference signals respectively having the upper and lower frequencies $f_3$ and $f_4$. Synchronizing signals also may be delivered prior to the information signals during the commutation cycle.

The channels or subcarriers within which frequency modulated information is transmitted have more or less been standardized in the telecommunication field. For example, various channels have been designated by the Research and Development Board and numbered from 1 to 18 for particular teleremoting frequencies. The Research and Development Board channel 18 has a center frequency of 70,600 cycles per second, with an upper limit of 75,250 cycles per second, a lower frequency limit of 64,750 cycles per second. The frequency converting system described herein is adapted for receiving information in any or all of the designated channels and is not inherently limited to any particular one of the operative frequency ranges.

Referring particularly to the FIGURE 1, commutated information signals are received by the information input terminal 12 of the detecting and computing portion 16 of the frequency converting system. The information signals may be received directly from a transmitting source such as a radio or may be derived from a record such as a magnetic tape transport.

The information input terminal 12 delivers input signals to a time control device 14 and to a synchronizing counter 16 which is responsive to synchronizing signals. The synchronizing counter 16 also receives timing pulses from an input terminal 18 and correspondingly activates one of thirty output control lines 42. The counter 16 delivers start signals to the time control device 14 to initiate sequential sampling operation during the commutation cycle. The time control device 14 upon receiving a start signal from the synchronizing counter 16 samples the information signals on the input terminal 12 and generates a time control period which is inversely related to the frequency of the input signal.

Throughout the time control period, the control device 14 delivers a signal to the control gate 20 allowing it to pass signals which are impressed at terminal 22. The signals on terminal 22 in the particular application now being described are clock pulses which appear at regular intervals and may be varied in frequency to compensate for errors. In other applications, the signals applied at terminal 22 may be used to generate desired timed functions.

The clock pulses passed by the gate 20 are received by a counter 23 which had previously been cleared to zero count by a signal from the synchronizing counter 16. The counter 23 after the termination of the time control period has a count which is related to the period $t_1$ of the information signal delivered to the input terminal 12.

During the counting operation, the count of the counter 23 is delivered to a comparator 24. When the count of the counter 23 reaches the count which corresponds to the period $t_1$ of the upper frequency limit $f_1$, the comparator 24 delivers a permissive signal to an input control gate 26.

When the input control gate 26 receives the permissive signal from the comparator 24, it also allows the delivery to a counter 28 of the clock pulses which are being received by the counter 23.

Since the counter 28 does not start counting the clock pulses until after a time corresponding to the period $t_1$ of the upper frequency limit $f_1$, the count of the counter 28 is proportional to the difference between the period $t_1$ of the input formation signal and the period $t_1$ of the upper limit frequency $f_1$, and may be represented as proportional to $(t_1-t_2)$.

Upon the completion of the time control period, the counters 23 and 28 have assumed their final counts. The respective counts of the counters 23 and 28 control an arithmetic network or divider 30.

The divider 30 initiates its dividing operation upon the receipt of a start division signal from the synchronizing counter 16 over the line 32. The start division signal is received after the termination of an active or "on" segment and at the beginning of the first half of the succeeding "off" segment. The divider 30 provides a quotient $X$ which is the count of the counter 28 divided by the count of the counter 23 and may be represented by $(t_1-t_2)/t_1$.

The quotient $X$ provided by the divider 30 is delivered to its output line 34 at the completion of the dividing operation.

In the operation of the detecting and computing portion 10 of the particular system illustrated, the commutated frequency modulated information which is delivered to the input terminal 12 comprises reference signals and data signals. The reference signals include a first reference signal having the upper limit frequency $f_1$ and a second reference having the lower limit frequency $f_2$. These reference signals are each presented at least once during a commutation cycle on respective segments. The remaining active or "on" segments have information data signals with a frequency $f$ which may vary between the upper and lower limit frequencies $f_1$ and $f_2$.

Upon the occurrence of the first reference signal having the frequency $f_1$, the synchronizing counter 16 sends a start signal to the time control device 14 which allows the gate 20 to deliver clock pulses to the counter 23 during the time control period generated by the control device 14. The counter 23 at the termination of the time control period registers a count $C_0$ which is directly related to the the period $t_1$ of the upper limit frequency $f_1$ as represented by

$$C_0 = k t_1$$

where $k$ is a factor of proportionality.

This signal is delivered over the line 36 to a primary gate 38 of the storage 11 of the system. A central control 40 which is actuated by the thirty control lines 42 of the synchronizing counter 16 delivers a permissive signal to the gate 38 at the completion of the count $k t_1$. The signal on line 36 is delivered by the gate 38 to a storage location 44. The storage location 45 presents its stored signal over the line 46 to the input of the comparator 24.

When the information signal appearing on the terminal 12 is the second reference signal having the lower limit frequency $f_2$, the synchronizing counter similarly initiates the generation by the control device 14 of a time control period which is proportional to the period $t_2$ of the reference signal. The gate 20 permits the passage of clock pulses from the terminal 22 to the counter 23 during the time control period. The comparator 24 delivers a gating signal to the gate 26 when the counter 23 has reached a count equal to the count representing the period $t_2$ which is received by the comparator 24 over the line 46 from the storage location 44.

Thus, at the end of the time control period the counter 23 contains a count $C_0$ which is proportional to the period $t_2$ of the second reference signal as represented by

$$C_0 = k (t_2-t_1)$$

The count of the counter 28 energizes the divider 30 providing the numerator, while the count of the counter 23 provides the denominator.

Upon the receipt of a start division signal upon the beginning of the first half of the "off" segment following
the "on" segment \((t_1, t_2)\), the synchronizing counter 16 delivers a start division signal over the line 32 to the divider 30. The divider delivers during the first half of the "off" segment an output signal \(X\) which is the quotient produced by the input signals and may be designated the reference correcting or normalizing factor and represented by

\[ X = \frac{C_1}{C_2} = \frac{(t_2 - t_1)}{t_2} \]

with the factors of proportionally cancelling each other in the division.

At the completion of the dividing operation by the divider 30, its output signal is present at the primary gate 43 of the storage 11. The gate 49 receives a gating signal from the central control 40 during the first half of the "off" segment upon the completion of the division by the divider 30. This allows the gate 48 to pass the normalizing factor output signal to the storage location 50.

With the receipt of a data signal on the input terminal 12, the apparatus operates in a similar manner so that the divider 30 producers during the first half of the succeeding "off" segments an output signal which may be designated a data output signal and represented by

\[ X = \frac{(t_2 - t_1)}{t} \]

where \(t\) is the period of the data signal having a frequency \(f\) between the upper and lower limit frequencies \(f_1\) and \(f_2\).

In this case, the central control 40 delivers a gating or permissive signal to the secondary gate 52 which passes the data output signal to a memory location 54. The permissive signal is delivered to the gate 52 during the first half of the "off" segment following an "on" segment providing a data signal upon the completion of the dividing operation of the divider 30.

After the storage of the data output information at location 54, the central control 40 delivers a gating signal to secondary gates 56 and 58. The gate 56 delivers the information signal at the location 54 to the counter 25 setting it to the corresponding count. In a similar manner, the gate 58 delivers the information stored at location 50 to the counter 23. The counter 23 is thus set to the corresponding count. The information set up in the counters 23 and 25 is presented to the divider 30. Upon receipt of a start division signal from the synchronizing counter 16, which is timed to occur after the counters 23 and 25 are thus set up, the dividing operation of the divider 30 is initiated and takes place during the second half of the said "off" segment. With the completion of the dividing operation by the divider 30, an output quotient \(X\) is produced which may be designated the converted or normalized output data signal and represented by

\[ X = \frac{(t_2 - t_1)}{t} \]

Upon the completion of this dividing operation by the divider 30, a secondary gate 60 receives a permissive signal from the central control 40 allowing it to pass the normalized output signal to the storage location 62. This information is also delivered to an output line 64 which may be directly connected by a switch 65 to the input of a thirty channel analog decommutator 66 or to a digital to voltage translator 67 which delivers a corresponding voltage signal to the decommutator 66. The above detecting and computing operations are performed for each data signal received at terminal 12. Thus, for the illustrated commutation cycle, two of the 27 active segments may contain reference information, while the remaining twenty-five segments may carry data information. This means that during a commutation cycle twenty-five data signals will be delivered to the output line 64 of the storage 12 during the "off" segment following its data "on" segment. Information received by the decommutator 66 may be decommutated into appropriate channels or output lines 62 under control of the output lines 42 of the synchronizing counter 16.

With regard to the storage 11, it is noted that the primary gates 43 and 45 are energized in connection with the occurrence of reference signals, while the secondary gates 52, 56, 58 and 60 are energized in the order stated to produce a normalized output signal upon the occurrence of each data input signal.

Reference signals are delivered to the input terminal 12 of the apparatus 10 during each commutation cycle. This provides adjustment for any variation or drift in the channel frequency which occurs over a period of time exceeding the commutation cycle. This is so, since the reference signals which are used in the computation of the normalized output data signals are thereby continually corrected to take into account such frequency or drift variations.

Short term error variations in the input information signals which occur within the period of the decommutation cycle can be corrected by compensating variations in the clock pulses delivered to the input terminal 22 as previously noted.

An analysis of the computing operation of the system will disclose that the normalized output signal is independent of the particular subcarrier band or channel utilized for carrying the information signals and automatically corrects for drift in the information signals. The normalized output signal for an information data signal having a frequency between an upper limit frequency \(f_1\) and a lower limit frequency \(f_2\) may be represented as follows:

\[ X = \frac{(t_2 - t_1)}{t} \]

If the following equalities are substituted in the above equation

\[ f_1 = \frac{1}{t} \]

then, it is equivalent to the following:

\[ X = \frac{(t_2 - t_1)}{t} \]

Since the above equation represents the computation carried out by the system to produce the normalized data output signals, the normalized data output signals produced by the system are not approximations but accurate representations of the input information signals in converted form.

The converting system also operates at high speed delivering in sequence each of the normalized output signals in real time during the respective "off" segments following the "on" segments during which data signals are delivered. Since the system is highly accurate and utilizes precise digital techniques, the output signals may be delivered with any degree of precision required by selecting the number of digits to be carried. Of course, the time control device 14, the frequency of the clock pulses delivered to the input terminal 22 and the number of stages of the counters 23 and 25 may be increased to the degree desired for the precision required of the normalized output signals. This is a design feature which may be varied with the particular apparatus and application under consideration.

Thus, the system allows any degree of precision required in the output signals because of its inherent qualities. The system also provides for error correction by variation in the frequency of the clock pulses delivered to the input terminal 22 and by periodically sampling the reference signals to correct for drift which has already been explained.

Refer now to FIGURE 2 for a description in greater detail of the detecting and computing portion 10 of the frequency converting system described above in connection with FIGURE 1.
The commutated information signals are received by the information input terminal 12 of the detecting and computing portion 10 of the frequency converting system. The information signals may be received directly from a transmitting source such as an air-borne device or may be derived from a record such as a magnetic tape transport.

The synchronizing signals of the information signals activate a detector 114 which delivers a synchronizing signal to a segment counter 116. The segment counter 116 may be of the binary type having a sufficient number of stages to count the commutator segments. For example, in this case where there are 60 commutator segments, a five stage binary counter would be sufficient since it can count up to 64. The synchronizing signal from the detector 114 initially sets the segment counter 116 to its starting state for its counting operation.

Timing pulses which are received at the input terminal 18 are delayed or generated by the commutator, being produced concurrently with the segment commutations. In this case where there are sixty segments, sixty pulses would be presented during each commutation cycle. The timing pulses may be directly received or may be received together with the commutated information from a magnetic transport or other such record.

The segment counter 116 is provided with thirty segment control lines 42, a particular one of which is activated upon the occurrence of each of the active or "on" segments. The segment counter 116 also delivers at an output line 122 a set pulse upon the occurrence of each of the "on" segments. The output pulses on the line 122, however, may be delayed until any switching or other transients which may occur upon the delivery of an information signal have sufficiently decreased.

Information signals on the input terminal 12 are also delivered to an axis crossing detector 124 which may be a flip-flop circuit adapted for high frequency operation. The axis crossing detector 124 delivers an output pulse on its line 126 each time the information signal having a frequency f crosses its axis in the positive going direction. The output pulses on line 126 are delivered to an input control 128.

The gate 128 does not deliver an output signal until it receives a permissive gating signal from a flip-flop circuit 130 in its set state. The flip-flop circuit 130 is actuated to its set state upon the occurrence of an output pulse on line 122 from the segment counter 116. The gate 128 then passes the output pulses from the axis crossing detector 124 to its output line 131.

The occurrence of an output signal on the line 122 from the segment counter 116 resets a cycle counter 135 to deliver an output signal after a predetermined number of cycles N. The cycle counter 132 counts the pulses delivered to the line 131 and after the occurrence of N cycles, it delivers an output signal to the line 134 which resets the flip-flop circuit 130. With the reset of the flip-flop circuit 130, the input control gate 128 is inhibited and does not deliver output pulses to the line 131.

The external control 136 allows control of the number of cycles N which the counter 132 will count upon being reset before it delivers an output pulse on its line 134. As will later become apparent, the optimum count N of the counter 132 will depend upon the frequency of the information signals detected by the system for maintaining the accuracy of the converted information over the various channels, or frequency ranges within which the information is delivered. Thus, for example, if the information signals are received in the Research and Development Board channel 18 having a center frequency of 70,000 cycles per second, then the count number N of 35 has been found appropriate when the clock pulses on terminal 22 have a frequency of approximately 10 megacycles.

It is noted that the control period determined by the counter 132 which extends from the time it is reset by a pulse on line 122 to the time it delivers an output signal on line 134, is proportional to the reciprocal of the frequency f of the information signal delivered to the information input terminal 12. For example, when the frequency f of the information increases, the interval of time needed to count the predetermined number of cycles N decreases, while when the frequency of the information signal decreases the control period during which the counter receives N cycles increases.

The system also includes means for detecting the absence of data during an "on" segment and delivering an invalid data signal. This means comprises a flip-flop circuit 138 which is set by a signal delivered to the line 122 by the segment counter 116, and is reset by the occurrence of an information pulse on the output line 131 of the input control gate 128. The flip-flop circuit 138 delivers a gating signal to an output gate 140 when in its set state. A delay flip 142 which is triggered by the occurrence of an output signal on the line 122 delivers an output pulse to the gate 140 after a predetermined delay period. If information pulses are not delivered to the line 131 within the delay period of the delay flip-flop 142, the flip-flop circuit 138 will not be reset and signals will be delivered concurrently by the flip-flop circuit 138 and delay flip circuit 142 to the output gate 140. This will result in the delivery of an invalid data output signal by the output gate 140.

This signal may be used in various ways to indicate that any output signal delivered by the system for the corresponding segment is incorrect.

A gate control flip-flop circuit 144 is placed in its set state upon the occurrence of information pulses on the line 131 and is reset by the occurrence of an output signal from the cycle counter 132 on the line 134. Thus, the flip-flop circuit 144 is maintained in its set state during the time control period produced by the cycle counter 132. The flip-flop circuit 144 when it is in its set state delivers a gating signal to the first input line 146 of a clock gate 148. The second input line 150 of the clock gate 148 is connected to the clock input terminal 22. The clock input terminal 22 receives activating signals or pulses of a predetermined frequency. The frequency of the input signals to terminal 22 may be varied, however, to take into account various correcting factors or in certain applications may be caused to vary with time to generate desired functions.

In the present instance, however, the correct clock signals which may have the illustrated frequency of 10 megacycles may be varied to take into account corresponding error variations in the frequency of the commutated information signals delivered to the input terminal 12. In this manner, the frequency variations due to wow and flutter and other such effects upon the information signals derived from a magnetic tape may be compensated for by corresponding variations in the clock signals delivered to the input terminal 22. It is noted that such variations in the frequency of the corrected clock signals take into account periodic variations in the information frequency f within the time control period of the cycle counter 132. Variations in the information signal frequency f due to drift and other long term variations, which extend over more than one commutation cycle, are corrected for in a manner which will be described hereinafter.

During the time control period when the flip-flop 144 is in its set state, the gate 148 passes clock pulses on terminal 22 to the line 154 which is connected to the input of a denominator counter 156 which had previously been cleared by a signal delivered to the line 122 from the segment counter 116. At the end of the time control period, the cycle counter 132 delivers its output pulse over line 134 placing the flip-flop circuit 144 in its reset state. This inhibits the gate 148 and terminates the delivery of clock pulses to the line 154. The final count C1 now registered by the denominator counter 156 is proportional to the period t of the information signal having a frequency f delivered to the input terminal 12 and may be presented by

\[ C_1 = k乏. \]
where $k$ is the constant of proportionality.

If the signal $f_2$ is a reference frequency having the upper limit frequency $f_2$ with a period $t_2$, then the final count $N_2$ of the denominator counter 156 will be proportional to the period $t_2$ as represented by

$$N_2 = k t_2$$

The denominator counter which may be a binary cascade type device delivers its count in digital form to its output lines 158. As described in connection with FIGURE 1, the count representing the period $t_2$ may be delivered by the set of output leads 160 to the storage 11.

Upon the occurrence of the "on" segment delivering the second reference signal having the lower limit frequency $f_2$ and the period $t_2$, the final count $N_2$ of the denominator counter 156 will be proportional to the period $t_2$ as represented by

$$N_2 = k t_2$$

When the denominator counter 156 is generating its count, this information is delivered by its output lines 158 to a series of carry gates 162 which form the comparator 24. The carry gates 162 also receive a digital signal corresponding to the period $t_2$ over its set of input leads 164. The signals delivered to the input leads 164 of the carry gates 162 may be derived from the storage 11 and delivered in connection with FIGURE 1 or from a manual control.

When the count of the denominator counter 156 which increases with time reaches the value corresponding to $t_2$, which is present on the input lines 164, an output signal is delivered to the line 166. The pulse on line 166 is delivered to a flip-flop circuit 168 which is placed in its set condition.

When the flip-flop 168 is in its set condition, it delivers a permissive signal over the line 170 to a control gate 172. This allows the passage of clock pulses on line 184 to the forward count line 174 of a numerator counter 176 which is initially cleared to its zero count. The counter 176 is of the reversible type controllably counting in the forward or backward directions.

The numerator counter 176 proceeds by counting in the forward direction the clock signals appearing on the line 184 until the termination of the time control period. Upon the termination of the time control period, the output signal delivered by the cycle counter 123 to the line 134 is received by the flip-flop circuit 168 resetting it and inhibiting the control gate 172.

The output of the numerator counter 176 will at the termination of the time control period have a count $N_2$ which is proportional to the difference in the information signal period $t_1$ and the first reference signal period $t_2$, which may be represented by

$$N_2 = k (t_1 - t_2)$$

where $k$ is the constant of proportionality.

An error detecting gate 176 is provided for detecting the occurrence of an incorrect signal in which the normalized output signal produced is less than the zero percent value. The gate 173 has a first input lead 187 receiving a gating signal from the flip-flop circuit 168 when it is in its reset state, and a second input lead 188 receiving the output signals delivered by the cycle counter 123 to the output line 134. Thus, if the flip-flop circuit 168 has not been placed in its set state by an output signal on the line 166 from the carry gates 162 when the cycle counter 123 delivers its output pulse to the input lead 123, the error gate 176 will pass an output signal to the line 134. Such an output signal indicates that the information signal received by the denominator counter 132 has a normalized value less than zero percent. This would correspond to a signal input having a frequency $f$ which is greater than the upper limit frequency $f_2$.

The denominator counter 156 and the numerator counter 176 are utilized in combination with other elements to be described to form an arithmetic or divider multiplier network 36.
The above result is obtained by the arithmetic circuit 30 with its operation control switch 196 in its first position as illustrated in FIGURE 2. This forms an open loop division circuit.

By placing the operation control switch 196 in its second position, the arithmetic network 30 forms a closed loop circuit which will perform a multiplication operation.

In the multiplying operation of the network 30, the X counter 200 delivers the output signal X which is equal to the count C0 times the count C2. This will be obvious from the following exposition:

\[ X = f_0 C_0 / f_2 C_2 \]

by substitution

\[ X = C_1 C_2 \]

Although in the frequency converting system particularly described, the arithmetic network 30 is used to perform a dividing operation, it will be evident to those skilled in the art that many variations and adaptations of the apparatus may be achieved by utilizing the arithmetic network for performing multiplying operations.

Thus with the numerator counter registering a count proportional to \((t - t_0)\), and the denominator counter having a count proportional to \(t\) at the termination of an "on" segment during which an information signal is delivered to the input terminal 12, a dividing operation is initiated at the beginning of the succeeding "off" segment by the delivery of an initiating pulse to the line 218 by the segment counter 116. The output signal delivered by the X counter 210 in this case may be represented as follows:

\[ X = C_1 C_2 (t - t_1) / t \]

where \(t\) is the period of the formation signal received at the input terminal 12 and the factors of proportionality \(k\) cancel each other in the division.

When the signal received at the input terminal 12 is a second reference signal having a frequency \(f_2\) with a period \(t_2\), then the output signal delivered by the counter 200 may be represented as follows:

\[ X = (t_2 - t_0) / t_2 \]

As previously noted, the above reference normalizing or correcting factor output signal of the X counter 210 is stored by the storage 11 for use in subsequent computing operations.

When the signal delivered to the input terminal is a data signal having a frequency \(f_3\) intermediate the upper and lower frequencies \(f_1\) and \(f_2\), then the output signal delivered by the X counter may be delivered to the storage 11 or delivered directly to the input or jam lines 228 of the numerator counter 176.

The input signal delivered to the lines 228 sets the counter 176 to the count of the data output signal of the counter 200. The reference normalizing or correcting factor represented by \((t_2 - t_1) / t_2\) which is derived from the storage 11 is also impressed upon the input or jam lines 230 of the denominator counter 156 at this time.

This sets the denominator counter 156 to the count of the normalizing factor. The arithmetic network 30 is now set up for a dividing operation which is carried out and completed during the second half of the "off" segment.

The dividing operation is initiated by the pulse which was delivered to the line 218 by the segment counter 116 after it has passed through a delay element 232 and the buffer 220 to the line 222. The delay element 232 receives the pulse on the line 218 which occurred at the beginning of the first half of the "off" segment and delivers a delayed-pulse to the line 222 occurring at the beginning of the second half of the "off" segment. The delay element 232 also provides a delay time which is sufficient to assure completion of the jamming operation setting up the respective counts on the counters 156 and 176 prior to the initiation of the dividing operation.

The pulse on line 222 is delivered to the reset lead 224 clearing the X counter 200 to zero. The delay 226 delivers the pulse on line 222 to the line 214 after sufficient delay to complete the reset of the X counter 200. The signal on the line 214 sets the flip-flop circuit 210 which delivers a gating signal to the gate 204. This starts the dividing operation.

The arithmetic operation is carried out as previously described. At the completion of the dividing operation, the numerator counter 176 upon registering a zero count delivers a carry signal over the line 216 to the flip-flop circuit 210 resetting it and preventing the delivery of further activating signals through the gate 204. It is noted that this operation automatically clears the numerator counter 176 to its zero count in preparation for a forward counting operation.

The X output lines 202 of the X counter 210 at the completion of the division operation deliver a normalized digital output signal which may be represented by:

\[ X = \frac{(t - t_1)}{t} \]

This information is provided before the completion of the second half of the "off" segment.

It is noted that the output of the X counter 200 will have a count equal to or intermediate zero and 100 percent levels, irrespective to the particular channel within which the information is being received. This is what is meant by a normalized output signal.

From the last equation it is noted that when the data signal delivered to the input terminal 12 is equal to \(f_1\) which is the upper limit frequency, the normalized digital output signal will be equal to the zero information level. When the data signal delivered to the input terminal 12 has a frequency equal to the lower limit frequency \(f_2\) then, the normalized digital output is equal to \(t_0\) since \(t_0 = t_1\). When the value of the data signal delivered to the input terminal 12 has a frequency \(f_3\) intermediate the upper and lower limit frequencies \(f_1\) and \(f_2\), the normalized digital output signal delivered by the X counter 200 will have the appropriate value intermediate the one and zero information levels.

An error detecting output line 234 is provided for indicating a signal having an information level exceeding the 100 percent value. This is achieved by delivering a carrying pulse from the X counter 200 to the line 134 when the count of the X counter 200 exceeds its maximum normalized value of one.

It will be evident that the accuracy which is achieved by the apparatus is inherently unlimited, since the precision may be increased by increasing the number of digits of the counters 156, 157, the output X counter 200, and correspondingly increasing the number of input control leads 189 of the binary rate multiplier 186.

The information delivered by the X counter 210 during the second half of the "off" segment is the normalized digital output signal corresponding to the data information signal delivered during the preceding "on" segment to the input terminal 12. This digital informa-
tion may be delivered to and stored in the storage 11 or directly delivered to an analog decommutator 66. The output signals from the X counter 200 may also be delivered directly or through the storage 11 to a digital to voltage translator 67 which produces an analog voltage signal at its output line 69. The output line 69 may, if desired, then deliver the sequentially occurring analog voltage signals to the analog decommutator 65 for separation and delivery to respective output leads 86.

In summary, the information input terminal 12 is adapted to receive commutated information signals during "on" segments including first and second reference signals with respective upper and lower limit frequencies \( f_1 \) and \( f_2 \), and data signals having information in frequency segments between the limit frequencies \( f_1 \) and \( f_2 \). Each of the "on" segments are separated by an "off" segment. A number of segments which occur during the commutation cycle provide synchronizing signals. The synchronizing information is detected and used to set the segment counter 116 to its start condition.

When an information signal is delivered with the first reference frequency \( f_2 \), the appropriate time control period is generated by the cycle counter 152, so that the denominator counter 156 registers a count proportional to the period \( t_1 \) at the conclusion of the counting operation. This takes place during the "on" segment. The count representing \( t_1 \) is delivered by the output lines 160 from the denominator counter 156 to the storage 11 for use during the remainder of the commutation cycle.

Upon the receipt of the "on" segment with the second reference frequency \( f_2 \), the apparatus samples the information signal, generating a time control period inversely related thereto and allows the delivery of clock signals to the denominator counter 156. As the denominator counter 156 increases its count, the comparator carry gates 162 deliver an output signal when the count is equal to the count representing the period \( t_1 \). The comparator gates 162 receive the count representing \( t_1 \) from the storage 11 or when desired from a manual control. The delivery of an output signal from the comparator gates 162 initiates the forward counting operation of the numerator counter 176.

At the end of the counting operation the denominator counter 156 has a count proportional to the period \( t_2 \) of the reference frequency \( f_2 \) while the numerator counter 176 has a count proportional to the difference in the periods represented by \( (t_2-t_1) \), where \( t_2 \) is a period of the lower reference frequency \( f_2 \). This takes place during the "on" segment.

Upon the completion of the "on" segment and the start of the "off" segment, an output pulse is delivered by the numerator counter 116 to its output line 218 initiating a dividing operation by the arithmetic network 30. The dividing operation is completed and a digital output signal is delivered by the X counter 200 during the first half of the "off" segment.

The output signal from the counter 200 which may be designated the digital normalizing or correcting factor and represented by \( (t_2-t_1)/t_2 \), is stored for use in producing normalized data output signals.

With the occurrence of each of the data signals which appear during the commutation cycle on the input terminal 22, the following operations are carried out. During the "on" segment the denominator counter 156 generates a count proportional to the period \( t \) of the data signal having a frequency \( f \). The numerator counter 176 produces a count proportional to the difference in the periods of the data signal and the first reference signal which difference is represented as proportional to \( (t-t_1) \).

At the beginning of the first half of the "off" segment succeeding the data "on" segment, an output signal is delivered by the segment counter 116 to its output line 218. This initiates a dividing operation by the arithmetic network 30 which is completed during the first half of the "off" segment. The output signal may at this time be represented by \( (t_2-t_1)/t_2 \).

At the beginning of the second half of the "off" segment following a data "on" segment, the data output delivered by the X counter 200 is impressed and registered upon the numerator counter, while the reference normalizing or correction factor from the storage 11 is impressed and registered upon the denominator counter 156.

With the numerator and denominator counters 176 and 156 thus set up, the arithmetic circuit 30 starts a dividing operation which is initiated by a delayed pulse from the output line 218 of the segment counter 116. The dividing operation of the network 30 is completed during the second half of the "off" segment. The output count of the X counter 200 of the arithmetic network 30 is a normalized digital output signal represented by

\[
\frac{(t-t_1)/t_2}{(t_2-t_1)/t_2}
\]

This normalized digital output information, which is delivered during the "off" segment following each "on" segment delivering a data signal, may be directly decommutated or first delivered to a digital to voltage translator to produce an analog voltage signal. The commutated analog voltage signal then may be delivered to the decommutator 66 for presentation upon respective output lines 68. Converted normalized information signals, thus, are delivered by this system in rapid succession each following the delivery of a data signal and preceding the delivery of a new data signal. This is substantially operation in real time.

It is noted that by receiving reference signals during each commutation cycle, this system automatically takes into account the drift which may occur and delivers a normalized output signal which is corrected for such drift variations. In the case where variations in the input information frequencies occur within the commutation cycle, as might be due to wow and flutter of a magnetic transport, this error is corrected by correspondingly varying the frequency of the clock signals delivered to the input terminal 22.

Of course, by receiving the reference frequency signals during each commutation cycle, the apparatus can readily be switched from one band or channel of frequencies to another channel without requiring adjustments and calibrations. The cycle counter 132, however, should have the number of cycles \( N \) which it is preset to count vary depending upon the range of upper and lower frequencies \( f_1 \) and \( f_2 \) of the particular channel in which information is to be received. This is for the purpose of obtaining the maximum of accuracy of the conversion system in use. For example, if the basic frequency of the corrected clock signal delivered to the input terminal 22 is not to be varied with change in the channel, then if the frequency range of the incoming signals to the input terminal is lowered, the cycle counter 132 should be preset to count a smaller number of cycles to maintain the substantially constant range of the time control period. If this were not done, the maximum time control period would cause the denominator counter 156 to receive an increased number of count pulses causing it to overflow. Where the input frequency range of the input terminal 22 is increased without increasing the preset count of the cycle counter 132, then the time control period would not be sufficient to allow a full count of the denominator counter 156.
by reducing the accuracy of the system. The preset value of the cycle counter 132 may easily be adjusted by the e-

ternal control lines 136 to increase its count N when the

cycle frequency is increased or to decrease its count N when the channel frequency is decreased. Or a compar-
able adjustment may be made in the frequency of the clock signal delivered to the input terminal 22.

It is also noted that in the event where drift of the information signals delivered to the input terminal 12 is not to be taken into account, the value representative of $t_1$ and the reference normalizing and correcting factor $(t_1 - t_2)/t_1$ need not be continuously generated, and may be manually preset for respective excitation of the com-

parator gates 162 and the denominator circuit 156.

The frequency converting system is adapted to receive data information having a frequency which is substantially constant during its segmental transmission period. How-

ever, should the frequency of the signal vary, the counting operation of the cycle counter 132 has an integrating effect in the generation of the time control period. Thus, the cycle counter 132 produces a control period responsive to the average value of the frequency $f$ during the sampling time. The averaging operation increases the reliability of the equipment.

Although the frequency converting system has been particularly described in connection with the receipt of commutated information signals, it will be obvious that the equipment may be utilized for periodically sampling a continuously varying frequency modulated information signal. If the signal varies between upper and lower fre-

quency limits $f_1$ and $f_2$, then this information may be uti-

lized to provide the normalized digital output signals varying between zero and 100 percent levels.

If it is not desirable under the circumstances to obtain a normalized digital output signal, then the digital output signal is delivered by the denominator counter 156 to the output lines 160 may be directly utilized, since this infor-

mation corresponds to the period of the information fre-

quency. Should it be desired to subtract a factor from the period of the sampled frequency, this may be achieved by the add/dotor gates 162 and the remainder can be obtained from the numerator counter 176.

It will thus be obvious that the frequency converting system provides a basic apparatus and method which may be appropriately adapted for periodically sampling contin-

uous varying frequency information or commutated frequency information. The computation portion of the system also lends itself to various counting and arithmetic operations to convert the frequency information delivered to the input terminal 12 to various digital forms and pro-

vides various arithmetic computations in highly efficient, accurate and high-speed operations.

The frequency converting system has great utility in producing output information which is a function of the frequency of the input information signal. For exam-

ple, the apparatus has been found useful wherein the rate of activating pulses delivered to the input terminal 22 is varied to take into account corrections as well as for the purpose of generating particular desired functions. For the latter use, the frequency or rate of the pulses to the input terminal 22 may increase or decrease as a particular function of time. Thus, the count in the counter 156 will depend upon the time control period which is responsive to the frequency of the information signal. Where the count produced by the counter 156 is to be a decreasing function, the denominator counter may be preset to the top value as by delivering this information to its jam lines 136, and the pulses delivered to the counter 156 then may be used to decrease its count at a controlled rate. Thus, the final count in the counter 56 will de-

pend upon the frequency of the input information signal as well as the controlled constant or varied rate at which

the activating signals are delivered to the input terminal 22.

Many other uses of the apparatus and system will be obvious from the description presented herein. It will

also be obvious to those skilled in the art that the inven-

tion may find wide application with appropriate modifica-

tion to meet the individual design circumstances but with-

out substantially departing from the essence of the inven-

tion.

What is claimed is:

1. A frequency converting apparatus comprising an axis crossing detector adapted to receive an information signal and deliver output pulses having a frequency corre-

sponding with the frequency of said signal, a cycle counting device adapted for being preset to deliver a carry sig-

nal after receiving a predetermined number of pulses, a first gate element, a first bistable circuit having a set state conditioned said first gate element for delivering pulses from said detector to said cycle counting device and a reset state inhibiting said first gate element, a sample control circuit initiating an operation by presetting said cycle counting device and placing said first bistable circuit in its set state, said first bistable circuit being reset by a carry signal from said cycle counting device, a first count-

ing unit, a second gate element receiving corrected clock signals, a second bistable circuit having a set state conditioned said second gate element for the delivery of corrected clock signals to said first counting unit and a reset state inhibiting said second gate; said second bistable circuit being set by a signal from said first gate element and reset by a carry signal from said cycle counting device, a second counting device, a second counting device, a second counting unit, a second gate element receiving cor-

rected clock signals from said second gate element, a third bistable circuit having a set state conditioned said second gate element for the delivery of the corrected clock signals to said second counting unit and a reset state in-

hibiting said third gate; said third bistable circuit being set by a signal from said first gate element and reset by a carry signal from said cycle counting device, an arithmetic circuit responsive to the counts of said first and second counting units, said first and second counting units being reset preparatory to the initiation of an operation by said sample control circuit.

2. The frequency converting apparatus of claim 1 in which said arithmetic circuit delivers an output signal representing the quotient of the final count of said second unit divided by the final count of said first unit recorded upon the termination of the counting period by the carry signal from said cycle counting device.

3. An apparatus for converting a frequency modulated information signal having a frequency $f$ variable within the range between an upper frequency $f_1$ with a period $t_1$ and a lower frequency $f_2$ with a period $t_2$ comprising a cycle counting device set to count a predetermined number of cycles of an information signal to determine a control period related to the reciprocal of the frequency $f$ of the information signal, a first counting unit adapted for counting clock signals during the control period of said device, a comparator network delivering an output signal when said first counting unit attains a count corresponding to the period $t_1$ of the upper frequency $f_1$, and a second counting unit counting clock signals concurrently with said first counting unit upon the occurrence of the output signal of said comparator network and producing a count directly related to the difference between the period $t$ of the information signal and the period $t_1$ of the upper frequency $f_1$.

4. The apparatus of claim 3 including an output cir-

cuit for delivering a digital output signal representing the quotient of the count of said second unit divided by the count of said first unit, said quotient being equal to

$$k(t_1 - t_2)/t$$

where $k$ is a constant of proportionality, said quotient being equal to

$$k(t_1 - t_2)/t_2$$
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when the information signal has a frequency \( f_2 \) with a period \( t_2 \).

5. The apparatus of claim 4 having means producing a converted output signal which is the quotient of the output signal produced by said output circuit for an information signal having a frequency \( f \) divided by the output signal produced by said output signal for an information signal having a frequency \( f_2 \) which is equal to

\[
\frac{(t_2-t_1)}{t_2} \quad \text{or} \quad \frac{(t_1-t)}{t_2-t_1}
\]

where

\[
t = \frac{1}{f}
\]

and

\[
t_1 = \frac{1}{f_1}
\]

6. The apparatus of claim 5 including a sampling control means to reset said cycle counting device after each counting operation for sequentially sampling said information signal, so that corresponding converted output signals are sequentially produced by the apparatus.

7. The apparatus of claim 6 for receiving a plurality of sequential information signals including a synchronizing detector associated with said sampling control means for coordinating the sampling of said information signals.

8. The apparatus of claim 7 adapted to periodically receive information signals having the frequency \( f_1 \) with the period \( t_1 \) and including an information storage receiving and retaining the count of said first counter corresponding to the period \( t_1 \) for delivery to said comparator network.

9. The apparatus of claim 8 adapted to periodically receive information signals each having a frequency \( f \) with a period \( t \) causing said output circuit to produce respective digital output signals represented by

\[
k \frac{t-t_1}{t}
\]

where \( k \) is a constant of proportionality for producing the converted output signals of said apparatus, the frequency \( f \) of each of said information signals being within the range between said upper and lower frequencies \( f_1 \) and \( f_2 \).

10. The apparatus of claim 9 adapted to periodically receive an information signal having the frequency \( f_2 \) with the period \( t_2 \), said storage receiving and retaining the count of said output circuit represented by

\[
k \frac{t_2-t_1}{t_2}
\]

where \( k \) is a constant of proportionality for producing the converted output signals of said apparatus.

11. The apparatus of claim 10 adapted to sequentially receive respective commutated information signals during "on" segments which are separated by "off" segments, said first and second counting units performing their clock signal counting operations for each information signal during its respective "on" segment, while said output circuit delivers its corresponding output signal during the "off" segment.

12. The apparatus of claim 11 in which the commutated information signals received by the apparatus include data signals having a frequency \( f \) with a period \( t \) and reference signals having respective frequencies \( f_1 \) and \( f_2 \) with periods \( t_1 \) and \( t_2 \), said first counting unit producing an output count signal corresponding to the period \( t_1 \) when said apparatus receives a reference information signal with a frequency \( f_1 \).

13. The apparatus of claim 12 in which said output circuit delivers during the first half of the "off" segment following an "on" segment an output signal represented by

\[
\frac{1}{f_1}
\]

of said upper frequency \( f_2 \), a time control device adapted to gate said clock pulses into said first counter, means coupling said information signal to said time control device, means connected to said time control device for causing said device to gate said clock pulses for a period

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where the data information signal has a frequency \( f \) with a period \( t \), and an output signal represented by

\[
k \frac{t-t_1}{t_2}
\]

where the reference information signal has a frequency \( f_2 \) with a period \( t_2 \), \( k \) being a constant of proportionality.

14. The apparatus of claim 13 including a central control means which during the second half of the "off" segment following a data information signal sets said first counting unit to the count produced by the output circuit during the preceding first half of the said "off" segment which is represented by

\[
k \frac{t_2-t_1}{t_2}
\]

while setting the count of said second counting unit to the count retained by said storage which is represented by

\[
k \frac{t-t_1}{t_2}
\]

said output circuit being controlled by said first and second counting units to produce during said second half of said "off" segment a digital output signal equal to

\[
k \frac{(t-t_1)}{t_2} \quad \text{or} \quad \frac{(t_2-t_1)}{t_2}
\]

which is equivalent to

\[
k \frac{f_1}{f_2}
\]

where

\[
t = \frac{1}{f}
\]

and

\[
t_1 = \frac{1}{f_1}
\]

15. The apparatus of claim 14 in which said central control means during the second half of said "off" segment following a data information signal sets said first counter to the count retained by said storage represented by

\[
k \frac{(t_2-t_1)}{t_2}
\]

while setting said second counting unit to the count produced by the output circuit during the preceding first half of said "off" segment.

16. The apparatus of claim 15 including a commutator device synchronized with the commutated information signals received by the apparatus and having a plurality of output lines for delivering respective commutated output signals produced by said output circuit during the second half of an "off" segment following receipt of a data information signal during an "on" segment.

17. The apparatus of claim 16 including a digital to analog translator receiving in digital form the converted output signals produced by said output circuit and delivering said converted signals in analog form to said commutator.

18. A system for converting a frequency modulated information signal having a frequency \( f \) variable within the range between an upper frequency \( f_1 \) and a lower frequency \( f_2 \) comprising, a source of clock pulses, a first counter adapted to generate an output signal when the count of said first counter corresponds to the period

\[
\frac{1}{f_1}
\]

of said upper frequency \( f_2 \), a time control device adapted to gate said clock pulses into said first counter, means coupling said information signal to said time control device, means connected to said time control device for causing said device to gate said clock pulses for a period
inversely related to the frequency of said information signal, a second counter, and means connected between said first and second counters and responsive to said output signal from said first counter for gating said gated clock pulses into said second counter.

19. A system according to claim 18, further including a divider, means coupling the outputs of said first and second counters to said divider whereby the output of said second counter is the numerator and the output of said first counter is the denominator, and means for actuating said divider after the gating period of said time control device.

20. A system for converting a frequency modulated information signal having a frequency \( f \) variable within the range between an upper frequency \( f_1 \) with a period \( t_1 \) and a lower frequency \( f_2 \) with a period \( t_2 \) comprising a time control device adapted to receive an information signal for determining a control period directly related to the reciprocal of the frequency \( f \) of the information signal, a first counting unit adapted for counting clock signals during the control period of said control device to produce a count directly related to the period \( t \) of said information signal, a second counting unit counting clock signals concurrently with said first counting unit after said first counting unit has attained a count corresponding to the period \( t_1 \) of the upper frequency \( f_1 \) and producing a count directly related to the difference between the period \( t \) of the information signal and the period \( t_2 \) of the upper frequency \( f_2 \), and an arithmetic divider circuit coupled to the outputs of said first and second counting units for delivering an output signal representing the quotient of the count of said second unit divided by the count of said first unit.

21. A system for converting a frequency modulated information signal having a frequency \( f \) variable within the range between an upper frequency \( f_1 \) with a period \( t_1 \) and a frequency \( f_2 \) with a period \( t_2 \) comprising a time control device adapted to receive an information signal for determining a control period related to the reciprocal of the frequency \( f \) of the information signal, a source of clock signals, a first counting unit adapted for counting said clock signals during the control period of said control device to produce a count related to the period \( t \) of said information signal, and a second counting unit counting said clock signals after the first counting unit has attained a count corresponding to the period \( t_1 \) of the upper frequency \( f_1 \).

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