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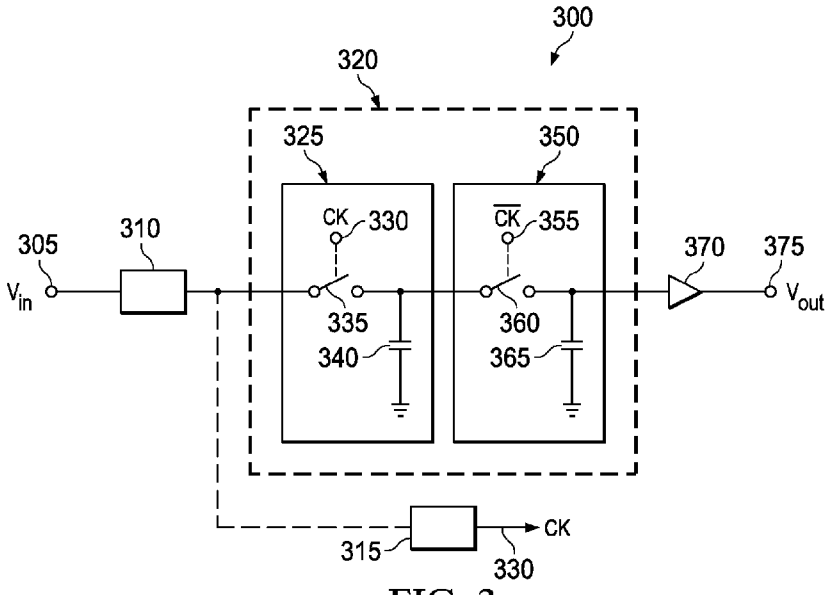


FIG. 3

(57) Abstract: A linear retimer (300) includes an equalizer (310), a clock recovery circuit (315), a sample and hold (S/H) circuit (320), and a linear driver (370). The equalizer receives an input signal (305) and outputs an equalized signal. The clock recovery circuit receives the equalized signal and outputs a clock signal (330). The S/H circuit receives the equalized signal and the clock signal and outputs a retimed signal. The linear driver receives the retimed signal and outputs a recovered signal (375). The S/H circuit is configured to preserve a voltage of the equalized signal in the retimed signal. In some examples, the S/H circuit is part of a linear three-tap feedforward equalizer, and the linear driver receives an output of the feedforward equalizer. The linear retimer can be placed between a transmitter and a channel or after the channel.

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[Continued on next page]

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— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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SAMPLE-AND-HOLD-BASED RETIMER SUPPORTING LINK TRAINING

BACKGROUND

[0001] Wired communications systems use link training to enable tuning of the finite impulse response (FIR) filters in the transmitters and receivers. However, nonlinear retimers cannot pass link training information directly from the input to the output. Instead, a digital signal processor detects the transmitter's FIR coefficients from the input signal and reconstructs it in the retimer output signal. The complex signal processing can consume large amounts of power.

SUMMARY

[0002] A retimer includes an equalizer, a clock recovery circuit, a sample and hold (S/H) circuit, and a linear driver. The equalizer receives an input signal and outputs an equalized signal. The clock recovery circuit receives the equalized signal and outputs a clock signal. The S/H circuit receives the equalized signal and the clock signal and outputs a retimed signal. The linear driver receives the retimed signal and outputs a recovered signal. The S/H circuit is configured to preserve a voltage of the equalized signal in the retimed signal. The retimer can be placed between a transmitter and a channel or after the channel.

[0003] In some examples, the S/H circuit is part of a three-tap feedforward equalizer, and the linear driver receives an output of the feedforward equalizer. In some examples, the S/H circuit is a first S/H circuit and the retimed signal is a first retimed signal. The three-tap FFE can include a second S/H circuit, a third S/H circuit, a first amplifier, a second amplifier, a third amplifier, and a summer. The second S/H circuit and the first amplifier receive the first retimed signal. The second S/H circuit outputs a second retimed signal, and the first amplifier outputs a first weighted signal. The third S/H circuit and the second amplifier receive the second retimed signal. The third S/H circuit outputs a third retimed signal, and the second amplifier outputs a second weighted signal. The third amplifier receives the third retimed signal and outputs a third weighted signal. The summer receives the first, second, and third weighted signals and combines them to obtain the FFE output signal.

[0004] In some examples, the S/H circuit includes two track and hold (T/H) circuits. One of the T/H circuits can include a preamplifier and a switched emitter follower. In some examples, the preamplifier includes a degeneration capacitor which has a capacitance chosen to extend a bandwidth

of the preamplifier. In some examples, the T/H circuit includes a feedforward capacitor coupled between the preamplifier and the switched emitter follower. A capacitance of the feedforward capacitor can be chosen to reduce hold mode feedthrough.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] For a detailed description of various examples, reference will now be made to the accompanying drawings in which:

[0006] FIG. 1 illustrates an example communication system including a nonlinear retimer.

[0007] FIG. 2 illustrates an example communication system including a linear retimer.

[0008] FIG. 3 illustrates a block diagram of an example linear retimer with a sample and hold circuit.

[0009] FIG. 4 illustrates a block diagram of an example linear retimer with a three-tap feedforward equalizer.

[0010] FIG. 5 illustrates an example track and hold amplifier for use in a sample and hold circuit.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0011] The disclosed retimers include a sample and hold (S/H) circuit to retime the received signal, which preserves the link training information while retiming jitter in the signal. Any appropriate S/H circuit may be used. The transmitter finite impulse response (FIR) coefficients are passed directly from the input to the output of the disclosed retimers without any complex digital signal processing. The retimers can be placed before or after the channel. A discrete-time linear feedforward equalizer can be implemented by cascading S/H circuits with weighted additions to reduce both precursor and postcursor inter-symbol-interference.

[0012] FIG. 1 illustrates an example communication system 100 including a nonlinear retimer 130 with a D flipflop 140. Communication system 100 includes a transmitter 110, the nonlinear retimer 130, and a receiver 150. A signal Vin 105 is provided to the transmitter 110 which includes a finite impulse response (FIR) filter 115. FIR filter 115 adds link training information to signal 120 output by transmitter 110, as shown in signal diagrams 120A-B which represent the voltage of signal 120 at a time t1 and signal 120 at time t2, respectively. Nonlinear retimer 130 includes an equalization module 135 and a D flipflop 140. The D flipflop 140 limits the voltage of signal 120 and cannot pass link training information to signal 145 output from nonlinear retimer 130.

[0013] The signal diagram 145A illustrates the constant voltage of signal 145 at time t1, in contrast to the varying voltage of signal 120 at time t1 as shown in signal diagram 120A. The signal diagram

145B illustrates the constant voltage of signal 145 at time t2, in contrast to the varying voltage of signal 120 at time t2. As illustrated in the signal diagrams 145A-B, the signal 145A at time t1 is the same voltage as the signal 145B at time t2, masking the link training information injected into signal 120 by the FIR 115 in transmitter 110. The signal 145 is provided to receiver 150 which outputs a signal Vout 155. Receiver 150 is unable to recover the link training information in signal 120 from FIR 115 in transmitter 110. A digital signal processor and a second FIR filter can be included in nonlinear retimer 130 to detect the link training information and reconstruct it at the second FIR filter, as described in U.S. Patent No. 9,210,008. However, the digital signal processor and a second FIR filter cause nonlinear retimer 130 to consume large amounts of power.

[0014] FIG. 2 illustrates an example communication system 200 including a linear retimer 230 with a sample and hold (S/H) circuit 240. Communication system 200 is substantially similar to communication system 100 shown in FIG. 1, but includes linear retimer 230 instead of nonlinear retimer 130. Linear retimer 230 includes S/H circuit 240 as a retiming element, rather than a flipflop such as D flipflop 140. The S/H circuit 240 is transparent to link training and can pass the transmitter FIR information reliably without the need for complex digital processing, while still retiming the jitter, causing linear retimer 230 to consume less power than nonlinear retimer 130. In addition because it is linear, retimer 230 can be placed before or after the channel such that the transmitter FIR filter 115 can equalize channels both before and after linear retimer 230.

[0015] The signal 245 output from linear retimer 230 is represented by signal diagrams 245A-B which illustrate voltage changes in signal 245A at time t1 and in signal 245B at time t2, in contrast to the constant voltage of signal 145 output from nonlinear retimer 130. Receiver 150 receives the signal 245 from linear retimer 230 and outputs signal Vout 255. As signal diagrams 245A-B illustrates, receiver 150 is able to retain the voltage changes in signal 120 output from transmitter 110 in the output signal 255. Although the example shown herein includes a signal with two voltage levels, the S/H circuit 240 linearly passes voltage information, and linear retimer 230 can be extended to three, four, or more voltage level signals as well.

[0016] FIG. 3 illustrates a block diagram of an example linear retimer 300 with a sample and hold circuit 320. Linear retimer 300 includes an equalizer 310, a clock and data recovery module 315, the S/H circuit 320, and a linear driver 370. Equalizer 310 can be any appropriate equalizer, such as a continuous time linear equalizer. In this example, S/H circuit 320 includes two track and hold (T/H) amplifiers 325 and 350. T/H amplifier 325 includes a switch 335 and a capacitor 340, and T/H

amplifier 350 includes a switch 360 and a capacitor 365. In T/H amplifier 325, switch 335 receives clock signal CK 330 from the clock and data recovery module 315 and is coupled between an output of equalizer 310 and T/H amplifier 350. Capacitor 340 is coupled to switch 335 and to ground 345.

[0017] In T/H amplifier 350, switch 360 receives a clock signal $\overline{CK}$ 355 that is inverted relative to clock signal CK 330, and is coupled between an output of T/H amplifier 325 and an input of linear driver 370. Capacitor 365 is coupled to switch 360 and to ground 345. Linear driver 370 receives the output from track and hold amplifier 350 and outputs the signal Vout 375. Because the S/H circuit 320 is linear, driver 370 is also linear to retain the transmitter FIR information.

[0018] FIG. 4 illustrates a block diagram of an example linear retimer 400 with a three-tap feedforward equalizer (FFE) 450. Linear retimer 400 is substantially the same as linear retimer 300 shown in FIG. 3, but includes a three-tap FFE 450 rather than a S/H circuit 320. Three-tap FFE 450 includes three S/H circuits 420A-C, three linear amplifiers 425A-C, and a linear summer 440. The three S/H circuits 420A-C each receive a clock signal CK 430 from the clock and data recovery module 415. S/H circuit 420A is coupled to an output of equalizer 410 and provides its output to S/H circuit 420B and to an amplifier 425A, which multiplies the output from S/H circuit 420A by a weight α-1.

[0019] S/H circuit 420B provides its output to S/H circuit 420C and to an amplifier 425B, which multiplies the output from S/H circuit 420B by a weight α0. S/H circuit 420C provides its output to an amplifier 425C, which multiplies the output from S/H circuit 420C by a weight α+1. Summer 440 subtracts the outputs of amplifiers 425A and 425C from the output of amplifier 425B, substantially cancelling out precursor and postcursor ISI. The output from summer 440 is provided to a linear driver 470, which outputs a signal Vout 475.

[0020] FIG. 5 illustrates an example T/H amplifier 500 for use in a S/H circuit such as S/H circuit 320 shown in FIG. 3. T/H amplifier 500 includes a preamplifier 540 with two switched emitter followers 550A-B. Preamplifier 540 includes a degeneration capacitor Cs 560 coupled in parallel with the degeneration resistor Rs. Preamplifier 540 exhibits a pole at approximately:

$$\frac{1}{(RL)(C1)},$$

where C1 represents an input capacitance of the switched emitter follower 550A or 550B, and a pole at approximately:

$$\frac{1+\frac{GmRs}{2}}{Rs\ Cs},$$

where Gm represents the transconductance of the transistors Q1 and Q2. Preamplifier 540 exhibits a zero at

$$\frac{1}{(Rs)(Cs)}.$$

The capacitance of Cs 560 can be chosen such that the zero at

$$\frac{1}{(Rs)(Cs)}$$

cancels out the pole at

$$\frac{1}{(RL)(C1)},$$

extending the bandwidth of T/H amplifier 500. Feedforward capacitors Cf 570A-B are coupled between preamplifier 540 and switched emitter followers 550A-B, respectively, and cancel hold mode feedthrough by opposing the effect of the base-emitter capacitance of transistors QEF1,2 respectively.

[0021] The term "couple" is used throughout the specification. The term may cover connections, communications, or signal paths that enable a functional relationship consistent with the description of the present disclosure. For example, if device A generates a signal to control device B to perform an action, in a first example device A is coupled to device B, or in a second example device A is coupled to device B through intervening component C if intervening component C does not substantially alter the functional relationship between device A and device B such that device B is controlled by device A via the control signal generated by device A.

[0022] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A retimer, comprising:

an equalizer configured to receive an input signal and output an equalized signal;

a clock recovery circuit configured to receive the equalized signal and output a clock signal;

a sample and hold (S/H) circuit configured to receive the equalized signal and the clock signal and output a retimed signal; and

a linear driver configured to receive the retimed signal and output a recovered signal.

2. The retimer of claim 1, wherein the S/H circuit is further configured to preserve a voltage of the equalized signal in the retimed signal.

3. The retimer of claim 1, wherein the S/H circuit comprises a first track and hold (T/H) circuit and a second T/H circuit.

4. The retimer of claim 3, wherein at least one of the first and second T/H circuits comprises:

a preamplifier; and

a switched emitter follower.

5. The retimer of claim 4, wherein the preamplifier further comprises a degeneration capacitor, wherein a capacitance of the degeneration capacitor is chosen to extend a bandwidth of the preamplifier.

6. The retimer of claim 4, wherein the at least one of the first and second T/H circuits further comprises a feedforward capacitor coupled between the preamplifier and the switched emitter follower, wherein a capacitance of the feedforward capacitor is chosen to reduce hold mode feedthrough.

7. The retimer of claim 1, wherein the retimer is configured to be placed between a transmitter and a channel.

8. The retimer of claim 1, wherein the retimer is configured to be placed after a channel.

9. The retimer of claim 1, wherein the S/H circuit comprises a linear three-tap feedforward equalizer (FFE), and wherein the linear driver is configured to receive an FFE output signal.

10. The retimer of claim 9, wherein the S/H circuit is a first S/H circuit, wherein the retimed signal is a first retimed signal, and wherein the linear three-tap FFE further comprises:

a second S/H circuit configured to receive the first retimed signal and output a second retimed signal;

a third S/H circuit configured to receive the second retimed signal and output a third retimed signal;

a first amplifier configured to receive the first retimed signal and output a first weighted signal;

a second amplifier configured to receive the second retimed signal and output a second weighted signal;

a third amplifier configured to receive the third retimed signal and output a third weighted signal; and

a summer configured to:

receive the first, second, and third weighted signals; and

combine the first, second, and third weighted signals to obtain the FFE output signal.

11. An apparatus, comprising:

an equalization circuit coupled to an input;

a clock recovery circuit coupled to an output of the equalization circuit;

a sample and hold (S/H) circuit coupled to an output of the clock recovery circuit and the output of the equalization circuit; and

a linear driver coupled to an output of the S/H circuit and to an output.

12. The apparatus of claim 11, wherein the S/H circuit comprises:

a first track and hold (T/H) circuit coupled to the output of the clock recovery circuit and the output of the equalization circuit; and

a second T/H circuit coupled to the output of the clock recovery circuit and an output of the first T/H circuit.

13. The apparatus of claim 12, wherein at least one of the first and second T/H circuits comprises:

a preamplifier coupled to an input of the at least one of the first and second T/H circuits;

a switched emitter follower coupled to an output of the preamplifier and to an output of the at least one of the first and second T/H circuits; and

a feedforward capacitor coupled between the preamplifier and the switched emitter follower.

14. The apparatus of claim 13, wherein a capacitance of the feedforward capacitor is chosen to reduce hold mode feedthrough.

15. The apparatus of claim 13, wherein the preamplifier exhibits a pole at:

$$\frac{1}{(RL)(C1)}$$

where RL represents a resistance of a load resistor in the preamplifier and C1 represents a capacitance of the switched emitter follower at the output of the preamplifier, wherein the preamplifier further comprises a degeneration capacitor, wherein the preamplifier exhibits a zero at:

$$\frac{1}{(Rs)(Cs)}$$

where Rs represents a resistance of a degeneration resistor in the preamplifier and Cs represents a capacitance of the degeneration capacitor, wherein the capacitance Cs is chosen such that the zero cancels out the pole.

16. The apparatus of claim 11, further comprising a linear feedforward equalizer (FFE) coupled to an output of the clock recovery circuit and the output of the equalization circuit, wherein the linear FFE comprises the S/H circuit.

17. An apparatus, comprising:

a first sample and hold (S/H) circuit configured to generate a first retimed signal;

a first amplifier configured to generate a first weighted signal based on the first retimed signal;

a second S/H circuit configured to generate a second retimed signal based on the first retimed signal;

a second amplifier configured to generate a second weighted signal based on the second retimed signal;

a third S/H circuit configured to generate a third retimed signal based on the second retimed signal;

a third amplifier configured to generate a third weighted signal based on the third retimed signal; and

a summer configured to combine the first, second, and third weighted signals.

18. The apparatus of claim 17, further comprising:

an equalization circuit configured to generate an input signal for the first S/H circuit;

a clock recovery circuit configured to generate a clock signal for the first, second, and third S/H circuits; and

a linear driver configured to generate an output signal based on an output from the summer.

19. The apparatus of claim 17, wherein at least one of the first, second, and third S/H circuits comprises a first track and hold (T/H) circuit and a second T/H circuit.

20. The apparatus of claim 19, wherein at least one of the first and second T/H circuits comprises:

a preamplifier; and

a switched emitter follower.

21. The apparatus of claim 20, wherein the preamplifier further comprises a degeneration capacitor configured to extend a bandwidth of the preamplifier.

22. The apparatus of claim 20, wherein the at least one of the first and second T/H circuits further comprises a feedforward capacitor coupled between the preamplifier and the switched emitter follower, wherein a capacitance of the feedforward capacitor is configured to reduce hold mode feedthrough.

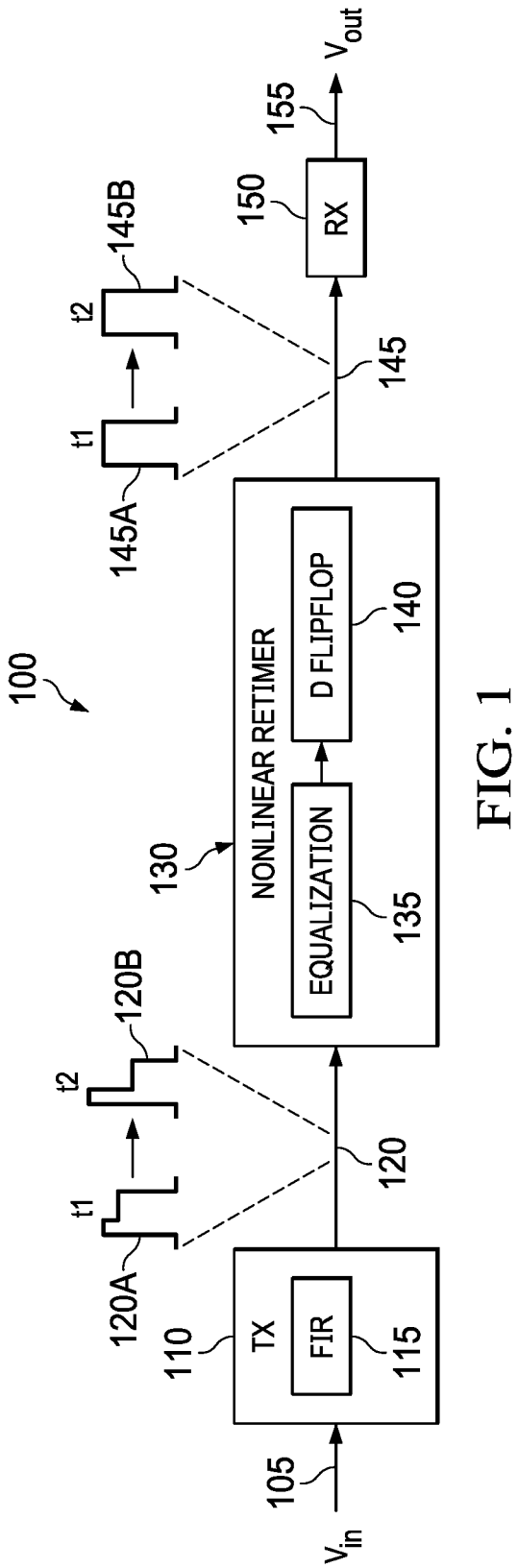

100
105
V_{in}
110
TX
FIR
115
120A
120B
t1
t2
120
130
NONLINEAR RETIMER
EQUALIZATION
135
D FLIPFLOP
140
145A
145B
145
150
RX
155
V_{out}

FIG. 1

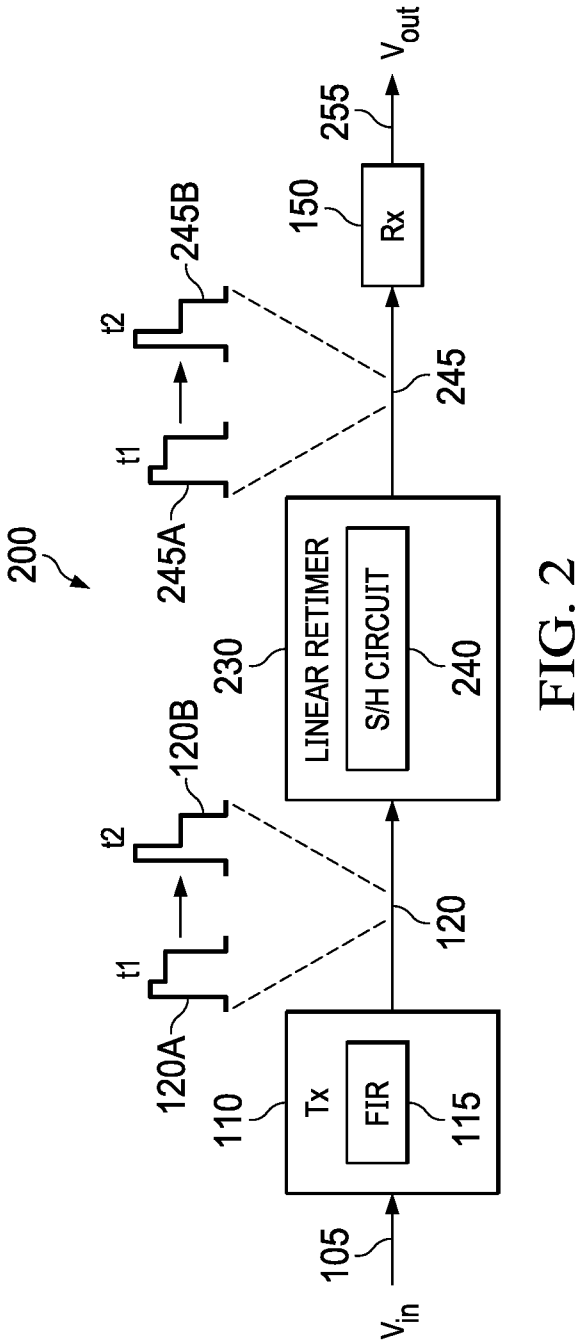

200
105
V_{in}
110
Tx
FIR
115
120A
120B
t1
t2
120
230
LINEAR RETIMER
S/H CIRCUIT
240
245A
245B
245
150
Rx
255
V_{out}

FIG. 2

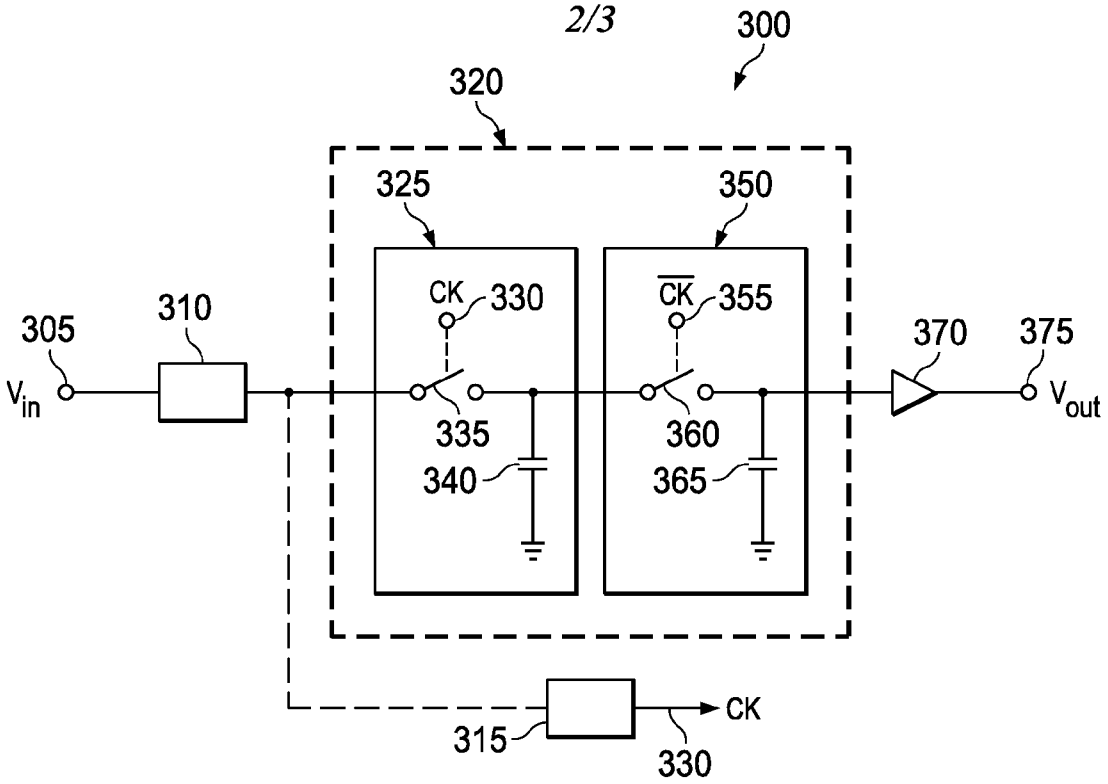

300
320
325
350
CK
330
CK
355
305
310
370
375
V_{in}
V_{out}
335
360
340
365
315
CK
330

FIG. 3

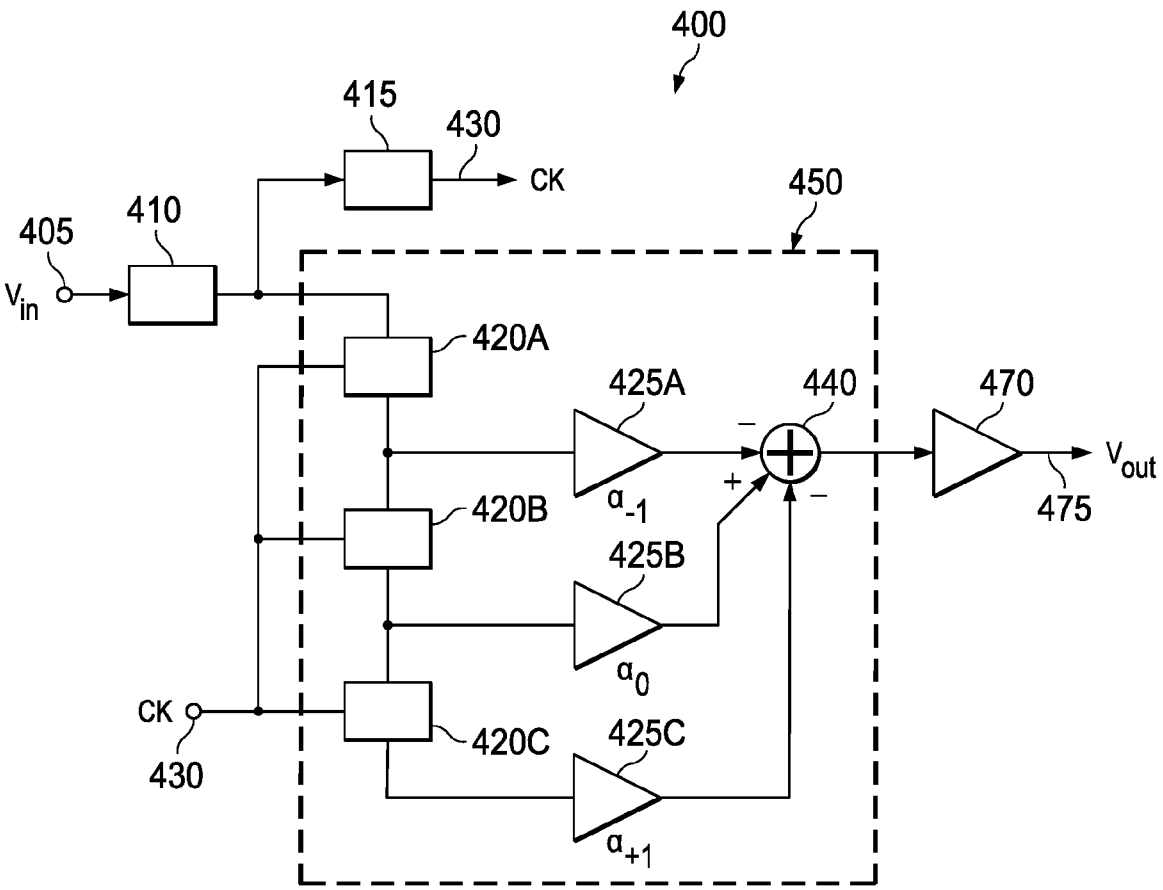

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415
430
CK
450
405
410
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420A
425A
440
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V_{out}
α_{-1}
475
420B
425B
α_0
CK
430
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425C
α_{+1}

FIG. 4

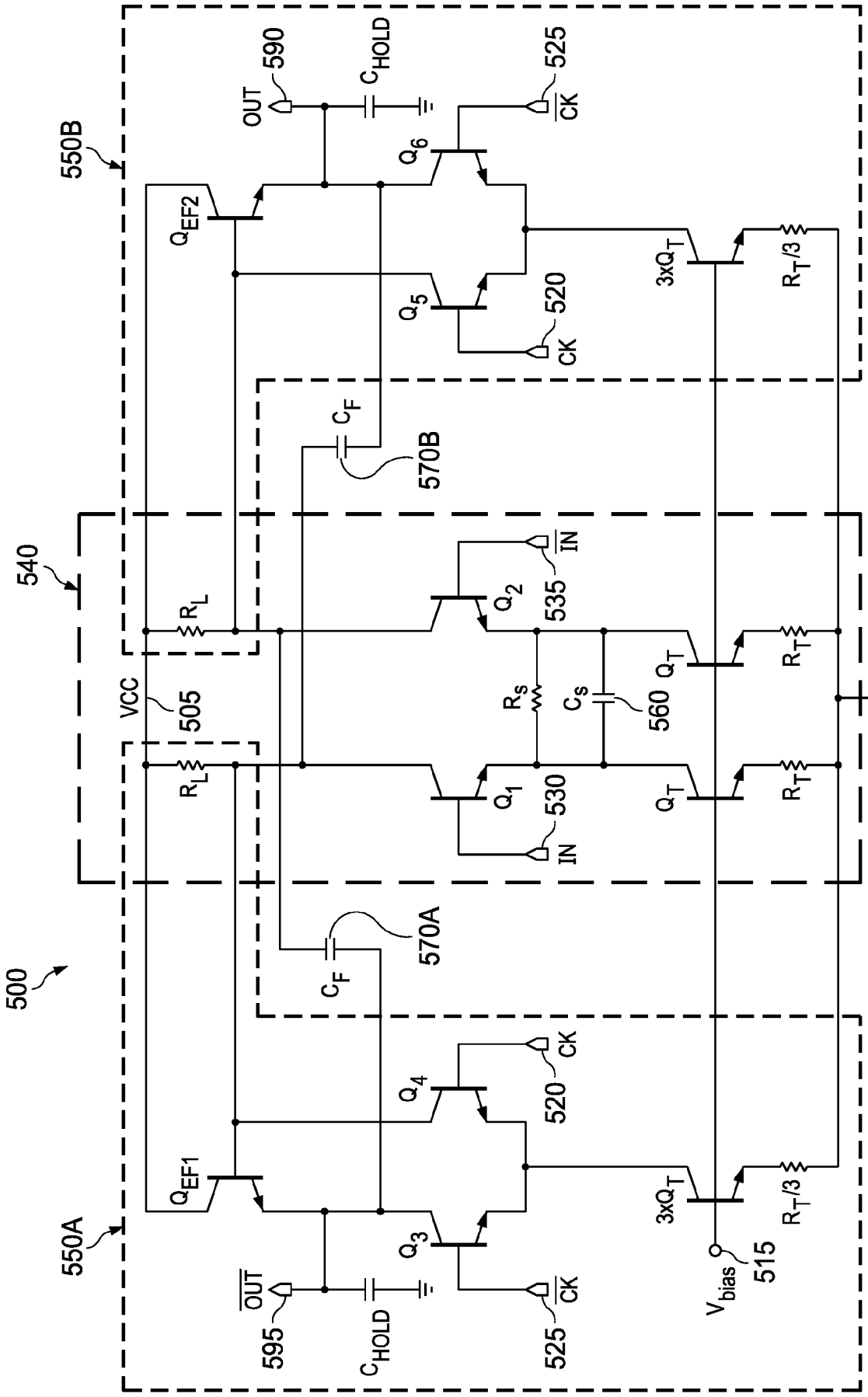

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550B
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OUT
590
C_{HOLD}
525
$\overline{CK}$
Q_6
Q_{EF2}
Q_5
520
CK
$3xQ_T$
$R_T/3$
C_F
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$\overline{IN}$
Q_2
535
R_L
VCC
505
R_s
C_s
560
Q_T
R_T
Q_1
530
IN
510
570A
Q_4
Q_{EF1}
Q_3
$\overline{OUT}$
595
V_{bias}
515

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2021/038220

A. CLASSIFICATION OF SUBJECT MATTER

H04L 7/00 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04L 7/00-7/027, 25/00-25/03, 1/00-1/18

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO Internal), USPTO, PAJ, Espacenet, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2019/0044760 A1 (INTEL CORPORATION) 07.02.2019, abstract, [0018], [0027], [0037]	1-22
A	US 9692589 B2 (INTEL CORPORATION) 27.06.2017	1-22
A	US 10659337 B2 (INPHI CORPORATION) 19.05.2020	1-22
A	US 2019/0363869 A1 (HUAWEI TECHNOLOGIES CO., LTD) 28.11.2019	1-22

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
14 September 2021 (14.09.2021)	14 October 2021 (14.10.2021)

Name and mailing address of the ISA/RU:	Authorized officer
Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	M. Smirnov Telephone No. 8(495)531-64-81