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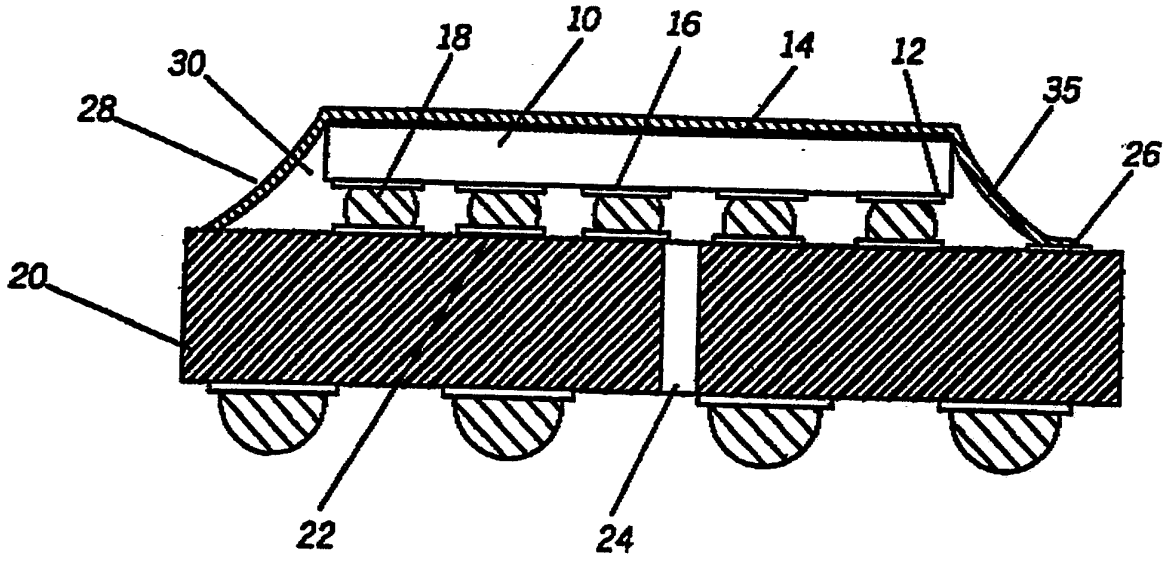
(54) Title: BACKPLANE GROUNDING FOR FLIP-CHIP INTEGRATED CIRCUIT



(57) Abstract

A semiconductor device package comprises a substrate (20) having a metallization pattern (22) on at least one surface, and a semiconductor device (10) having an active surface (12) and a grounded surface (14) on opposed sides. The semiconductor device is electrically attached to the substrate metallization pattern with the active surface (12) facing the substrate. A polymeric underfill material (30) substantially fills the space between the semiconductor device and the substrate. An electrically conductive material (35) covers the exposed grounded surface (14) of the semiconductor device and at least a portion of the metallization pattern (22), providing electrical connection between the grounded surface of the semiconductor and the metallization pattern (22) on the substrate.

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BACKPLANE GROUNDING FOR FLIP-CHIP INTEGRATED CIRCUIT

Technical Field

This invention relates generally to a semiconductor device package, and more specifically to a flip chip semiconductor device.

Background

Silicon integrated circuit chips are typically packaged in sealed enclosures, such as chip carriers or dual in-line packages (DIP), and interconnected with other components on printed circuit boards. The integrated circuit is typically connected to a carrier substrate with the active or upper surface of the integrated circuit facing away from the carrier substrate. Interconnections between the IC and the substrate is typically made by thin metal wires or wirebonds welded between the pads of the IC and the circuitry on the printed circuit board.

In an alternate packaging configuration known as flip chip, the integrated circuit is bonded directly to the substrate by means of solder bumps or other metal interconnects and is mounted with the active surface facing the printed circuit board. This type of interconnection eliminates the expense, unreliability, and low productivity of manual or automated wirebonding. It also allows the use of interior or array contacts as opposed to the limitation of using peripheral contacts with wirebonding methodology. The flip chip or control-collapse-chip-connection (C4) utilizes solder bumps deposited on wettable metal terminals of the chip and a matching footprint of solder wettable terminals on the substrate. The upside down flip chip is aligned to the substrate, and all interconnections are made simultaneously by reflowing the solder. This is opposite to the traditional method of bonding where the active side of the chip is facing up and is wirebonded to the substrate.

When chips are mounted in the conventional manner, that is, wirebonded, a ground connection to the backside ground plane of the chip can be made by forming a conductive connection between the backside ground plane of the chip and the ground of the printed circuit board. This is easily performed by means of conductive epoxy or solder,

for example. In flip-chip devices the connection of the ground plane of the IC to the ground of the substrate is more difficult because now the ground plane is facing away from the substrate. Wirebonds may be formed between the ground of the IC and the ground of the substrate but this negates the advantages realized by the flip-chip mounting scheme.

A method of achieving a ground connection between the back side ground of the flip chip and the ground of the circuitry is needed that eliminates the cumbersome, costly and unreliable wirebonds.

Summary of the Invention

Briefly, according to the invention, there is provided a semiconductor device package comprising a substrate having a metallization pattern on at least one surface, and a semiconductor device having an active surface and a grounded surface on opposed sides. The semiconductor device is electrically attached to the substrate metallization pattern with the active surface facing the substrate. A polymeric underfill material substantially fills the space between the semiconductor device and the substrate. An electrically conductive material covers the exposed grounded surface of the semiconductor device and at least a portion of the metallization pattern, providing electrical connection between the grounded surface of the semiconductor and the metallization pattern on the substrate.

In another embodiment, the semiconductor device package is a pad grid array chip carrier. The chip carrier comprises a printed circuit substrate having a metallization pattern on at least one surface and a flip chip. The flip chip has an active surface on one side and a grounded surface on a second opposed side. The flip chip is electrically attached to the metallization pattern with the active surface facing the printed circuit substrate. An underfill material substantially fills the space between the flip chip and the substrate metallization pattern, and a metal coating electrically connects the grounded surface of the flip chip to at least a portion of the metallization pattern.

Brief Description of the Drawings

FIG. 1 is a cross-sectional view of a flip chip mounted to a substrate with the back plane ground connection in accordance with the present invention.

Detailed Description of the Preferred Embodiment

Referring to FIG. 1, which is intentionally not to scale in order to clearly show certain features, an integrated circuit 10 has an active surface 12 on one side and a ground plane 14 on an opposite side. The active surface 12 consists of all the conventional circuitry found on an integrated circuit, for example, transistors, resistors, arrays, input/output pads, and passivation. The ground plane 14 is typically a continuous metal surface but may also have a pattern. The input/output pads 16 on the active surface 12 of the integrated circuit or flip chip 10 are metallized by attaching solder bumps 18 to the pads. The metallization of the pads may also be accomplished with other types of metallization, such as bonding a gold ball or plating or depositing other metals.

A carrier substrate 20 has a metallization pattern or conductor pattern 22 corresponding to the input/output pads and solder bumps 18 of the flip chip integrated circuit. In addition, the substrate 20 also has a ground connection 26 which may consist of a ground plane, a single runner, or a number of runners. The substrate may be a rigid or flexible printed circuit board material such as FR-4, reinforced polyimide, reinforced polyester, fluoropolymers, CEM, paper-phenolic, KAPTON®, or it may be a ceramic material. In the preferred embodiment, the substrate 20 is a printed circuit board material and has a size approximately the same or slightly larger than the integrated circuit, so as to form a chip carrier. The chip carrier is typically leadless and may be a perimeter type carrier or a pad grid array chip carrier with a plurality of solderable connections arranged in an array on the underside of the carrier substrate. Alternatively, pins may also be provided on the substrate. In an alternate embodiment, the carrier substrate 20 may be a much larger size and also contain other components, such as resistors, capacitors, switches, typically found on a printed circuit board.

The integrated circuit 10 is connected to the substrate 20 with the active surface 12 facing the metallization pattern 22. Interconnection

between the IC 10 and the substrate 20 is made by means of the solder bumps 18 which are aligned with the pads 22 of the substrate and reflowed.

After connection of the integrated circuit 10 to the substrate 20, the flip-chip assembly is underfilled with a sealing material 30. A liquid polymer, typically an epoxy, urethane, or an acrylic, is applied to the gap formed between the flip chip and the substrate. The sealing material 30 is applied around the perimeter of the IC 10 or can, alternatively, be applied from the backside of the substrate through a hole 24 in the substrate. An example of an underfill material may be found in U.S. Patent No. 4,999,699. The underfill polymer material 30 serves to environmentally protect the active surface 12 of the flip-chip IC and also to aid in mechanical attachment of the flip chip to the substrate. The underfill material 30 fills the void between the flip chip and the substrate and also extends a certain distance beyond the perimeter of the flip chip. Surface tension and wetting factors cause a concave fillet 28 to be formed around the perimeter of the flip chip. The liquid polymer material 30 is then cured by an appropriate means such as placing it in an oven to thermal cure, or by room temperature curing in the case of a two-product material, or by ultraviolet light, by radiation curing, or by radio-frequency energy.

In order to connect the back plane ground 14 of the flip chip 10 to the ground 26 of the substrate 20, a continuous film or coating of a conductive material is applied over the flip chip and the substrate. The coating of conductive material 35 is applied and covers the flip-chip IC, the concave fillets of the underfill material, portions of the substrate 20, and the ground connection 26 of the substrate. In this way connection is made between the substrate ground 26 and the back plane ground 14 of the IC. The conductive coating 35 may take several forms, depending upon the desired package. For example, if a pad array chip carrier is being fabricated, the conductive coating 35 may be a sputtered metal film such as copper, aluminum, titanium, chrome, or nickel. The sputtered film 35 may be additionally plated up by means of electroless or electro-plated metals, such as copper, to give it higher conductivity and greater physical resistance to abrasion. If the flip-chip IC 10 is part of a larger assembly, such as a circuit board or mother board having additional components,

the electrically conductive coating 35 may be formed by means of a conductive epoxy that is screen printed over the IC or dispensed on the IC and the substrate. Examples of conductive polymers are metal-filled epoxies or urethanes filled with copper, nickel, silver, gold, steel, stainless steel, or other metals.

In applying the underfill material 30 between the flip chip 10 and the substrate 20, it is very important that the underfill material not be allowed to extend beyond the flip chip so far that it covers the ground connection 26 on the substrate. A convenient way of preventing this is to apply a damming material in the area of the ground pin in order to prevent the spread of underfill material The use of a damming material or a barrier wall when encapsulating an integrated circuit is disclosed in U.S. Patent No. 4,843,036, which patent is incorporated herein by reference. The same techniques are used when applying an underfill material. In addition, the ground 26 may also be covered with a temporary masking, such as a photoresist or a latex mask, in order to prevent the underfill material 30 from covering the ground. The underfill material may be later removed by mechanical abrasion, by chemical etching, or removal with a laser beam. In any event, the ground connection 26 on the substrate 10 must be uncontaminated and available to be connected to the back plane ground 14 by the conductive material 35.

In this way, a simple and robust connection is easily and economically made between the back plane ground of a flip-chip IC and the ground of the substrate. This connection eliminates the need for wirebonding and it provides a package that also protects the active surface and the integrated circuit from environmental damage. These examples are presented by way of explanation and not by way of limitation and the invention herein is not intended to be limited except as by the appended claims.

What is claimed is:

Claims

1. A semiconductor device package, comprising:
a substrate having a metallization pattern on at least a first surface;
a semiconductor device having an active surface on a first side and a grounded surface on a second opposed side, said semiconductor device electrically attached to the substrate metallization pattern with the active surface facing the substrate first surface;
a polymeric underfill material substantially filling a space between the semiconductor device and the substrate metallization pattern; and
an electrically conductive material coating the grounded surface of the semiconductor device and at least a portion of the metallization pattern, and providing electrical connection between the grounded surface and said portion of the metallization pattern.

2. The semiconductor device package as described in claim 1, wherein the electrically conductive material covers portions of the polymeric underfill material, and portions of the substrate.

3. The semiconductor device package as described in claim 1, wherein the substrate is a ceramic, a flexible film, or printed circuit board material selected from the group consisting of FR-4, polyimide, CEM, paper-phenolic, or fluoropolymer.

4. A pad grid array chip carrier, comprising:

a printed circuit substrate having a metallization pattern on at least a first surface;

a flip chip having an active surface on a first side and a grounded surface on a second opposed side, said flip chip electrically attached to said metallization pattern with said active surface facing said printed circuit substrate first surface;

an underfill material substantially filling a space between the flip chip and the substrate metallization pattern; and

a metal coating electrically connecting the grounded surface of the flip chip and at least a portion of the metallization pattern.

5. The pad grid array chip carrier as described in claim 4, wherein the metal coating also covers portions of the underfill material, and portions of the printed circuit substrate.

6. The pad grid array chip carrier as described in claim 4, wherein the substrate is a printed circuit board material selected from the group consisting of FR-4, polyimide, CEM, paper-phenolic, or fluoropolymer.

7. The pad grid array chip carrier as described in claim 4, wherein the substrate is substantially the same size as the flip chip and forms a chip carrier.

8. A method of electrically connecting a back plane ground of a flip chip semiconductor to a substrate circuit, comprising the steps of:

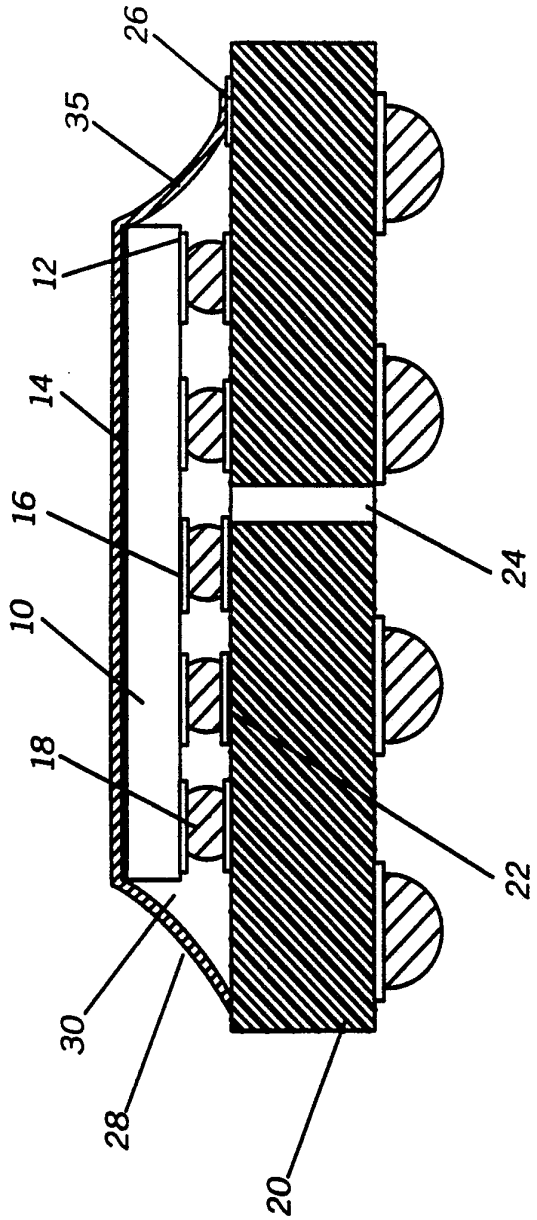
providing the flip chip connected to the substrate and having underfill between the flip chip and the substrate; and

coating the flip chip and portions of the substrate circuit with a conductive material so as to electrically connect the back plane ground to the substrate circuit.

9. The method as described in claim 8, wherein the conductive material is metal or a conductive polymer.

10. The method as described in claim 8, wherein the conductive material is applied by sputtering.

FIG.1



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/00720

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H01L 23/28,23/02,23/12
US CL :257,659; 361,397

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257,659; 361,397

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS, US Pat, Text File: Semiconductor Device, Substrate, Polymeric, Metallization, File Chip, Grid Array

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US,A, 4,999,699 (CHRISTIE ET AL) 12 MAY 1991 See abstract	1-7
Y	US,A, 4,820,013 (FUSE) 11 APRIL 1989 See fig. 1	1-7
A	US,A, 4,848,036 (SCHMIDT ET AL) 27 JUNE 1989 See claim 1	1 & 4
A	US,A, 4,996,629 (CHRISTIANNSEN ET AL) 26 FEBRAURY 1991 See col. 3, lines 6-49	

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 28 APRIL 1993	Date of mailing of the international search report 15 JUN 1993
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer DAVID Ostrowski Telephone No. (703) 308-0956

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/00720

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A, 4,801,999 (HAYNARD ET AL) 31 JANUARY 1989 See abstract	1&4
A	US,A, 3,811,183 (CELLING) 21 MAY 1974 See col. 3, lines 20-43	1-7
A,P	US,A, 5,121,190 (HSIAO ET AL) 09 JUNE 1992 See abstract & claim 1	1&4
A	US,A, 3,614,546 (AVINS) 19 OCTOBER 1971 See abstract	
A	US,A, 3,858,455 (NAYLOR) 15 JUNE 1971 See abstract	

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/00720

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

See attached sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1,2,3,4,5,6,7

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

Box II Observations where unity of invention is lacking (Cont'd)

Group I, claims 1-7, drawn to the invention, classified in class 257, subclass 697
Group II, claims 8-10, drawn to the invention, classified in class 437, subclass 180.

The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown(1) that the process as claimed can be used to make other and materially different products or (2) that the product as claimed can be made by another and materially different process. In the instant case, unpatentability of the group I invention would not necessarily imply unpatentability of the method of the group II invention, since the device of the group I invention could be made by processes materially different than that of the group II invention, for example, in claim 8, coat the entire substrate with the conductive material and then remove the conductive material selectively.

Because these inventions as recited in the claims do not have in common the same or corresponding "special technical features" as set forth in PCT Rule 13, unity of invention is lacking.