A method of entering memory module mounted on a memory system or a plurality of memories mounted on the memory module into a test mode, and a first register and a second register for performing the method are introduced. Each of the memory manufacturers provides a different MRS code for entering the memory into the test mode and a different method of entering the memory into the test mode from one another. As a result, the number of the test MRS is stored in the first register for controlling the memory, and the test MRS codes are programmed into the second register. Additionally, each of the bits stored in the first register used for determining the number of the test MRS corresponds to each of the second registers that store a corresponding test MRS code, respectively.
FIG. 7

START

SYSTEM BOOTING S602

OPERATING SYSTEM LOADING S604

F=1 ? S606

YES

SETTING MEMORY TEST MODE S612

NO

STANDBY MODE S608

PROGRAMMING MEMORY TEST REGISTER S610

PERFORMING TEST OPERATION S614

TEST IS COMPLETED? S616

YES

TEST MODE RELEASE F = 0 S618

NO

A

B
FIG. 8

START

ABP

MTE0=0 ?

YES

MTE1=0 ?

NO

DRO ACCESS

S702

S704

NO

A

S706

S708

YES

DR1 ACCESS

S710

S712

YES

MTEi=i ?

NO

DRI ACCESS

S714

B
METHOD AND APPARATUS FOR INTERFACING BETWEEN TEST SYSTEM AND EMBEDDED MEMORY ON TEST MODE SETTING OPERATION

BRIEF DESCRIPTION OF DRAWINGS

[0001] The above objects and other advantages of the present invention will become more apparent by describing in detail the exemplary embodiments thereof with reference to the accompanying drawings, in which:

[0002] FIG. 1 is a table illustrating a conventional normal mode MRS code of SDRAM;

[0003] FIG. 2 is a block diagram illustrating a motherboard of a system on which a memory is mounted according to an example embodiment of the present invention;

[0004] FIG. 3 is a block diagram illustrating a memory control hub shown in FIG. 2 according to an example embodiment of the present invention;

[0005] FIG. 4 is a table illustrating a memory test register shown in FIG. 3 according to an example embodiment of the present invention;

[0006] FIGS. 5 and 6 are timing diagrams for explaining an operation of a programmed test mode enter sequence shown in FIG. 4 according to an example embodiment of the present invention;

[0007] FIGS. 7 and 8 are flow charts for explaining an operation of a test mode enter sequence of a memory according to an example embodiment of the present invention; and

[0008] FIG. 9 is a block diagram illustrating a hub of a memory system according to an example embodiment of the present invention.

TECHNICAL FIELD

[0009] The present invention relates to a method and apparatus for interfacing between a memory test mode and an embedded memory, and more particularly to a method and apparatus, for interfacing between a memory test mode and an embedded memory, which are capable of improving a test environment of a memory that is only accessible via a logic circuit.

BACKGROUND ART

[0010] According as a density of a semiconductor IC has increased, a test for the semiconductor IC becomes more complex and becomes more difficult. Particularly, according as capacity of a semiconductor memory device increases to a unit of the GB (Giga Bit), overhead on a memory test time and a cost for testing the memory increases.

[0011] An SOC (System On Chip), an MML (Memory Merged Logic), a DSP (Digital Signal Processor), and a CPU (Central Processing Unit) embed a memory in those chips, and an FB-DIMM (Fully Buffered Dual Inline Memory Module) includes a hub and a memory embedded in its module. Consequently, it is difficult to test the embedded memory since a direct access to the memory from an outside of the chip or an outside of the memory module is impossible.

[0012] In the semiconductor memory module, it is required that the memory module mounted on a slot of a main board in a computer be tested. However, it is difficult to access the memory in the system board test environment outside the memory module.

[0013] As described above, in the memory test environment accessible only through the logic circuit, a test apparatus and an embedded self-test technique that consider the interface between the memory and the logic circuit are required.

[0014] According as an operation speed of a system on which a memory is mounted has increased and an amount of data to be processed has increased, performance of a main memory is considered as an important factor for upgrading performance of entire system.

[0015] The main memory sets up addresses and data for controlling a chip set of the system, the central processing unit (CPU) and peripheral devices. Accordingly, a fault of the main memory fatally affects performance of the entire system. The main memory includes a synchronous DRAM module.

[0016] The SDRAM includes a mode setting register (MSR). The SDRAM may operate in the programmed mode by programming a value of the MSR.

[0017] The MSR of the SDRAM may be programmed by storing a mode register set (MRS) command with address data in the MSR.

[0018] FIG. 1 is a table illustrating a conventional normal mode MRS code of SDRAM.

[0019] Referring to FIG. 1, an operation mode of the memory is determined based on data input to address input terminals of the memory A0 through A15, and BA0 through BA2.

[0020] Data input to each of the address input terminals are stored in a mode register of the memory chip, and a burst type, a burst length, a latency, a test operation mode, and ODT (On-Die Termination) DLL are set using the mode register.

[0021] An MRS (Mode Register Set) is applied to the memory during a system booting process, or is applied to the memory during DRAM initialization process of an ATE (Automatic Test Equipment). The normal MRS is standardized thus all of the systems use the normal MRS.

[0022] However, a test MRS used for testing the memory isn’t standardized and each of the memory manufacturers provide a different test MRS from one another.

[0023] Each of the memory manufacturers provides a unique test mode enter sequence so as to prevent the memory from entering into the test mode due to some errors in other operations except the test operation.

[0024] For example, the test mode enter sequence is continuously applied to the memory as many as several cycles. When all of the test mode enter sequences are applied, the memory enters into the test mode.

[0025] Accordingly, each of the memory manufacturers provides a test device, for the memory, that is capable of setting a unique test MRS.
However, when an embedded memory that can't be directly accessed or the memory is accessed through a logic circuit such as a system memory test environment, it was difficult to implement applications of a system. As a result, the test device for the memory couldn't control the test MRS of the embedded memory.

Further, in a system environment where a normal operation is performed after the system booting process is performed and then the operating system is loaded, it was impossible that the memory enters into the test mode.

OBJECT OF THE INVENTION

One object of the present invention provide a method of setting a test mode capable of improving a flexibility of a memory test environment by programming a test mode enter sequence into a register in a memory interface unit.

Another object of the present invention also provides a memory interfacing method and an apparatus using the same, which allow various memories having a different test mode enter sequence from one another and allow the various memories to adaptively enter into the test mode.

Still another object of the present invention also provides a hub for a memory module, a memory module and a system mounted with a memory that are suitable for performing the above-stated objects.

Still another object of the present invention also provides a method and an apparatus for freely setting a test mode entrance regardless of an operating condition of a system.

EMBODIMENTS OF THE INVENTION

In some embodiments of the present invention, there is provided a test mode interfacing method of a memory chip includes: programming test mode enter sequence data into a memory test register, the test mode enter sequence data corresponding to an embedded memory to be tested; checking whether a test mode setting command is inputted or not during a normal operation of the system; accessing the test mode enter sequence data programmed into the memory test register when the test mode setting command is inputted and then setting the embedded memory to the test mode.

An embedded memory in a broad meaning represents an embedded memory mounted in the SOC, a plurality of memories in a memory module that communicates with an external device in a method of packet data transmission such as the FBDIMM (Fully Buffered Dual Inline Memory Module), a memory that is mounted on a system board such as a motherboard and that is accessible through a predetermined logic circuit.

Generally, the embedded memory in a narrow meaning represents the embedded memory mounted in the SOC.

A normal operation mode of the system represents an operation state after an initial booting process of the system is performed and then, an operating system is loaded.

The test mode enter sequence data includes a sequence enable data for representing the number of the test mode enter sequence and test mode enter command data corresponding to the number of the test mode enter sequence.

The sequence enable data include a set of consecutive valid bits used for counting the number of the test mode enter sequences.

Each of the valid bits correspond to the test mode enter command data.

In a step of setting a test mode, one bit, for example, an LSB (Least Significant Bit) among the sequence enable data is accessed and then, the accessed bit value is verified whether the bit value is the valid value or not.

In response to the valid bit, a corresponding test mode enter command data is accessed and then a test mode setting signal is provided to the embedded memory in response to the accessed test mode enter command data.

The described above steps are continuously repeated corresponding to the number of the valid bits until the invalid bit appears, and when all of the test mode enter sequences are completed, the embedded memory is set to the test mode.

A readable/writable register is adapted for the memory test register.

In particular, a portion of a system PCI (Peripheral Component Interconnection) configuration register, or a portion of a configuration register in an AMB chip (Advanced Memory Buffer) of the FBDIMM (Fully Buffered Dual Inline Memory Module) may be used for the memory test register.

The register in which the sequence enable data are stored is named ‘TMESRR’ (Test Mode Enter Sequence Set Register), and the register in which the test mode enter command data are stored is named ‘TMESDR’ (Test Mode Enter Sequence Data Register).

The apparatus according to example embodiments of the present invention includes a controller configured to check the memory test register into which the test mode enter sequence data that correspond to the embedded memory to be tested are programmed, and configured to check whether the test mode setting command is applied or not during the normal operation mode of the system. The controller is also configured to access the test mode enter sequence data programmed into the memory test register when the test mode setting command is applied, and configured to set the embedded memory to the test mode.

It is noted that the controller is included in the SOC chipset, a memory controller hub chipset of the system memory, or the AMB (Advanced Memory Buffer) of the FBDIMM.

Hereinafter, example embodiments of the present invention will be mentioned with reference to attached drawings.

A FIRST EXAMPLE EMBODIMENT

A System Board Environment

FIG. 2 is a block diagram illustrating a main board of a system on which a memory is mounted according to an example embodiment of the present invention.
Referring to FIG. 2, the main board includes a CPU (Central Processing Unit; 200), a memory 220 and a memory control hub (MCH; 240 or North Bridge) chip set for controlling a graphic card 230, an input/output control hub (ICH; 270 or South Bridge) for controlling a PCI slot 250 and a port 260, a bus 280 for interfacing between the MCH 240 and the ICH 270.

In example embodiments of the present invention, a register of the MCH 240 includes a memory test register.

FIG. 3 is a block diagram illustrating a memory control hub shown in FIG. 2 according to an example embodiment of the present invention.

In the block of the memory control hub, only essential points will be described below.

Referring to FIG. 3, the memory control hub 240 includes a controller 242, a first register 244, a second register 246, a flag register 248 and I/O circuit 249.

A synchronous memory or a synchronous memory module is coupled to the controller 242 of the memory control hub 240 through the I/O circuit 249.

The controller 242 provides command signals CMD, address signals ADDR and data signals DATA to a plurality of memory chips 220.

Data read from the plurality of memory chips 220 are provided to the controller 242 as the data signals DATA. That is, the data signals DATA includes read data and write data.

The first register 244 is a test mode enter sequence set register (TMESSR) where test mode enter sequence sets are programmed.

The second register 246 is a test mode enter sequence data register (TMESDR) where test mode enter sequence data are programmed.

FIG. 4 is a table illustrating a first register and a second register shown in FIG. 3 according to an example embodiment of the present invention.

Referring to FIG. 4, the TMESRR 324 includes set bits MTE0 through MTE23 composed of 24 bits. The TMESRR 324 stores the number of test mode enter sequences. For example, if the test mode enter sequence includes 10 cycles, the set bits MTE0 through MTE9 are set to a logically valid value ‘1’, respectively, the other set bits MTE10 through MTE23 are set to a logically invalid value ‘0’, respectively.

It is noted that the logically valid value ‘1’ represents a valid set bit, and the logically invalid value ‘0’ represent an invalid set bit.

As a result, the TMESRR 324 composed of 24 bits has a programmed set bit value of ‘00 dFFh’ (0000 0000 0000 0111 1111 1). The TMESRR 324 is composed of 24 bits.

The TMESDR 326 includes 24 data registers DR0 through DR23, and the 24 data registers DR0 through DR23 correspond to each of the set bits MTE0 through MTE23 composed of 24 bits.

For example, the set bit MTE0 corresponds to the data register DR0, and the set bit MTE23 corresponds to the data register DR23.

Consequently, the test mode enter sequence data are programmed in the data register DRi corresponding to the set bit MTEi having the value of ‘1’.

As shown in FIG. 4, the valid data are stored in each of the data registers DR0 through DR9 corresponding to each of the set bits MTE0 through MTE9 having the value of ‘1’.

Each of the data registers DRi includes memory command information MTA23 through MTA19 such as CKE, CS, RAS, CAS, and WE, and memory address information MTA18 through MTA0.

In the example of embodiment of the present invention, each of the data registers DRi is composed of 24 bits, however, the total bit composition is not limited to 24 bits. That is, DQ or DQS may be added.

Accordingly, test operators may program the first register 244 and the second register 246 based on each of the test mode enter sequences made by each of the memory manufacturers.

FIGS. 5 and 6 are timing diagrams for explaining an operation of a programmed test mode enter sequence shown in FIG. 4 according to an example embodiment of the present invention.

Referring to FIG. 5, each of the data registers DR0, DR2, DR5, and DR8 corresponding to the set bits MTE0, MTE2, MTE5, and MTE8 has the logically invalid value ‘0’, and the data register DR4 corresponding to the set bit MTE4 has the logically invalid value ‘0’.

Referring to FIG. 6, command sequence is applied to the memory chip 220 in sequence of MRS, NOP, MRS, NOP, CKE, MRS, NOP, NOP, MRS, –NOP synchronized with clock signals CK+ and CK– since data, stored in each of the data registers DR0 through DR9 corresponding to the set bits MTE0 through MTE9 of the first register 244, are sequentially read.

Corresponding to the four MRS commands, the MRS address data are provided to the memory chip 220 four times. That, three times dummy test MRS and once normal test MRS are performed, respectively.

The memory chip 220 enters into a test mode based on the fourth test MRS.

The three times dummy test MRS is for preventing the memory chip 220 entering into the test mode due to an abnormal operation, and the three time dummy test MRS may be variable by each of the manufacturers.

Alternatively, the normal test MRS may be continuously performed after two times dummy test MRS.

As described above, the memory may be tested by programming the test mode enter sequences in the first register and the second register.

In the example embodiment of the present invention, after an operating system is loaded as well as during a system booting process, a flag register 248 shown in FIG. 3 is further included so that the memory chip 220 enters into the test mode.

That is, when a value of the flag register 248 is ‘0’, the memory chip 220 may enter into the test mode during the
system booting process, and when the value of the flag register 248 is ‘1’, the memory chip 220 may enter into the test mode during some time periods except the system booting process.

[0080] FIGS. 7 and 8 are flow charts for explaining an operation of a test mode enter sequence of a memory according to an example embodiment of the present invention.

[0081] Referring to FIG. 7, when a power is on, a system processor 210 shown in FIG. 2 as the CPU executes ROM BIOS to initialize a system (step S602).

[0082] That is, the system processor 210 executes ROM BIOS to perform a POST (Power On Self Test).

[0083] The POST includes a CPU test, a ROM BIOS check sum test, a DMA controller test, an interrupt controller test, a timer test, a main memory size check, an interrupt vector table initialization, a video test, a memory test, a coprocessor check, each port check, a disk controller check, a keyboard check, and a mouse check.

[0084] Data for the memory test register are programmed in the CMOS BIOS, and during the system booting process, the data stored in the CMOS BIOS are written into the memory test register TMESSR and TMESDR.

[0085] While the data in the CMOS BIOS are written to the memory test register, a value of the MTE0 is read. If the value of the MTE0 is ‘0’, a memory test mode setting does not occur, or if the value of the MTE0 is ‘1’, data of the data register DR0 are transferred to the memory chip 220 to perform the memory test mode setting.

[0086] When the POST process is completed, an operating system is loaded (step S604).

[0087] That is, the operating system stored in a hard disk is loaded to the memory, and users may use a computer under control of the operating system.

[0088] A value of the flag register 248 is checked (step S606), and when the value of the flag register 248 is ‘0’, a normal operation standby mode is performed (step S608).

[0089] During the normal operating standby mode, test operators programs the memory test registers 244, 246 and 248 when the test operators needs to test the memory (step S610).

[0090] The test mode enter sequence data corresponding to the memory to be tested are provided to the system, and the test mode enter sequence are stored in the TMESSR 244 and the TMESDR 246 included in the PCI CFG register. Then the test mode enter sequence data are programmed.

[0091] According as the test mode enter sequence data of the memory test register are programmed, the value of the flag register 248 is set to ‘1’.

[0092] At the step of S606, when the value of the flag register 248 is ‘1’, the memory test mode setting is performed (Step S612).

[0093] FIG. 8 is a flowchart for explaining a memory test mode setting step S612 shown in FIG. 7 according to an example embodiment of the present invention.

[0094] Referring to FIG. 8, when a value of the flag register is ‘1’, the controller 242 provides an ABP command to the memory to precharge all of the memory cells in the memory (step S702).

[0095] The controller 242 checks (or verifies) whether the MTE0 of the TMESSR 244 has the value ‘0’ (step S704).

[0096] When the value of the MTE0 is ‘0’, it is determined that the data register DR0 of the TMESDR 246 is not programmed or it is determined as a failure. As a result, a node A (i.e., current process flow) passes through the step S618 of FIG. 7, and the node A is released from the test mode.

[0097] In the step S704, when the value of the MTE0 is ‘1’, the controller 242 accesses the data register DR0 of the TMESDR 246 (step S706). The test MRS command corresponding to the data fetched from the data register DR0 is applied to the memory.

[0098] Continuously, the controller 242 checks (or verifies) whether the MTE1 of the TMESSR 244 has the value ‘0’ (step S 708).

[0099] When the value of the MTE1 is ‘0’, it is determined that the data register DR1 of the TMESDR 246 is not programmed or it is determined as a failure. As a result, the current process flow passes through a node B shown in FIG. 7 and then, the step S614 of FIG. 7 is performed. In the step S614, a predetermined test operation is performed.

[0100] In the step S616, the controller checks whether the predetermined test operation is completed or not. When the predetermined test operation is completed, the step S616 is performed.

[0101] In the step S708, when the value of the MTE1 is ‘1’, the controller 242 access the data register DR1 of the TMESDR 246 (step S710).

[0102] The memory test mode setting process is continuously performed until the data register DRi of the TMESDR 246 is accessed to perform the test MRS sequence corresponding to the data fetched from the data register DRi (step S714).

[0103] As described above, each the value of the MTE0 through the MTE9 is checked to sequentially access each test mode enter sequence data of the data register DR0 through DR9. Accordingly, the test MRS command sequence shown in FIG. 6 is generated, and the generated test MRS command sequence is applied to the memory.

[0104] When the test MRS command sequence is applied to the memory as many as 10 cycles, the memory successively enters into the test mode and then the memory is set to the test mode.

[0105] However, if one cycle among the 10 cycles is determined as a failure, the memory doesn’t enter into the test mode.

[0106] Therefore, a system operator may freely test the memory by programming the memory test register.

A SECOND EXAMPLE EMBODIMENT

A Packet Type Memory Module

[0107] FIG. 9 is a block diagram illustrating a hub of a memory system according to an example embodiment of the present invention.
Referring to FIG. 9, the hub of the memory system includes a data transmitting/receiving unit 812, a first interface unit 814, a second interface unit 816 and a data processing unit 818.

The data transmitting/receiving unit 812 includes a first receiver SRx, a first transmitter STx, a second receiver NRx, and a second transmitter NTx.

The first receiver SRx included in a first module 800-1 is coupled to a bus 802 so as to receive a south bound packet (SBP) from a memory controller 800.

The SBP received through the first receiver SRx is coupled to the first transmitter STx. The first transmitter STx is coupled to a first receiver SRx included in an adjacent module 800-2 so as to transmit the SBP.

The bus 802 and a bus 804 are for transferring the SBP. The buses 802 and 804 transfer an identical SBP, respectively, however, the buses 802 and 804 are isolated from each other. Thus, the buses 802 and 804 are coupled to each other in a point-to-point configuration.

The first interface unit 814 includes a flag register RG1, a test mode enter sequence register (TMESCR; RG2), a test mode enter sequence data register (TAMESDR; RG3) and a detection register RG4 so that the first interface unit 814 transmits/receives system management information to/from the memory controller 800 through a system management bus 809.

The first interface unit 814 stores a test mode setting signal, provided from the memory controller 800 through the SMBUS 809 as shown in FIG. 9, in the flag register RG1, and stores the number of the test mode enter sequences in the test mode enter sequence register (TMESCR; RG2) and stores the test mode enter sequence data in the test mode enter sequence data register (TAMESDR; RG3).

That is, a test set flag value composed of 1 bits is stored in the RG1, and a sequence enable data composed of 24 bits are stored in the RG2, and 24 test mode enter command data composed of 24 bits are stored in the RG3.

As mentioned above, after the registers RG1, RG2 and RG3 included in the memory module are programmed, the data processing unit 818 performs the test mode set sequence based on the process illustrated in FIGS. 7 and 8, and then the memory chips in the memory module enter into the test mode.

As a result, test operators may easily program the test mode sequences that are matched with the test mode sequence corresponding to each of the memory chips in the memory module.

EFFECTS OF THE INVENTION

As stated above, the memory module having a BIST circuit or at least one memory mounted on the system may easily enter into the test mode regardless of memory manufacturers. Therefore, memory test time and memory test coverage may be improved.

This invention has been described above with reference to the aforementioned embodiments. It is evident, however, that many alternative modifications and variations will be apparent to those having skills in the art in light of the foregoing description. Accordingly, the present invention embraces all such alternative modifications and variations as fall within the spirit and scope of the appended claims.

1. A test mode interfacing method of an embedded memory, the method comprising:

programming test mode enter sequence data into a memory test register, the test mode enter sequence data corresponding to the embedded memory to be tested;

checking whether a test mode setting command is inputted or not during a normal operation of a system; and

accessing the test mode enter sequence data programmed in the memory test register when the test mode setting command is inputted, and then setting the embedded memory to the test mode.

2. The test mode interfacing method of claim 1, wherein the test mode enter sequence data comprises:

sequence enable data for representing the number of the test mode enter sequences; and

a plurality of test mode enter command data corresponding to the number of the test mode enter sequences.

3. The test mode interfacing method of claim 2, wherein the sequence enable data includes a set of consecutive valid bits for counting the number of the test mode enter sequences.

4. The test mode interfacing method of claim 3, wherein each of the consecutive valid bits corresponds to each of the test mode enter command data.

5. The test mode interfacing method of claim 4, wherein the setting the embedded memory to the test mode comprises:

accessing one bit among the sequence enable data;

determining whether the accessed bit has a valid bit value or an invalid bit value;

accessing the test mode enter command data corresponding to the sequence enable data in response to the valid bit;

providing a test mode setting signal to the embedded memory in response to the accessed test mode enter command data; and

repeating the accessing one bit, the determining, the accessing the test mode enter command data corresponding to the sequence enable data in response to the valid bit, and the providing a test mode setting signal as many as the number of the valid bits until the accessed sequence enable data is determined as the invalid bit value.

6. The test mode interfacing method of claim 2, wherein the test mode enter command data includes test mode register set command data and address data.

7. The test mode interfacing method of claim 1, wherein the memory test register includes a PCI (Peripheral Component Interconnection) configuration register of the system.

8. The test mode interfacing method of claim 1, wherein the memory test register includes a configuration register in an AMB (Advanced Memory Buffer) of an FBDIMM (Fully Buffered Dual Inline Memory Module).
9. A test mode interfacing apparatus of an embedded memory, the apparatus comprising:

- a memory test register into which test mode enter sequence data are programmed, the test mode enter sequence data corresponding to an embedded memory to be tested; and

- a controller configure to check whether a test mode setting command is inputted or not during a normal operation of a system, and configured to access the test mode enter sequence data programmed into the memory test register when the test mode setting command is inputted, and configured to set the embedded memory to the test mode.

10. The test mode interfacing apparatus of claim 9, wherein the test mode interfacing apparatus is included in a system chip set, and wherein the memory test register includes a PCI (Peripheral Component Interconnection) configuration register in the system chip set.

11. The test mode interfacing apparatus of claim 9, wherein the test mode interfacing apparatus is included in an AMB (Advanced Memory Buffer) chip set of an FMDIHM (Fully Buffered Dual Inline Memory Module), and wherein the memory test register includes a configuration register in the AMB chip set.

12. The test mode interfacing apparatus of claim 9, wherein the test mode interfacing apparatus is included in an SOC (System On Chip) chip set, and wherein the memory test register includes a configuration register of the SOC chip set.

13. The test mode interfacing apparatus of claim 9, wherein the test mode enter sequence data programmed into the memory test register comprises:

- sequence enable data for representing the number of the test mode enter sequences; and

- test mode enter command data corresponding to the number of the test mode enter sequences.

14. The test mode interfacing apparatus of claim 13, wherein the sequence enable data includes a set of consecutive valid bits for counting the number of the test mode enter sequences.

15. The test mode interfacing apparatus of claim 14, wherein each of the consecutive valid bits corresponds to each of the test mode enter command data.

16. The test mode interfacing apparatus of claim 15, wherein the controller, when the test mode setting command is inputted, accesses one bit among the sequence enable data, determines whether the accessed bit has a valid bit value or an invalid bit value, accesses the test mode enter command data corresponding to the sequence enable data in response to the valid bit, provides a test mode setting signal to the embedded memory in response to the accessed test mode enter command data, and

repeats the accessing one bit, the determining, the accessing the test mode enter command data corresponding to the sequence enable data in response to the valid bit, and the providing a test mode setting signal as many as the number of the valid bits until the accessed sequence enable data is determined as the invalid bit value.

17. The test mode interfacing apparatus of claim 13, wherein the test mode enter command data includes test mode register set command data and address data.

18. An interfacing method in which a test mode enter sequence of a memory chip is programmable, the method comprising:

- reading one setting bit from test mode enter sequence setting register;

- determining whether the read setting bit has a valid bit value or an invalid bit value;

- reading corresponding enter sequence data from the test mode enter sequence data register in response to the valid setting bit;

- performing the test mode enter sequence by repeating the reading one setting bit, the determining, the reading corresponding enter sequence data, and the providing a test mode setting signal as many as the number of the valid setting bits until the read setting bit is determined as the invalid bit value.

19. The interfacing method of claim 18, wherein the valid setting bits include the number of test mode enter sequences of the memory chip, and are programmed into the test mode enter sequence setting register.

20. The interfacing method of claim 19, wherein the valid setting bits are sequentially read from an LSB (Least Significant Bit) to an MSB (Most Significant Bit) of the test mode enter sequence setting register.

21. The interfacing method of claim 18, wherein the test mode enter sequence data are sequentially pre-programmed into the test mode enter sequence data register as a data sequence corresponding to the test mode enter sequence of the memory chip.

22. The interfacing method of claim 18, wherein the test mode enter sequence data includes the mode register set command data of the memory chip and address data.

23. The interfacing method of claim 18, further comprising the mode register set command data of the memory chip and address data.

24. An interfacing apparatus in which a test mode enter sequence of a memory chip is programmable, the apparatus comprising:

- a test mode enter sequence setting register that stores at least one setting bit;

- a test mode enter sequence data register that stores at least one enter sequence data; and

- a controller configured to read one setting bit from the test mode enter sequence setting register, configured to determine whether the read setting bit has a valid bit value or an invalid bit value, configured to read corresponding enter sequence data from the test mode enter sequence data register in response to the valid setting bit, configured to provide a test mode setting signal to the memory chip in response to the read enter sequence data, and configured to perform the enter sequence by repeating the reading one setting bit, the determining, the reading corresponding enter sequence data, and the providing a test mode setting signal as many as the
number of the valid setting bits until the read setting bit is determined as the invalid bit value.  

25. The interfacing apparatus of claim 24, wherein the valid setting bits includes the number of test mode enter sequences of the memory chip, and are pre-programmed in the test mode enter sequence setting register.  

26. The interfacing apparatus of claim 24, wherein the enter sequence data are sequentially pre-programmed in the test mode enter sequence data register as a data sequence corresponding to the test mode enter sequence of the memory chip.  

27. The interfacing apparatus of claim 24, wherein the interfacing apparatus corresponds to a hub mounted in a memory controller or a memory module.  

28. A hub for a memory module, the hub comprising:  

a test mode enter sequence setting register that stores at least one setting bit;  

a test mode enter sequence data register that stores at least one enter sequence data;  

an output circuit configured to output a test mode setting signal to at least one memory chip; and  

a controller configured to read one setting bit from the test mode enter sequence setting register, configured to determine whether the read setting bit has a valid bit value or an invalid bit value, configured to read corresponding enter sequence data from the test mode enter sequence data register in response to the valid setting bit, configured to provide a test mode setting signal to a memory chip in response to the read enter sequence data, and configured to perform the enter sequence by repeating the reading one setting bit, the determining, the reading corresponding enter sequence data and the providing a test mode setting signal as many as the number of the valid setting bits until the read setting bit is determined as the invalid bit value.  

29. A memory module comprising:  

a plurality of memory chips that is able be set to a test mode;  

a test mode enter sequence setting register that stores at least one setting bit;  

a test mode enter sequence data register that stores at least one enter sequence data;  

an output circuit configured to output a test mode setting signal to at least one memory chip; and  

a controller configured to read one setting bit from test mode enter sequence setting register, configured to determine whether the read setting bit has a valid bit value or an invalid bit value, configured to read corresponding enter sequence data from the test mode enter sequence data register in response to the valid setting bit, configured to provide a test mode setting signal to a memory chip in response to the read enter sequence data, and configured to perform the enter sequence by repeating the reading one setting bit, the determining, the reading corresponding enter sequence data and the providing a test mode setting signal as many as the number of the valid setting bits until the read setting bit is determined as the invalid bit value.  

30. A system on which a memory is mounted comprising:  

at least one memory chip that is able be set a test mode; and  

a memory controller configured to read one setting bit from a first register, configured to determine whether the read setting bit has a valid bit value or an invalid bit value, configured to read corresponding enter sequence data from a second register in response to the valid setting bit, configured to provide a test mode setting signal to the memory in response to the read enter sequence data, and configured to perform a test mode enter sequence by repeating the reading one setting bit, the determining, the reading corresponding enter sequence data and the providing a test mode setting signal as many as the number of the valid setting bits until the read setting bit is determined as an invalid bit value.