

[54] **SEQUENCING TIMERS**
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328/131, 317/141 S
[51] Int. Cl. **H03k 17/28**, H03k 17/30,
H03k 17/72
[58] Field of Search 307/227, 228, 293, 252 F;
328/129, 130, 131; 317/141 S

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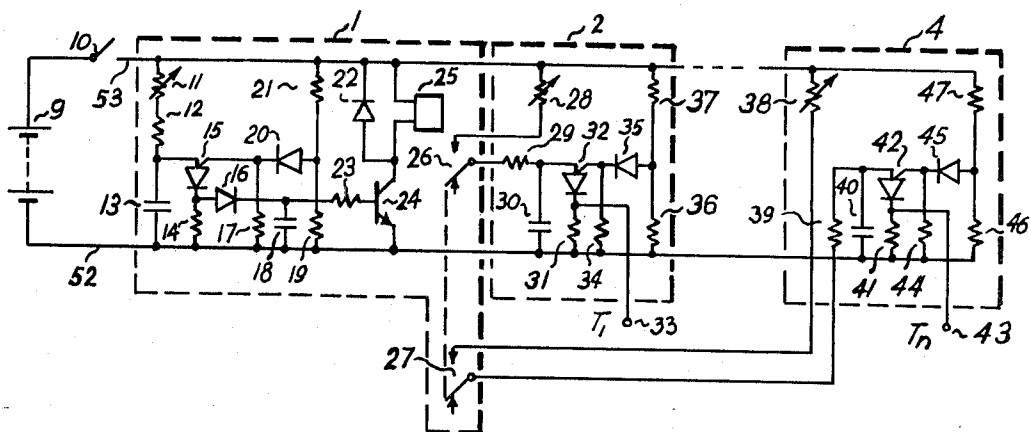
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Primary Examiner—Stanley D. Miller, Jr.

[57] **ABSTRACT**
A sequencing timer for providing independently ad-
justable time intervals of same or different durations
starting at the same time or at the end of the preced-
ing interval as applicable. Clock frequency, produced
in a clock oscillator, is used to synchronise the incre-
mental charging of one or more capacitors each being
part of an adjustable RC timer. Using a relay with
multiple, mutually isolated, contacts operated at given
clock frequency both high insulation of the timing ca-
pacitor and its incremental charging are achieved. As
result, stable short or long time intervals are obtained
on relatively wide ambient temperature range. Inde-
pendent intervals can range from seconds to hours.

8 Claims, 9 Drawing Figures



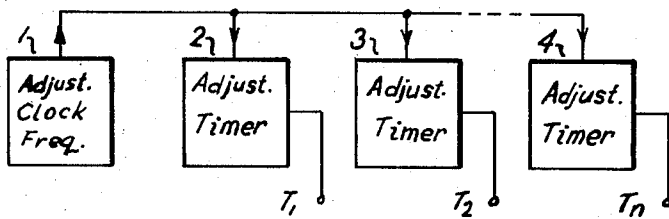


Fig. 1

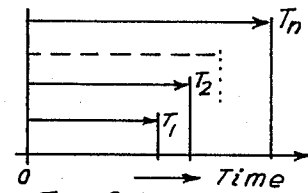


Fig. 2

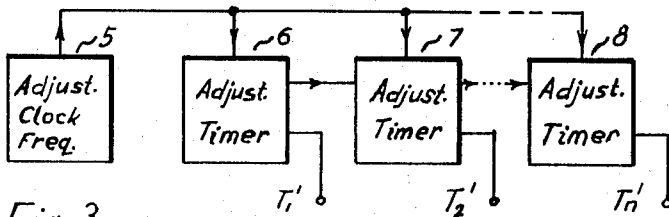


Fig. 3

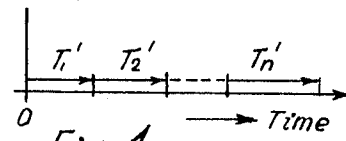


Fig. 4

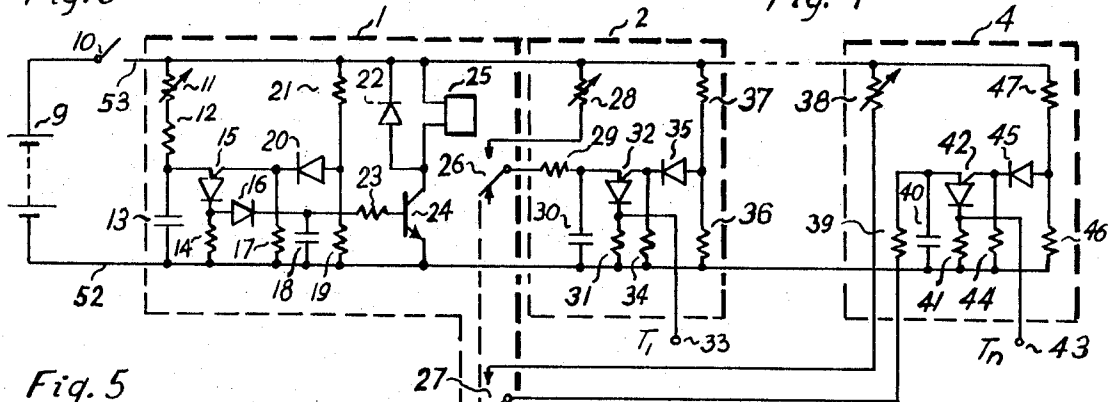


Fig. 5

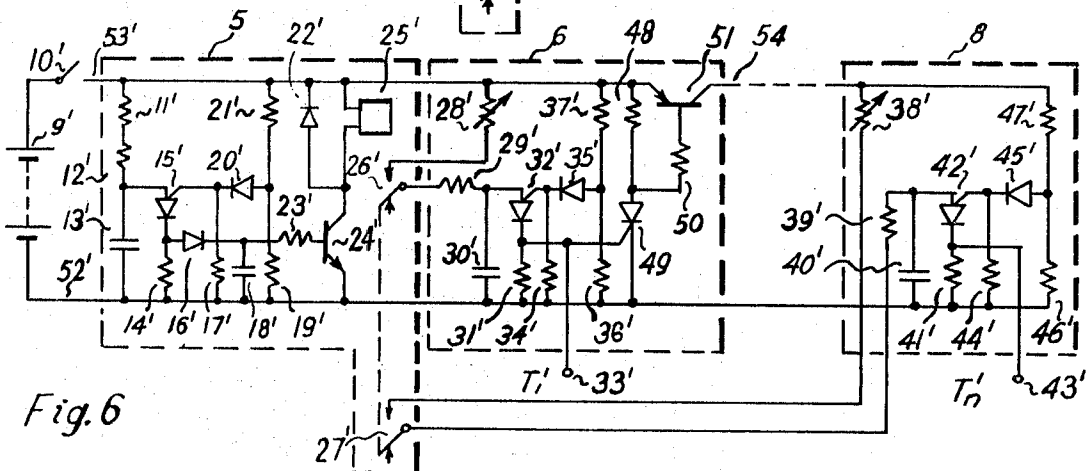


Fig. 6

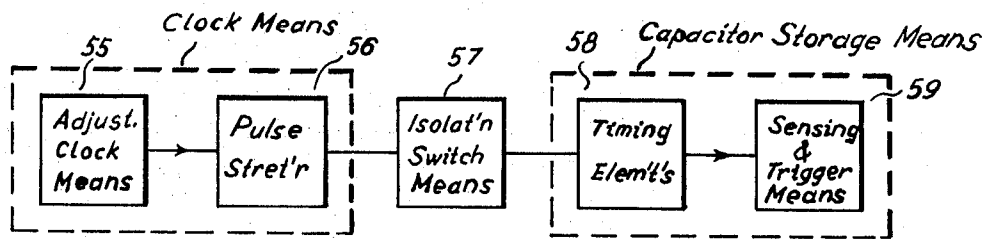


Fig. 7

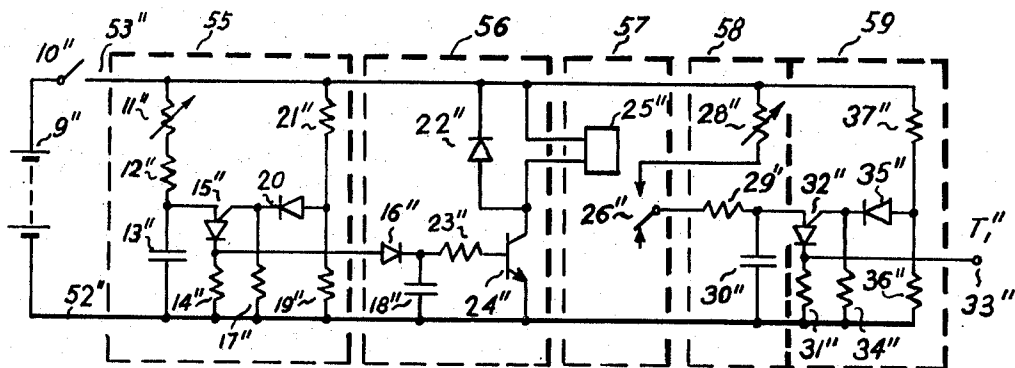


Fig. 8

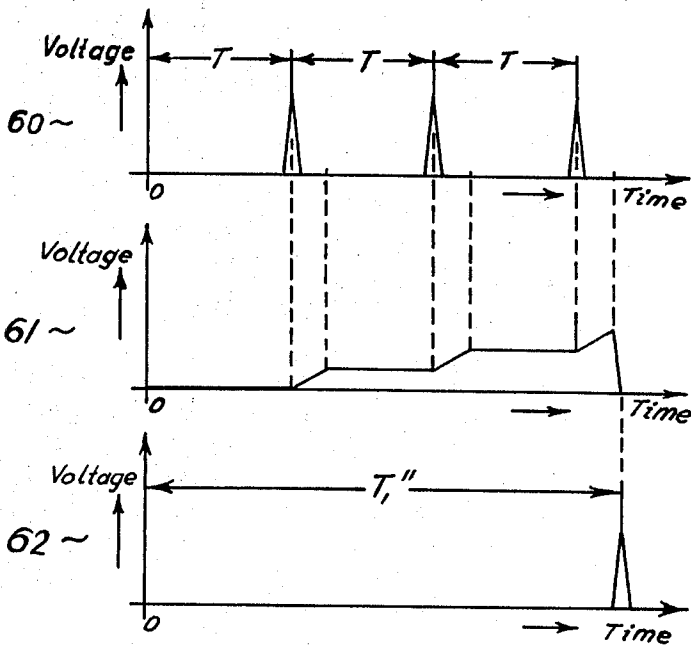


Fig. 9

SEQUENCING TIMERS

BACKGROUND OF THE INVENTION

This invention relates to timing devices in general, particularly to sequenced timing performed electronically and specifically to sequenced timing with independently adjustable delays in wide limits. And as a special case when timer has one single sequence it is called simply 'timer' in this case "increment timer." See the following Table I containing some distinctive features and advantages.

TABLE I

1. The subject "sequencing timers" have long time delays for example on the order of at least 1 hour;
2. They are also 'sequencing', that is, adapted to generate a plurality of successive time-indicating signals;
3. It is also adapted for stable operation in the face of relatively widely - varying ambient temperatures, such as approx. -30° to -70° C;
4. It is also adapted to be implemented with "off-the-shelf" components such as resistors, capacitors, semiconductors, relays, etc., that are widely available "at retailer," rather than being specially fabricated or exhibiting "excess values;"
5. It is relatively small and compact as opposed to electro-mechanical devices for same purpose;
6. It is relatively "non-mechanical," having no motor, cams, springs, etc. as in the prior art, can be sealed, needs no maintenance;
7. It operates with a relatively low power consumption, e.g. on the order of 0.1 watt or less as opposed to several watts for electro-mechanical devices;
8. It is economical since it cost less than cam timers; etc.

Mechanical and electro-mechanical devices are well known in the art for example cam timers, spring operated timers, etc. Electronic timers, even with a single interval, do not exceed 5 or 10 minutes except in special cases. As example, see the description of an electronic sequencer in Motorola's "Semiconductor Power Circuits Handbook," page 6-27, FIG. 6-23, First Edition, November 1968.

Therefore, one objective of the invention is to provide long time intervals (in order of an hour and longer) for a wide ambient temperature range and using regular semiconductor and other electronic components such as those available from retailer's shelves. It is also an objective of this invention to provide long time intervals by use of not more than 1 micro - farad capacitors, and not more than 10 Megohms resistors as variable timing means.

Mechanical and electromechanical systems of sequencing long time delays, though reliable and accurate, are bulky, require relatively high amount of power for operation, require maintenance and are subject to corrosion in some instances.

It is, therefore, a further objective of this invention to provide reliable, relatively accurate, small in size device which would not require much electric power for operation, any maintenance and be corrosion resistive.

It is also an objective of this invention to provide an economical long delay timer.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a block diagram of a sequence timer with common starting time or parallel mode of operation.

FIG. 2 is a representation of timing intervals per FIG. 1.

1.

FIG. 3 is a block diagram of a sequence timer with successive timing intervals or series mode of operation.

FIG. 4 is a representation of time intervals per FIG. 3.

3.

FIG. 5 is an example of a preferred embodiment per FIG. 1.

FIG. 6 is an example of a preferred embodiment per FIG. 3.

FIG. 7 is a generalized block diagram of the sequencing timer.

FIG. 8 is an example of a preferred embodiment per FIG. 7.

FIG. 9 is timing diagram of the timer per FIG. 8.

DESCRIPTION OF OPERATION

Referring to FIG. 1, an adjustable clock frequency source designated 1 produces periodic adjustable frequency pulses and supplies them to a number n of adjustable increment timers. (An increment timer is a modified RC type timer whose timing capacitor is not being charged continuously but rather in small increments thus, producing long time intervals — as known in the art.) For practical reasons only 3 adjustable timers are shown and designated 2, 3 and 4 with respective time delays T_1 , T_2 and T_n . As one can expect, n can take any integer from 1 to infinity — or in practice up to a reasonably high number like 10 or as necessary. When n takes value 1, timer of FIG. 1 becomes an 'increment timer,' when $n = 2$ or more a true sequence timer results. All adjustable timers, in this case, are being "pulsed" by adjustable clock frequency source at the same time from the very beginning, thus starting their respective timing intervals at the same time — which is then called parallel mode of operation. FIG. 2 represents graphically respective time intervals $T_1, T_2, \dots, T_n$, each being indicated by the length of an appropriate arrow, and vividly suggests the name "parallel mode of operation."

Referring now to FIG. 3 we find again an adjustable clock frequency source designated 5 in this case, and adjustable timers designated 6, 7 and 8 with their respective time intervals $T_1', T_2', \dots, T_n'$. In this arrangement timer 6 is being pulsed first. At the end of its timing interval T_1' it fires and initiates operation of timer 7, which similarly initiates operation of the succeeding timer etc. This process continues on and on until $(n - 1)$ st timer initiates the operation of the last adjustable timer in the chain — timer n which fires at the end of its timing interval T_n' thus completing the sequence. System can be now reset manually or automatically by depriving all of them of electric power for a short period of time. This type of operation readily suggests the name "series mode of operation" which is even more pronounced in FIG. 4 where the length of arrow represents the length of the respective timing interval, while its position on time axis represents its sequencing position timewise.

Referring to FIG. 5 is represents an example of the embodiment of FIG. 1 without square 3 for sake of space savings. In addition note a d-c power source designated 9 and power switch designated 10. Square 1 represents adjustable clock frequency source based on a relatively new voltage sensing and triggering device called Programmable Unijunction Transistor (PUT). For detailed information on PUT's please see General

Electric's Application Note 60.20 and also: "Semiconductor Data Handbook," First Edition, 1971, pages 702 - 707. Since PUT operates in same way as well known Unijunction Transistor (UJT) and information on its operation is readily available it will not be given here for the sake of brevity.

Before we proceed let us note the similarity between FIGS. 5 and 8. This is obvious since FIG. 8 is special case of FIG. 5 when $n = 1$, i.e., number of sequences is 1. Accordingly, circuit elements in FIG. 8 are designated with same numbers and double primed for sake of distinction. An additional difference between these figures is the lack of contacts 27 in FIG. 8 since they are not needed. Consequently, FIG. 9 is applicable to both figures and explanation of operation of one figure will suffice. Since blocks designated 55, 56 and 57 in FIG. 8 are identical to block 1 of FIG. 5 (except for contacts 27) and FIG. 8 is a special case of FIG. 5 it is also a special case of FIG. 1. Comparing FIG. 7 to FIGS. 1 and 3 one will notice difference in rearrangement of squares. Block designated 'Capacitor Storage Means' in FIG. 7 is same as 'Adjustable Timer' blocks in FIGS. 1 and 3. Thus FIG. 7 is a more generalized diagram of an increment type sequence timer. Consider now FIG. 8 in connection with FIG. 7. FIG. 7 is a functional block diagram consisting of 3 basic elements: clock means, isolation means and storage capacitor means. Clock means consists of adjustable clock means and a pulse stretcher designated respectively 55 and 56. Pulse stretcher 56 is used to enable isolation switch means 57 to respond properly and operate timing elements 58 as adjustable clock means 55 dictates. Output from timing elements 58 is fed to sensing and trigger means 59. Corresponding squares in FIG. 8 are designated with same numbers as blocks in FIG. 7 allowing us to see that adjustable clock means 55 is an adjustable in frequency, temperature compensated PUT oscillator, pulse stretcher 56 stores charge from capacitor 13'' in its capacitor 18'' discharging it slowly through resistor 23'' and transistor 24'' causing relay contacts 26'' to remain closed for much longer period than the duration of pulse from 55 is and enabling operation of relay 25'' by extremely short pulses. Block 57 is, then, a relay with set of contacts — in this case. Timing elements are resistors 28'', 29'' and capacitor 30'' — all located in block 58. Finally, block 59 consists of a temperature compensated PUT circuit as used in sensing and trigger applications like in timers, oscillators and has its counterpart in block 55. Refer now to FIGS. 8 and 9. Adjustable clock means 55 delivers a pulse once per interval T (designated 60 in FIG. 9). At the nearly same time contacts 26'' are closed allowing capacitor 30'' to be charged for a small increment as indicated in 61 (FIG. 9) at the end of first period T (interval T named above). This is repeated again and again until voltage across capacitor 30'' is high enough to trigger PUT 32'' allowing discharge of capacitor 30'' through PUT 32'' and resistor 31'' after a time delay T_1 as indicated in 62 (FIG. 9) when an output pulse will appear on terminal 33''.

Back to FIG. 5, the interconnection of elements in block 1 is as follows: Negative terminal of the d-c power source designated 9 is connected to a common lead designated 52, while positive terminal is connected to one side of power switch 10, whose other end is connected to the supply lead designated 53. Timing elements consisting of a series connection of a timing

capacitor designated 13, a fixed resistor designated 12 and a variable resistor designated 11 — are connected respectively between said common and said supply lead 53. Interconnection of capacitor 13 and resistor 12 is connected to anode electrode of a PUT designated 15 and having its cathode electrode connected to said common lead through a resistor designated 14. A resistor designated 17 is connected between common lead and the gate electrode of PUT 15, their interconnection being connected to the cathode electrode of temperature effects compensating diode designated 20, while its anode electrode is connected to the interconnection of reference voltage resistors designated 19 and 21 and connected, respectively, with remaining ends to common and the supply leads. When voltage across capacitor 13 reaches potential slightly higher than reference potential across resistor 17, PUT 15 abruptly decreases resistance between its anode and cathode electrodes allowing capacitor 13 to discharge as fast as elements connected to cathode permit. Discharge current forms a positive going pulse across resistor 14 approximately triangular in shape and of a typical duration 5 - 10 microseconds. Said discharge current is fed through diode designated 16 since its anode is connected to PUT's cathode and resistor 14. Diode 16 has its cathode connected to resistor designated 23, while capacitor designated 18 is connected to said interconnection and with remaining plate to common terminal (lead) 52. Capacitor 18 stores the received charge from capacitor 13. Said resistor 23 has its remaining end connected to the base electrode of an NPN type transistor designated 24 having its emitter electrode connected to common terminal (lead) 52 and its collector electrode to interconnection of a relay coil designated 25 and anode of a kick-back voltage protective diode designated 22 whose cathode and the remaining end of relay coil 25 are connected to lead 53. Charged capacitor 18 supplies the base current for transistor 24 for some 5 msec. Diode 16 becomes reverse biased as soon as voltage across it reaches reference potential less a junction voltage drop (about 0.6 to 0.8 Volt), thus, prevents capacitor 18 discharge through resistor 14. Transistor 24 is driven into saturation causing relay contacts 26 and 27 to change positions from those in the drawing to opposite ones and remain there for few msec. Oscillator pulse of some 5 microseconds duration has been "stretched" to msec. Period of oscillation must be, therefore, longer than duration of the stretched pulse (5 msec in this case) in order to permit relay contacts to stay also open and allow incremental charging of capacitor 30 in block 2 and capacitor 40 in 4.

Note now that value of capacitor 13 need not be larger than 1 microfarad since period of oscillation up to 1 sec. can be covered with a resistor being adjustable up to 1 megohm or so. Capacitor 18 is of about same value as capacitor 13. Capacitor 13 should be of a low leakage type like mylar, polyester, metalized paper or any similar. Capacitor 18 in turn is an electrolytic type with such temperature leakage characteristic as to compensate for voltage drop changes in associated semiconductors (16 and 24). Temperature effects on PUT 15 are compensated by diode 20. This way adjustable clock frequency oscillator will be stable in wide temperature limits, since PUT's have low leakage between gate and anode electrodes.

Let us consider now block 2 which is circuitwise identical to all remaining blocks. Assuming, for example only, contacts 26 permanently closed, block 2 is then identical to oscillator in block 1 and its operation needs no long explanations. Its time delay with same values as in block 1 would be certainly identical (up to 1 sec. as anticipated). However, contacts 26 are most of the time open and capacitor 30 can be charged in small increments only as clock frequency from block 1 dictates. Assuming perfect isolation of capacitor 30, while contacts are open, and that portion of time contacts are closed is only a fraction of the clock frequency period, then it is clear that the time delay of the block 2 will be hundreds of times longer and even thousands of times longer than clock frequency period resulting in delays of over 1 hour. Regarding temperature influence same holds for block 2 as for oscillator in block 1, and in addition, during the time contacts 26 are open insulation resistance is extremely high and leakage current negligible by all standards even at highest operative temperatures. The only leakage current to which timing capacitor 30 is exposed is through the gate - anode junction of PUT 32. This leakage is small and typically equals less than 5 nanoamperes at 75° C ambient temperature, at 10 Volts reverse voltage. This leakage can be compensated by proper choice of capacitance and resistance characteristics versus ambient temperature of capacitor 30 yielding possibility of making time delays of many hours with accuracies better than 10 percent.

Some counters and timers using incremental charging in different ways known in prior art are shown in the following U.S. patents:

A. S. Fitz Gerald	Pat. No.	2,110,015 (Cl.177-353)
D. F. Moore	Pat. No.	2,915,632 (Cl.250-27)
C. W. Harrison	Pat. No.	2,924,708 (Cl.250-27)
B. B. Nichols	Pat. No.	3,105,158 (Cl.307-88.5)
J. Rywak	Pat. No.	3,158,757 (Cl.307-88.5)
H. B. Kadah	Pat. No.	3,378,698 (Cl.307-225)
A. F. Goodwin	Pat. No.	3,456,554 (Cl.89-135)

Additional improvements on circuits given in this application are: use of constant current source instead of resistors for timing purposes, use of additional sets of contacts to isolate storage capacitor from PUT's while awaiting incoming charging period, use of a single reference voltage source for all adjustable timers — resulting in better circuit economy, pulsing of anodes or gates to decrease peak point current etc.

Referring now to FIG. 6 one will note that the clock frequency oscillator in block 5 is identical to that of block 1 in FIG. 5. Blocks 6 and 8, however, differ partially as compared to blocks 2 and 4 in FIG. 5, which is necessary to assure serial operation. This is achieved by triggering f.e. Silicon Controlled Rectifier (SCR) designated 49 in block 6, FIG. 6. Cathode electrode is connected to common lead 52', gate to cathode of PUT 32' and anode to a resistor designated 48 having other end connected to the supply lead 53'. To the interconnection anode - resistor 48 a base current limiting resistor is connected, being designated 50, and having remaining end connected to the base electrode of a PNP transistor designated 51, emitter being connected to supply lead 53', while collector to a lead designated 54 which will supply the successive timer with the d-c power needed for its operation. As PUT 32' fires at the end of its timing interval, T_1 , SCR 49 will be triggered

into conduction bringing the potential across its anode to about 1 Volt above common lead 53'. The rest of the supply voltage will be impressed across resistor 50 and base-emitter junction of transistor 51 causing it to enter saturation and supply nearly full voltage from source 9' to the adjustable timer that follows block 6. This process continues until last sequence is performed by adjustable timer, here designated, 8.

It is to be noted that besides usual delay adjustment for each sequence a common adjustment by changing clock frequency is an advantage. Also the possibility to do adjustments of time delays by changing reference voltage and pulse stretching are options not to be disregarded. And possibilities do not end here as those skilled in the art know — yet the basis remains the same.

I claim:

1. A sequencing timer having a plurality of sequences all starting at the same time and produces a pulse at the end of each sequence, consists of:

a d-c power source, having a positive and a negative terminal, said negative terminal is connected to a common lead, said positive terminal is connected to the first terminal of a power switch, while the second terminal of said power switch is connected to a supply lead,

a clock frequency source includes a timing resistor connected between said supply lead and a first terminal of a current limiting resistor whose second terminal is connected to the first plate of

a storage capacitor having the second plate connected to said common lead,

interconnection of said current limiting resistor and said storage capacitor is connected to the anode electrode of a Programmable Unijunction Transistor (PUT) whose cathode electrode is connected through a pulse forming resistor to said common lead,

gate electrode of said PUT is connected through a biasing resistor to said common lead, said interconnection of gate electrode and biasing resistor is connected also to the cathode electrode of

a compensating diode having anode electrode connected to interconnection of two PUT reference voltage resistors connected between said common and said supply lead,

said PUT cathode electrode is connected to a pulse stretching circuit which includes

anode electrode of a blocking diode whose cathode electrode is connected to the first plate of a capacitor, having the second plate connected to said common lead, a base resistor connected between the said diode-capacitor interconnection and a base electrode of

an n-p-n transistor having emitter electrode connected to said common lead and the collector electrode connected through a relay coil to said supply lead, a transient protection diode is connected across said relay coil having cathode electrode connected to the positive end of said coil, said relay coil operating

multiple sets of mutually isolated contacts, each set of contacts is utilized to pulse at least one sequencing circuit which includes

a normally open contact connected through a timing resistor to said supply lead,

a common contact being connected through a current limiting resistor to the interconnection of the first plate of a

storage capacitor, having second plate connected to said common lead, and an anode electrode of a PUT, whose cathode electrode is connected to an output terminal and to the first terminal of a cathode resistor, having second terminal connected to said common lead,

the gate electrode of said PUT is connected through a biasing resistor to said common lead and to the cathode electrode of a biasing diode, whose anode electrode is connected to the interconnection of the two PUT reference voltage resistors connected between said common and said supply lead.

2. Circuit as recited in claim 1 and having said timing resistor adjustable to provide varying of the clock frequency thus, duration of all sequence intervals.

3. Circuit as recited in claim 1 and having said timing resistor adjustable, within said sequencing circuit, to provide independently adjustable intervals in each and every sequence.

4. Circuit as recited in claim 1 and having one single sequence by provision of a single set of contacts and a single sequencing circuit.

5. A sequencing timer having the plurality of sequences, the first sequence starting at the moment the power is supplied to the circuitry, the second sequence starting at the end of the first sequence, the n th sequence starting at the end of $n - 1$ st sequence, a pulse is produced at the end of each sequence, said sequencing timer consisting of:

a d-c power source, having a positive and a negative terminal, said negative terminal is connected to a common lead, said positive terminal is connected to the first terminal of a power switch, while the second terminal of said power switch is connected to a supply lead,

a clock frequency source includes a timing resistor connected between said supply lead and a first terminal of a current limiting resistor whose second terminal is connected to the first plate of

a storage capacitor having the second plate connected to said common lead, interconnection of said current limiting resistor and said storage capacitor is connected to the anode electrode of a Programmable Unijunction Transistor (PUT) whose cathode electrode is connected through a pulse forming resistor to said common lead,

gate electrode of said PUT is connected through a biasing resistor to said common lead, said interconnection of gate electrode and biasing resistor is connected also to the cathode electrode of

a compensating diode having anode electrode connected to interconnection of two PUT reference voltage resistors connected between said common and said supply lead,

said PUT cathode electrode is connected to a pulse stretching circuit which includes

anode electrode of a blocking diode whose cathode electrode is connected to the first plate of a capacitor, having the second plate connected to said common lead, a base resistor connected between the said diode-capacitor interconnection and a base electrode of

an n-p-n transistor having emitter electrode connected to said common lead and the collector electrode connected through a relay coil to said supply lead, a transient protection diode is connected across said relay coil having cathode electrode connected to the positive end of said coil, said relay coil operating

multiple sets of mutually isolated contacts, each set of contacts is utilized to pulse at least one sequencing circuit, the first set of contacts is utilized to pulse the first sequencing circuit which includes a normally open contact connected through a timing resistor to said supply lead,

a common contact being connected through a current limiting resistor to the interconnection of the first plate of a

storage capacitor, having second plate connected to said common lead, and an anode electrode of a PUT, whose cathode electrode is connected to an output terminal and to the first terminal of a cathode resistor, having second terminal connected to said common lead,

the gate electrode of said PUT is connected through a biasing resistor to said common lead and to the cathode electrode of a biasing diode, whose anode electrode is connected to the interconnection of the two PUT reference voltage resistors connected between said common and said supply lead, the first sequence output terminal is also connected to the gate electrode of the first Silicon Controlled Rectifier (SCR) having the cathode electrode connected to said common lead and anode electrode connected through

a first anode resistor to said supply lead, said anode electrode is also connected through

a first base resistor to the base electrode of

a first p-n-p transistor whose emitter electrode is connected to said supply lead and, collector electrode connected to the next sequencing circuit thus acts as the first supply lead,

a second set of contacts which consists of a normally open contact and a common contact, these contacts being used to pulse a second sequencing circuit, which is of identical configuration as described first sequencing circuit, said second set of contacts operates associated circuit after the first sequencing time interval is over, said second sequence circuit being able to deliver a pulse at the end of said second sequence interval, and supply the power to the third sequencing circuit, an n th set of contacts which consists of a normally open contact and a common contact, these contacts are used to pulse the n th sequencing circuit, n being an integer larger than two,

normally open contact is connected to the first terminal of the n th timing resistor whose second terminal is connected to the collector electrode of $n - 1$ st sequencing circuit, said collector electrode acting as the $n - 1$ st supply lead,

the common contact is connected through the n th limiting resistor to

the first plate of an n th storage capacitor which has the second plate connected to said common lead, said first plate is also connected to the anode electrode of the

n th PUT having cathode electrode connected through the n th cathode resistor to said common

lead, said cathode is also connected to an n th output terminal, gate electrode of said n th PUT is connected through an n th biasing resistor to said common lead, said interconnection of biasing resistor and gate electrode is connected also to the cathode electrode of an n th compensating diode whose anode electrode is connected to the interconnection of the two n th PUT reference voltage resistors connected between said common and said $n - 1$ st supply lead, said n th sequence circuit being able to produce a pulse at the end of the n th sequence interval.

6. The circuit of claim 5 and having said timing resistor adjustable to provide adjustable clock frequency which causes the change in duration of all sequences.

7. The circuit of claim 5 and having said first timing resistor adjustable, and said n th timing resistor adjustable to provide independently adjustable interval in each and every sequence.

8. The circuit of claim 5 having one single sequence by provision of a single set of contacts and a single sequencing circuit.

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