(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 December 2003 (18.12.2003)

PCT

(10) International Publication Number
WO 03/105243 A1

(51) International Patent Classification⁷: **H01L 33/00**, 27/15

(21) International Application Number: PCT/US03/16912

(22) International Filing Date: 29 May 2003 (29.05.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/163,099 4 June 2002 (04.06.2002) US

(71) Applicant: **KOPIN CORPORATION** [US/US]; 695 Myles Standish Boulevard, Tauton, MA 02780 (US).

(72) Inventor: **CHOI, Hong, K.**; 18 Terrapin Lane, Sharon, MA 02067 (US).

(74) Agents: **PIERCE, N. Scott** et al.; Hamilton, Brook, Smith & Reynolds, P.C., 530 Virginia Road, P.O.Box 9133, Concord, MA 01742-9133 (US).

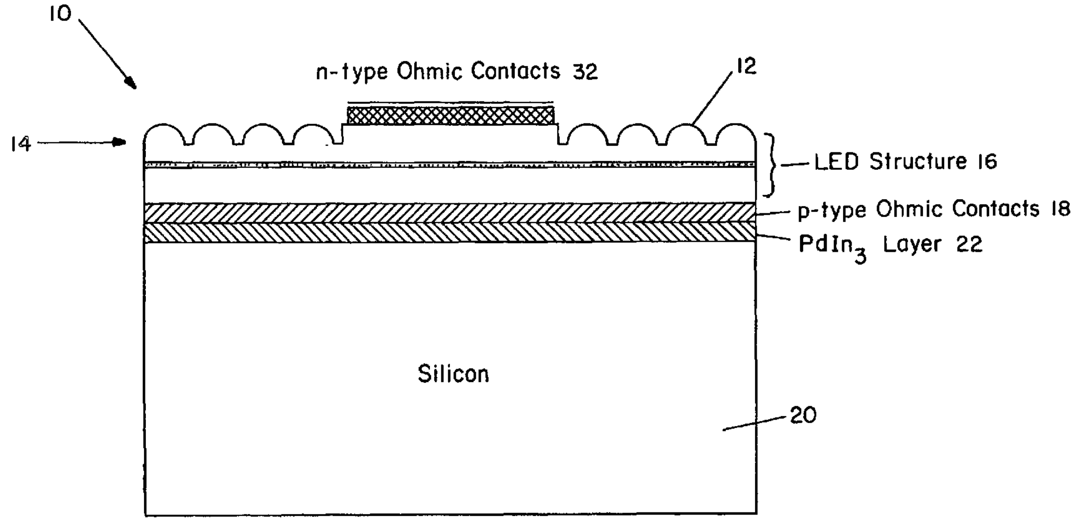
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: HIGH-EFFICIENCY LIGHT-EMITTING DIODES



(57) Abstract: Light-emitting diodes (LEDs) have at least one light-emitting surface that is patterned, thereby improving the ratio of internal to external efficiency. A " patterned light-emitting surface"is a surface that has a plurality of raised elements that are spaced in a non-random pattern. In one embodiment, the light-emitting diodes are gallium nitride based group III-V diodes that have a multiple quantum-well active region between an n-doped GaN layer and a p-doped GaN layer. The n-doped GaN layer has a surface that is patterned.

WO 03/105243 A1

HIGH-EFFICIENCY LIGHT-EMITTING DIODES

BACKGROUND OF THE INVENTION

High-efficiency light-emitting diodes (LEDs) are desired for many applications such as displays, printers, short-haul communications, optoelectronic computer interconnects. However, there is a significant gap between the internal efficiency of LEDs and their external efficiency. The internal quantum yield of a good-quality diode can exceed 99%. However, external efficiency is less than 30% and typically is as low as 2%. The reason for the difference in the internal and external efficiency of LEDs is that light generated internally in the semiconductor material of the diode must pass through the interface between the semiconductor and air, for example, or another optically transmissive medium, such as an optically transmissive epoxy resin. Light is both refracted and internally reflected at the interface according to Snell's Law. At a critical angle (θ_c), and at any angle larger than the critical angle, light traveling through a medium having a higher refractive index and striking an interface with a medium having a lower refractive index will be totally internally reflected. The critical angle is dependent on the refractive index of the two media and is given by the following formula:

$$\sin \theta_c = \eta_2/\eta_1$$

wherein:

η_1 is the refractive index of the higher refractive index material.

η_2 is the refractive index of the lower refractive index material.

As can be seen from the above formula, the critical angle becomes smaller when there is a large difference between the refractive index of the two materials forming the interface, such as in the case of a semiconductor/air interface. The smaller the critical angle, the more light is internally reflected rather than transmitted through the interface. Multiple internal reflections result in reabsorption of a large percentage of photons generated within the semiconductor material.

One method that has been used to reduce this problem is to shape the entire light-emitting surface into a spherical dome. This increases the probability that a photon generated inside the semiconductor material will strike the interface at an angle smaller than the critical angle. However, fabrication of a large spherical dome is difficult and expensive to manufacture because it requires deep etching. Therefore, a need exists for improved photon extraction from LEDs which both improves the external efficiency of LEDs and reduces the cost of manufacture.

SUMMARY OF THE INVENTION

The present invention is a light-emitting diode having at least one patterned surface that emits light. The pattern on the light-emitting surface improves photon extraction from the semiconductor material of the diode.

In one embodiment, the light-emitting diode has an n-doped semiconductor layer in contact with a p-doped semiconductor layer and at least one patterned light-emitting surface. Alternatively, the n-doped semiconductor layer and a p-doped semiconductor layer of the diode are separated by an active region. In this embodiment, the active region has a first surface in contact with a first surface of the n-doped semiconductor layer and a second surface in contact with a first surface of the p-doped semiconductor layer. The active region can include, for example, a material that has a lower band-gap energy and higher refractive index than the n-doped and p-doped semiconductor layers. Alternatively, the active region can consist of a single quantum-well layer and two surrounding barrier layers in which the barrier material has a band-gap energy larger than the quantum-well layer but equal to or smaller than the n-doped and p-doped semiconductor layers. The active region can also include multiple quantum-well layers and multiple barrier layers alternately stacked. The patterned surface is a surface of the n-doped semiconductor layer or a surface of the p-doped semiconductor layer. Alternatively, the light-emitting diode has a transparent substrate having first and second surfaces. The first surface of the transparent substrate is in contact with a surface of the n-doped semiconductor layer or a surface of the p-doped semiconductor layer, and the second surface of the transparent substrate is the patterned light-emitting surface. Preferred transparent substrates are formed of GaAs, InP and GaN.

In another embodiment, the light-emitting diode has an n-doped $In_xGa_{1-x}N$ layer and a p-doped $In_xGa_{1-x}N$ layer on a silicon substrate, wherein $0 \leq x \leq 1$. A first surface of the n-doped $In_xGa_{1-x}N$ layer emits light and is patterned. A first surface of the p-doped $In_xGa_{1-x}N$ layer is in contact with a second surface of the n-doped $In_xGa_{1-x}N$ layer. A second surface of the p-doped $In_xGa_{1-x}N$ layer is coated with an ohmic contact, which can include one or more layers. The ohmic contact is bound to a substrate, such as silicon, germanium, gallium arsenide or a metal, with a conducting layer, such as $PdIn_3$. In one embodiment, the ohmic contact layer is coated with a reflective layer, such as a metallic layer, and the reflective layer is bound to the substrate with a conducting layer.

In another embodiment, the light-emitting diode has an n-doped GaN layer and a p-doped GaN layer which are separated by a multiple-quantum-well active region composed of multiple $In_xGa_{1-x}N$ well layers and multiple $In_yGa_{1-y}N$ barrier layers that are alternately stacked, wherein $y < x$, $0 < x \leq 1$, and $0 \leq y \leq 1$. A first surface of the n-doped GaN layer emits light and is patterned. The active region is between the n-doped GaN layer and the p-doped GaN layer. Preferably, a second surface of the n-doped GaN layer is in contact with a first surface of the active region, and a second surface of the active region is in contact with a first surface of the p-doped GaN layer. Optionally, a second surface of the p-doped GaN layer is coated with the ohmic contact layers and light reflecting layers, which are bound to a silicon substrate or metal with a conducting layer such as $PdIn_3$.

The patterned surface of the LEDs of the invention are, preferably, patterned as an array of hemispherical, pyramidal, or hexagonal pyramidal (i.e., pyramidal structures having a hexagonal base) surface structures. Typically, the diameters of the base of the hemispherical structures or the diagonals of the pyramidal or hexagonal pyramidal structures are about 0.5 μm to about 20 μm.

As with other electronic devices, there exists a demand for more efficient LEDs, and in particular, LEDs that will operate at higher intensity while using less power. Higher intensity LEDs, for example, are particularly useful for displays or status indicators in various high ambient light environments. High efficiency LEDs with lower power consumption, for example, are particularly useful in various portable electronic equipment applications. In particular, there is a demand for efficient LEDs that will emit light in the green, blue and ultraviolet regions of the visible spectrum (e.g., efficient III-V nitride LED). Blue and green LEDs composed of III-V nitrides typically show a forward current of 20 mA and a forward voltage of 3.4 V to 3.6 V which are higher by about 2 V or more than those of red LEDs made of GaAlAs semiconductors. Therefore, more efficient blue and green LEDs would be desirable.

The gap between the internal and external efficiency of LEDs of the invention having a patterned light-emitting surface generally is less than that of an LED having a planar light-emitting surface because the patterned surface allows more opportunity for internally generated light to strike the interface between the semiconductor and an optically transmissive medium, such as air, at an angle less than the critical angle than does a planar light-emitting surface. Since light striking the interface at an angle which is less than the critical angle will be transmitted instead of internally reflected, less light that is internally generated by the LED is reflected back into the semiconductor layers an reabsorbed. In addition, deep etching of the light-emitting surface is not required because creation of a pattern, such as an array of individual hemispherical or pyramidal structures, does not require shaping of the entire light-emitting surface. Thus, the cost of manufacture of LEDs of the invention is relatively low.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows the processing steps to obtain an LED with a hemispherical surface structure: a) the photoresist is patterned by a standard photolithography step;

b) the photoresist is baked at a high temperature to form rounded edges; and c) the semiconductor is etched using the photoresist mask with an anisotropic etching technique to form a hemispherical surface structure.

Fig. 2 is a cross-sectional representation of one embodiment of a composite LED of the invention.

Fig. 3 is a schematic representation of steps of one method of making the diodes of the invention.

Fig. 4 is a plan view of a light-emitting surface of an LED of the invention having a patterned array of hemispherical structures.

Fig. 5 is a plan view of a light-emitting surface of an LED of the invention having a patterned array of pyramidal structures.

Fig. 6 is a plan view of a light-emitting surface of an LED of the invention having a patterned array of hexagonal pyramidal structures.

DETAILED DESCRIPTION OF THE INVENTION

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

The present invention includes LEDs having a patterned light-emitting surface which generally results in improved photon extraction over LEDs having a flat light-emitting surface. The phrase "light-emitting surface," as used herein, refers to a surface of the LED through which light generated within the semiconductor material of the diode is transmitted. The light-emitting surface is a surface that is in contact with another optically transmissive medium, such as air or a transparent polymer, such as an epoxy. A "patterned light-emitting surface," as defined herein, is a surface that has a plurality of raised elements that are spaced in a non-random pattern. A patterned light-emitting surface is a surface in which the incident angle for transmission of light is varied and, thus, provides more opportunities for internally generated light to strike the surface at less than the critical angle and, thereby, be emitted from the diode. Preferably, the raised elements have curved sides. In one preferred embodiment, the raised elements on a patterned light-emitting surface are an array of hemispherical elements. In another preferred embodiment, the raised elements on a patterned light-emitting surface are an array of pyramidal elements having a square or hexagonal base. Preferably, the raised elements have a maximum width at their base in a range of between about 0.5 μm and about 20 μm. When the raised elements are an array of hemispherical surface structures, the diameter at the base of each hemisphere is about 0.5 μm to about 20 μm. When the raised elements are an array of pyramidal surface structures, the diagonal at the base of each pyramid is about 0.5 μm to about 20 μm.

In one embodiment, LEDs of the invention have an n-doped semiconductor layer in contact with a p-doped semiconductor layer and at least one patterned light-emitting surface. The patterned light-emitting surface is, for example, a light-emitting surface of the n-doped semiconductor or a light-emitting surface of the p-doped semiconductor. In an alternative embodiment, an active region separates the n-doped semiconductor layer from the p-doped semiconductor layer, such that a first surface of the active region is in contact with a first surface of the p-doped semiconductor layer and a second surface of the active region is in contact with a first surface of the n-doped semiconductor layer. In one embodiment, the active region includes a material that has a lower band-gap energy and higher refractive index than the n-doped and p-doped semiconductor layers. The larger-band-gap n-doped and p-doped semiconductor layers create potential barriers on both sides of the active region and cause carriers (i.e., holes and electrons) to be confined in the active region where they combine to emit light. Alternatively, the active region includes a single quantum-well layer and two surrounding barrier layers having a band-gap energy larger than the quantum-well layer but equal to or smaller than the n-doped and p-doped semiconductor layers. The active region includes multiple quantum-well layers and barrier layers alternately stacked. An active layer is a layer that has a band-gap which is smaller than the band-gap of both the p-doped semiconductor layer and the n-doped semiconductor layer that form the diode.

LEDs of the invention optionally include a substrate on which the n-doped and p-doped semiconductor layers that form the pn-junction of the diode are grown. When the substrate is transparent to the light emitted by the diode, a light-emitting surface of the substrate can be patterned to improve photon extraction from this surface instead of, or as well as, a surface of the one of the semiconductor layers forming the pn-junction. Examples of substrates that are transparent to visible light include sapphire, GaAs, InP and GaN. Examples of LEDs grown on transparent substrates include InGaAs on GaAs, InGaAsP on InP, and InGaN on GaN.

One method of forming a pattern of hemispherical structures on the surface of a substrate or semiconductor layer is shown in Fig. 1. First, an array of photoresist pattern is formed by using a standard photolithography step. Then the photoresist is heated at a high enough temperature to form rounded edges. The photoresist shape is then transferred to the semiconductor by a suitable anisotropic etching technique, such as reactive ion etching or inductively-coupled plasma. The exact shape depends on the starting photoresist shape and the etch rate ratio between the photoresist and semiconductor.

In an alternative embodiment, the substrate on which the n-doped and p-doped semiconductor layers are grown can be removed. Removal of the insulating substrate can be advantageous because it can provide a means of making electrical back-contacts on the LED or, alternatively, facilitates bonding a substrate to the LED that has more ideal thermal and electrical properties but has a surface on which the semiconductor layers that form the pn-junction of the diode do not grow well. One method of removing the substrate is a laser lift-off procedure in which the surface of a group III-nitride layer that is in contact with a transparent substrate is heated with a short laser pulse, typically about 5 ns to about 50 ns, through an optically transmissive substrate to decompose a localized surface area of the group III-nitride and, thus, separate it from the substrate. The decomposition of the material is highly localized because heat is generated quickly by the laser so that a localized high temperature is reached before the heat is conducted away from the area. This procedure takes advantage of the low decomposition temperatures of group III-nitrides, which decompose to form a group III metal and nitrogen gas. The group III metal which is deposited on the surface of the remaining group III-nitride layer is typically removed from the remaining group III-nitride layer by holding the surface over fuming HCl. The wavelength of light from the laser preferably is just above the absorption edge of the group III-nitride material to avoid degradation of the crystal quality of the remaining group III-nitride layer. For example, when the group III-nitride is GaN, the wavelength of radiation from the laser preferably is about 355 nm, which is just above the absorption edge of GaN. However, successful lift-off of GaN thin films can be performed using radiation having a wavelength of 248 nm, which is substantially above the absorption edge of GaN.

The epitaxial layers that form the pn-junction of LEDs generally are higher quality if they are grown on a substrate that has a similar crystal symmetry. However, the substrate on which a high-quality film can be grown may not have the most desirable thermal and electrical properties. For instance, silicon and GaAs have more desirable thermal and electrical properties than sapphire, but a high quality film of a group III-nitride cannot be grown on either material. Thus, group III-nitrides are generally grown on sapphire. However, this disadvantage can be overcome by removing the substrate after fabrication of the LED using, for example, the laser lift-off procedure described above, and then using a wafer bonding technique to bind a more preferred substrate to the LED.

Fig. 2 is a cross-sectional view of one embodiment of a composite LED (10) having an array of hemispherical elements (12) on a light-emitting surface (14) of the LED structure (16). The LED structure (16) includes a p-doped layer in contact with an n-doped layer or a p-doped layer and an n-doped layer sandwiching an active region. The p-type ohmic contact (18) of the LED structure (16) is bound to a silicon substrate (20) through a $PdIn_3$ layer (22).

Fig. 3 is a schematic representation of steps of a method of preparing the composite LED (10) of Fig. 2. In one embodiment, an LED structure (16) of a group III-nitride is grown by metalorganic chemical vapor deposition (MOCVD) on a sapphire substrate (24). In this embodiment, an n-doped GaN layer (not shown) having a thickness of about 2 μm to about 6 μm is grown on the sapphire substrate, followed by a multi-quantum-well active region consisting of multiple $In_xGa_{1-x}N$

well layers having a thickness in the range of about 1 nm to about 5 nm and multiple $In_yGa_{1-y}N$ barrier layers having a thickness in the range of about 3 nm to 15 nm (not shown) in which $0 < x \leq 1$, preferably x is about 0.4, and $0 \leq y \leq 1$, preferably y is less than about 0.05. A p-doped GaN layer (not shown) having a thickness of about 200 nm to about 300 nm is grown over the active region. Ni/Au metal electrodes are then deposited on the p-doped GaN layer forming the p-type ohmic contact layer (18). A Pd layer (26) having a thickness of about 50 nm to about 150 nm is deposited on the p-contacts by electron beam evaporation at a base pressure of about 1×10^{-7} Torr, followed by an In layer (28) having a thickness of about 0.5 μm to bout 2 μm. The In layer (28) is deposited by thermal evaporation at a base pressure of about 5×10^{-7} Torr. Separately, a Si substrate (20) is coated by a Pd layer (30) having a thickness of about 50 nm to about 150 nm. The In layer of the Pd-In coated LED is then placed in contact with the Pd layer of the Si substrate and bonded by applying pressure of about 2.8 MPa at a temperature of about 200°C. At this temperature, molten In is formed and reacts with Pd in a "wafer bonding reaction" to form a $PdIn_3$ compound that has a melting point of 664°C. Thus, the reaction is complete when a solid $PdIn_3$ layer (22) forms. The thickness of the Pd layers (26 and 30) and the In layer (28) are chosen such that the molar ratio of the sum of the Pd layers (26 and 30) to the In layer (28) is between about 1:1 to about 1:3 to ensure that all of the In reacts with Pd.

After the wafer bonding reaction is complete, the sapphire substrate can be removed by directing a laser through the sapphire substrate at the surface of the LED structure in contact with the substrate. This will decompose a localized surface region of the group III-nitride layer into group III metal and nitrogen gas. After removal of the group III metal with fuming HCl, the surface can be patterned by using the technique described above or other methods known to those skilled in the art.

EQUIVALENTS

While this invention has been particularly shown and described with references to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention encompassed by the appended claims.

CLAIMS

What is claimed is:

1. A light-emitting diode, wherein the improvement comprises at least one patterned light-emitting surface.

2. The diode of Claim 1, wherein the patterned surface includes an array of essentially hemispherical surface structures.

3. The diode of Claim 2, wherein each hemisphere has a diameter at its base in the range of about 0.5 μm to about 20 μm.

4. The diode of Claim 1, wherein the patterned surface includes an array of pyramidal surface structures having an essentially square base.

5. The diode of Claim 4, wherein each pyramid has a diagonal at its base in the range of about 0.5 μm to about 20 μm.

6. The diode of Claim 1, wherein the patterned surface includes an array of pyramidal surface structures having an essentially hexagonal base.

7. The diode of Claim 6, wherein each hexagonal pyramid has a diagonal at its base in the range of about 0.5 μm to about 20 μm.

8. The diode of Claim 1, wherein the patterned surface that emits light is a semiconductor surface.

9. A light-emitting diode, comprising:
   a) a diode structure including:
      i) an n-doped semiconductor layer in contact with a p-doped semiconductor layer; or
      ii) an n-doped semiconductor layer having a first surface in contact with a first surface of an active region and a p-doped semiconductor layer having a first surface in contact with a second surface of the active region; and
   b) at least one patterned light-emitting surface, whereby light emitted is transmitted through the patterned surface.

10. The diode of Claim 9, wherein the patterned light-emitting surface is a surface of the n-doped semiconductor or a surface of the p-doped semiconductor.

11. The diode of Claim 10, wherein the patterned light-emitting surface includes an array of essentially hemispherical surface structures.

12. The diode of Claim 11, wherein each hemisphere has a diameter at its base in the range of about 0.5 μm to about 20 μm.

13. The diode of Claim 10, wherein the patterned light-emitting surface includes an array of pyramidal surface structures having an essentially square base.

14. The diode of Claim 13, wherein each pyramid has a diagonal at its base in the range of about 0.5 μm to about 20 μm.

15. The diode of Claim 10, wherein the patterned surface includes an array of pyramidal surface structures having an essentially hexagonal base.

16. The diode of Claim 15, wherein each hexagonal pyramid has a diagonal at its base in the range of about 0.5 μm to about 20 μm.

17. The diode of Claim 9, wherein the p-doped semiconductor layer and the n-doped semiconductor layer are GaN and the active region has multiple quantum-well layers comprising $In_xGa_{1-x}N$, wherein $0 \prec x \leq 1$, and multiple barrier layers comprising $In_yGa_{1-y}N$, wherein $0 \leq y \leq 1$ and $y \prec x$.

18. The diode of Claim 9, further comprising a transparent substrate having a first surface and a second surface, wherein the first surface is in contact with a surface of the n-doped semiconductor layer or a surface of the p-doped semiconductor layer, and wherein the second surface of the substrate is the patterned light-emitting surface.

19. The diode of Claim 18, wherein the second substrate surface includes an array of essentially hemispherical surface structures.

20. The diode of Claim 19, wherein each hemisphere has a diameter at its base in the range of about 0.5 μm to about 20 μm.

21. The diode of Claim 18, wherein the second substrate surface includes an array of pyramidal surface structures having an essentially square base.

22. The diode of Claim 21, wherein each pyramid has a diagonal at its base in the range of about 0.5 μm to about 20 μm.

23. The diode of Claim 18, wherein the patterned surface includes an array of pyramidal surface structures having an essentially hexagonal base.

24. The diode of Claim 23, wherein each hexagonal pyramid has a diagonal at its base in the range of about 0.5 μm to about 20 μm.

25. The diode of Claim 18, wherein the substrate includes GaAs and the n-doped and the p-doped semiconductor layers include InGaAs.

26. The diode of Claim 18, wherein the substrate includes InP and the n-doped and the p-doped semiconductor layers include InGaAsP.

27. The diode of Claim 18, wherein the substrate includes GaN and the n-doped and the p-doped semiconductor layers include InGaN.

28. A light-emitting diode, comprising:

a) an n-doped GaN layer having a first and a second surface, wherein the first surface emits light and is patterned;

b) a multiple quantum-well active region having a first surface in contact with the second surface of the n-doped GaN layer, wherein the multiple quantum-well active region comprises multiple $In_xGa_{1-x}N$ well layers, wherein $0 \prec x \leq 1$, and multiple $In_yGa_{1-y}N$ barrier layers, wherein $0 \leq y \leq 1$ and $y \prec x$;

c) a p-doped GaN layer having a first and a second surface, wherein the first surface of the p-doped GaN layer is in contact with a second surface of the active region and the second surface is in contact with an ohmic contact layer and a light reflecting layer; and

d) a silicon, germanium, gallium arsenide or metallic substrate bound to the ohmic contact layer with an electrically-conducting bonding layer.

29. The diode of Claim 28, wherein a reflective layer is between the ohmic contact layer and the bonding layer.

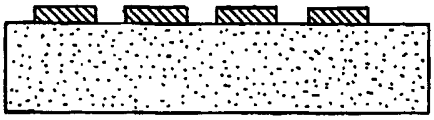


FIG. 1A

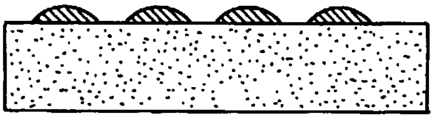


FIG. 1B

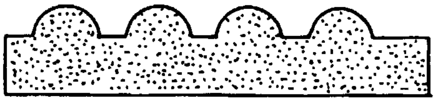


FIG. 1C

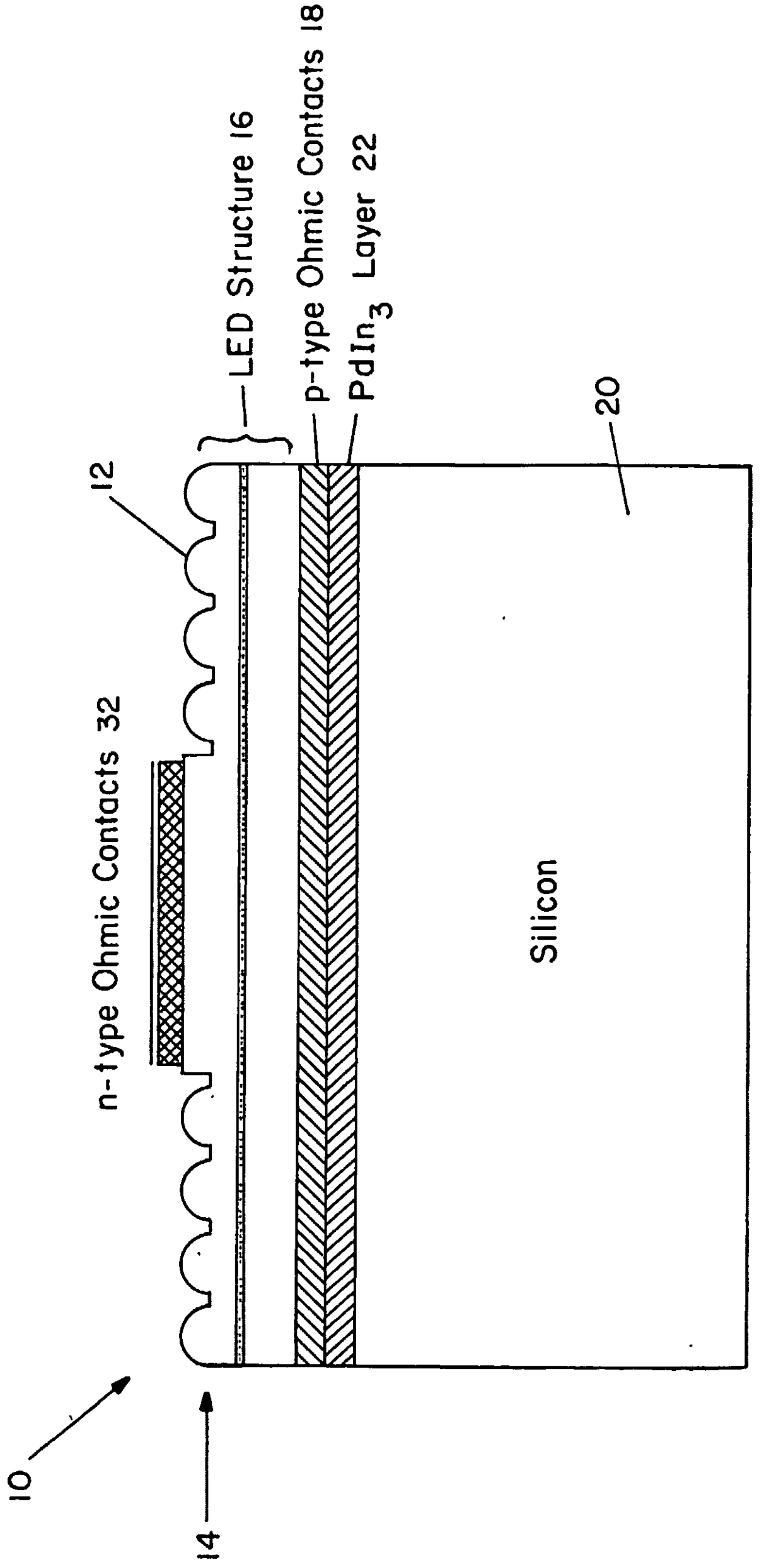

n-type Ohmic Contacts 32
LED Structure 16
p-type Ohmic Contacts 18
$PdIn_3$ Layer 22
12
20
Silicon
10
14

FIG. 2

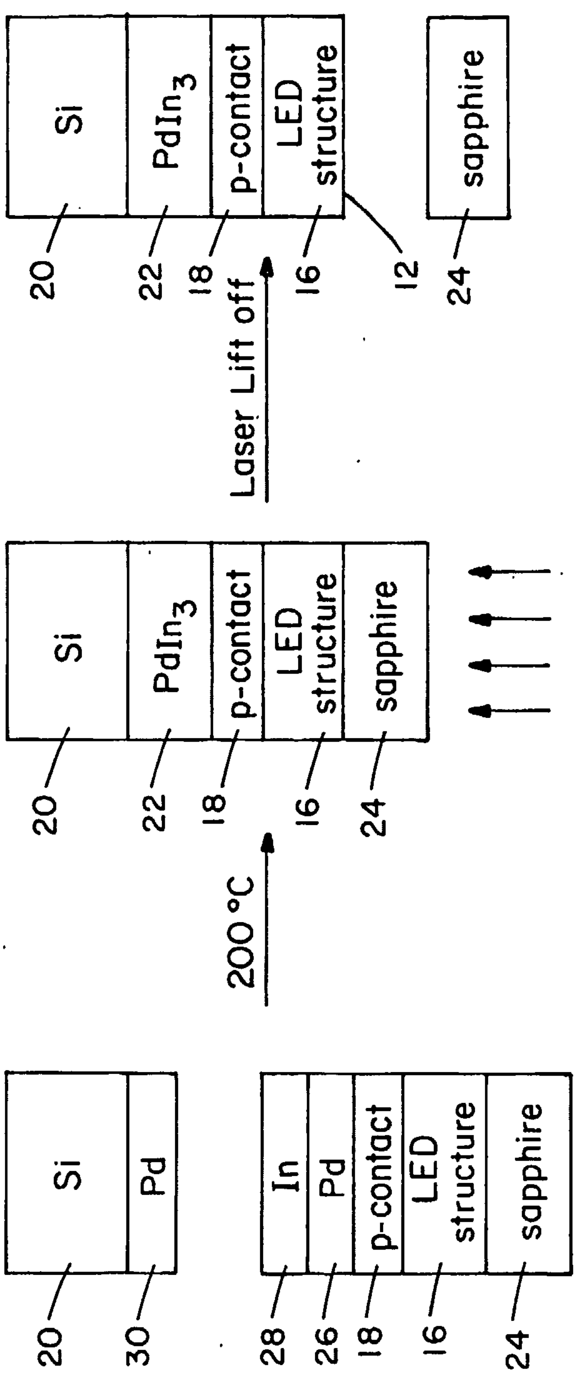

Si
Pd
20
30
In
Pd
p-contact
LED structure
sapphire
28
26
18
16
24
200 °C
Si
PdIn3
p-contact
LED structure
sapphire
20
22
18
16
24
Laser Lift off
Si
PdIn3
p-contact
LED structure
sapphire
20
22
18
16
12
24

FIG. 3

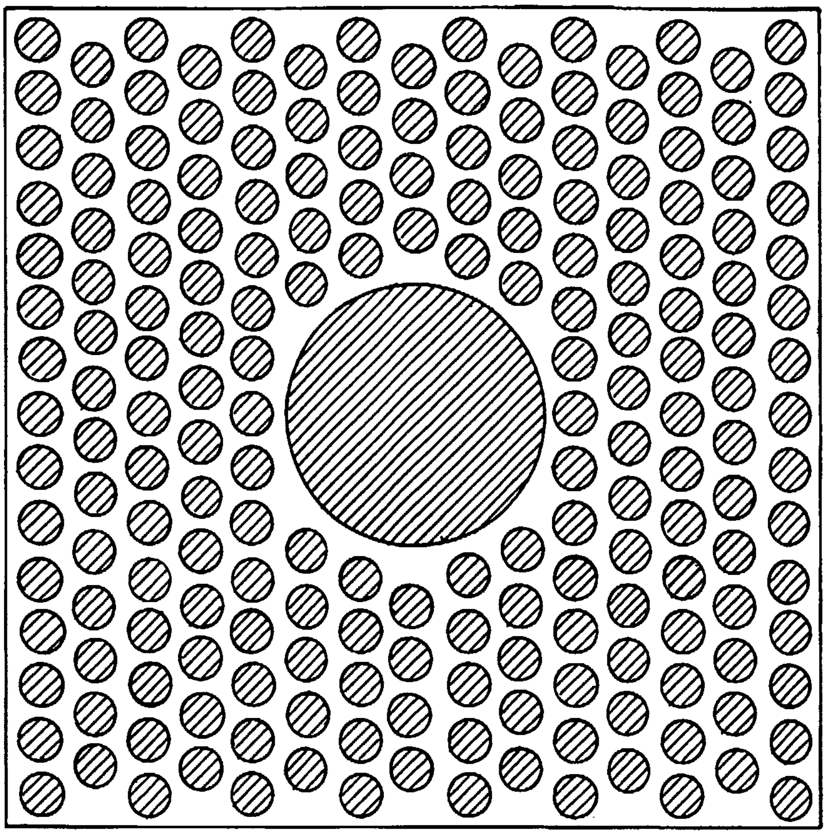


FIG. 4

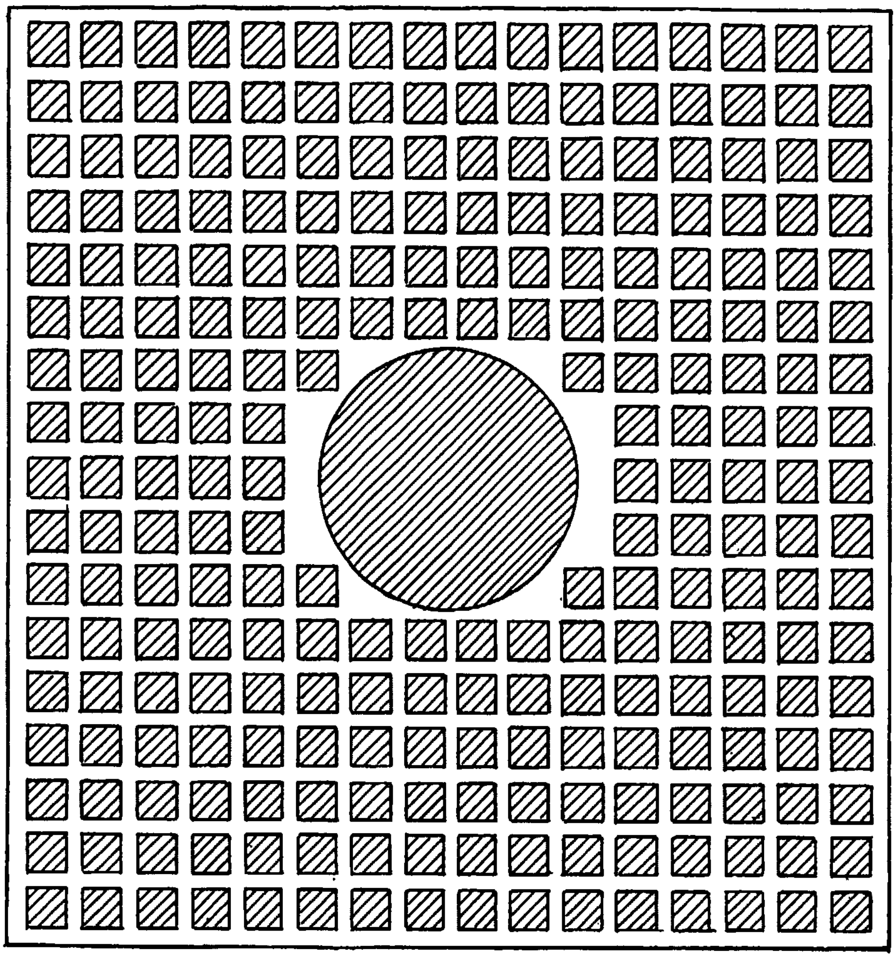


FIG. 5

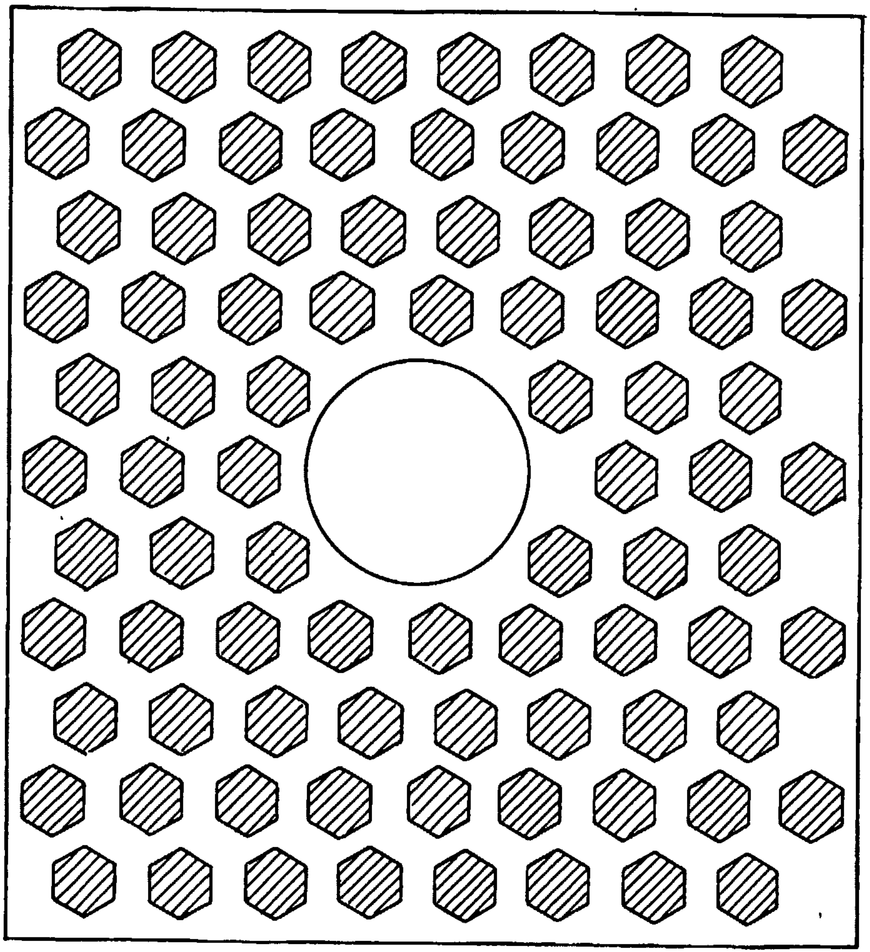


FIG. 6

INTERNATIONAL SEARCH REPORT

Int ial Application No
PCT/US 03/16912

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L33/00 H01L27/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

PAJ, EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 10, 17 November 2000 (2000-11-17) -& JP 2000 196152 A (TOSHIBA CORP), 14 July 2000 (2000-07-14) abstract -& US 6 495 862 B1 17 December 2002 (2002-12-17) the whole document ---	1-29
X	PATENT ABSTRACTS OF JAPAN vol. 014, no. 336 (E-0953), 19 July 1990 (1990-07-19) & JP 02 113524 A (HITACHI LTD;OTHERS: 01), 25 April 1990 (1990-04-25) abstract --- -/--	1,2,8,9, 11,18,19

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search 7 August 2003	Date of mailing of the international search report 14/08/2003
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Authorized officer Werner, A

INTERNATIONAL SEARCH REPORT

Int ial Application No
PCT/US 03/16912

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	DE 24 21 590 A (SIEMENS AG) 13 November 1975 (1975-11-13) claims 1,5,6; figure 1 ---	1
X	DE 199 11 717 A (OSRAM OPTO SEMICONDUCTORS GMBH) 28 September 2000 (2000-09-28) figure 3 ---	1
A	YANG J W ET AL: "SELECTIVE AREA DEPOSITED BLUE GAN-INGAN MULTIPLE-QUANTUM WELL LIGHTEMITTING DIODES OVER SILICON SUBSTRATES" APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 76, no. 3, 17 January 2000 (2000-01-17), pages 273-275, XP000919607 ISSN: 0003-6951 the whole document -----	17,25-29

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte ial Application No

PCT/US 03/16912

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 2000196152 A	14-07-2000	US 2003062530 A1 US 6495862 B1	03-04-2003 17-12-2002
JP 02113524 2 A		NONE	
DE 2421590 A	13-11-1975	DE 2421590 A1	13-11-1975
DE 19911717 A	28-09-2000	DE 19911717 A1	28-09-2000