

- [54] **VARIABLE RATE DISPLAY GENERATOR**
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- [51] Int. Cl. .... **G06f 3/14**
- [58] Field of Search ..... **340/324 A; 315/18**

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[57] **ABSTRACT**

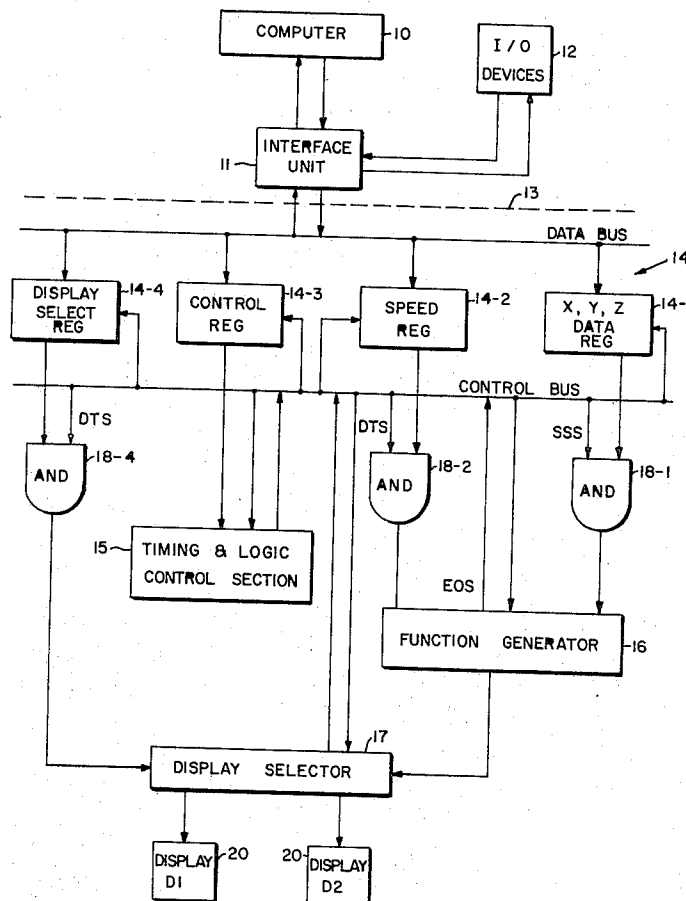
A computer controlled multi-station display system utilizing a single display generator unit time shared by display indicators which have different writing rates. The display generator includes a register bank which receives and holds display indicator select and writing rate information as well as symbol tracing information. A control section routes the display select information to a display selector and the writing rate and the symbol tracing information to a function generator which produces X, Y and Z axis modulating signals at a rate which corresponds to the writing rate information. The display selector routes the generated X, Y and Z signals to a display indicator having a writing rate corresponding to the rate at which the X, Y and Z signals are produced. The function generator is illustrated as including a character generator having circuitry for varying rate at which characters are written on the display surface of the indicator.

16 Claims, 4 Drawing Figures

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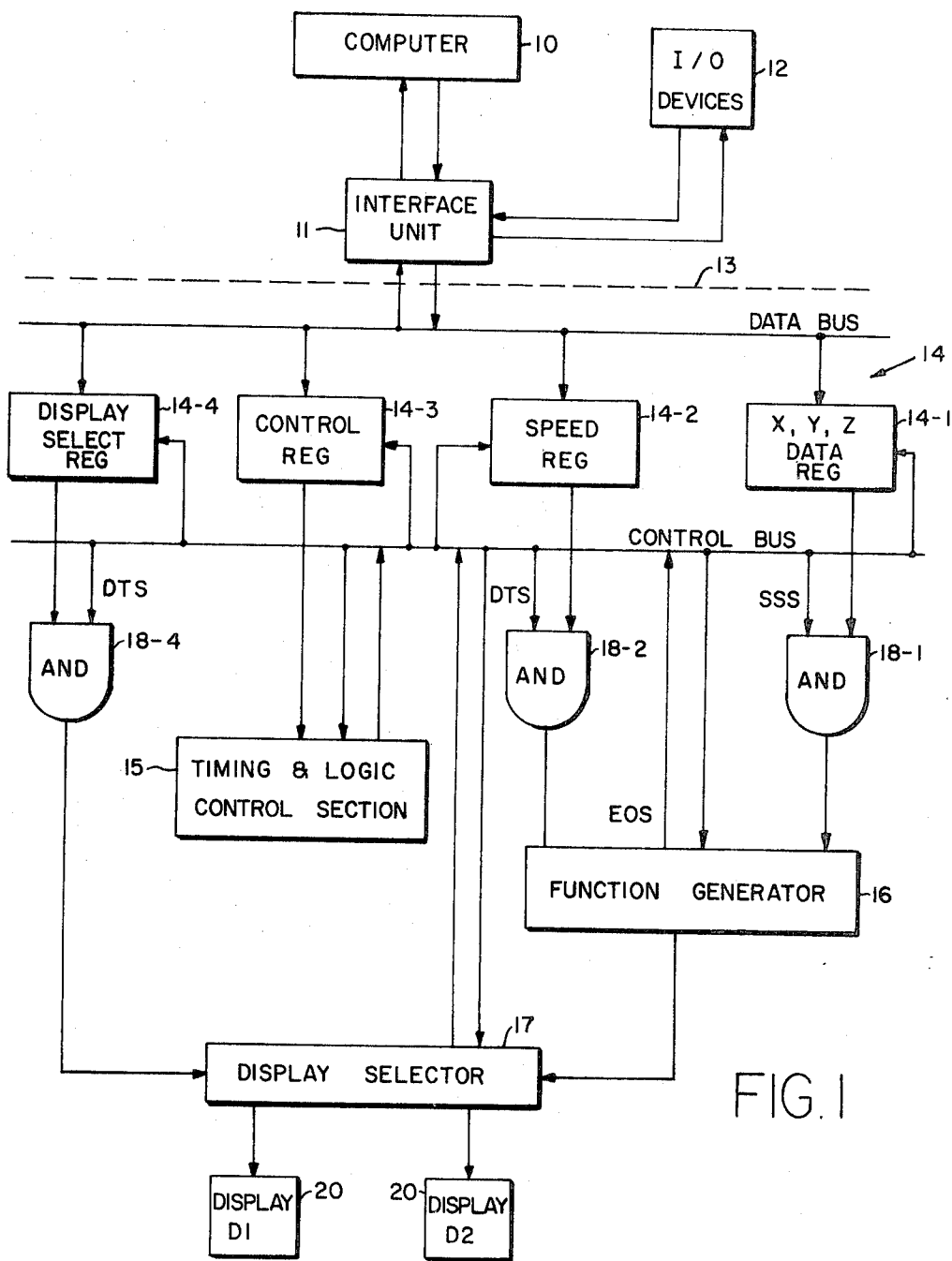
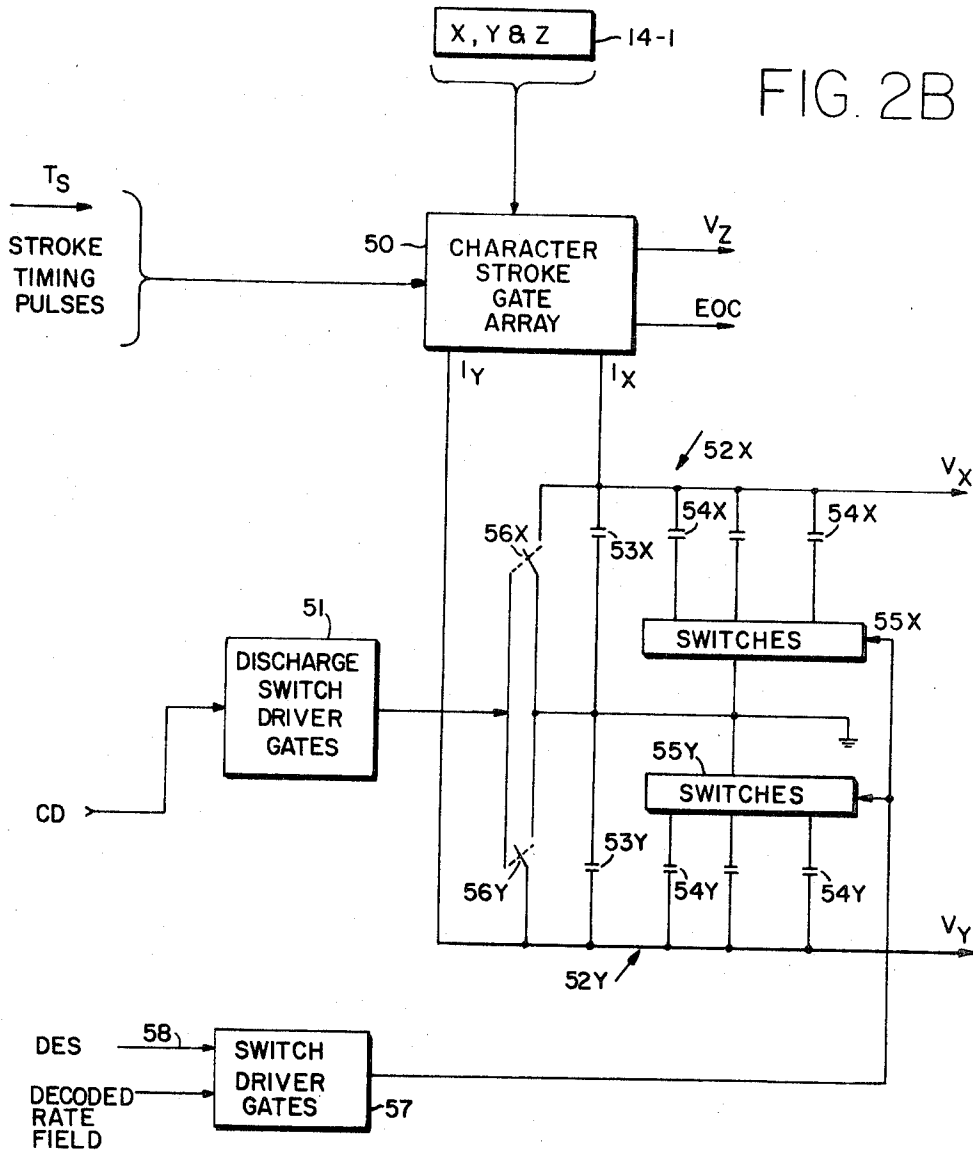


FIG. 1

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FIG. 2B

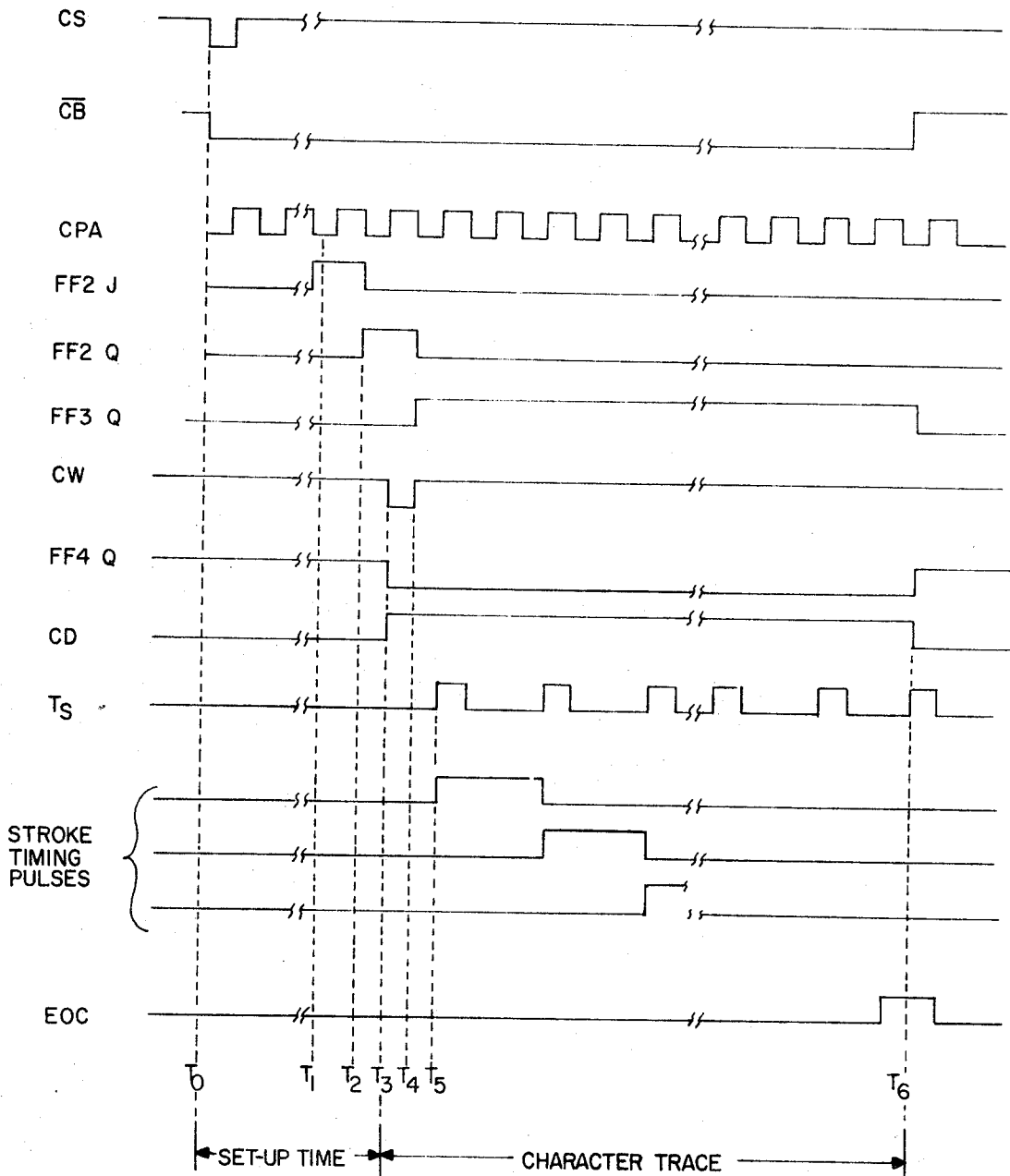


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FIG. 3



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## VARIABLE RATE DISPLAY GENERATOR

### BACKGROUND OF THE INVENTION

This invention relates to information systems and in particular to techniques and apparatus for providing display of information.

One type of present day information system employs a cathode ray tube (CRT) type indicator which is driven by a suitable signal source of X, Y and Z modulation. The signal source in some applications takes the form of a simple video source including sweep controls, such as radar or television. In other applications, the signal source takes the form of a digital computer which controls the visual presentation of symbolic data (alphanumeric, lines, conics and the like) on the CRT screen. In some applications the digitally generated symbolic data can be mixed with video under the control of the computer.

In many computer controlled display systems, the computer has stored in its memory an instruction set indicative of a symbolic set to be displayed. The instruction set is applied at a suitable refresh rate to a display generator which responds to the instructions to generate the X, Y and Z modulation indicative of the set of symbols. The X, Y and Z modulation is then applied to the CRT indicator to present a visual display of the symbol set. The computer generally responds to various input devices, such as keyboards, light guns, sensing devices, and others so as to update the instruction set in real time (i.e., a relatively short response time).

Computer controlled display systems have generally employed various types of CRT indicators. Where large amounts of data are to be presented at one time, high speed indicators (on the order of 500,000 inches per second writing rate) have been employed. In other cases, CRT projection type indicators (on the order of 250,000 inches per second) have been employed. In still other cases, CRT hard copy indicators (on the order of 5,000 to 10,000 inches per second) have been employed. In general, each such display has required a separate display generator and a separate refresh channel to the computer memory. Because of this, multi-station display environments have not been able to efficiently monitor data on a real time basis.

Multi-station real time display system environments, such as automatic checkout systems, human factor study systems, simulation systems, educational training systems, avionic systems and others, generally require different visual presentations of the data content for different purposes. For instance, an automatic checkout system for an aircraft may require that a large amount of dynamically changing data be displayed on a single indicator at one station. For this purpose, a high speed indicator may be employed. At another station, only a portion of the data may be required to be displayed on a CRT projection type indicator. At still other stations, a portion of the data may be required to be displayed on a CRT hard copy unit.

### BRIEF SUMMARY OF THE INVENTION

An object of the present invention is to provide novel and improved techniques and apparatus for generating information at variable rates.

Another object is to provide display apparatus capable of operating plural display indicators which have different writing rate capabilities.

Yet another object is to provide display apparatus in which plural display indicators having different writing rates share a single display generator.

Still another object is to provide a character generator capable of dynamically shifting over a wide range of generating rates.

Briefly the display apparatus of the invention is embodied in a computer controlled display generator which responds to an instruction set provided by a computer to generate driving energy at different rates for one or more display indicators. The display generator includes function generator means responsive to the instruction set to generate the driving energy

at selected generating rates. A display selector means also responsive to the instruction set couples the generated driving energy to a selected one or ones of the display indicators.

The function generator is embodied in apparatus having means for producing X and Y axis modulation signals. Rate varying means is coupled to the X and Y signal producing means to vary the rate at which the X and Y signals are produced. In one embodiment, the rate varying means produces timing signals at a selected one of plural frequencies. The producing means receives these timing signals and operates at the selected frequency to generate constant currents of different values each having a time duration which is a function of the selected frequency. In this embodiment, the producing means further includes a ramp generator having a plurality of capacitors and switching means responsive to the timing means to selectively couple said capacitors across one another in combination. Each of the combinations corresponds to a different timing signal frequency such that the same change in voltage is produce for any one of the constant currents at all operating frequencies.

### BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings like reference characters denote like structural elements, and

FIG. 1 is a block diagram of a computer controlled display apparatus embodying the present invention;

FIGS. 2A and 2B are block diagrams in part and circuit schematic diagrams in part of a variable rate character generator further embodying the invention;

FIG. 3 is a waveform diagram of various ones of the timing signals produced and employed in the FIGS. 2A and 2B character generator embodiment.

### DESCRIPTION OF PREFERRED EMBODIMENTS

Referring to FIG. 1 an information display system embodying the invention is illustrated as including a digital computer 10 associated with an interface unit 11 by way of which computer 10 communicates with various input - output (I/O) devices 12 and display generation apparatus 13 (shown below the dashed line). In FIG. 1, communication buses or data flow paths are illustrated as single lines. However, it is to be understood that each such bus or path may consist of a large number of conductors. For example, the DATA BUS consists of a number of conductors equal to the number of bits in a word. In addition where such a bus or path is applied as an input to a gate, it is assumed that the gate actually consists of a number of gates equal to the number of bits carried by the bus or path, such that each bit is applied to a different gate.

The computer 10 has a memory in which is stored in digital form instructions for producing various patterns of X, Y and Z modulation for application to plural display indicator channels 20. Although only two such channels designated D1 and D2 are illustrated, it is to be understood that many more channels may be employed. The illustrated display indicators are, for the purpose of example, considered to be CRT type indicators having different beam deflection speed ranges. Thus, indicator D1 has a deflection (writing) speed of W1 and D2 has a writing speed of W2.

The display generation apparatus 13 fetches the instructions from the memory of computer 10, processes the instructions, generates X, Y and Z modulation, and selects which one of the display indicators D1 or D2 is to be connected to receive the X, Y and Z modulation.

Each set of instructions in the memory of computer 10 is updatable by means of a stored program contained therein and by means of various peripheral devices 12, for example, light guns, tape or card reader devices, keyboard devices and the like. The updating or current sensor data is coupled via an interface unit 11 to computer 10 where it is processed according to the stored program to update the instruction set.

The display generator 13 includes a register section 14, a timing and logic control section 15, a function generator 16

and a display selector 17. The instructions are fetched from the memory of computer 10 under the control of the timing and control section 15. To this end, the register section 14 includes a control register means 14-3 for receiving the instructions from computer 10 via a DATA BUS and interface unit 11. The timing and control section 15 then processes or interprets the received instructions. The instructions may require data contained therein to be loaded into various ones of the registers in section 14 and/or may require various beam deflection patterns to be generated. The timing and logic section 15 responds to the instructions to cause the data to be loaded into the specified registers as well as to cause the function generator 16 to generate the specified beam deflection patterns and the display selector 17 to select one of the indicators D1 or D2 to receive the generated beam deflection pattern. For this purpose a CONTROL BUS is shown in FIG. 1 to receive control information from control section 15 and to translate such information to various ones of the registers in section 14, or to the function generator 16 or to the display selector 17, as required. In addition, the CONTROL BUS is adapted to receive other control signals from the various parts of the display generator 13 and to translate such other control signals to the timing and logic section 13. These other control signals may represent response status information, such as end of character and end of line generation by the function generator.

Although the control register 14-3 is illustrated as a single block, it is to be understood that the control register may include a number of registers. For example, the control register may include a memory data register for receiving incoming instructions from the computer 10, an instruction register for holding a current instruction while it is being processed and a memory address register for holding the address of the next instruction to be fetched. In addition, the control register may include other registers associated with the modification of the memory address register and still other registers associated with the timing, frame synchronization, and the operation mode of the display generator 13.

Each beam deflection pattern to be applied to either of the CRT indicators D1 and D2 must be repetitively generated (refreshed) in order to present a continuous (non-flickering) visual display. By way of example for a 60 hertz refresh rate, display generator 13 must fetch the set of instructions from computer 10 and process them to generate X, Y and Z modulation 60 times every second or once every 16.6 milliseconds. To this end, the display generator 13 includes a frame sync or refresh generator (not shown) which provides a refresh clock or sync signal to operate the control section 15 and hence, the display generator at a 60 hertz rate or other suitable rate.

A feature of the present invention is that the display generator 13 can be time shared by the different writing rate indicators D1 and D2 in contrast to prior art systems where separate display generators are required for each such indicator. To this end, the register section 14 includes a display select register 14-4, a speed register 14-2 as well as an X, Y and Z register means 14-1. The register means 14-1 is employed in the conventional manner as a buffer and holding register means for the X, Y and Z data indicative of a particular symbol (either alphanumeric, line, or conic) or of a simple beam deflection positioning move in which the beam is ordinarily blanked. The display select register 14-4 is employed to hold a digital number or bit field indicative of the display indicator D1 or D2 to be selected. The speed register 14-2 is employed to hold a bit field indicative of the writing rate for the selected indicator and as such controls the rate at which the X and Y deflection signals and the Z unblanking signal are generated. That is, the slopes of the X and Y beam deflection voltages are determined, in part, by the bit field of the speed register 14-2.

A typical operational sequence would be to first load the display select and speed registers 14-4 and 14-2, respectively. When the loading operation has been completed, the timing section 15 transmits a data transfer signal DTS by way of the CONTROL BUS to AND gates 18-4. The DTS signal enables

AND gates 18-4 to pass the display select bit field to the display selector 17. The display selector 17 is, for example, a crossbar type switch which responds to the display select bits to connect one of the indicators D1 or D2, say D1, to the output of the function generator 16.

The DTS signal also enables AND gates 18-2 to pass the writing rate bit field to the function generator 16. The writing rate bit field conditions the function generator to generate X, Y and Z signals corresponding to the X, Y and Z digital data at a specific generating rate corresponding to the value W1 of the field. The X, Y and Z data for a desired symbol are then loaded into the X, Y and Z register means 14-1. After this loading operation is staticized, the timing and control section 15 transmits a symbol start signal SSS to enable AND gates 18-1 to pass the X, Y and Z data to the function generator 16. The function generator 16 then responds to the X, Y and Z digital data to produce X, Y and Z modulation at a rate determined by the numeric value W1 of the writing rate bit field as pointed out above.

When the symbol has been generated, the function generator 16 transmits an end of symbol signal EOS to control section 15 via the CONTROL BUS to signify that X, Y and Z data for the next symbol may now be received. The control section 15 responds thereto to load the X, Y and Z register 14-1 and to issue another symbol start signal SSS. This operation continues until X, Y and Z modulation has been generated for all the symbols contained in a current instruction set. This symbol generation then continues repetitively at the refresh rate.

As pointed out previously, while a particular instruction is being processed, other instructions in the set may be updated or made current. For example, suppose indicator D1 is displaying a symbol set and an operator at indicator D2 requests via I/O devices 12 (for example a keyboard) that the information be presented to D2. The computer 10 responds to this request to format a new display select instruction and a new writing rate instruction for loading register 14-4 and 14-2. These new instructions are then inserted into the instruction set to replace the former D1 and W1 values. When these instruction locations are again addressed, the display generator 13 responds to the new values D2 and W2 to select display D2 and conditions function generator 16 to operate at the W2 rate.

It is to be understood that the foregoing operational sequence is exemplary and that many other modes are possible. For instance, a current instruction set could be updated so as to cause the display generator to access an entirely different instruction set in another segment of the computer memory. A significant advantage of the FIG. 1 embodiment is that the display indicators D1 and D2 can time share the display generator 13 so as to present common or unique sets of symbols and/or video images on both indicators for simultaneous visual observation. This, of course, involves appropriate formatting and interleaving of the instruction set so as to provide display select instructions at appropriate points in the refresh cycle so as to couple the proper indicator channel to the function generator 16 and/or to a video (either radar or television) source (not shown) at the proper times. Graphic or video data can be mixed with graphic or symbolic data for display on a common CRT screen by producing the symbol set during the normal end of sweep dead time interval for the case of radar or during the vertical retrace interval for the case of television. In addition, the symbol set can also be produced on an asynchronous basis by sweep stealing (radar) or line stealing (television) in order to present large amounts of symbolic data. These video mixed mode options are unnecessary to an understanding of the present invention, and are therefore not specifically illustrated.

Although the function generator 16 may include any type of symbol generator, such as a line (or vector), conic, character and other types of symbol generators, the invention is herein illustrated in FIGS. 2A and 2B in a character generator embodiment. For an example of a line generator embodiment reference is made to a co-pending application entitled Varia-

ble Rate Line Generator, Ser. No. 817,786, filed Apr. 21, 1969, by Robert D. Stoddard, Arnold Schumacher and John R. Longland and assigned to the assignee of the present application.

Referring next to FIGS. 2A and 2B, the variable rate character generator embodiment of the invention is shown to include in FIG. 2B a character stroke gate array 50, X and Y ramp generators 52X and 52Y, respectively, and in FIG. 2A a clock or timing signal producing means 60 (below the dashed line). In FIG. 2A the clock signal producing means responds to a symbol start signal, designated as character start (CS), from the CONTROL BUS, to produce a master stroke timing signal  $T_s$ , the frequency of which is a function of the speed or writing rate bit field provided by a portion 14-2a of register means 14-2 of FIG. 1. The frequency of timing signal  $T_s$  is also a function of a size bit field which is provided by another portion 14-2b of register 14-2 of FIG. 1. The timing signal producing means also produces a number of stroke timing pulses and a character draw (CD) timing signal. As shown in the common time base waveform diagram of FIG. 3, the CS,  $T_s$ , and CD signals serve to apportion the operation of the character generator into a set up time  $t_0$  to  $t_3$  followed by a character trace time  $t_3$  to  $t_6$ . Although only three stroke timing pulses are shown in FIG. 3 the clock signal producing means provides one such stroke pulse during each period of the timing signal  $T_s$ .

In FIG. 2B the character gate stroke array 50 receives X, Y and Z coded character data from register means 14-1, decipheres the coded data and, in combination with X and Y ramp generators 52X and 52Y, provides X and Y axis stroke deflection signals  $V_x$  and  $V_y$  and a Z axis unblanking signal  $V_z$ . At each character location on the display indicator screen, the CRT beam is deflected in a pattern determined by the  $V_x$  and  $V_y$  deflection signals and unblanked in accordance with the  $V_z$  unblank signal. Thus, the stroke gate array 50 generates or writes a character on the face of the CRT according to the cursive writing technique by generating a unique set or pattern of strokes (vectors or lines) which together make up the character.

The array 50 includes a decoder (not shown) for decoding the character data and a buffered stroke gate array (not shown) of which different stroke gates receive different ones of the stroke pulses. The decoded character data enables a unique set of the stroke gates such that a particular sequence of the stroke pulses are selected. The occurrence of each of the selected stroke pulses signifies a change in stroke or vector direction such that the time difference between successive selected strokes constitutes the tracing time of a stroke. The outputs of the stroke gates are buffered under the control of the stroke timing signal  $T_s$  and applied to a current generator (not shown). The current generator responds to the  $T_s$  clocked buffering of each selected stroke pulse to produce constant currents  $I_x$  and  $I_y$ , the values of which correspond to the X and Y components of the stroke. Thus, the currents  $I_x$  and  $I_y$  for each character are essentially a sequence of constant currents, the values of which, though independent of the frequency of timing signal  $T_s$ , are changeable upon the occurrence of the selected stroke pulses. That is, the values of  $I_x$  and  $I_y$  are the same for a given stroke for any of the writing rates. The stroke gate array also contains means (not shown) for producing the  $V_z$  unblank signal in synchronism with the stroke currents  $I_x$  and  $I_y$  and for producing an end of character (EOC) signal upon the generation of the last stroke of a selected character. For a more specific description of a stroke gate array which could be employed, reference is made to a co-pending application Ser. No. 665,116, filed Sept. 1, 1967, for Richard Bouchard, entitled CHARACTER DISPLAY SYSTEM U.S. Pat. No. 3,533,096 issued Oct. 6, 1970 and assigned to the present assignee.

The Z axis unblank circuitry is not shown in FIG. 2B since it is unnecessary to an understanding of the present invention. Suffice it to say here, that the array 50 includes Z axis circuitry which responds to the start and end of the various strokes to selectively unblank the CRT beam so as to trace the character.

The stroke currents  $I_x$  and  $I_y$  are applied to X and Y ramp generator sections 52X and 52Y respectively. The ramp generator sections 52X and 52Y are substantially identical and like components are designated by like reference numerals followed by alphabetic characters X and Y to indicate corresponding locations in the X and Y sections, respectively. Consequently, only the X ramp generator section 52X will be described in detail.

The X ramp generator 52X includes a bank of capacitors comprised of capacitor 53X and plural capacitors 54X. The capacitor 54X is connected between the  $I_x$  stroke current lead and circuit ground. The capacitors 54X have separate serially connected switches, designated collectively as 55X, which are selectively operable to connect capacitors 54X in various combinations in circuit between the  $I_x$  current lead and circuit ground. The switches 55X, for example, may be transistor type switches. The X ramp generator 52X further includes a discharge switch 56X which is open during character trace time intervals and closed during set-up intervals. It is to be noted that discharge switch 56X is shown as ganged with discharge switch 56Y to illustrate that both the X and Y capacitor banks are discharged at the same time. Like the switches 55X, the switch 56X may be of a transistor type, but is shown as a simple switch for ease of description.

The discharge switches 56X and 56Y are driven by discharge switch driver gates 51. The discharge gates 51 respond to the trailing edge of the CD signal (end of character trace period) at time  $t_0$  to close switches 56X and 56Y and to the leading edge thereof (start of character trace) at time  $t_3$  to open switches 56X and 56Y. The capacitor switches 55X and 55Y are driven by switch driver gates 57.

The switches 55X and 55Y are driven by switch driver gates 57 which are selectively enabled by the decoded rate or speed bit field. The switch driver gates 57 also respond to a driver enabling signal DES on lead 58. The DES signal conditions driver gates 57 to close all of the switches 55X and 55Y at the end of a character trace to assure that all of the capacitors 54X and 54Y are discharged. The DES signal enables the gates 57 during the set-up time  $t_0$  to  $t_3$  (FIG. 3) to open selected ones of the switches 55X and 55Y in response to the decoded rate field.

To summarize the foregoing discussion, the charging interval  $\Delta t$  for a particular stroke is selected according to the writing rate or speed bit field. In addition, the capacitance value is also selected as a function of the writing rate such that the same amount of beam deflection energy is produced for any particular stroke for all writing rates. That is, the values of both C and  $\Delta t$  in the charging relation (equation 1) of  $C \Delta V = I \Delta t$  are each varied in accordance with the writing rate so as to insure a constant value of  $\Delta V$  (voltage change) at all writing rates for any one particular value of current I. The effect of this is that the slopes of the beam deflection increments  $\Delta V_x$  and  $\Delta V_y$  change from one writing rate to another for a particular stroke. Thus, for a selected writing rate or charging interval  $\Delta t$ , the stroke gate array 50 and the ramp generators 52X and 52Y produce beam deflection signals  $V_x$  and  $V_y$  consisting of a succession of analog voltage ramps, each of which corresponds to a particular stroke and all of which form the character called for by the character code. When the writing rate ( $\Delta t$ ) is changed for this particular character, the slopes of the analog ramps also change, but the voltage changes  $\Delta V$  do not change.

For one example of the character generator embodiment employing a two bit character size code, a three bit speed code six capacitors each for 54X and 54Y, and a maximum 22 stroke per character capability, Table I shows the maximum writing time in microseconds (Usec) for selected sizes and speeds. It is noted that one dit equals the amount of displacement caused on the display surface area by changing either the X OR Y coordinate data one least significant bit.

TABLE I

CHARACTER WRITING RATES

(Maximum Tracing Time for a 22 Stroke Character)

Character Size	1	2	3	4	
Size Code	00	01	10	11	
Nominal Character Height	16 Dits	32 Dits	48 Dits	64 Dits	
Speed Range	Speed Code	$\mu\text{sec}$	$\mu\text{sec}$	$\mu\text{sec}$	$\mu\text{sec}$
1	000	3.3	6.6	9.9	13.2
2	001	6.6	13.2	19.8	26.4
4	010	13.2	26.4	39.6	52.8
8	011	26.4	52.8	79.2	105.6
16	100	52.8	105.6	158.4	211.2
32	101	105.6	211.2	316.8	422.4
64	110	211.2	422.4	633.6	844.8

The timing signal producing means 60 (FIG. 2A) will now be described in detail. In the description, which follows, a number of J-K flip-flops are employed. Briefly, a J-K flip-flop is one which yields a predictable output for every possible combination of input signal levels. The J-K flip-flop exhibits the properties reflected in the following Truth Table wherein  $t_n$  represents the bit time before a clock pulse,  $t_n + 1$  represents the bit time after a clock pulse and  $Q_n$  represents the state of the flip-flop during the  $t_n$  bit time.

TRUTH TABLE

$t_n$ J	K	$t_n + 1$ $Q_{n+1}$
0	0	$Q_n$
0	1	0
1	0	1
1	1	$Q_n$

For the purpose of the following description, the convention of positive logic is arbitrarily adopted wherein the binary "1" and "0" signal levels correspond to the most positive (HI) and most negative (LO) signal levels, respectively. With reference to the above TRUTH TABLE, if "0" signal levels are applied to both J and K input terminals, the flip-flop remains in its pre-existing state  $Q_n$ , i.e., there is no change in the state of the flip-flop. If "1" signal levels are applied to both the J and K input terminals, the state of the flip-flop is reversed from the pre-existing state, i.e., the flip-flop acts as a triggerable flip-flop. If "0" and "1" signal levels are applied to the J and K terminals, respectively, the Q output assumes a "0" level. Finally, if "1" and "0" levels are applied to the J and K terminals, respectively, the Q output assumes a "1" level. In addition, each of the illustrated J-K flip-flops includes a preset (R) input terminal which when driven LO ("0" level), sets the flip-flop in a DC manner (independently of the clock rate) to the  $Q = "1"$  state.

When it is desired to trace a character, the timing and logic control 15 (FIG. 1) transmits a negative going character start CS pulse to the CONTROL BUS. In the FIG. 3 waveform diagram, the leading edge of the CS pulse occurs at time  $t_0$ . Referring now to FIG. 2A, the CS pulse is received by the character generator at the R input of a character busy flip-flop FF1. The character busy flip-flop FF1 is operable to provide a "1" level character busy CB signal at its Q output for the duration of the set-up and character trace times and a "0" level signal at all other times. To effect this operation, the flip-flop FF1 has its J terminal grounded ("0" level) and its K terminal connected to receive the end of character EOC signal at the termination of the character trace. The clock terminal C of FF 1 receives a synchronizing clock signal  $C_s$  from the timing and logic control section 15 (FIG. 1) via the CONTROL BUS. Prior to

receipt of the CS pulse and specifically at the end of the previous character trace, the EOC "1" signal pulse places FF1 in a condition where its outputs Q and  $\overline{Q}$  (CB and  $\overline{CB}$ , respectively) are "0" and "1" levels, respectively. That is, after the EOC signal returns to the "0" level, succeeding  $C_s$  clock pulses effect no switching of the flip-flop (both J and K are "0"). When the character start CS signal drives the R input to the "0" level, the FF 1 Q and  $\overline{Q}$  outputs become "1" and "0" levels, respectively. The duration of the CS pulse is sufficient to permit FF 1 to switch. When the  $C_s$  pulse terminates, succeeding  $C_s$  clock signals do not switch FF 1 since both the J and K inputs are receiving "0" levels. The  $\overline{Q}$  or  $\overline{CB}$  signal is coupled to a Preset Line which is coupled to various parts of the timing signal section 60 as illustrated by the dashed lines, the dashed lines being broken to simplify the drawing. The waveform of the  $\overline{CB}$  signal is illustrated in FIG. 3.

The "1" level Q output or CB signal initiates an oscillator 61 to produce clock signal CPO. The oscillator 61, for example, may be a blocking type oscillator. The CPO clock signal is divided by a speed frequency divider 62 which is programmable in accordance with the decoded bit field of the speed or writing rate register 14-2a. For this purpose a decoder 63, which may be of a conventional type, is provided. The output of the speed frequency divider 62 is a clock signal CPA, the waveform of which is shown in FIG. 3. The CPO clock signal waveform is not shown in FIG. 3 in order to simplify the drawings. The speed frequency divider 62, for example, may include a binary counter and an output gate array which is programmable in accordance with the decoded speed bit field so as to divide the CPO clock signal by various powers of two. For the previously mentioned three bit speed field example, the speed frequency dividers would be 1, 2, 4, 8, 16, 32, and 64.

The CPA clock signal is utilized to drive a size frequency divider 75 as well as a number of flip-flops and gates. The size frequency divider 75 is programmable in accordance with the size bit field provided by register portion 14-2b. This size bit field is decoded (by means not shown). The output of divider 75 is delayed before application to a clock control unit 66. To this end the output of divider 75 is applied as one input to NAND gate 65. Another input of the NAND gate 65 receives the CPA clock signal. A third input of NAND gate 65 is coupled to the Q output of flip flop FF 3. By definition, a NAND gate is one in which its output is a "0" level only when all of its inputs are "1" levels. When any one or more of a NAND gates inputs is a "0" level, the output is "1" level.

The NAND gate 65, then, is operable to pass the output of divider 63 only when both the CPA signal and the Q output of FF 3 are both "1" levels. The CPA clock signal, of course, is periodically a "1" level signal in coincidence with the slower frequency output of divider 75. For example, a size division by a factor of 2 produces a "1" level of the size divided signal in coincidence with every other "1" level of the CPA signal. The NAND gate 65 is inhibited by the Q output of FF 3 in order to institute a delay into the timing signal apparatus 60 to thereby provide the set-up time (FIG. 3).

To effect the set-up delay, the CPA signals are further applied to a programmable delay 64 which is operable to produce a "1" signal pulse at its output after a delay which is triggered by the receipt of the clock signal CPA. The delay 64, for example may include a ring counter which is clocked at the CPA rate and gating arrangement which is programmed by the decoded speed bits to respond to an output of one of the counter stages to produce the one signal pulse output of the delay section 64. It is noted that the programmable delay section 64 is preset by the  $\overline{CB}$  signal to assure that the ring counter is clear before a new character is generated. The output waveform of delay 64 is designated in FIG. 3 as FF 2 J. The waveform diagram in FIG. 3 is broken between times  $t_0$  and  $t_1$  to illustrate that the set-up time is variable in accordance with the writing rate or speed bit field.

The "1" signal level of the delay section 64 is applied directly to the J input of a flip-flop FF 2 and by way of an in-

verter 67 to the K input of FF 2. Both FF 2 and FF 3 are clocked by the CPA signal and both are preset by the  $\overline{CB}$  signal so as to drive their respective Q outputs to "0" levels at time  $t_0$  when the character start CS signal is received by FF 1. The waveforms of the CPA clock signal and of the J input of the FF 2 flip flop are shown in the waveform diagram of FIG. 3. Thus, so long as the output of delay 64 (FF 2 J waveform in FIG. 3) is a "0" level, the J inputs to both flip-flops FF 2 and FF 3 are "0" levels and their corresponding outputs are also "0" levels as illustrated prior to  $t_1$  in FIG. 3. During the next bit time (negative going edge of CPA) after the output of delay 64 becomes a "1" level, flip flop FF 2 switches and its output Q assumes a "1" level as shown at time  $t_2$  in FIG. 3.

The next trailing edge of the CPA clock occurs at time  $t_4$  and switches FF 3 to provide a "1" level signal at its Q output. This "1" level signal enables NAND gate 65 to produce the clock signal  $\overline{T_s}$ , the complement  $T_s$  of which is illustrated in the waveform diagram of FIG. 3. The clock signals  $\overline{T_s}$  are illustrated, by way of example, for a size division of 2. The  $T_s$  clock signal are applied to the clock control unit 66 which responds thereto to provide the stroke timing pulses and the stroke timing signal  $\overline{T_s}$  as positive going waveforms. That is, unit 66 inverts the  $T_s$  signal to provide the complement  $\overline{T_s}$ . The signal  $\overline{T_s}$  has the same period as the  $T_s$  clock signal and (though not so illustrated) may be shaped as by narrowing.

Referring again to the time  $t_2$  (FIG. 3), the FF 1 Q output "1" signal level is shown in FIG. 2B to be further applied as an input to a NAND gate 68. Another input of the NAND gate 68 receives the Q output of FF 3. The FF 3 Q output is also a "1" level the time  $t_2$  and remains so until time  $t_4$ . The NAND gate 68 has another input which is clocked by the CPA signal such that it produces a negative going pulse interval from time  $t_3$  to  $t_4$ , designated as a character write CW signal in FIGS. 2B and 3. The CW pulse signal is applied to the R input of another flip-flop FF 4. The FF 4 flip flop responds to the character write CW signal to drive its Q output to a "0" level. The Q output is inverted by an inverter 69 to provide the character draw CD signal as shown in FIGS. 2B and 3. The FF 4 flip-flop has its K terminal grounded ("0" level) and its J input connected to receive the EOC signal. Since EOC is also a "0" level for the duration of the character set-up and trace times, the clock signal  $T_s$  does not cause FF 4 to change states while the character is being traced. Thus the character draw CD signal remains a "1" level for the duration of the character trace interval. Since the EOC signal assumes a "1" level in response to the end of character EOC signal, the FF 4 flip-flop will then switch on the next  $T_s$  trailing edge to thereby drive its Q output to the "1" level and terminate the character draw signal. The  $T_s$  timing signal can be utilized to terminate the character draw signal in so far as there is a switching delay associated with flip flops FF 1 and FF 2 before the timing signal  $T_s$  terminates.

Referring again to time  $t_1$  (FIG. 3), the output of delay unit 64 is further employed to enable the switch driver gates 57 which drive switches 55X and 55Y. To this end, the output of delay 64 is coupled to the S input of a two NAND gate 70a. The output of NAND gate 70a and the output of another two input NAND gate 70b are cross coupled to one input of the other. The remaining input of gate 70b receives an input R. The R input is coupled by way of a differentiator 71 to receive the CD signal from the output of inverter 69. The output of gate 70a (also designated as driver enabling signal DES) is further coupled via lead 58 to condition the switch driver gates 57.

The NAND gates 70a and 70b operate as follows. Assume that prior to time  $t_1$  (FIG. 5) the outputs of NAND gates 70a and 70b are "0" and "1" respectively. Also prior to time  $t_1$  the S input is a "1" (the inverted "0" output of delay 64). Finally, the differentiator 71 provides a "0" at the R input of gate 70b. At time  $t_1$  the inverted output of delay 64 becomes a "0" and NAND gate 70a switches to provide a "1" signal value of DES to the switch driver gates 57. The switch driver gates 57 responds to the "1" signal level to open selective ones of the

switches 55X and 55Y. At time  $t_3$ , the differentiator 71 responds to the rising edge to provide a below ground signal to the R input. However, NAND gate 70b does not respond thereto since both of its inputs must go positive in order for it to switch. Thus, the outputs of both NAND gates 70a and 70b are "1"'s at time  $t_1$  and remain so until time  $t_6$ . At time  $t_6$ , the differentiator 71 responds to the falling edge of the CD signal to provide a positive going "1" pulse signal to the R input of NAND gate 70b. The NAND gate 70b then switches at this time to provide a "0" at its output. The duration of the differentiated pulse at the R input is sufficient to span the negative going transition which occurs at the S input due to the resetting of the delay 64 by the  $\overline{CB}$  signal. Thus, just after time  $t_6$  the S input becomes a "1" and the R input becomes a "0" when the differentiated positive going pulse terminates. The NAND gate 70a switches at this time to provide a "0" at its output. The "0" level value of DES causes the switch driver gates 57 to close all of the switches 55X and 55Y to assure complete discharging of the capacitors 54X and 54Y.

To summarize the character generator operation, the timing signal producing means 60 produces timing signals CD,  $T_s$  and the stroke timing pulses at a rate or frequency which is a function of the numeric value of the speed or writing rate number (set of digital data). The character generating array 50 and ramp generators 52X and 52Y respond to these timing signals to produce the X, Y and Z modulating signals at a rate corresponding to the speed bit rate.

There has been described a computer-controlled display generator capable of producing X, Y and Z modulating signals at variable rates. In the illustrated embodiment the generating rate has been shown as dependent on symbol size and display indicator writing rate. However, it is to be understood that the variable generating rate techniques can be employed in various other manners. For example, the code contained in register 14-2a could represent parameters other than indicator writing rates. Thus, if both the 14-2a and 14-2b register code represented variable sizes, one could be employed to vary the capacitor banks 52X and 52Y and the other one to vary the frequency of the timing signals. Such a scheme could then present characters in different size ranges with the character size in each range being further variable within its range.

The display generator is capable of being time-shared by plural display indicators having different writing rates as in a multistation display environment. Though illustrated with a cursive writing techniques, the variable rate character generator technique is equally applicable to raster scan, dot generating and other writing techniques. Although the illustrated embodiments have been described as driving CRT type indicators, the invention is also applicable to any type indicator which responds to modulating drive energy in three directions. Thus, display generator apparatus embodying the present invention can be employed to drive X-Y plotter mechanisms having a marking (or imaging) instrument, such as pin, knife, photohead and the like. In such mechanisms, the X and Y signals move the imaging instrument in a plane parallel to the imaging medium (paper, photographic film, and others), while the Z axis signal provides the pin up and down (light beam on and off) information to trace patterns on the medium. The immediately above comments are also applicable to milling machine mechanisms, where the marking instrument is a tool which is urged against and away from a work piece by the Z axis modulation. Of course, the instruction set need not be repeated or refreshed for either of the plotter or milling mechanism applications. In addition, where it is desired not to operate in real time, the X, Y and Z axis signals for the plotter or milling machining applications can be formatted in an appropriate numerical control code for storage on a paper or magnetic tape which is later read by the plotter or milling mechanism.

What is claimed is:

1. The combination comprising:  
plural display indicators having different writing rates;

signal providing means for providing first, second and third sets of digital data, the values of the first set being indicative of the different writing rates, the values of the second set being indicative of analog signal increments and the values of the third set being indicative of the different indicators;

a function generator coupled to the signal providing means and responding to the first and second sets of data to produce said analog signal increments at rates which are selectable according to the first set of data; and

a display indicator selector coupled to the signal providing means and responding to the third set of data to operatively couple the analog signal increments to corresponding ones of the indicators whereby the selected analog signal rate corresponds to the writing rate of a selected indicator.

2. The invention according to claim 1 wherein the signal providing means includes a data source for providing a set of instructions which includes said first, second and third data sets; and

a register coupled to said data source and having a display select portion for receiving the third data set, a writing rate portion for receiving the first data set and a further register portion for receiving the second data set; and wherein said function generator is coupled to said writing rate and further portions of said register.

3. The invention according to claim 2 wherein the register further includes a control register portion coupled to said data source for receiving said instructions; and wherein a control means processes each instruction received by the control register portion so as to route the first, second and third data sets to the corresponding portions of the register.

4. The invention according to claim 3 wherein the display indicators are cathode ray tube indicators; and wherein the signal providing means provides the instruction set repetitively at a refresh rate.

5. The invention according to claim 7 wherein said second data set is comprised of character codes; and wherein said function generator includes a character generator responsive to said character codes to generate said analog signal increments whereby characters are traced upon the display screen of a selected indicator.

6. The combination comprising signal providing means for providing a first digital number and sets of second digital numbers;

a timing generator coupled to said signal providing means to receive said first digital number for producing timing pulses at selected frequencies which are functions of the value of said first digital number;

means coupled to said signal providing means and to said timing generator for converting said second digital number sets into sequences of constant currents at selected ones of said frequencies;

a ramp generator coupled to said conversion means for receiving said current sequences to produce corresponding voltage ramp sequences; and

means coupled to said signal providing means and to said ramp generator for controlling changes in voltage of said voltage ramps in accordance with the value of said first digital number so that the same changes in ramp voltage occur for the same valued sets of second digital numbers for different values of the first digital number.

7. The invention according to claim 6 wherein said ramp generator includes a plurality of capacitors coupled to receive said current sequences so as to produce said ramp sequences; and wherein said control means includes capacitor switch means coupling said capacitors across one another in combinations selected in accordance with the value of said first digital number.

8. The invention according to claim 7

wherein said control means further includes discharge switch means for discharging said capacitors at the termination of the sequence of currents;

wherein said timing means includes means for indicating the start and end of each said current sequence; and

wherein said discharge switch means responds to said indicating means to open and close at the start and end of each said current sequence, respectively.

9. The invention according to claim 8 wherein one of said capacitors is connected across said discharge switch means; and wherein said capacitor switching means responds to said indicating means to connect all of the remaining capacitors across said discharge switch at the end of each said current sequence and to disconnect selected ones of the remaining capacitors at the start of each said current sequence.

10. Display apparatus comprising first and second display indicators responsive to X and Y axis modulation to trace symbols on their respective display surfaces at first and second writing rates, respectively;

a data source for providing instructions including a display indicator select field indicative of said first and second indicators, a writing rate field indicative of said first and second writing rates and symbol trace fields;

a function generator coupled to said data source to convert said symbol trace fields to X and Y axis modulation signals at first and second operating frequencies which are functions of the value of said writing rate field, which signals have the same amplitude limits for the same symbols at both said writing rates; and

a display selector switch coupled to said data source and responsive to said indicator select field to couple said X and Y modulation signals produced at said first and second frequencies to said first and second indicators, respectively.

11. The invention according to claim 10 wherein said function generator includes a timing generator responsive to said writing rate field to produce timing pulses at said first and second frequencies; and means responsive to said timing pulses to transform said symbol trace fields into said X and Y axis modulation signals.

12. The invention according to claim 11 wherein said transforming means includes means responsive to said timing pulses to convert said symbol trace fields to X and Y sequences of constant currents;

X and Y ramp generators coupled to receive said X and Y constant current sequences to produce corresponding X and Y voltage ramp sequences which form said X and Y axis signals; and

means responsive to said writing rate fields for controlling changes in voltage of said ramps such that the X and Y signals have the same amplitude limits for the same symbols at both said writing rates.

13. The invention according to claim 12 wherein said X and Y ramp generators includes a plurality of X and Y capacitors coupled to receive said X and Y current sequences so as to produce said X and Y ramp sequences, respectively; and

wherein said control means includes X capacitor switches coupling said X capacitors across one and another and Y capacitor switches coupling said Y capacitors across one and another in combinations according to the value of said writing rate field.

14. The invention according to claim 13 wherein said control means further includes X and Y discharge switches connected in circuit with said X and Y capacitors, respectively, for discharging said X and Y capacitors at the termination of each sequence of currents;

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wherein said timing generator includes means for indicating the start and end of each said current sequence; and wherein said X and Y discharge switches respond to said indicating means to open and close at the start and end of each said current sequence, respectively.

15. The invention according to claim 14

wherein one of said X capacitors and one of said Y capacitors are connected across said X and Y discharge switches, respectively; and

wherein said X and Y capacitor switches respond to said indicating means to connect all of the remaining X capacitors and Y capacitors across said X and Y discharge

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switches, respectively, at the end of each said current sequence and to disconnect selected ones of the remaining X and Y capacitors at the start of each said current sequence.

16. The invention as set forth in claim 11

wherein said instructions further include a symbol size field indicative of the size of a symbol defined by said symbol trace field;

wherein said timing generator also responds to said symbol size field so that said first and second frequencies are a function of both said writing rate and symbol size fields.

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