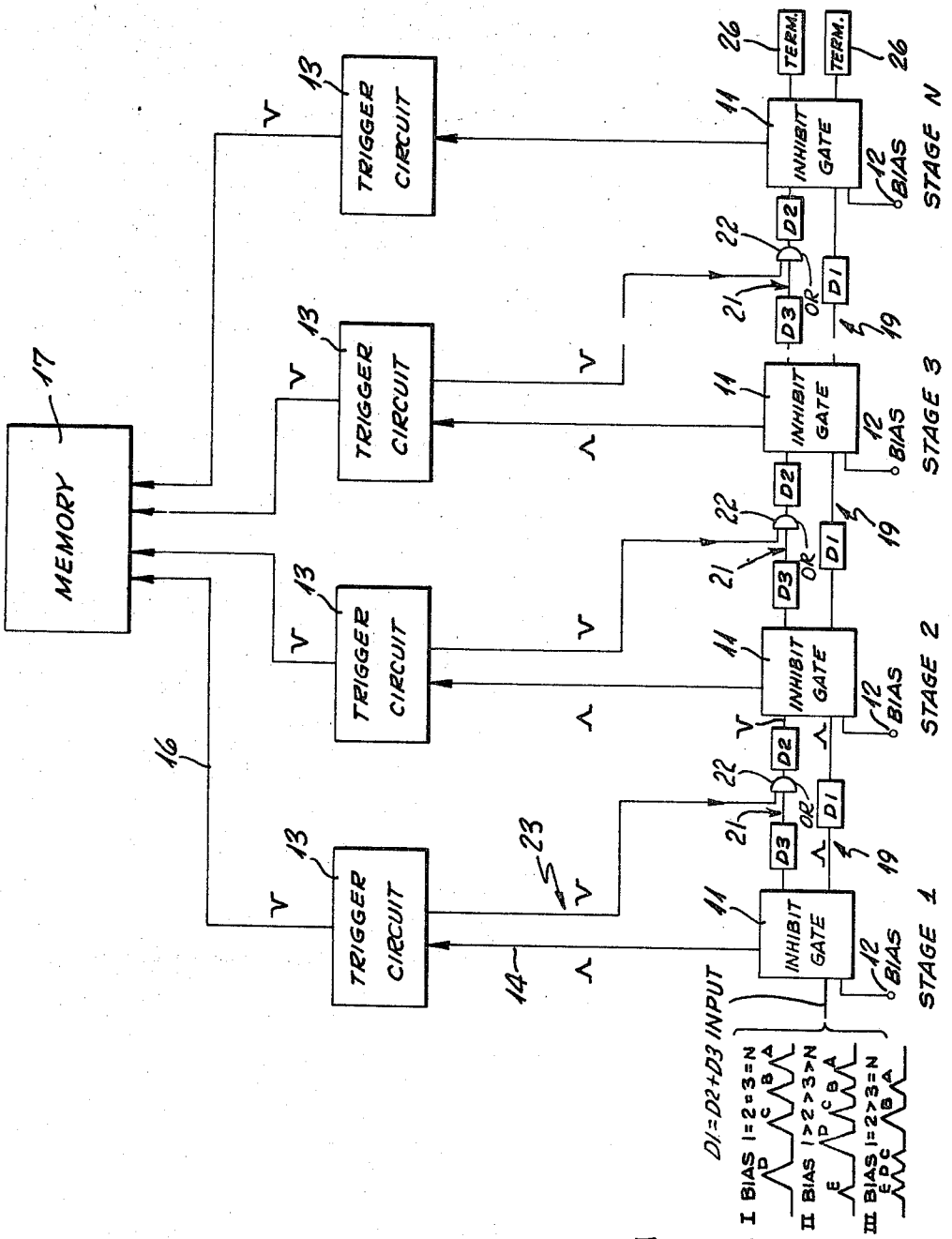
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PULSE SORTING APPARATUS AND METHOD

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PULSE SORTING APPARATUS AND METHOD

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25 Claims

This invention relates generally to a pulse sorting apparatus and method, and more particularly to a pulse sorting apparatus and method for counting or scaling and for sorting of pulses according to amplitude.

Heretofore, previous pulse sorting devices have been serial in their basic operation so that the resolution of the instrument or apparatus was dependent upon the resolution of the first input circuit. Thus, with serially connected binaries often used in such devices, the resolution was dependent upon the resolution of the first binary. As is well known, each binary has a definite time delay before it switches, a switching time, and then a recovery time before it can be switched back. Because of these inherent limitations in binaries and with the present state of the art, the maximum pulse repetition rate which can be accommodated is approximately 50 megacycles per second. Even with such repetition rates, special apparatus and techniques are required. There is, therefore, a definite need for apparatus which can assimilate much higher pulse repetition rates.

In general, it is an object of the present invention to provide a pulse sorting apparatus and method suitable for use with a wide range of pulse repetition rates, that is, from very low pulse repetition rates to vary high pulse repetition rates.

Another object of the invention is to provide a pulse sorting apparatus and method of the above character which has very good double pulse resolution.

Another object of the present invention is to provide a pulse sorting apparatus and method of the above character which can be utilized for counting or scaling.

Another object of the invention is to provide a pulse sorting apparatus and method of the above character which can be utilized for sorting pulses in accordance with their amplitudes.

Another object of the invention is to provide a pulse sorting apparatus and method of the above character which is relatively simple.

Additional objects and features of the invention will appear from the following description in which the preferred embodiment has been shown in detail in conjunction with the accompanying drawing.

Referring to the drawing:

The sole figure is a block diagram of the apparatus incorporating the present invention.

In general, the pulse sorting apparatus consists of a plurality of stages in which each of the stage is capable of sorting pulses at a predetermined rate. The stages are serially connected so that when the pulse repetition rate is greater than that which can be accommodated by a single stage, the pulses are sorted by succeeding stages. An anticoincidence or inhibitor circuit is provided to prevent a pulse which has been sorted in one stage from being sorted in a succeeding stage.

As shown in the drawing, the apparatus consists of a plurality of stages, numbered stage **1**, stage **2**, stage **3**, and stage N. Stage N indicates that the apparatus can consist of any desired number of stages. The number of stages required is primarily dependent upon the resolution of each of the stages and the pulse repetition rate which is likely to be encountered by the apparatus.

Each of the stages consists of an "inhibit" gate **11** of conventional construction which is provided with a bias **12**. The output of the "inhibit" gate **11** in connected to a trigger circuit **13** by a conductor **14**. The trigger circuit **13** is also of any suitable type such as a one-shot or blocking oscillator. The output of the trigger circuit **13** of each of the stages is connected by a conductor **16** to a memory **17**. The memory **17** also can be of any suitable type such as a plurality of scalers, a magnetic tape, or core memory. If a total number of counts is desired, the scalers can be connected to a visual readout device or digital printing device. The memory can also, if desired, include separate readouts for each stage depending upon the end use of the pulse sorting apparatus.

As shown in the block diagram, the stages are serially connected and all feed into the memory **17**. Two separate circuits **19** and **21** are provided for connecting the gate of one stage to the gate of the succeeding stage. As shown, the circuit **19** includes a delay line **D1**, whereas the circuit **21** includes delay lines **D2** and **D3**. A suitable pulse directing device **22** often called a unidirectional two input "or" gate using linear or nonlinear active or passive elements, such as a hybrid transformer, or a diode, transistor or vacuum tube "or" gate, is a part of the circuit **21** and is connected between the delay lines **D2** and **D3**. A circuit **23** connects the output of the trigger circuit of the preceding stage to the pulse directing device **22** in the circuit **21** connecting the preceding stage to the succeeding stage. The output of the gate in the final or last stage is connected to terminating devices **26**.

The delay lines **D1**, **D2** and **D3** are constructed in such a manner that the time delay in

$$D1=D2+D3$$

where **D3** is equal to therelay in the trigger circuit and the conductors leading to and from the trigger circuit. The time delay provided by each of the delay lines is determined by the input pulse characteristics and the speed of operation of the gate and trigger circuits. It should be noted that under certain high speed conditions, the separate delay lines can be eliminated and their functions performed by the delay provided by the interconnecting conductors.

Operation of the apparatus in performing my method for scaling may now be briefly described as follows: Let it be assumed that pulses of the type shown in Group I are being applied to the first stage of the pulse sorting apparatus and it is desired to scale or count the pulses.

Let it be assumed that the bias on the gates of various stages have been adjusted so that the same bias is applied to each of the gates. In this way, the gates can all pass pulses of the same amplitude, and any gate can pass the pulses. The "inhibit" gate **11** in each of the stages is open for receipt of the train of pulses. As soon as pulse A arrives at the "inhibit" gate **11** of the first stage, the gate triggers the trigger circuit **13** which causes a first output pulse to be applied to the memory **17**.

The original pulse applied to "inhibit" the gate **11** of the first stage is also applied to the circuit **19** which includes the delay line **D1**. The trigger circuit **13** is also

connected to the conductor **23** to apply a second output pulse substantially equal in length to the input pulse to the pulse directing device or a unidirectional "or" gate **22**. The unidirectional "or" gate ensures that the pulse from the trigger circuit will move in a forward direction and not rearwardly. The second output pulse from the trigger circuit, therefore, progresses through the delay line D2 and into the "inhibit" gate **11** of the next stage and arrives at the "inhibit" gate **11** in coincidence with the delayed pulse on circuit **19** so that it cancels the effect of the other and, therefore, the "inhibit" gates **11** of the second and succeeding stages cannot operate their respective trigger circuits. Once the pulses are in coincidence, they remain in coincidence because each pulse encounters the same amount of time delay in its circuit as it progresses from one stage to the next. The delay lines, therefore, ensure that when a pulse has operated a trigger circuit, the same pulse will not trigger the trigger circuits of succeeding stages. The time delay provided by the delay lines D2 and D3 is equal to the time delay provided by the delay line D1 and hence equal delay is placed in each of the lines.

Therefore, it can be seen that the first pulse A from the series of pulses will only trigger the first stage and for that reason only one input pulse is applied to the memory **17**.

Now let it be assumed that a second pulse B arrives at the "inhibit" gate **11** of the first stage at a time before the trigger circuit of the first stage has recovered. Since pulse B cannot cause operation of the trigger circuit of the first stage, an output pulse is not applied to the conductor **23**. As the pulse B passes through the circuit **19** including the delay line D1, a time delay will occur. However, since no pulse is applied to the circuit **21** from the conductor **23**, there will be no cancelling or inhibit pulse provided at the time the pulse B arrives at gate **11** of the second stage. Pulse B, therefore, passes through the "inhibit" gate **11** of the second stage and operates the associated trigger circuit **13**. The associated trigger circuit **13** then causes a pulse to be applied to the memory **17**. The pulse B continues on the circuit **19** connecting the "inhibit" gate **11** of the second stage to the "inhibit" gate **11** of the third stage. However, in this case, since the trigger circuit **13** for the second stage has been triggered or actuated, a pulse will be supplied to the circuit **21** connecting the "inhibit" gate **11** of stage **2** to the "inhibit" gate **11** of stage **3** and, therefore, a pulse arrives on circuit **21** at the "inhibit" gate **11** in coincidence with the pulse arriving on circuit **19**, so that the succeeding gates of the apparatus cannot operate their respective trigger circuits. Thereafter, both the pulses pass through the succeeding stages until they are dissipated in the terminations **26** of the last stage.

Now let it be assumed that the third pulse C arrives so rapidly that the trigger circuits of both stage **1** and stage **2** have not recovered. When this is the case, no inhibit pulse is generated by the trigger circuits of the first and second stages. Pulse C, therefore, passes through both of the gates of stage **1** and stage **2** and passes into the "inhibit" gate **11** of stage **3**. The "inhibit" gate **11** of stage **3** causes operation of its trigger circuit and the application of another pulse to the memory **17**.

From the foregoing, it is apparent that any number of stages can be provided so that the pulse sorting apparatus will be capable of assimilating any pulse repetition rate. For example, if necessary, six or seven stages can be provided. When a sufficient time interval elapses, the trigger circuit of the first stage will recover and its sensitivity return to its normal value. When this occurs, the first stage will again be operated by the next succeeding pulse as, for example, by pulse D of the series I. It is possible to visualize that the pulse repetition rate may be so slow that all of the pulses can be sorted by the first stage without help from the additional stages.

It is readily apparent that as the pulses are supplied to the memory **17**, they can be combined as they arrive in the memory or they can be separately stored. For example, it may be desirable to maintain the pulses from each stage in a separate storage element so that time interval statistics can be provided.

Now let it be assumed that it is desired to sort into groups from a series of pulses of different amplitude the pulses which have the same amplitudes. In such a situation, the gates are biased in decreasing steps. That is, the bias on gate **11** of the first stage is greater than the bias on the gate **11** of the second stage. Now let it be assumed that a train of pulses as designated by II is applied to the input of the apparatus. Pulse A is the first pulse. It is of medium amplitude and is applied to the gate **11** of the first stage. Let it be assumed that the bias on the gate **11** of the first stage is such that it cannot be overcome by pulse A. When such is the case, the trigger circuit **13** of the first stage will not be operated and pulse A will travel down the circuit **19** including the delay line D1 to the second gate. Since the gate **11** of the second stage has a bias which is less than the gate **11** of the first stage, let it be assumed that the pulse A is of sufficient amplitude to overcome the bias on the gate. The gate will trigger the trigger circuit **13** which applies a pulse to the memory **17** and generates an inhibit pulse. Thereafter, the pulse A is inhibited in the succeeding gates.

Then let it be assumed that a pulse B of an amplitude still less than that of pulse A is applied to the input of the apparatus. Since pulse B is of low amplitude, it cannot overcome the bias on the gate on stage **1** and on the gate of stage **2**. However, it can overcome the bias on the gate **11** of stage **3** to cause operation of the trigger circuit of stage **3** and cause the application of a pulse to the memory **17**. After the trigger circuit of the third stage has been triggered, the pulse B cannot operate the succeeding stages because of the generation of an inhibit pulse by the trigger circuit of stage **3** in a manner hereinbefore described.

Now let it be assumed that a pulse C of large amplitude is applied to the apparatus. This pulse has an amplitude which is sufficient to overcome the bias on the gate **11** of the first stage and causes operation of a trigger circuit **13** for the first stage and the application of a pulse to the memory **17**. None of the succeeding gates can be operated because of the generation of an inhibit pulse by the first stage.

Thereafter, a pulse D is applied to the apparatus and since the pulse D is of substantially the same amplitude as pulse A, the gate **11** for stage **2** will again be operated to cause triggering of the trigger circuit **13**, and the application of another pulse to the memory **17**.

After the pulse D, a pulse E of small amplitude is applied to the apparatus which causes the operation of the gate **11** of stage **3** and the associated trigger circuit to cause a pulse to be applied to the memory **17**.

From the foregoing, it can be seen that the apparatus is particularly useful for sorting pulses of various amplitudes. For example, as shown above, pulses of large amplitude will be sorted by the first stage, whereas the pulses of medium amplitude will be sorted by the second stage and pulses of low amplitude will be sorted by the third stage. By varying the bias applied to each of the gates of the stages, it is possible to sort pulses of any amplitude. The pulses can be sorted into any number of groups by merely providing additional stages with a different bias applied to each stage.

This same type of apparatus may also be utilized for sorting pulses of different amplitudes in which the pulses in the train of pulses occur at a repetition rate which is greater than the resolution of any one individual stage. When such is the case, additional stages with the same bias are provided with one following the other, so that any pulse repetition rate can be accommodated by the apparatus. For example, it may be desirable to provide two stages which have the same bias. Thus, for a pulse train of the type shown in III, it may be desirable to

adjust the bias on the gates of the first and second stages so that they equal and so that the bias on the gate of the third stage is equal to the bias on the gate of the succeeding stage, but in which the bias on stage 3 and the succeeding stage is substantially less than the bias on stages 1 and 2. Such apparatus could be utilized for sorting pulses in a pulse train into two different groups. With the pulse train shown in III, the first pulse A would have an amplitude insufficient to overcome the bias on the gates of stages 1 and 2 but sufficient to overcome the bias on the gates of stages 3 and 4. Therefore, pulse A would cause the operation of the trigger circuit of the third stage. An inhibit pulse is generated which inhibits the operation of the succeeding trigger circuits.

The pulse B of the train has an amplitude which is sufficient to overcome the bias on the gate 11 of the first stage and cause triggering of the trigger circuit 13. The succeeding trigger circuit of stage two is not operated because an inhibit pulse is generated in a manner hereinbefore described. The next pulse C causes operation of the trigger circuit 13 of the third stage. However, as shown in train III, two additional pulses D and E of the same amplitude as pulse C follow pulse C in rapid succession. Pulse D arrives at the gate 11 of the stage 3 when the trigger circuit for that stage has not recovered. An inhibit pulse is not generated and, therefore, the next succeeding gate triggers its associated trigger circuit. By the time the pulse E arrives, the trigger circuit for stage 3 has recovered and pulse E is sorted by that stage. It is readily apparent that, if desired, an additional stage having the same bias as the gates of stages 3 and 4 can be provided in the event the spacing between the pulses is so close that the trigger circuits of both 3 and 4 have not recovered when the third pulse of the same amplitude arrives.

It should be pointed out that the inhibit gate 11 of stage 1 the "or" gate 22 immediately following stage 1 and the delay line D3 between the gate 11 of stage 1 and said "or" gate 22 are unnecessary because the gate 11 of the first stage never performs an inhibit function and no pulse travels through D3. These components have merely been included to indicate that all of the stages can be identical if desired to facilitate manufacture.

As pointed out above, the pulse sorting apparatus can readily accommodate pulses of different amplitudes. However, it is desirable that all of the pulses have substantially the same length. Therefore, to simplify the apparatus, it may be desirable to provide a pulse shaping circuit at the input to the apparatus so that all of the pulses applied to the input of the apparatus will have a known length.

It is apparent from the foregoing that I have provided a new and improved pulse sorting apparatus and method which can be utilized for sorting pulses having close double pulse spacing and/or a high repetition rate. The double pulse resolution is not dependent upon the resolution of the trigger circuit or the memory because of the use of a plurality of stages. The repetition rate which can be accommodated by my apparatus can be N times the maximum repetition rate of the trigger circuit where N is equal to the number of stages in the apparatus. The repetition rate is only limited by the double pulse resolution of the apparatus which is primarily limited by the time jitter and minimum triggering pulse width of the trigger circuit. My pulse sorting apparatus and method can be utilized for counting or scaling and for the sorting of pulses in accordance with their amplitude.

It is also readily apparent that in constructing the gates, trigger circuits and the like, that vacuum tubes, transistors or any other type of semiconductors may be utilized.

I claim:

1. In a pulse sorting apparatus, a memory, a single stage connected to the memory for sorting pulses, said stage including a monostable trigger circuit, the speed of sorting by said stage being determined by the characteristics of the stage, the stage being unable to sort another pulse until the trigger circuit has recovered, and at least one additonal stage connected to the memory and having its input serially connected to said first named stage to receive the pulses after they are received by the first named stage and for sorting all of the input pulses which are not sorted by the first stage, each additional stage including a gate and a monostable trigger circuit connected to the gate, the number of stages required being dependent on the rate and distribution of the input pulses relative to the resolution characteristics of the stages.

2. Apparatus as in claim 1 wherein said gates of each additional stage are inhibit gates and wherein said trigger circuits generate inhibit pulses substantially equal in length to the input pulses which are applied to the gates of succeeding stages to prevent an input pulse sorted by one stage from being sorted by another stage.

3. Apparatus as in claim 1 wherein delay lines are utilized for connecting the stages.

4. In a pulse sorting apparatus, an input terminal, a memory, a plurality of stages, means connecting the input terminal to the first stage each of said stages comprising an inhibit gate, a trigger circuit connected to said inhibit gate, means connecting the trigger circuit to the memory, circuit means serially connecting said inhibit gates of said stages, and additional circuit means connecting the trigger circuit of each stage to the circuit means connecting the gate of the corresponding stage to the gate of the succeeding stage, the trigger circuit of a stage upon receiving an input pulse generating an inhibit pulse having a length substantially equal to the length of the input pulse, the inhibit pulse being applied to the gates of succeeding stages to prevent the operation of the trigger circuits of the succeeding stages by the input pulse when the same input pulse has caused the operation of a preceding stage.

5. Pulse sorting apparatus as in claim 4 wherein the gates of each of the stages are provided with equal bias to provide substantially uniform triggering levels for the stages.

6. Pulse sorting apparatus as in claim 4 wherein certain of the gates are provided with different biases to provide different triggering levels for the corresponding stages.

7. Pulse sorting apparatus as in claim 4 wherein the bias on the gate of a preceding stage is greater than the bias on the gate of a succeeding stage to provide an incrementally decreasing triggering level for the stages.

8. Apparatus as in claim 4 wherein the bias on the gates of a preceding group of stages is greater than the bias on the gates of a succeeding group of stages to provide an incrementally decreasing triggering level for the groups of stages.

9. Pulse sorting apparatus as in claim 4 wherein the circuit means connecting the gate of a succeeding stage to the gate of a preceding stage includes at least one delay line.

10. In a pulse sorting apparatus, an input terminal, a memory, a plurality of stages, the first stage including a trigger circuit connected to the memory, each of the other stages comprising an inhibit gate, a trigger circuit connected to the inhibit gate, and means connecting the trigger circuit to the memory, circuit means connecting the input terminal to the trigger circuit of the first stage and to the inhibit gate of the stage following the first stage, circuit means serially connecting the inhibit gates of said other stages, circuit means connecting the trigger circuit of the first stage to the inhibit gate of the stage following the first stage, and additional circuit means connecting the trigger circuit of each of said other stages to the circuit means connecting the inhibit gate of the corresponding stage to the inhibit gate of the succeeding stage, the trigger circuit of a stage serving to generate an inhibit pulse of substantially the same length as the input pulse to inhibit the succeeding gates when an input pulse has operated the trigger circuit.

11. In a pulse sorting apparatus, a memory, an input,

a plurality of serially connected stages, the first stage including a trigger circuit connected to said memory, each of the other stages comprising an inhibit gate, a trigger circuit connected to the inhibit gate and means connecting the trigger circuit to the memory, first circuit means for said other stages including a delay line connecting the inhibit gate of each stage to the inhibit gate of the succeeding stage, second circuit means for said other stages including a pair of delay lines and a pulse directing device connected between the pair of delay lines, said second circuit means connecting the inhibit gate of each stage to the inhibit gate of the succeeding stage, third circuit means including a delay line connecting the trigger circuit of the first stage to the gate of the second stage, fourth circuit means connecting the input to the trigger circuit of the first stage and to the inhibit gate of the stage following the first stage, said fourth circuit means including a delay line connected to the inhibit gate of the stage following the first stage and means connecting the trigger circuit of each of said other stages to the pulse directing device which directs the pulses to the inhibit gate of the succeeding stage.

12. Apparatus as in claim **11** wherein the time delay provided by the delay line in the first circuit means is substantially equal to the sum of the time delays provided by the pair of delay lines in the second circuit means.

13. Pulse sorting apparatus as in claim **12** wherein the time delay provided by one of the delay lines in the second circuit means is substantially equal to the time delay in the trigger circuit of the preceding stage and wherein the time delay provided by the other of the delay lines in the second circuit means is equal to a predetermined value.

14. In a method for sorting pulses, sorting input pulses at a rate not exceeding a predetermined rate in one stage, sorting input pulses occurring at a rate greater than the predetermined rate in succeeding stages, and generating an inhibit pulse of a length substantially equal in length to the input pulse to prevent an input pulse sorted by one stage from being sorted by succeeding stages.

15. In a method for sorting pulses, sorting pulses in one stage, the maximum rate of sorting being determined by the characteristics of the stage, sorting pulses not sorted by such one stage with additional stages, and generating inhibit pulses substantially coincident with the input pulses to prevent a pulse sorted by one stage from being sorted by succeeding stages.

16. In a method for sorting a plurality of input pulses by utilizing a plurality of serially connected stages adapted to accept pulses, causing each input pulse to be applied to each stage sequentially in time, generating an inhibit pulse in each stage which accepts an input pulse and applying the inhibit pulse to each succeeding stage in substantial coincidence with the input pulse so that the input pulse is canceled to thereby prevent registration of the same input pulse in a succeeding stage.

17. In a method for sorting and registering a plurality of input pulses utilizing a plurality of serially connected stages adapted to accept pulses, causing each input pulse to be applied to each stage sequentially in time so that each stage has time to accept or ignore an input pulse before the input pulse is applied to the succeeding stage, sorting and registering input pulses in each stage up to a rate determined by the resolution characteristics of the stage, generating an inhibit pulse in each stage which accepts an input pulse, and applying the inhibit pulse to the succeeding stages in substantial coincidence with the input pulse so that the input pulse is canceled in the succeeding stages to thereby prevent registration of the same input pulse in the succeeding stages.

18. In a method for sorting pulses in a plurality of serially connected stages adapted to accept pulses, applying all of the received input pulses to all operative and inoperative stages so that each pulse is applied to each stage sequentially in time, accepting any given input pulse in the first operative stage encountered by the input pulse and generating an inhibit pulse in each stage accepting a pulse and applying the same to the succeeding stages to prevent the succeeding stages from accepting the same input pulse.

19. In a method for sorting pulses with a plurality of serially connected stages adapted to register pulses, applying each input pulse to each of the stages sequentially in time, generating an inhibit pulse in each stage registering an input pulse, applying the inhibit pulse to the stages succeeding the stage accepting the pulse so that the inhibit pulse is substantially coincident in time, and travels in substantial coincidence with the registered input pulse to prevent succeeding stages from registering the same pulse.

20. A method as in claim **19** wherein every pulse is registered by the first stage of the serially connected stages unless the first stage is incapable of registering a pulse.

21. In a pulse sorting apparatus for sorting a plurality of input pulses, a plurality of stages where n represents the total number of stages, each of the stages being receptive to an input pulse before the first input pulse is received, at least $n-1$ stages being receptive before the second input pulse is received, at least $n-2$ stages being receptive before the third input pulse is received, etc., means connecting the stages serially so that each input pulse is applied to each stage in a time sequence so that each stage has time to accept or ignore an input pulse before the succeeding stage has received the same input pulse, each stage having means for accepting a pulse and means for generating a time coincident inhibit pulse each time the stage accepts the pulse, means for applying the inhibit pulse to the succeeding stages so that the inhibit pulses accompany the input pulses through the succeeding states to cancel the input pulses to thereby prevent the acceptance of an input pulse by a succeeding stage after it has been accepted by a preceding stage.

22. A pulse sorting apparatus as in claim **21** wherein each stage includes an inhibit gate and in which the input pulses and the inhibit pulses are applied to the inhibit gates.

23. In a pulse sorting apparatus, a plurality of stages capable of sorting and storing pulses, each of the stages having a trigger circuit for accepting pulses and an inhibit gate, means serially connecting the stages to apply the input pulses to the inhibit gate of each stage in a time sequence, the operating sequence of the stages being determined by the rate and distribution of the input pulses relative to the resolution characteristics of the stages, the operating sequence being random when the input pulse distribution is random, the trigger circuit of each stage including means for generating an inhibit pulse when it accepts an input pulse and means for applying the inhibit pulse to the inhibit gates of the succeeding stages to cancel the input pulse which has been accepted by a preceding stage to thereby inhibit the inhibit gates to prevent the succeeding stages from accepting the same input pulse, the inhibit gates of the stages being arranged so that all the trigger circuits are normally ready to accept input pulses.

24. In a pulse sorting apparatus, a plurality of stages, means connecting the first stage to said input circuit, each of the stages comprising an inhibit gate, a trigger circuit connected to the gate and a memory connected to the trigger circuit, circuit means serially connecting the stages including a delay line connecting the inhibit gate of each stage to the inhibit gate of the succeeding stage, additional circuit means serially connecting the inhibit gates of said stages, said additional circuit means including a pair of delay lines and a pulse directing device connected between the pair of delay lines and circuit means connecting the trigger circuit of each stage to the pulse directing device which directs the pulse to the inhibit gate of the succeeding stage.

25. In a method of sorting pulses with a plurality of serially connected stages, applying each input pulse to each stage sequentially in time and generating an inhibit pulse to prevent an input pulse sorted by one stage from being sorted by another stage.

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U.S. Cl. X.R.

307—208, 220, 233, 238; 328—105, 108, 138, 153

U.S. DEPARTMENT OF COMMERCE

PATENT OFFICE

Washington, D.C. 20231

UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3,437,940 April 8, 196

Zoltan Tarczy-Hornoch

It is certified that error appears in the above identified patent and that said Letters Patent are hereby corrected as shown below:

In the heading to the printed specification, line 5, "Zelta Research" should read -- Zeta Research --.

Signed and sealed this 7th day of April 1970.

(SEAL)
Attest:

Edward M. Fletcher, Jr.
Attesting Officer

WILLIAM E. SCHUYLER, J
Commissioner of Paten