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[Continued on next page]

(54) Title: APPARATUS AND METHOD FOR STORAGE DEVICE READING

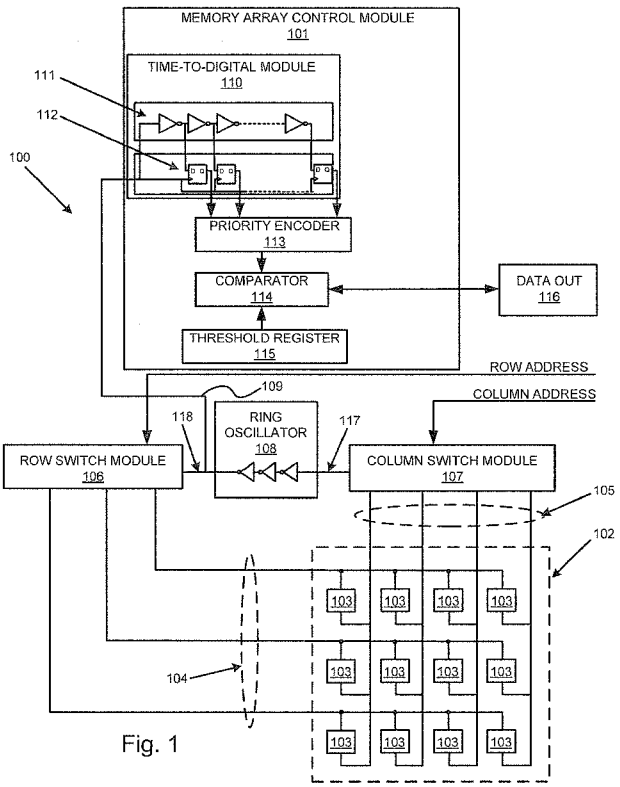

Fig. 1

(57) Abstract: According to an example, a method for storage device reading may include receiving an input signal indicative of a period of oscillation of a ring oscillator coupled to a storage device of a plurality of storage devices, and measuring the period of oscillation of the ring oscillator by a time-to-digital circuit. The method for storage device reading may further include determining a value of data stored in the storage device based on the measurement.

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— *as to the identity of the inventor (Rule 4.17(i))*

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— *with international search report (Art. 21(3))*

APPARATUS AND METHOD FOR STORAGE DEVICE READING

BACKGROUND

[0001] In a storage device, such as a memristor, when current flows in one direction through the storage device, the electrical resistance increases, and when current flows in an opposite direction, the electrical resistance decreases. When the current is stopped, the last resistance in the memristor is retained. Further, when the flow of charge begins again, the resistance of the memristor reverts to a value when the memristor was last active. Such storage devices can be formed in an array configuration that includes a plurality of storage devices disposed, for example, in a row and column format. Each of the storage devices in the array can be individually addressed to read or write to the storage device. For example, a row and column can be individually addressed to read or write to a corresponding storage device.

BRIEF DESCRIPTION OF DRAWINGS

[0002] Features of the present disclosure are illustrated by way of example and not limited in the following figure(s), in which like numerals indicate like elements, in which:

[0003] Figure 1 illustrates an architecture of a storage device reading apparatus, according to an example of the present disclosure;

[0004] Figure 2 illustrates a method for storage device reading, according to an example of the present disclosure; and

[0005] Figure 3 illustrates a computer system, according to an example of the present disclosure.

DETAILED DESCRIPTION

[0006] For simplicity and illustrative purposes, the present disclosure is described by referring mainly to examples. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present disclosure. It will be readily apparent however, that the present disclosure may be practiced without limitation to these specific details. In other instances, some methods and structures have not been described in detail so as not to unnecessarily obscure the present disclosure.

[0007] Throughout the present disclosure, the terms "a" and "an" are intended to denote at least one of a particular element. As used herein, the term "includes" means includes but not limited to, the term "including" means including but not limited to. The term "based on" means based at least in part on.

[0008] A ring oscillator may be connected between a row and column of a storage device, such as a memristor array, to read a bit stored in a memristor addressed by the row and column. The ring oscillator exhibits a characteristic period of oscillation that can be used to determine a value of the bit in the memristor addressed by the row and column. One technique for measuring the period of oscillation may include using an output of the ring oscillator to clock a counter for sufficient cycles to discriminate between frequencies that may be 10% or less different. This technique can take a relatively long time to determine the period of oscillation based, for example, on the number of cycles it can take to discriminate between different frequencies. Another technique for measuring the period of oscillation may include using a counter clocked by a fixed clock that is of a significantly higher frequency than the ring oscillator. Such a counter can be started on an edge of the ring oscillator output, and stopped at a fixed number of edges later. However, such a counter can add complexities and additional power consumption needs to the overall read/write process.

[0009] A storage device reading apparatus and a method for storage device reading are disclosed herein, and provide for measurement of the period of

oscillation of a ring oscillator with minimal latency. According to an example, the storage device reading apparatus may include a time-to-digital circuit (i.e., of a time-to-digital module) that is used to measure the period of oscillation of a ring oscillator. The measured period of oscillation may be used to determine a value of a bit in a memristor addressed by a row and column in a memory array, such as a memristor array. The time-to-digital circuit may include a series of buffers and a register (for example, a set of latches or flip-flops). The ring oscillator output may be fed to the series of buffers and to a clock input of the register. The length of the series of buffers may be chosen such that the fastest possible propagation delay time of the series of buffers is at least one-half of the longest period that the time-to-digital circuit is designed to measure. A priority encoder circuit may be applied to the register output, and the resulting binary value may represent a measurement of the ring oscillator period. The use of the time-to-digital circuit minimizes any latency in measurement of the period of oscillation of a ring oscillator.

[0010] According to an example, the method for storage device reading may include receiving an input signal which is the output of a ring oscillator coupled to a storage device of a plurality of storage devices, and measuring the period of oscillation of the ring oscillator by a time-to-digital circuit.

[0011] Figure 1 illustrates an architecture of a storage device reading apparatus 100, according to an example. Referring to Figure 1, the apparatus 100 is depicted as including a memory array control module 101 to control a memory array 102 and various other operations of the apparatus 100. The memory array 102 may include a plurality of data storage devices 103, such as memristors. Each of the data storage devices 103 may be individually addressable by row address lines 104 and column address lines 105. A row switch module 106 may couple various aspects of the apparatus 100 to selected ones of the storage devices 103 by the row address lines 104. Similarly, a column switch module 107 may couple various aspects of the apparatus 100 to selected ones of the storage devices 103 by the column address lines 105. A ring oscillator 108 has a characteristic period of oscillation that can be used to determine a value of a bit in the particular storage

device 103 addressed by the row address lines 104 and the column address lines 105. An output 109 of the ring oscillator 108 may be fed to a time-to-digital module 110 that includes a time-to-digital circuit. For example, the output 109 of the ring oscillator 108 may be fed to a series of buffers 111 of the time-to-digital module 110. The output of each of the buffers 111 may be fed to a corresponding flip-flop of a series of flip-flops 112. The flip-flops 112 may be clocked with the oscillating signal of the ring oscillator 108, which is included in the output 109. A priority encoder 113 may determine a binary value corresponding to the period of the ring oscillator 108. The binary value corresponding to the period of oscillation of the ring oscillator 108 may be compared using a comparator 114 to a value stored in a threshold register 115. The output of the comparison by the comparator 114 may be output at 116.

[0012] The apparatus 100 and the various components thereof may be implemented in hardware using a variety of digital logic circuits, such as system-on-chips (SoC), application-specific integrated circuits (ASIC), etc. Additionally or alternatively, the apparatus 100 and the various components thereof that perform various other functions in the apparatus 100, may comprise machine readable instructions stored on a non-transitory computer readable medium. In addition, or alternatively, the apparatus 100 and the various components thereof may comprise hardware or a combination of machine readable instructions and hardware.

[0013] The memory array control module 101 may control the memory array 102 and various other operations of the apparatus 100. For example, the memory array control module 101 may store data values within the memory array 102, read data values from the memory array 102, control operations of the row switch module 106 and the column switch module 107, receive data values from and provide data values to a source of the apparatus 100, etc. The memory array control module 101 may store (i.e., write or program) data values to the data storage devices 103, for example, by direct-current (DC) pulses formatted to increase or decrease the non-volatile electrical resistance of the selected data storage device 103. The memory array control module 101 may also retrieve (i.e.,

read) data values stored in the data storage devices 103 by the ring oscillator 108.

[0014] The data storage devices 103 may store at least two distinct data values based on electrical characteristics thereof. For example, the data storage devices 103 may include electrical characteristics such as resistance, capacitance, inductance, or a combination thereof. Each data storage device 103 may store one bit of binary data-value (e.g., 0 or 1) based on a non-volatile adjustment in electrical resistance thereof. The data storage devices 103 may also store other types of data-values (e.g., base-three, base-eight, etc.). The memory array 102 may include a plurality of the data storage devices 103, such as memristors. In the example of Figure 1, the memory array 102 is illustrated as including twelve data storage devices 103. However, those skilled in the art would appreciate in view of this disclosure that the memory array 102 may include any number of the data storage devices 103. Each of the data storage devices 103 may be individually addressable by one of the row address lines 104 and the column address lines 105 to write to or read stored data values.

[0015] The row switch module 106 may couple various aspects of the apparatus 100 to selected ones of the storage devices 103 by the row address lines 104. Similarly, the column switch module 107 may couple various aspects of the apparatus 100 to selected ones of the storage devices 103 by the column address lines 105. The row and column switch modules 106 and 107, respectively, may include, field-effect transistors (FETs), pass FETs, pass gates, diodes, bipolar transistors, electromechanical switches, or other devices.

[0016] The ring oscillator 108 exhibits a characteristic period of oscillation that can be used to determine a value of a bit stored in the particular storage device 103 addressed by the row address lines 104 and the column address lines 105. The ring oscillator 108 may be defined by or include an odd-number of logical inverter gates coupled in a series-circuit arrangement. The ring oscillator 108 may include an input node 117 and an output node 118. The ring oscillator 108 may also include the output 109 that is fed at the output node 118 to the time-to-digital module 110 that includes the time-to-digital circuit. The ring oscillator 108 may be

coupled to selected ones of the storage devices 103 by the row and column switch modules 106 and 107, respectively. A particular storage device 103 may define part of a feedback pathway or loop when coupled to the ring oscillator 108 by the input node 117, the output node 118, the row switch module 106 and the column switch module 107. A selected storage device 103 may be disposed in a series arrangement in a feedback loop with respect to the ring oscillator 108. The feedback loop may be formed upon coupling of the selected storage device 103 with the ring oscillator 108 by the row switch module 106 and the column switch module 107. For example, the ring oscillator 108 may be selectively coupled to the storage devices 103 by the by the row address lines 104 and the column address lines 105 so as to establish a feedback loop.

[0017] The ring oscillator 108 may include a period of oscillation that can be used to determine a value of a bit stored in the particular storage device 103 addressed by the row address lines 104 and the column address lines 105. Generally, the period of the oscillation of the ring oscillator 108 may be measured to determine whether the storage device 103 addressed by the row address lines 104 and the column address lines 105 is in a high or a low resistance state. For example, the ring oscillator 108 may include a period of oscillation corresponding to a data value (e.g., a bit) stored in one of the storage devices 103 coupled thereto.

[0018] The output 109 of the ring oscillator 108 may be fed to the series of buffers 111 of the time-to-digital module 110. The output of each buffer of the series of buffers 111 may be fed to a corresponding flip-flop of the series of flip-flops112. Each of the flip-flops 112 may be clocked with an un-buffered oscillating signal of the output 109 of the ring oscillator 108. Each buffer of the series of buffers 111 may include a propagation delay. For example, if the set of outputs of the buffers 111 is viewed as a parallel bus and the parallel bus is clocked on a rising edge of output 109, the first flip-flop of the series of flip-flops112 records the value prior to the rising edge, that is, a zero. As further buffers 111 and corresponding flip-flops 112 are considered, at a given point, the total delay of the buffers 111 exceeds one-half of the period of the output 109. That flip-flop of the

series of flip-flops112, and flip-flops 112 further down the series see a value that was present prior to the previous falling edge of the output 109, that is, a one. The location of the transition of the input signal to the series of buffers 111 from 1 to 0, or from 0 to 1, may correspond to the measurement of the period of oscillation of the ring oscillator 108.

[0019] As discussed herein, the flip-flops 112 may be clocked with the un-buffered oscillating signal of the output 109 of the ring oscillator 108. According to an example, each of the flip-flops 112 may be a positively edged triggered flip-flop (e.g., 20 bits wide). At an instance that a positive edge on the flip-flop clock occurs, the result of the transition from 0 to 1 of the ring oscillator 108 will not have been observed by any of the buffers in the series of buffers 111. At this stage, a first bit of a flip-flop will record a 0. All flip-flop bits thereafter will also record 0's until the ring oscillator 108 output signal (i.e., output 109) has been sufficiently delayed to see a previous 1 to 0 transition. At this point, the flip-flops 112 will see 1's instead of 0's. Moreover, shorter periods of the ring oscillator 108 will result in that transition being seen earlier (that is, more leftward) as a parallel output of the flip-flop bits.

[0020] The length of the series of the buffers 111 may be chosen such that the fastest possible propagation delay time of the series of the buffers 111 is at least one-half of the longest period that the time-to-digital module 110 is designed to measure. For example, if the length of the series of the buffers 111 is too short (e.g., less than ½ of the longest possible period of oscillation of the ring oscillator 108), then for the longest period of oscillation of the ring oscillator 108, the most delayed signal at the far end of the series of the buffers 111 would still result in a value of 0. Thus, a length of the series of the buffers 111 (i.e., the number of buffers needed) may be determined by dividing the longest possible period of oscillation of the ring oscillator 108 by 2, and dividing the result by the propagation delay of each buffer of the series of buffers 111.

[0021] The priority encoder 113 may include a find-first-one circuit (or a find-first-zero circuit) to determine a binary value corresponding to the period of

oscillation of the ring oscillator 108. The priority encoder 113 may receive a series of 1's followed by 0's, or vice versa, from the flip-flops 112, and encode the received series into a binary value. The priority encoder 113 may include a set of parallel inputs form the flip-flops 112 and generate a binary encoded output. According to an example, if the priority encoder 113 includes 20 bits of input and 5 bits of output, if the last bit in the flip-flops 112 (that is, the rightmost bit) is a 1 and the remaining bits are 0, then the output of the priority encoder 113 is a binary 1 (i.e., 00001). According to another example, if the priority encoder 113 includes 20 bits of input and 5 bits of output, if the second bit (that is, second from left most bit) in the flip-flops 112 is a 1, then the output of the priority encoder 113 is a binary 19 (i.e., 10011). Therefore, for the priority encoder 113, an output corresponding to a low number may correspond to a low frequency of the ring oscillator 108 (e.g., a first value of a bit stored in a storage device 103), and an output corresponding to a high number may correspond to a high frequency ring oscillator 108 (e.g., a second value of a bit stored in the storage device 103).

[0022] A threshold may be set such that a lower number on the output of the priority encoder 113 causes the comparator 114 to drive a logic zero, and a higher number then the threshold causes the comparator 114 to drive a logic one, or vice-versa. For example, if a storage device 103 stores a 1 or 0, the threshold may be set in a middle of the possible range of outputs of the priority encoder 113.

[0023] Figure 2 illustrates a flowchart of method 200 for storage device reading, corresponding to the example of the storage device reading apparatus 100 whose construction is described in detail above. The method 200 may be implemented on the storage device reading apparatus 100 with reference to Figure 1 by way of example and not limitation. The method 200 may be practiced in other apparatus.

[0024] Referring to Figure 2, for the method 200, at block 201, an input signal indicative of a period of oscillation of a ring oscillator coupled to a storage device of a plurality of storage devices may be received. For example, referring to Figure 1, the time-to-digital module 110 of the memory array control module 101 may receive an input signal (i.e., the output 109 of the ring oscillator 108) exhibiting a

characteristic period of oscillation of the ring oscillator 108 coupled to a storage device 103 of a plurality of storage devices (i.e., the memory array 102).

[0025] At block 202, the period of oscillation of the ring oscillator may be measured by a time-to-digital circuit. For example, referring to Figure 1, the period of oscillation of the ring oscillator 108 may be measured by the time-to-digital circuit (e.g., the time-to-digital module 110 that includes a time-to-digital circuit).

[0026] At block 203, a value of data stored in the storage device may be determined based on the measurement. For example, referring to Figure 1, a value of data stored in the storage device 103 may be determined based on the measurement.

[0027] Figure 3 shows a computer system 300 that may be used with the embodiments described herein. The computer system 300 may represent a generic platform that may include components that may be in a server or another computer system. The computer system 300 may be used as a platform for the apparatus 100. The computer system 300 may execute, by a processor or other hardware processing circuit, the methods, functions and other processes described herein. These methods, functions and other processes may be embodied as machine readable instructions stored on computer readable medium, which may be non-transitory, such as, for example, hardware storage devices (e.g., RAM (random access memory), ROM (read only memory), EPROM (erasable, programmable ROM), EEPROM (electrically erasable, programmable ROM), hard drives, and flash memory).

[0028] The computer system 300 may include a processor 302 that may implement or execute machine readable instructions performing some or all of the methods, functions and other processes described herein. Commands and data from the processor 302 may be communicated over a communication bus 304. The computer system 300 may also include a main memory 306, such as, for example, a random access memory (RAM), where the machine readable instructions and data for the processor 302 may reside during runtime, and a secondary data storage 308, which may be non-volatile and stores machine

readable instructions and data. The memory and data storage may be examples of computer readable mediums. The memory 306 may include a storage device reading module 320 including machine readable instructions residing in the memory 306 during runtime and executed by the processor 302. The storage device reading module 320 may include the modules of the apparatus 100 shown in Figure 1.

[0029] The computer system 300 may include an I/O device 310, such as, for example, a keyboard, a mouse, a display, etc. The computer system 300 may include a network interface 312 for connecting to a network. Other known electronic components may be added or substituted in the computer system 300.

[0030] While the embodiments have been described with reference to examples, various modifications to the described embodiments may be made without departing from the scope of the claimed embodiments.

What is claimed is:

1. A method for storage device reading, the method comprising:

receiving an input signal indicative of a period of oscillation of a ring oscillator coupled to a storage device of a plurality of storage devices;

measuring the period of oscillation of the ring oscillator by a time-to-digital circuit; and

determining a value of data stored in the storage device based on the measurement.

2. The method of claim 1, wherein the storage device is a memristor.

3. The method of claim 1, whereinthe plurality of storage devices represent a memristor array.

4. The method of claim 1, wherein measuring the period of oscillation of the ring oscillator by the time-to-digital circuit further comprises:

feeding the input signal to a series of buffers of the time-to-digital circuit; and

feeding the input signal to a clock input of a flip-flop associated with each buffer of the series of buffers.

5. The method of claim 1, further comprising:

determining a length of a series of buffers of the time-to-digital circuit such that a fastest possible propagation delay time of the series of buffers is at least one-half of a longest period of oscillation of the ring oscillator.

6. The method of claim 1, wherein determining the value of data stored in the storage device based on the measurement further comprises:

using a find-first-one circuit for an output of a series of flip-flops of the time-to-digital circuit to determine the value of data stored in the storage device.

7. The method of claim 1, wherein determining the value of data stored in the storage device based on the measurement further comprises:

using a find-first-zero circuit for an output of a series of flip-flops of the time-to-digital circuit to determine the value of data stored in the storage device.

8. The method of claim 1, wherein determining the value of data stored in the storage device based on the measurement further comprises:

using a priority encoder for an output of a series of flip-flops of the time-to-digital circuit to generate a binary value corresponding to the period of oscillation of the ring oscillator.

9. The method of claim 1, wherein determining the value of data stored in the storage device based on the measurement further comprises:

determining the value of a bit stored in the storage device.

10. A storage device reading apparatus comprising:

a time-to-digital circuit to receive an input signal indicative of a period of oscillation of a ring oscillator coupled to a storage device of a plurality of storage devices, and to measure the period of oscillation of the ring oscillator; and

a priority encoder to determine a value of data stored in the storage device based on the measurement for an output of a series of flip-flops of the time-to-digital circuit to generate a binary value corresponding to the period of oscillation of the ring oscillator.

11. The storage device reading apparatus of claim 10, wherein the storage device is a memristor.

12. The storage device reading apparatus of claim 10, wherein the plurality of storage devices represent a memristor array.

13. The storage device reading apparatus of claim 10, wherein a length of a series of buffers of the time-to-digital circuit is determined such that a fastest possible propagation delay time of the series of buffers is at least one-half of a longest period of oscillation of the ring oscillator.

14. The storage device reading apparatus of claim 10, wherein the data is a bit stored in the storage device.

15. A non-transitory computer readable medium having stored thereon machine readable instructions for storage device reading, the machine readable instructions when executed cause a computer system to:

receive an input signal indicative of a period of oscillation of a ring oscillator coupled to a storage device of a plurality of storage devices;

measure the period of oscillation of the ring oscillator by a time-to-digital circuit by feeding the input signal to a series of buffers of the time-to-digital circuit, and feeding the input signal to a clock input of a flip-flop associated with each buffer of the series of buffers; and

determine, by a processor, a value of data stored in the storage device based on the measurement.

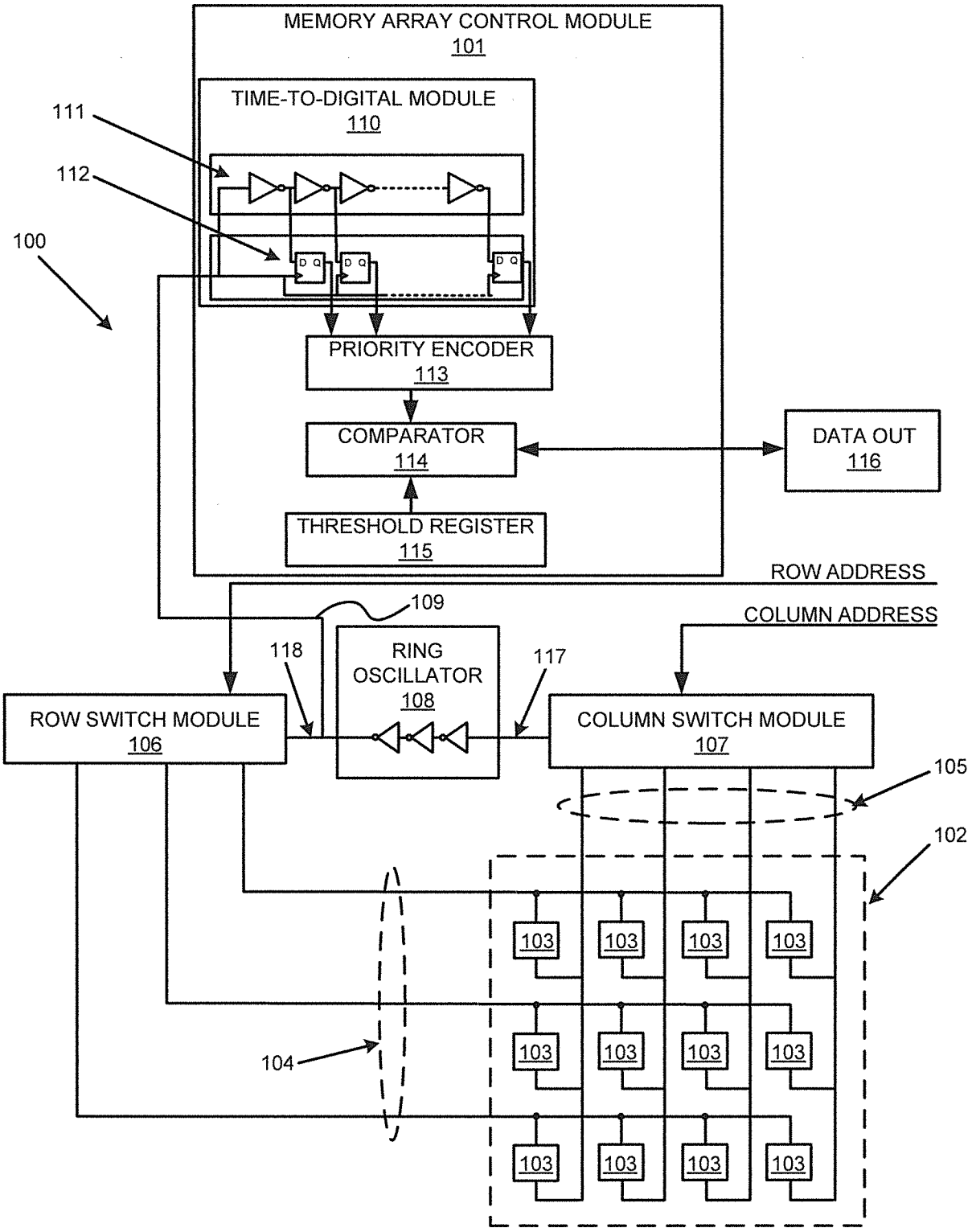
MEMORY ARRAY CONTROL MODULE
101
TIME-TO-DIGITAL MODULE
110
111
112
100
PRIORITY ENCODER
113
COMPARATOR
114
DATA OUT
116
THRESHOLD REGISTER
115
ROW ADDRESS
COLUMN ADDRESS
109
118
RING
OSCILLATOR
108
117
ROW SWITCH MODULE
106
COLUMN SWITCH MODULE
107
105
102
103
104

Fig. 1

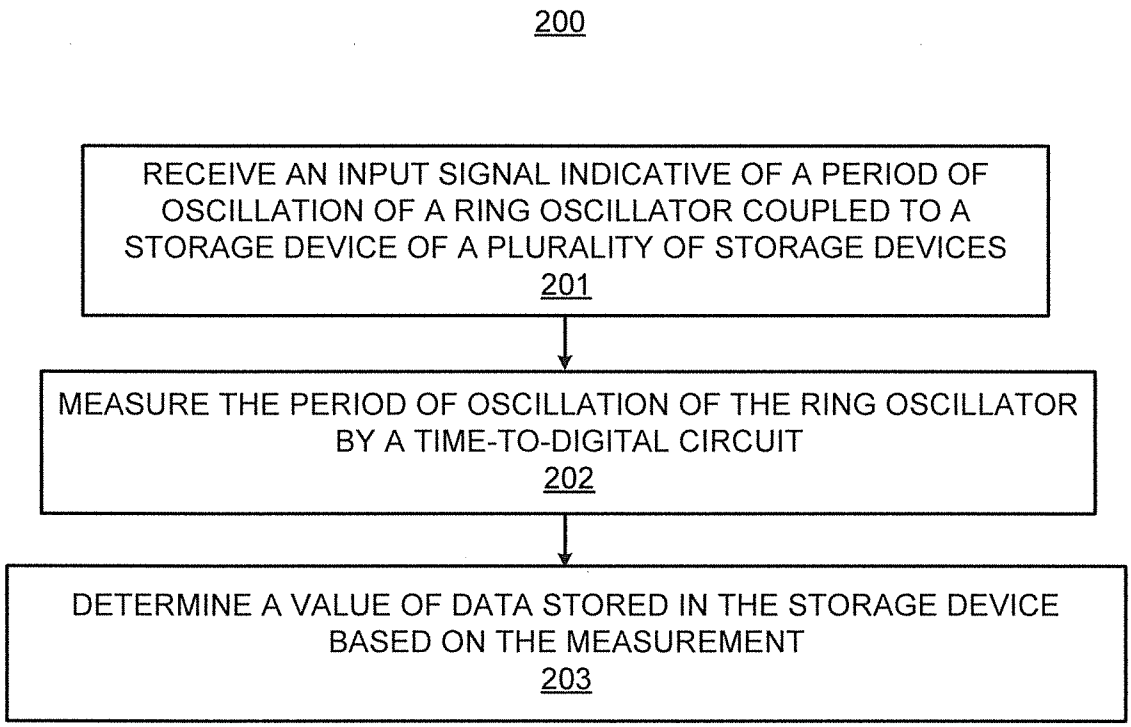
200
RECEIVE AN INPUT SIGNAL INDICATIVE OF A PERIOD OF OSCILLATION OF A RING OSCILLATOR COUPLED TO A STORAGE DEVICE OF A PLURALITY OF STORAGE DEVICES
201
MEASURE THE PERIOD OF OSCILLATION OF THE RING OSCILLATOR BY A TIME-TO-DIGITAL CIRCUIT
202
DETERMINE A VALUE OF DATA STORED IN THE STORAGE DEVICE BASED ON THE MEASUREMENT
203

Fig. 2

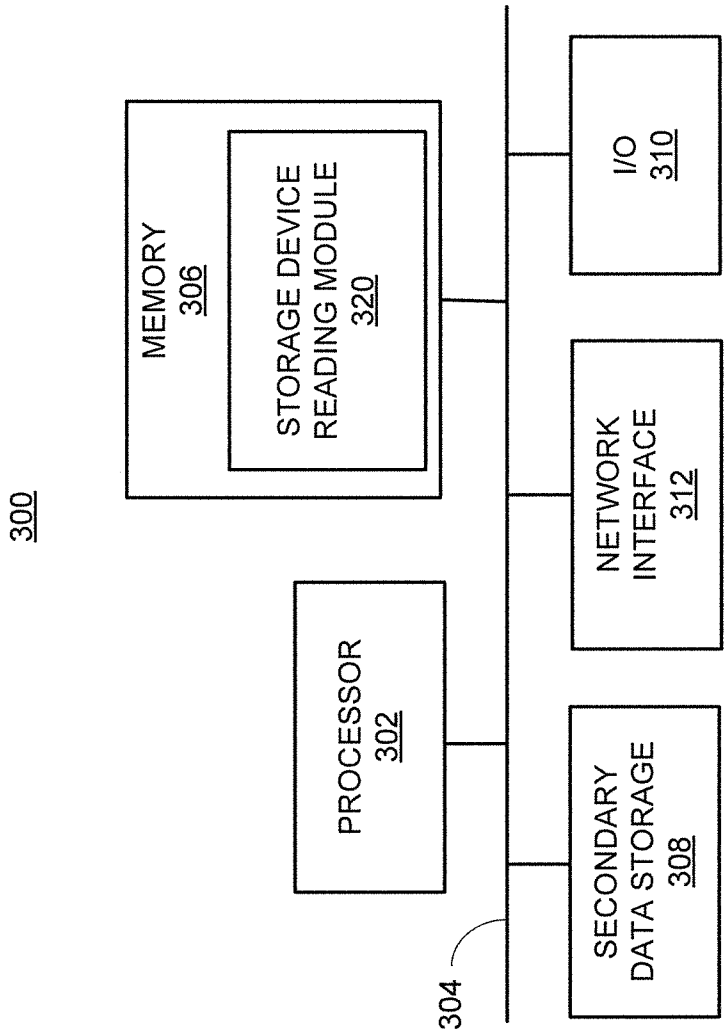
300
MEMORY
306
STORAGE DEVICE
READING MODULE
320
PROCESSOR
302
304
SECONDARY
DATA STORAGE
308
NETWORK
INTERFACE
312
I/O
310

Fig. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/034409

A. CLASSIFICATION OF SUBJECT MATTER

G11C 7/10(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C 7/10; G11C 8/16; G01R 33/00; H01L 29/41; G11C 8/04; H01L 23/48; H01L 21/02; H03K 17/30; G11C 11/18; G11C 11/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: memristor, ring, oscillator, measure, period

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2012-060807 A1 (HEWLETT-PACKARD DEVELOPMENT COMPANY L.P.) 10 May 2012 See paragraphs [0015]-[0048]; claim 14; and figure 1.	1-3,9
A		4-8,10-15
A	US 2012-0195099 A1 (FENG MIAO et al.) 02 August 2012 See paragraphs [0041]-[0045]; and figure 4.	1-15
A	US 2012-0273955 A1 (ZVI OR-BACH et al.) 01 November 2012 See paragraph [0275]; and figure 17B.	1-15
A	WO 2012-067660 A1 (HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.) 24 May 2012 See paragraphs [0028]-[0032]; and figures 7, 8.	1-15
A	EP 2503556 A1 (TECHNISCHE UNIVERSITAT DRESDEN) 26 September 2012 See paragraphs [0035]-[0047]; and figure 1.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 December 2013 (26.12.2013)	**27 December 2013 (27.12.2013)**

Name and mailing address of the ISA/KR
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea
Facsimile No. +82-42-472-7140

Authorized officer
YANG, Jeong Rok
Telephone No. +82-42-481-5709

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/034409

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