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# (54) SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

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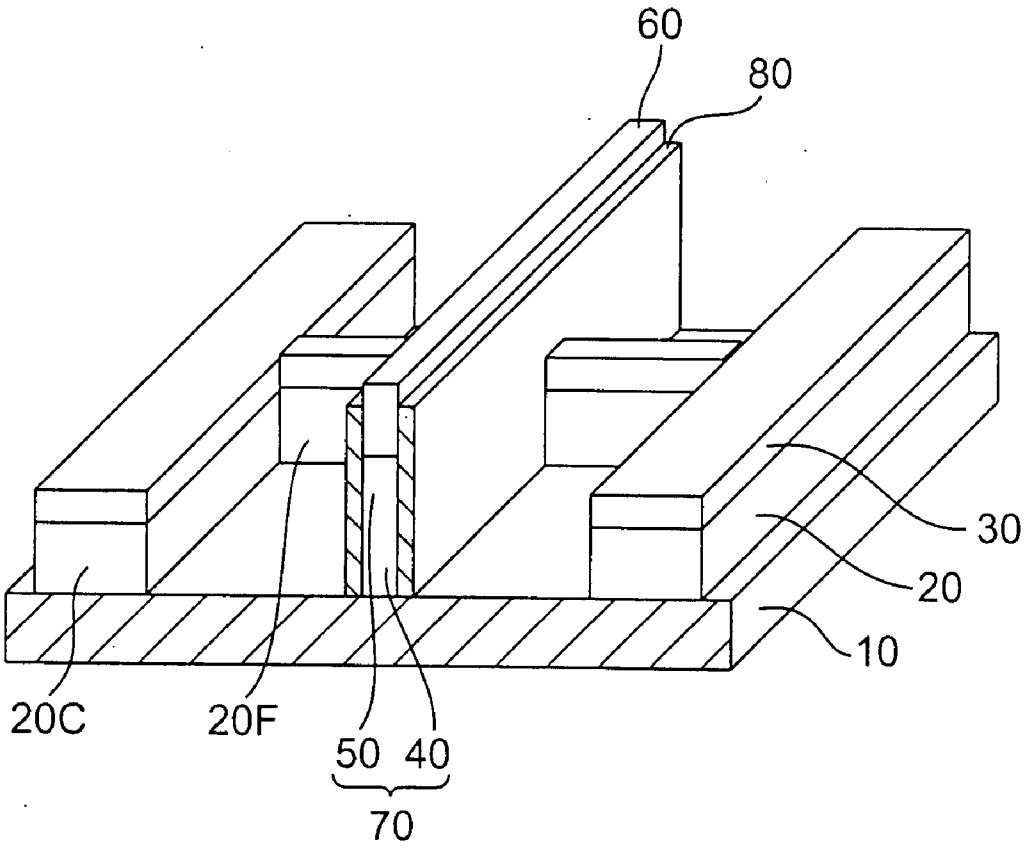
(52) **U.S. Cl.** ..... **257/401**

(57) **ABSTRACT**

There is provided a semiconductor device including: convex semiconductor layers formed on a semiconductor substrate via an insulating film; gate electrodes formed on a pair of facing sides of the semiconductor layers via a gate insulating film; a channel region formed of silicon between the gate electrodes in the semiconductor layers; a source extension region and a drain extension region formed of silicon germanium or silicon carbon on both sides of the channel region in the semiconductor layers; and a source region formed of silicon so as to adjoin to the opposite side of the channel region in the source extension region, and a drain region formed of silicon so as to adjoin to the opposite side of the channel region in the drain extension region in the semiconductor layers.



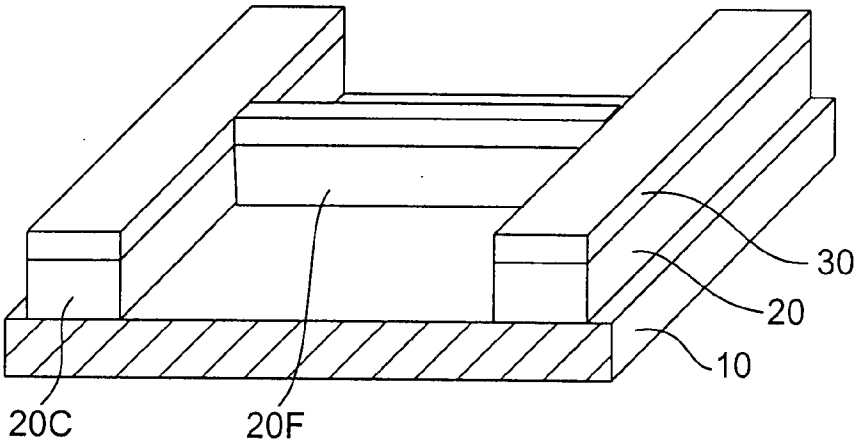



FIG. 1

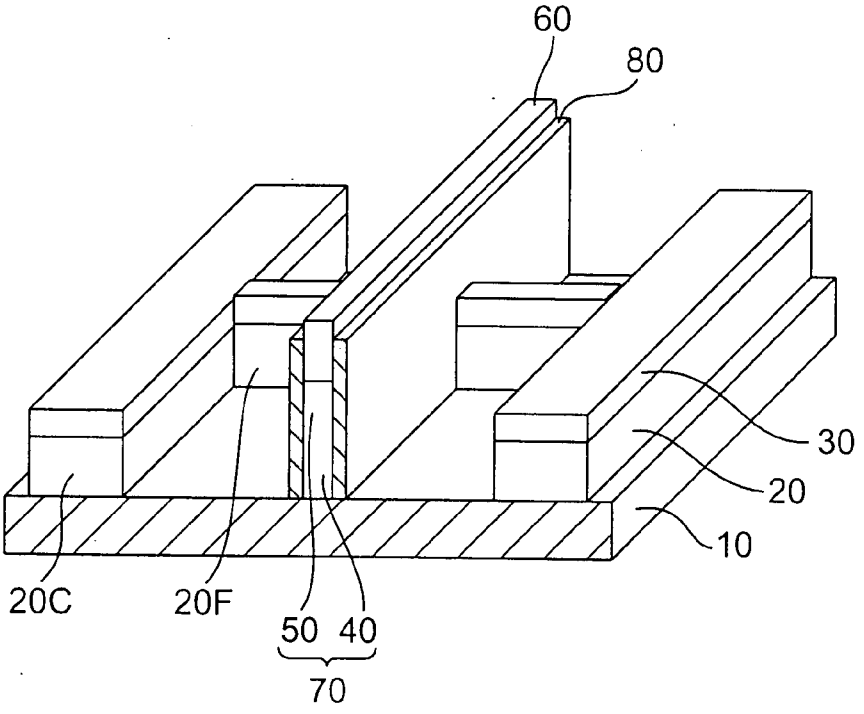



FIG. 2

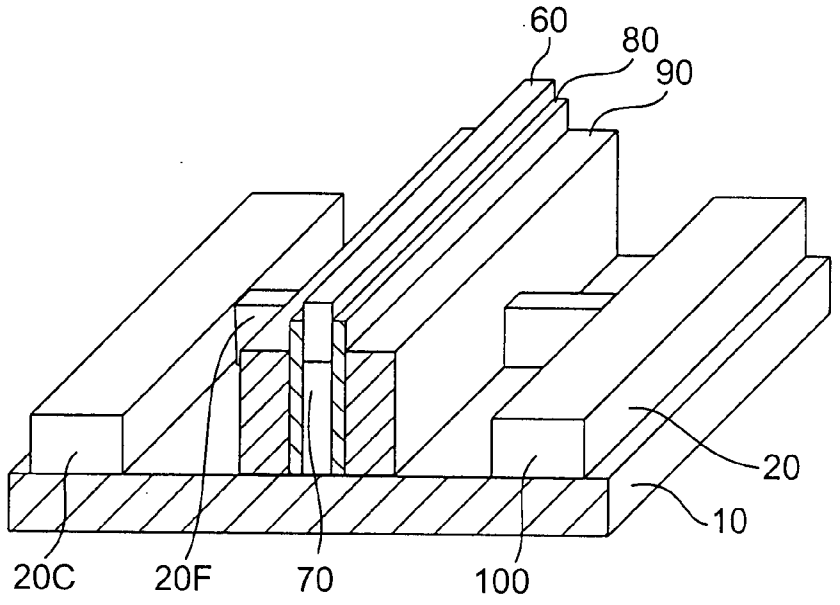



FIG. 3

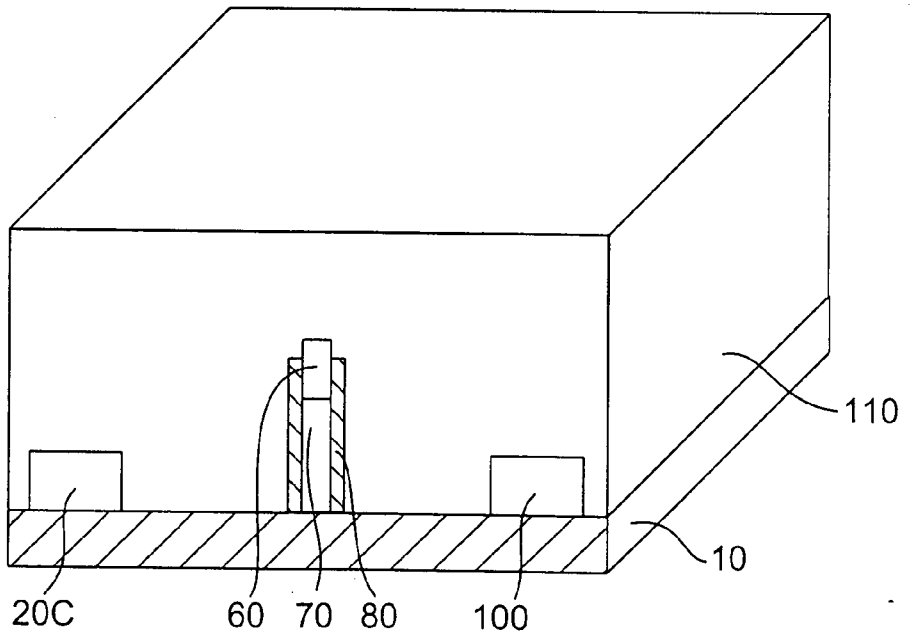



FIG. 4

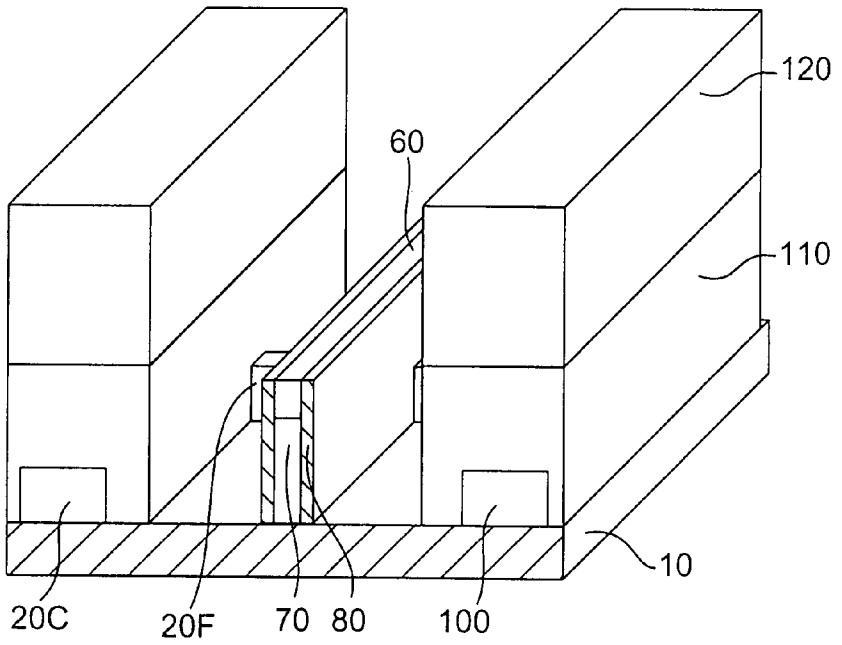



FIG. 5

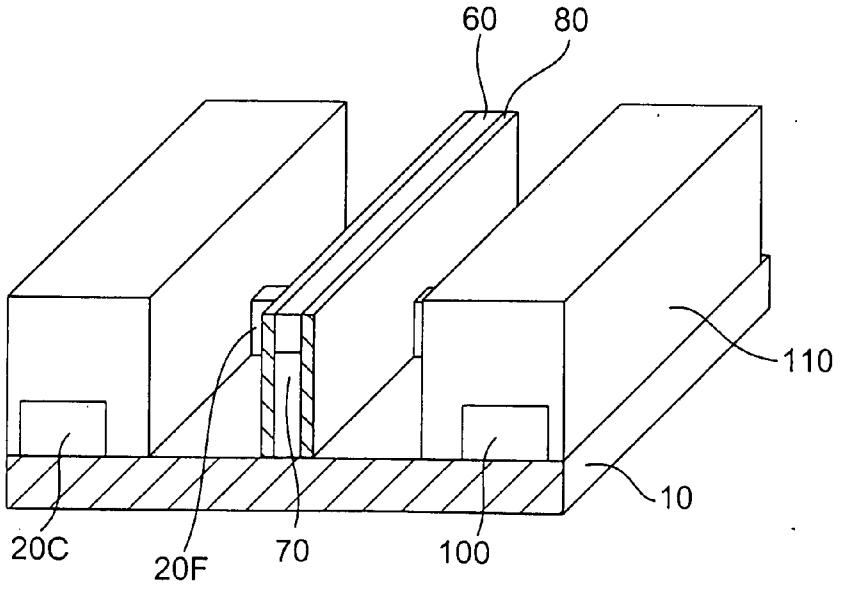



FIG. 6

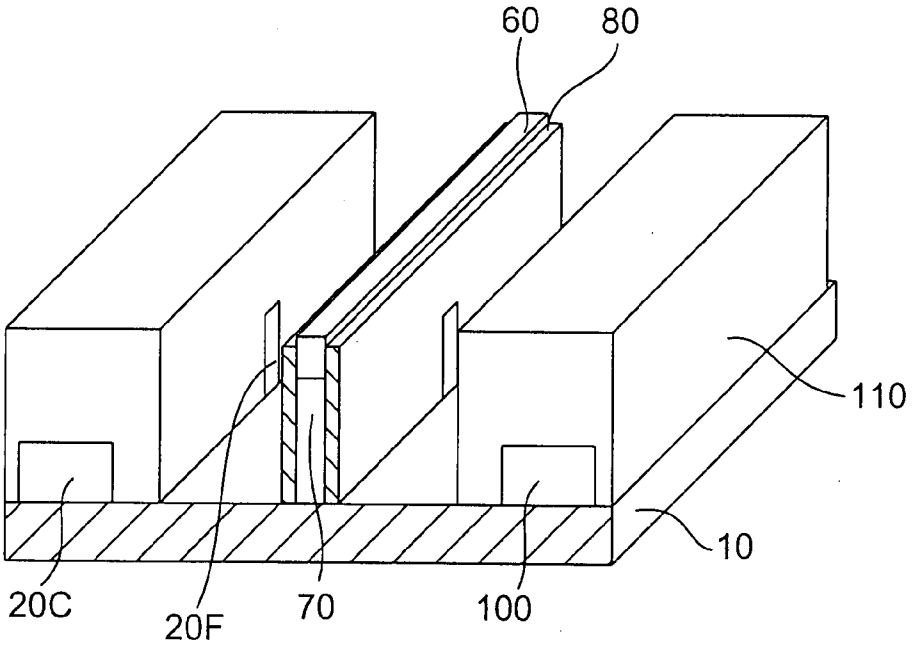



FIG. 7

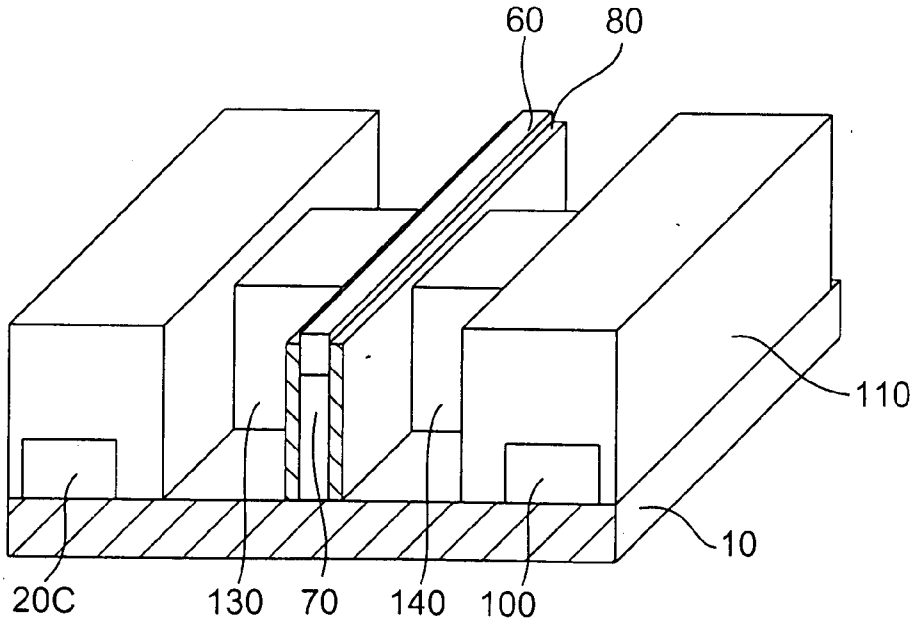



FIG. 8

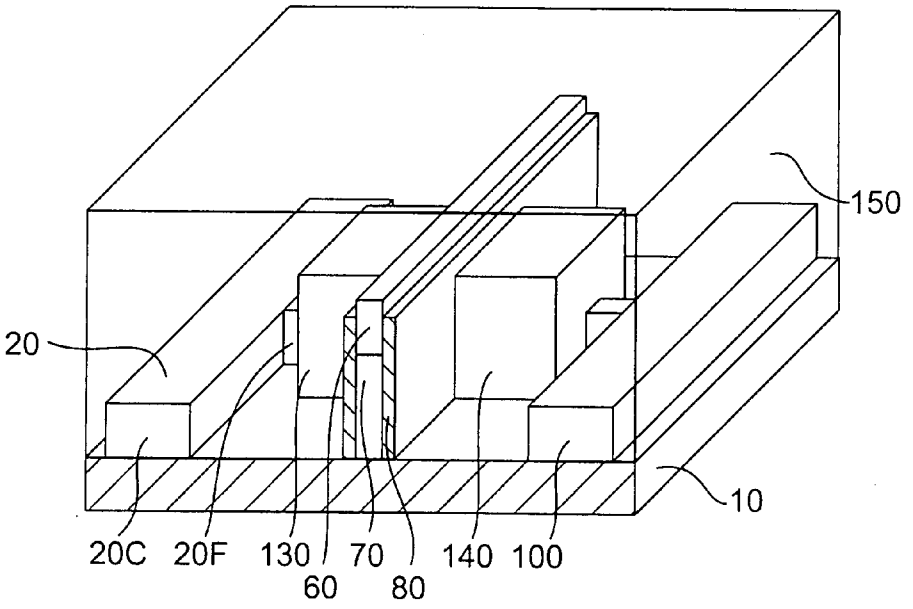

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FIG. 9

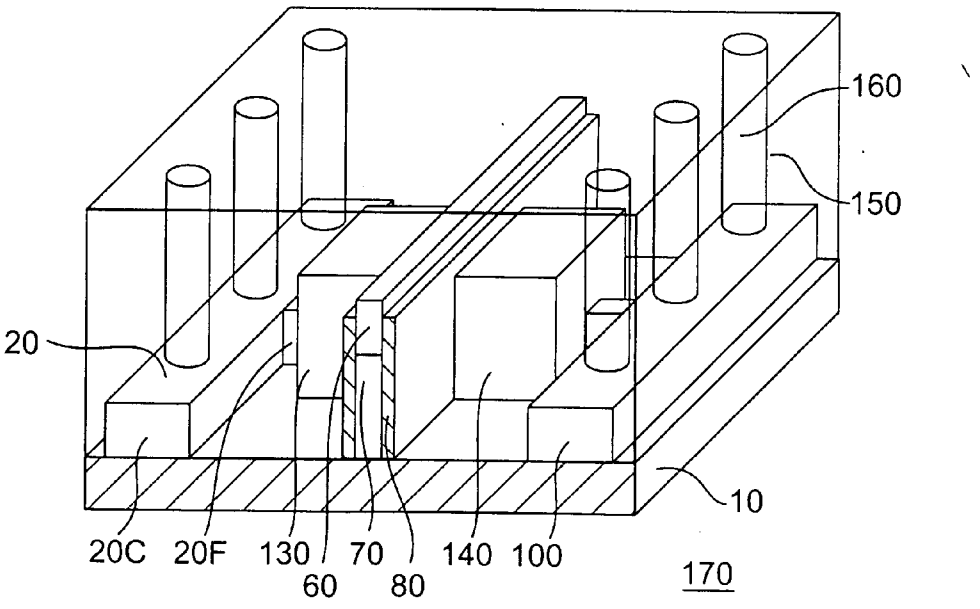
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FIG. 10

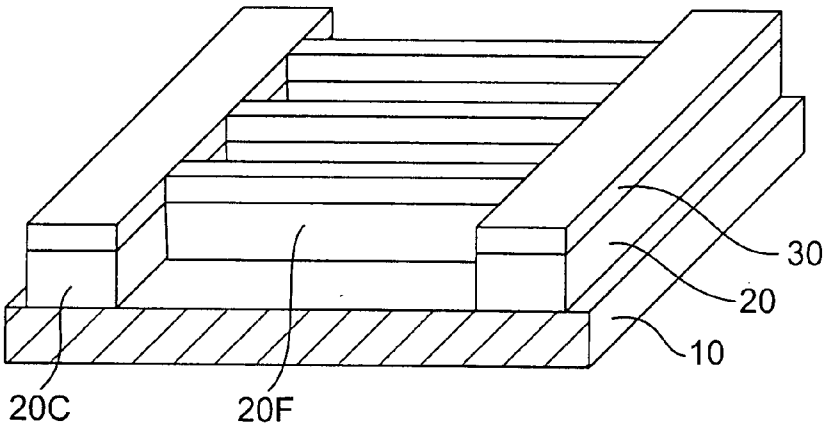


FIG. 11

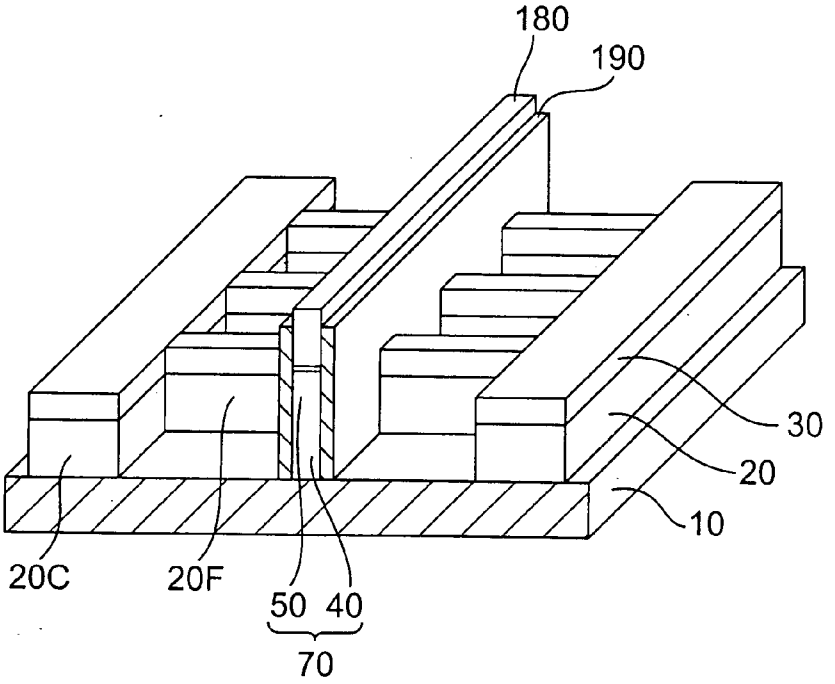


FIG. 12

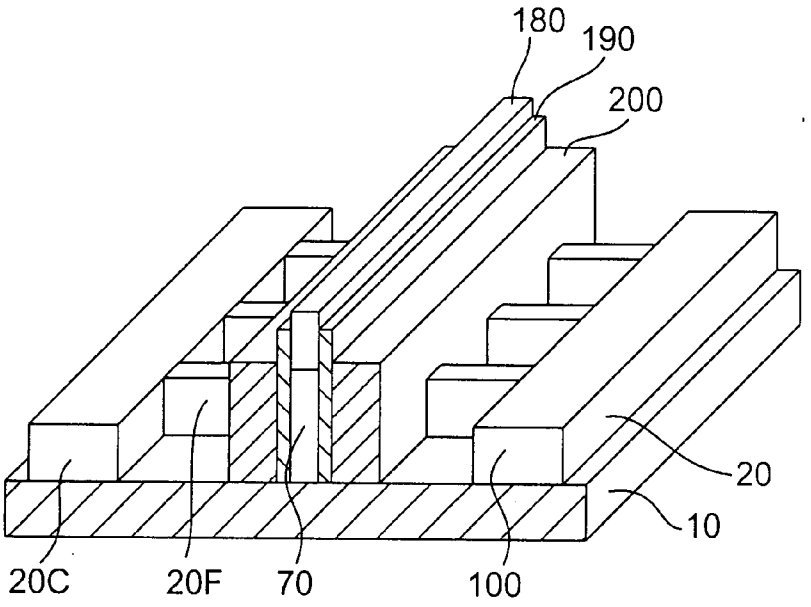


FIG. 13

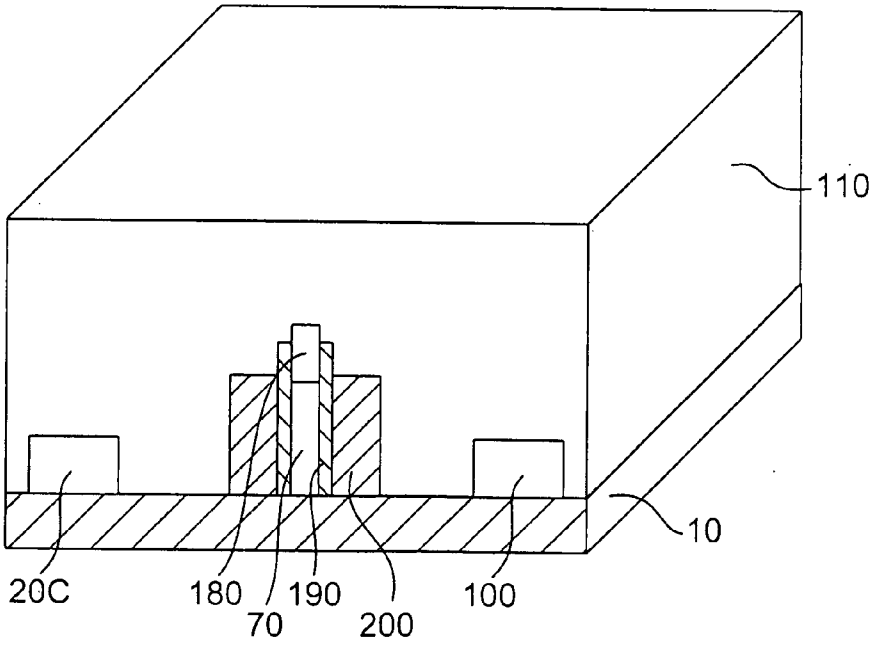


FIG. 14

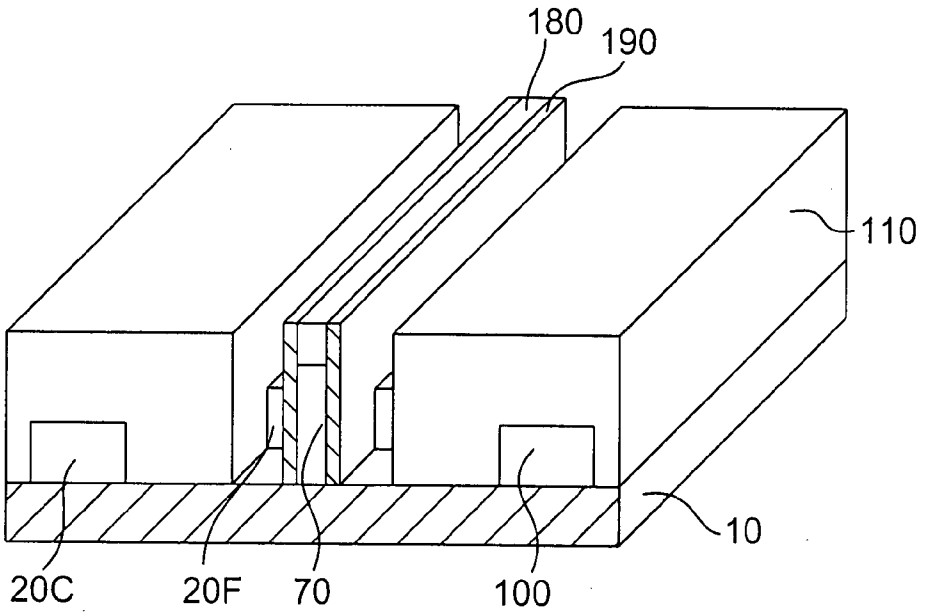


FIG. 15

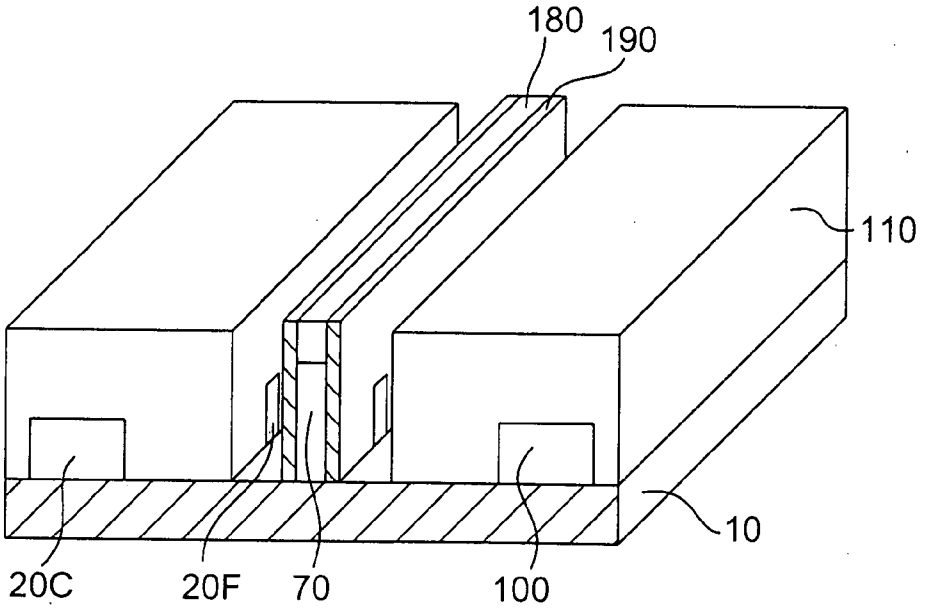


FIG. 16

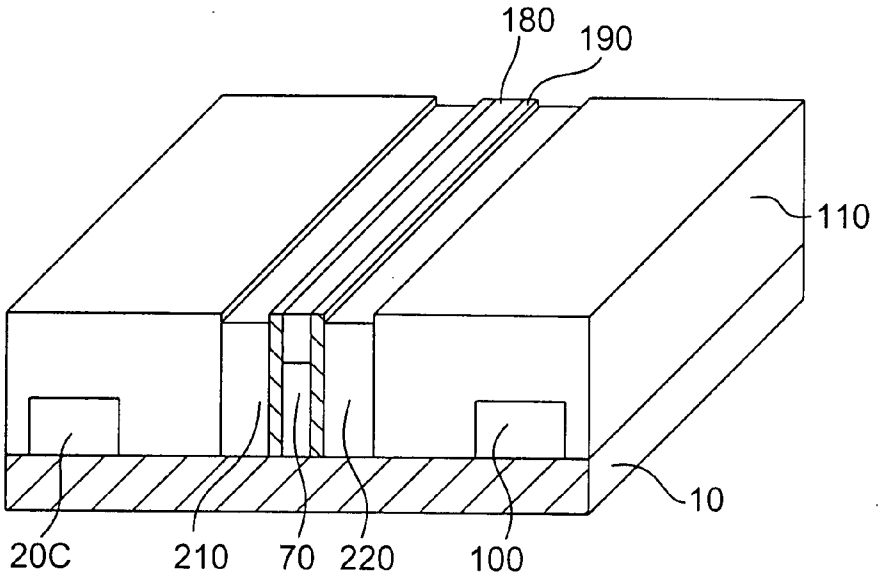
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FIG. 17

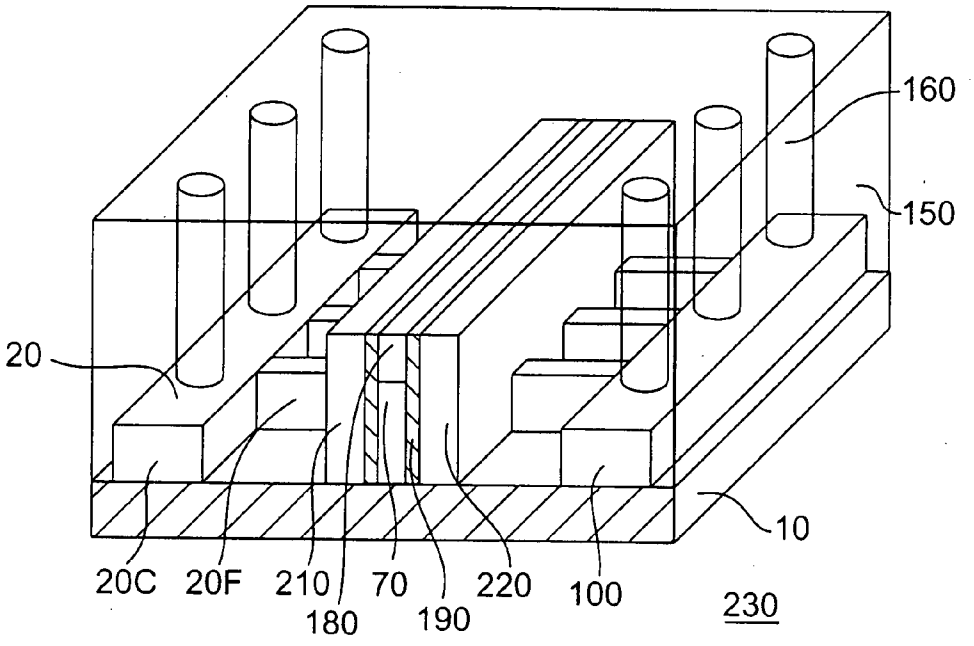
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FIG. 18

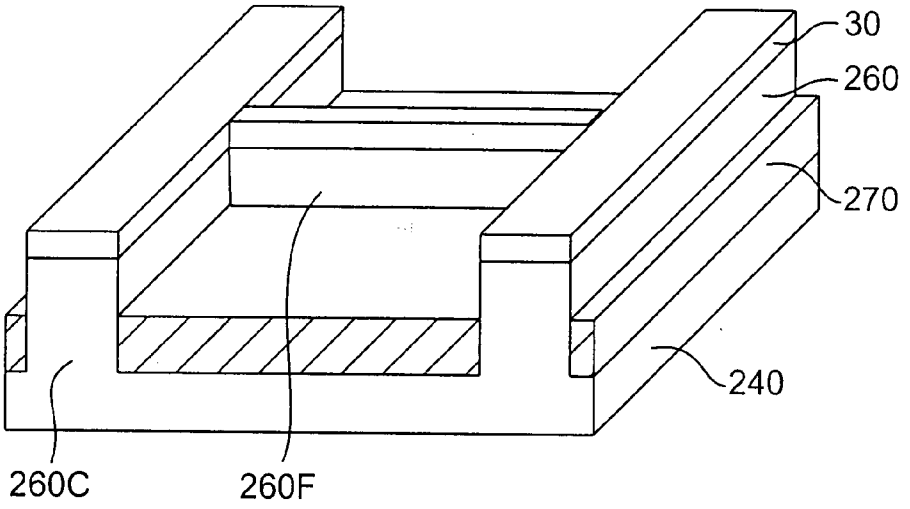


FIG. 19

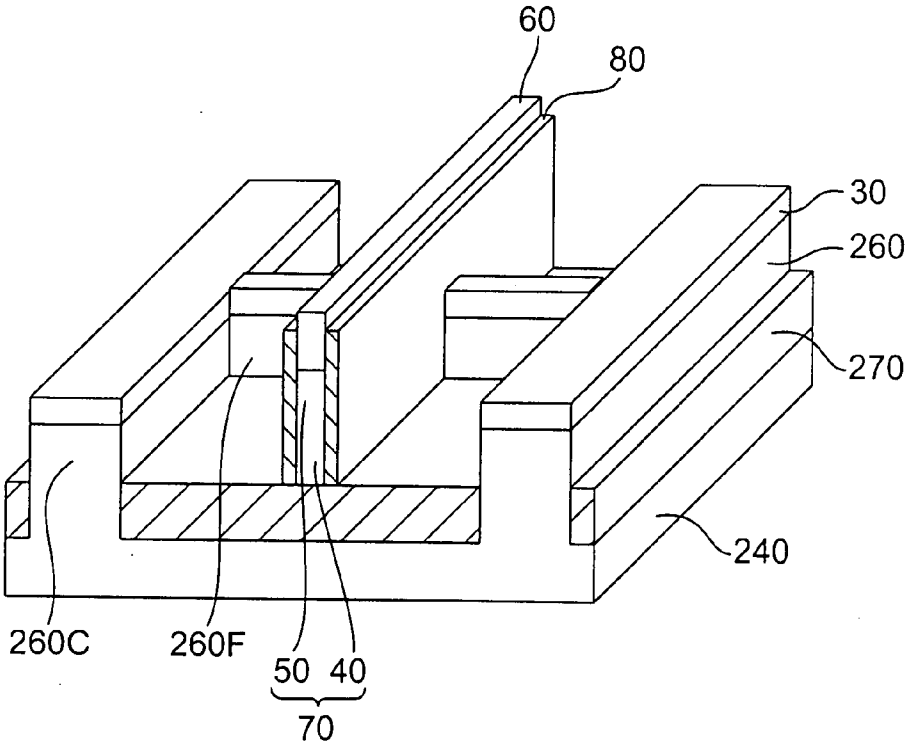


FIG. 20

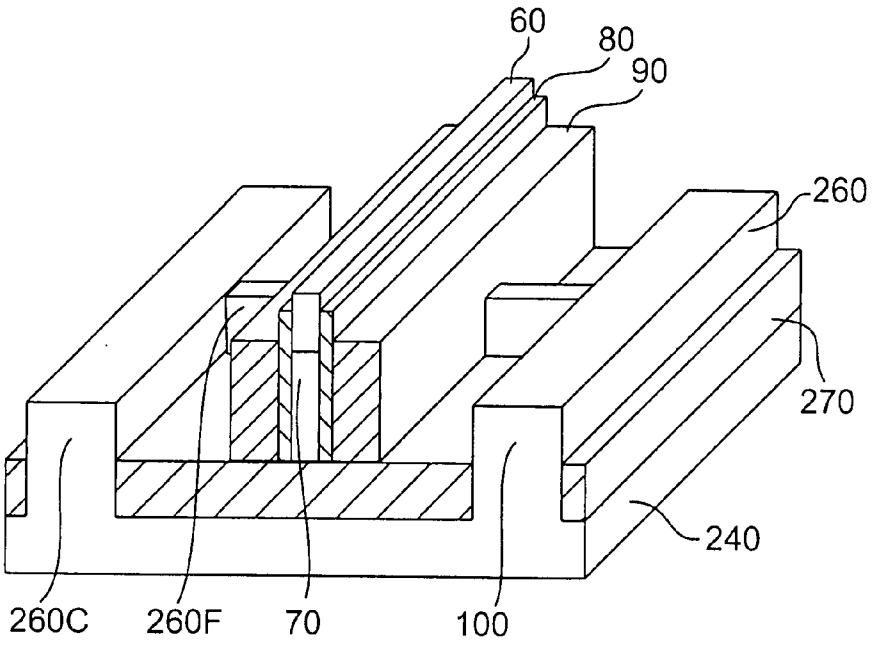
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FIG. 21

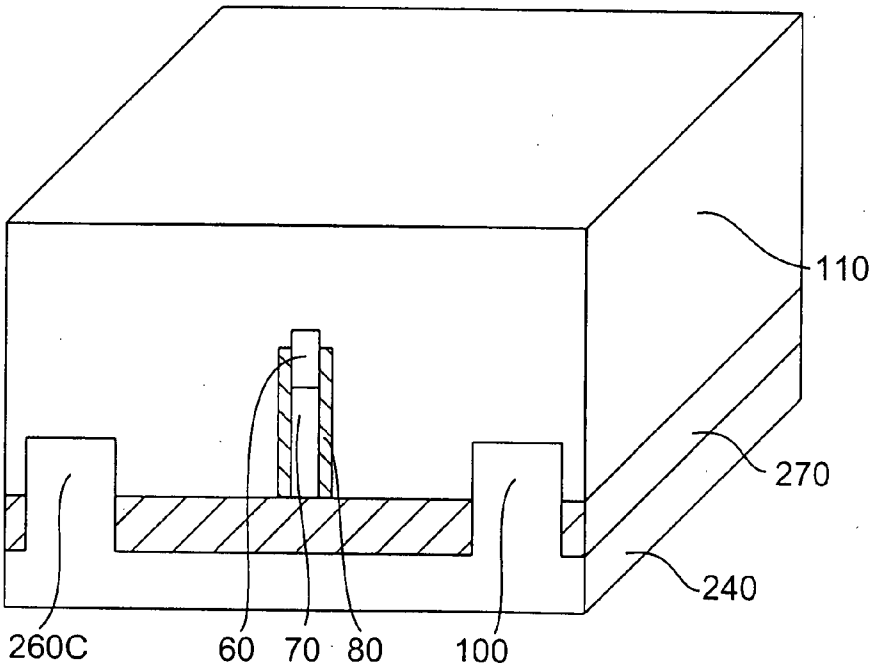
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FIG. 22

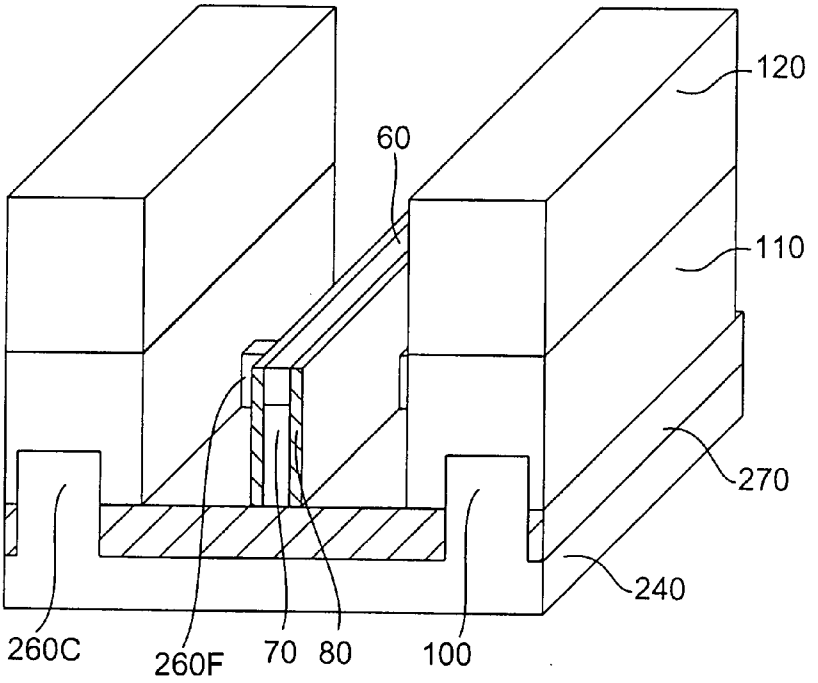
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FIG. 23

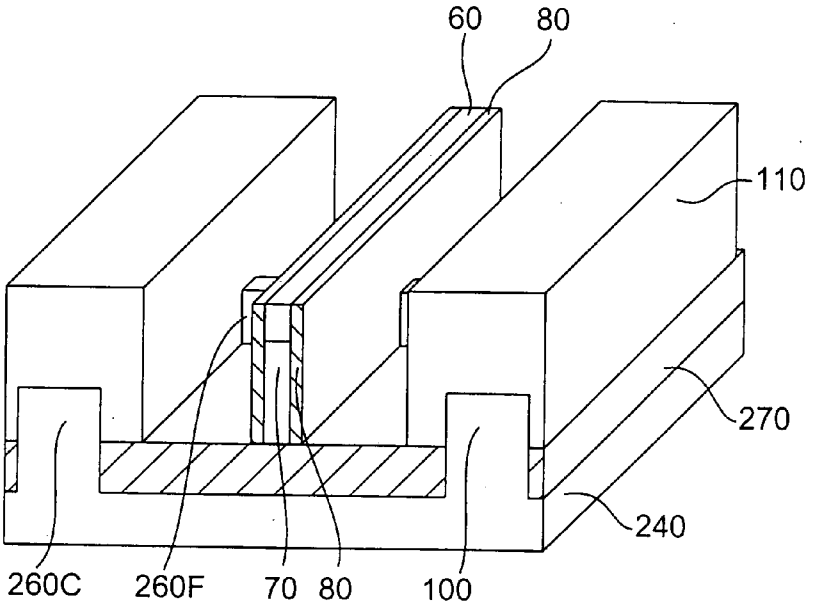
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FIG. 24

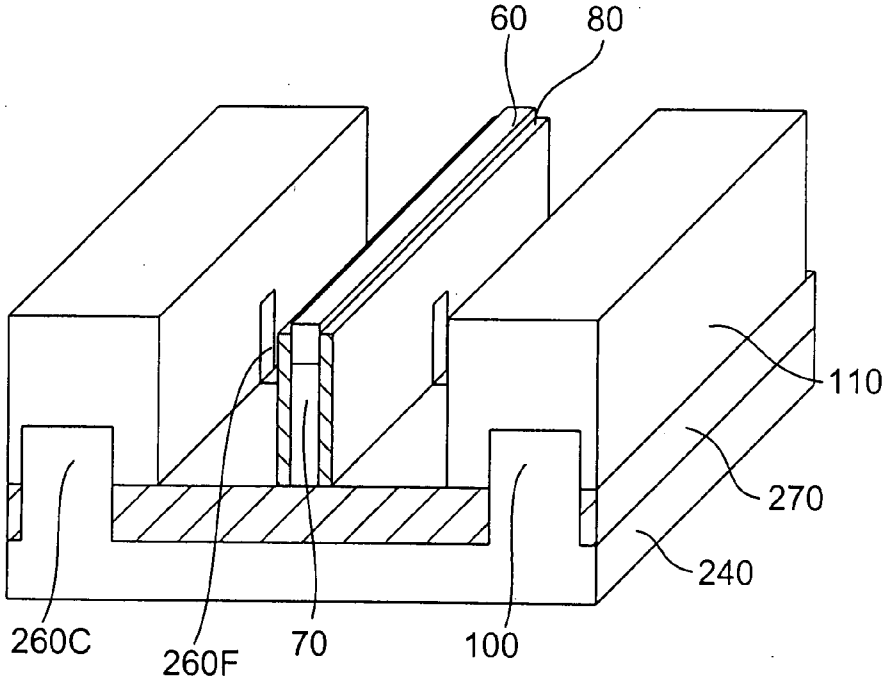
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FIG. 25

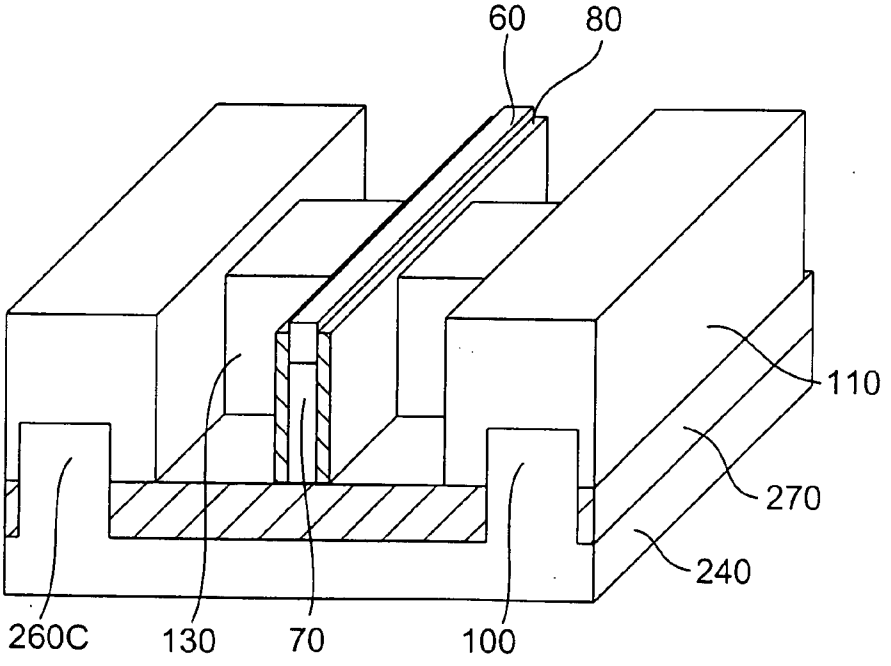
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FIG. 26

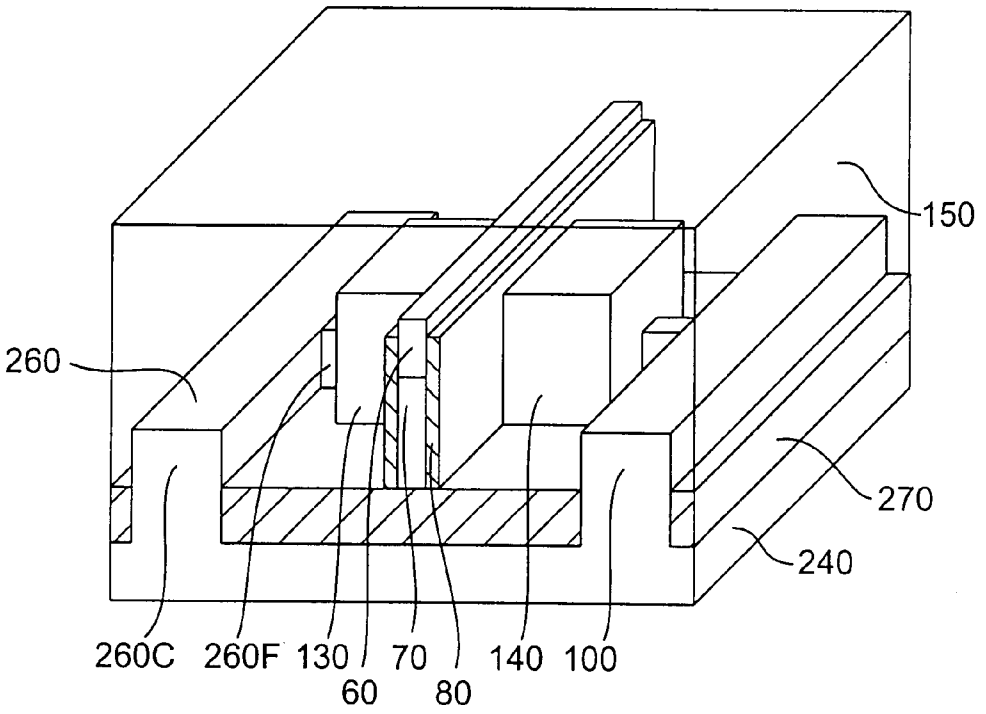
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FIG. 27

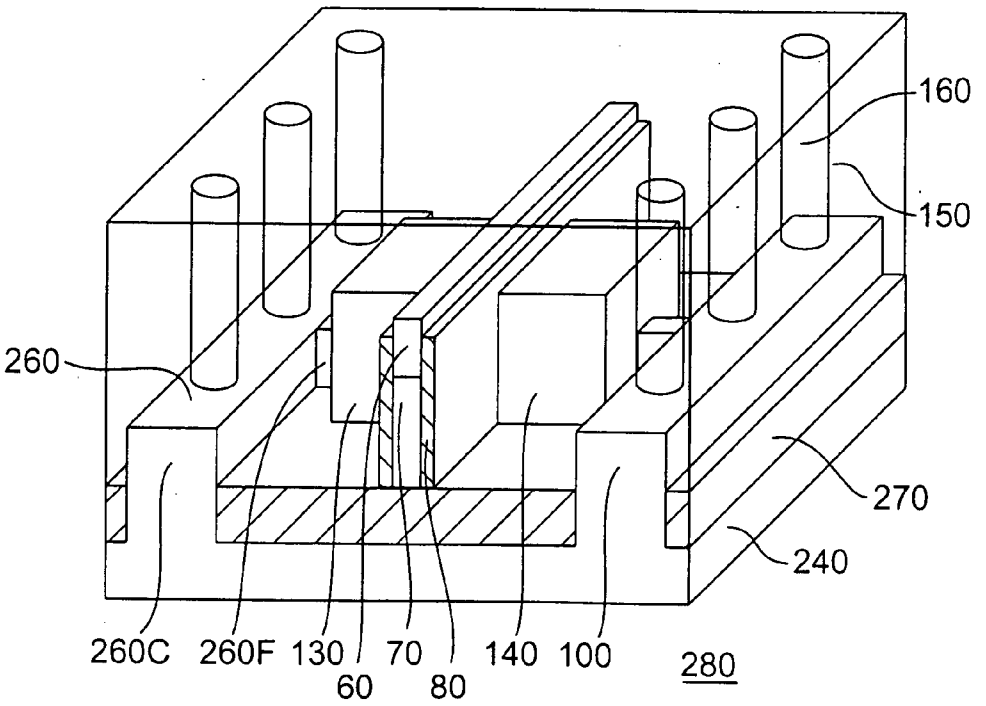
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FIG. 28

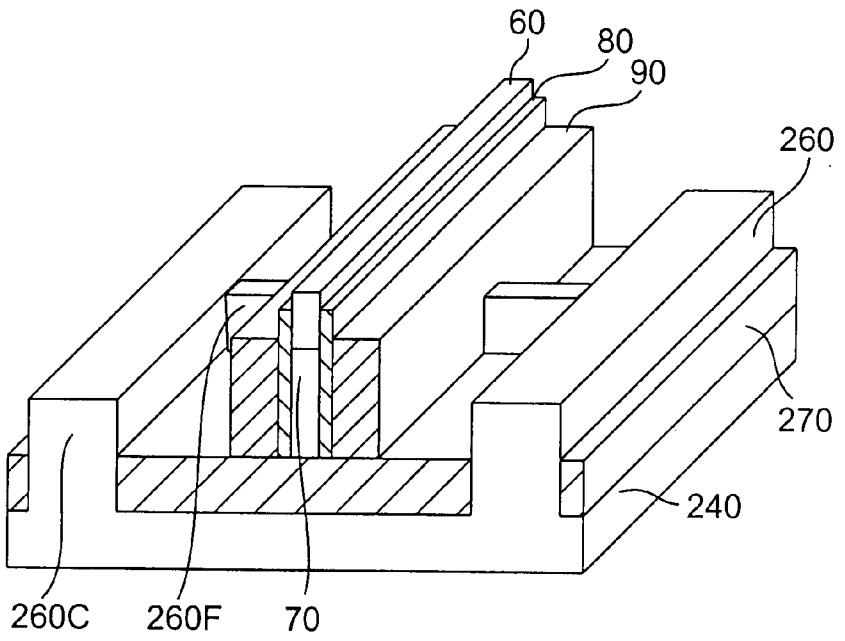
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FIG. 29

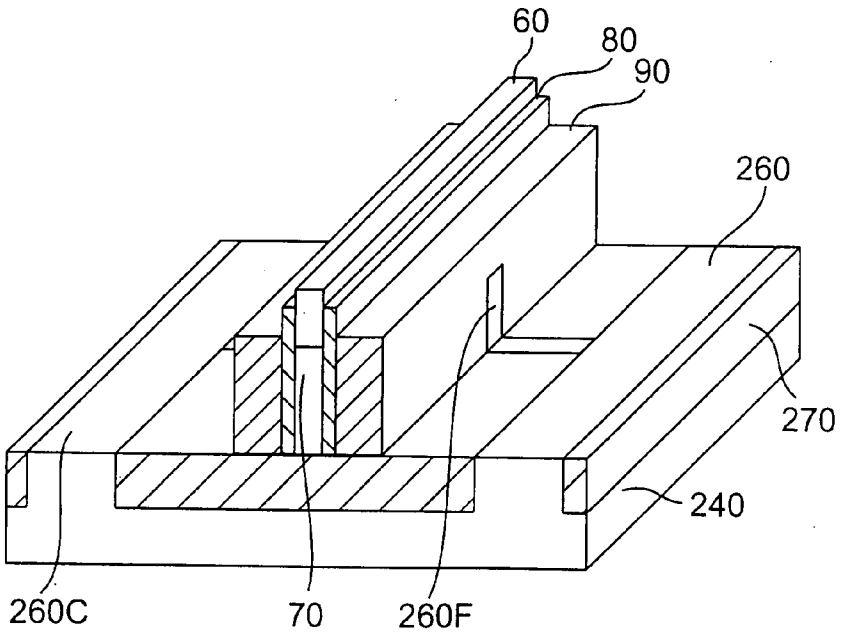
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FIG. 30

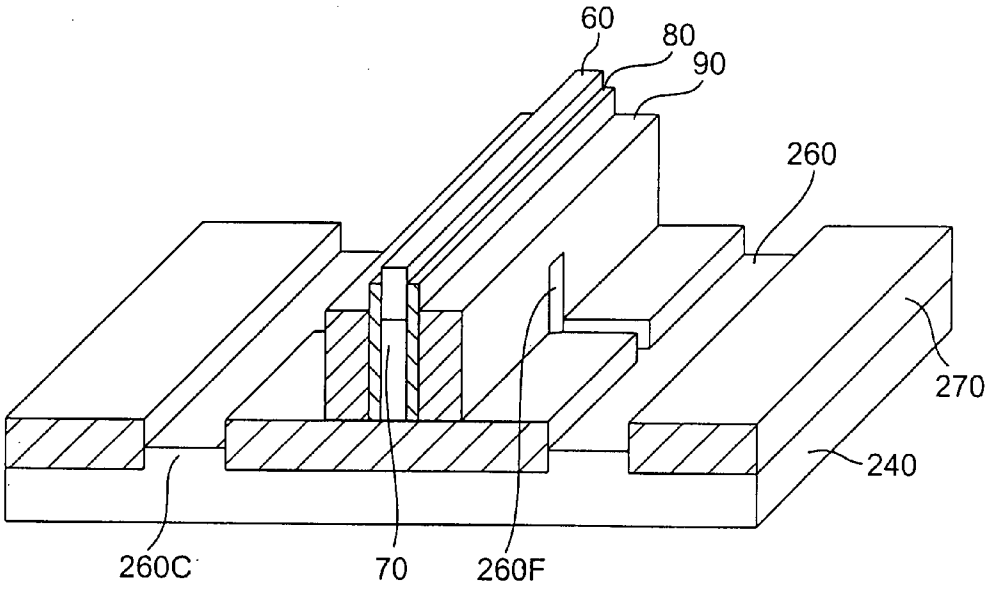


FIG. 31

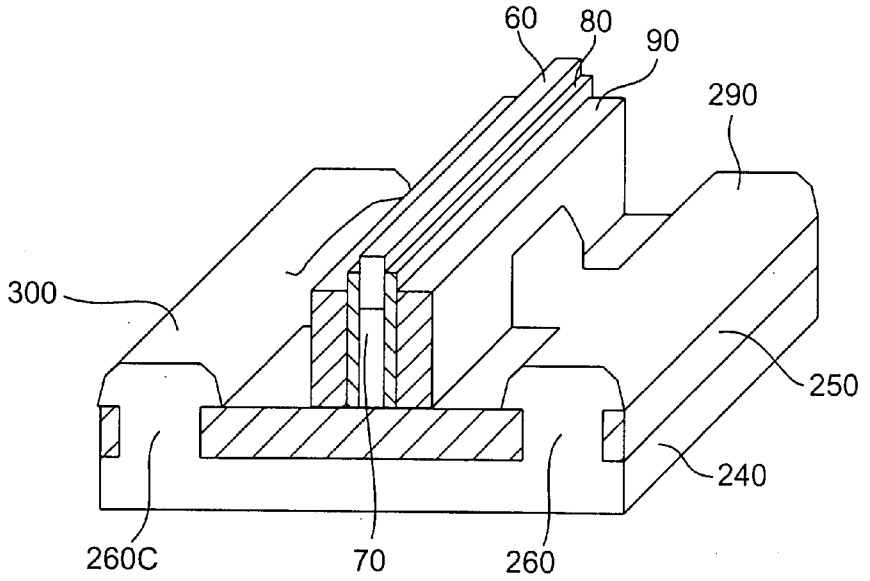
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FIG. 32

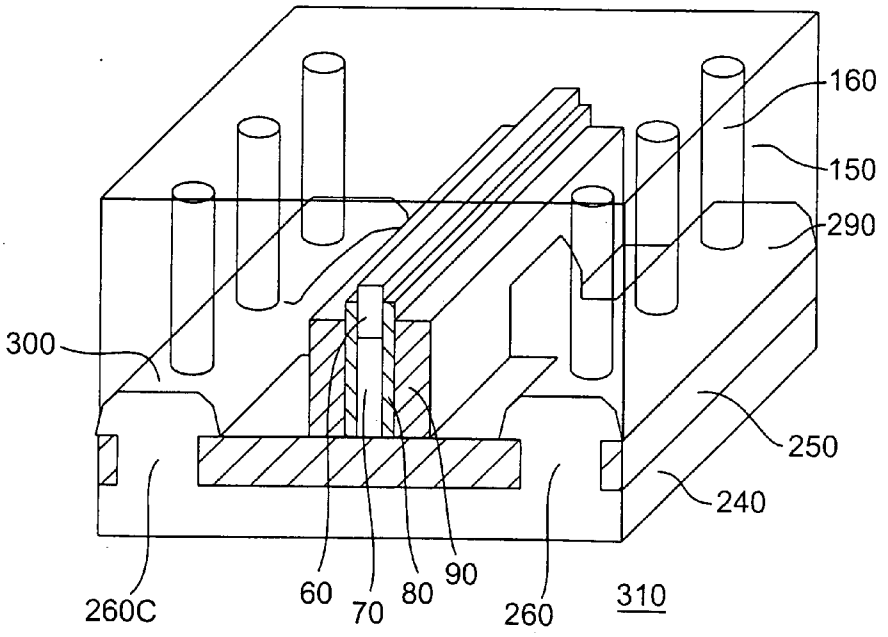
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FIG. 33

# SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

## CROSS REFERENCE TO RELATED APPLICATION

[0001] This application is based upon and claims benefit of priority under 35 USC 119 from the Japanese Patent Application No. 2006-69580, filed on Mar. 14, 2006, the entire contents of which are incorporated herein by reference.

## BACKGROUND OF THE INVENTION

[0002] The present invention relates to a semiconductor device and a method for manufacturing the same.

[0003] In recent years, an MOSFET of a so-called double-gate structure has been developed for the size reduction, low power consumption, and high speed of transistors; and among these, the MOSFET wherein a semiconductor layer is formed to have a Fin shape, is called a FinFET.

[0004] In a planar-type MOSFET, on the other hand, a technique to improve the mobility of carriers by applying stress to the channel region has been developed.

[0005] For example, in the planar-shaped PMOSFET, the mobility of holes is improved by burying silicon germanium (SiGe) in the source/drain region, and applying a compressive stress to the channel region. In the planar-shaped NMOSFET, on the other hand, the mobility of electrons is improved by burying silicon carbide (SiC) in the source/drain region, and applying a tensile stress to the channel region.

[0006] In recent years, also in the FinFET, a method wherein silicon germanium is used in the source/drain region has been proposed (for example, refer to Non-Patent Document 1). By this method, the driving current of the FinFET can be increased by etching the source/drain forming region in the semiconductor layer to the middle to remove a predetermined quantity thereof, and epitaxially growing silicon germanium.

[0007] According to this method, however, although etching must be stopped in the middle, there was a problem wherein it was difficult to stop etching evenly throughout the entire surface of the source/drain forming region.

[0008] Therefore, when a FinFET was formed on the SOI substrate, if the buried insulating film was exposed by performing etching to the bottom of the source/drain forming region, there was a problem wherein silicon was completely disappeared from the source/drain forming region including the contact plug forming region in semiconductor layers composed of silicon, and thereby, silicon germanium could not be epitaxially grown.

[0009] Furthermore, according to this method, since silicon germanium is formed only in the upper portion of the source/drain forming region, there was a problem wherein stress was applied only to the upper portion of the channel region, and stress was not sufficiently applied to the bottom portion of the channel region to adversely affect the electrical properties of the device.

[0010] The document regarding a FinFET that uses silicon germanium in the source/drain region will be shown below:

[0011] 2005 Symposium on VLSI Technology Digest of Technical Papers, pp. 194-195.

## SUMMARY OF THE INVENTION

[0012] A semiconductor device according to an embodiment of the present invention includes:

[0013] convex semiconductor layers formed on a semiconductor substrate via an insulating film;

[0014] gate electrodes formed on a pair of facing sides of the semiconductor layers via a gate insulating film;

[0015] a channel region formed of silicon between the gate electrodes in the semiconductor layers;

[0016] a source extension region and a drain extension region formed of silicon germanium or silicon carbon on both sides of the channel region in the semiconductor layers; and

[0017] a source region formed of silicon so as to adjoin to the opposite side of the channel region in the source extension region, and a drain region formed of silicon so as to adjoin to the opposite side of the channel region in the drain extension region in the semiconductor layers.

[0018] A method for manufacturing a semiconductor device according to an embodiment of the present invention includes:

[0019] depositing a mask material on a first semiconductor layer formed of silicon on a semiconductor substrate via a buried insulating film, and patterning the mask material and the first semiconductor layer, to form a first semiconductor layer having a convex shape;

[0020] forming gate insulating films on a pair of facing sides of the first semiconductor layer;

[0021] depositing a gate electrode material of the buried insulating film, the gate insulating films, and the mask material, and pattering the gate electrode material, to form a gate electrode on the pair of facing sides and the upper surface of the first semiconductor layer via the gate insulating films and the mask material;

[0022] forming gate electrode sidewalls on the sides of the gate electrode, and removing the mask material formed on the first semiconductor layer and not coated by the gate electrode and the gate electrode sidewalls;

[0023] forming a source region and a drain region by the ion implantation of a predetermined impurity into the first semiconductor layer using the gate electrode and the gate electrode sidewalls as masks;

[0024] forming an insulating film on the buried insulating film, the first semiconductor layer, the gate electrode, and the gate electrode sidewalls;

[0025] forming a mask having a pattern wherein the upper surfaces of the gate electrode sidewalls are opened on the insulating film;

[0026] exposing a part of the first semiconductor layer by etching the insulating film and the gate electrode sidewalls using the mask;

[0027] removing the mask, and etching off the exposed first semiconductor layer;

[0028] forming a second semiconductor layer composed of silicon germanium or silicon carbide on the removed region; and

[0029] forming a source extension region and a drain extension region by the ion implantation of a predetermined impurity into the second semiconductor layer using the gate electrode and the insulating film as masks.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0030] FIG. **1** is a longitudinal sectional view showing a cross-sectional structure of an element in each step in the method for manufacturing a semiconductor device according to the first embodiment of the present invention;

[0031] FIG. **2** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0032] FIG. **3** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0033] FIG. **4** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0034] FIG. **5** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0035] FIG. **6** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0036] FIG. **7** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0037] FIG. **8** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0038] FIG. **9** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0039] FIG. **10** is a longitudinal sectional view showing a cross-sectional structure of an element in each step in the method for manufacturing the same semiconductor device;

[0040] FIG. **11** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing a semiconductor device according to the second embodiment of the present invention;

[0041] FIG. **12** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0042] FIG. **13** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0043] FIG. **14** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0044] FIG. **15** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0045] FIG. **16** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0046] FIG. **17** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0047] FIG. **18** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0048] FIG. **19** is a longitudinal sectional view showing a cross-sectional structure of an element in each step in the method for manufacturing a semiconductor device according to the third embodiment of the present invention;

[0049] FIG. **20** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0050] FIG. **21** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0051] FIG. **22** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0052] FIG. **23** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0053] FIG. **24** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0054] FIG. **25** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0055] FIG. **26** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0056] FIG. **27** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0057] FIG. **28** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0058] FIG. **29** is a longitudinal sectional view showing a cross-sectional structure of an element in each step in the method for manufacturing a semiconductor device according to the fourth embodiment of the present invention;

[0059] FIG. **30** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0060] FIG. **31** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device;

[0061] FIG. **32** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device; and

[0062] FIG. **33** is a longitudinal sectional view showing a cross-sectional structure of the element in each step in the method for manufacturing the same semiconductor device.

## DETAILED DESCRIPTION OF THE INVENTION

[0063] The embodiments of the present invention will be described below referring to the drawings.

### (1) First Embodiment

[0064] FIGS. **1** to **10** illustrate the method for manufacturing a semiconductor device according to the first embodiment of the present invention. First, as FIG. **1** shows, an SOI substrate wherein a buried insulating film **10** and a semiconductor layer **20** having a thickness of about 50 nm sequentially laminated on a semiconductor substrate (not shown) is prepared. The semiconductor substrate and the semiconductor layer **20** are composed of, for example, silicon single crystals, and the buried insulating film **10** is composed of, for example, silicon oxide ($SiO_2$) film.

[0065] After depositing a mask material **30** composed, for example, of a silicon nitride (SiN) film having a thickness of about 70 nm on the semiconductor layer **20**, the mask material **30** and the semiconductor layer **20** are sequentially patterned by lithography and RIE, to form a convex semiconductor layer **20** consisting of a fin **20**F and a contact plug forming region **20**C.

[0066] As FIG. **2** shows, a gate insulating film (not shown) composed, for example, of hafnium nitride silicate (HfSiON) film is formed on each of a pair of facing sides of the fin **20**F. After depositing a gate electrode material **40** composed, for example, polysilicon, having a thickness of about 250 nm as a first layer using CVD or the like, the gate electrode material **40** is planarized by CMP using the mask material **30** as a stopper.

[0067] After depositing a gate electrode material **50** composed, for example, of polysilicon, having a thickness of about 50 nm as a second layer using CVD or the like, a mask material **60** composed, for example, of a silicon nitride (SiN) film having a thickness of about 120 nm is deposited on the gate electrode material **50**. The mask material **60** and the gate electrode materials **50** and **40** are sequentially patterned using lithography and RIE to form a gate electrode **70**.

[0068] Thereafter, a first gate electrode sidewall material composed, for example, of a silicon nitride film of a thickness of about 5 nm is deposited on the entire surface, and the first gate electrode sidewall material is etched using RIE to form first gate electrode sidewalls **80** on the sides of the gate electrode **70** and the mask material **60**.

[0069] As FIG. **3** shows, after depositing a second gate sidewall material composed, for example, of a TEOS film having a thickness of about 30 nm, the second gate electrode sidewall material is etched using RIE, to form second gate electrode sidewalls **90** on the sides of the first gate electrode sidewalls **80**.

[0070] At this time, in the semiconductor layer **20**, the mask material **30** formed on the source/drain forming region where a source/drain region is subsequently formed is removed, and the film thickness of the mask material **60** formed on the gate electrode **70** reduced to about 50 nm.

[0071] Thereafter, by performing ion implantation into the semiconductor layer **20** by plasma doping or angle ion implantation using the mask material **60**, and the first and second gate electrode sidewalls **80** and **90** as masks, a source/drain region **100** having a deep junction depth in the lateral direction in the drawing is formed in the contact plug forming region **20**C and a part of the fin **20**F in the semiconductor layer **20**. In this case, silicon can be epitaxially grown on the upper surface and sides of the exposed semiconductor layer **20** before performing ion implantation.

[0072] Then, a silicide, such as nickel silicide (NiSi) (not shown), is formed on the surface portion of the source/drain region **100**. As FIG. **4** shows, after depositing a thick insulating film **110** composed, for example, of a TEOS film, the insulating film **110** is planarized using CMP.

[0073] As FIG. **5** shows, a photo-resist is applied onto the insulating film **110**, and exposed and developed to form a resist mask **120** having a pattern wherein the upper surface of the second gate electrode sidewall **90** is opened. By etching the insulating film **110** and the second gate electrode sidewall **90** by RIE using the resist mask **120** as a mask, a part of the insulating film **110** and the second gate electrode sidewall **90** are removed to expose a part of the fin **20**F.

[0074] As FIG. **6** shows, after removing the resist mask **120**, as FIG. **7** shows, the exposed fin **20**F is etched off by RIE.

[0075] As FIG. **8** shows, by vapor-phase growth or solid-phase growth, silicon germanium is epitaxially grown using the sides of the fin **20**F exposed on the sides of the first gate electrode sidewalls **80** and the insulating film **110** as seeds to form a fin **130** higher and wider than the fin **20**F.

[0076] Next, an impurity, such as boron (B), is ion-implanted into the fin **130** to form a source/drain extension region **140**, having a shallow junction depth in the lateral direction in the drawing and sharp impurity concentration distribution, in the fin **130**. In this case, boron-doped silicon germanium can be formed as the fin **130**.

[0077] As FIG. **9** shows, an insulating film composed, for example, of a TEOS film is deposited, and the insulating film is planarized using CMP to form an interlayer insulating film **150**. As FIG. **10** shows, contact plugs **160** are formed in the interlayer insulating film **150**, and wiring steps are conducted to fabricate a FinFET **170**, which is a PMOSFET.

[0078] In the FinFET **170**, which is a PMOSFET, fabricated using the above-described methods, as FIG. **10** shows, the buried insulating film **10** is formed on a semiconductor substrate (not shown), a semiconductor layer **20** having a fin **20**F and a contact plug forming region **20**C composed of silicon, and a fin **130** composed of silicon germanium is formed on the buried insulating film **10**.

[0079] In the fin **20**F (not shown) formed in the vicinity of the center portion of the semiconductor layer **20**, a channel region (not shown) is formed. On both sides of the channel region and in the fin **130**, a source/drain extension region **140** is formed; and in the fin **20**F and the contact plug forming region **20**C, a source/drain region **100** is formed so as to sandwich the source/drain extension region **140**.

[0080] On both sides of the fin **20**F in the vicinity of the channel region, a gate insulating film (not shown) is formed; and on the upper surface in the vicinity of the channel

region, a mask material **30** (FIG. **2**) is formed. On both sides and the upper surface of the fin **20**F, a gate electrode **70** is formed via the gate insulating film and the mask material **30** to stride the fin **20**F. On the upper surface of the gate electrode **70**, a mask material **60** is formed, and on the sides of these gate electrode **70** and mask material **60**, gate electrode sidewalls **80** are formed.

[**0081**] On the buried insulating film **10**, the semiconductor layer **20**, the mask material **60**, and the gate electrode sidewalls **80**, an interlayer insulating film **150** is formed; and on the upper surface of the contact region **20**C in the semiconductor layer **20**, contact plugs **160** are formed.

[**0082**] As described above, according to the first embodiment, in the FinFET **170**, which is a PMOSFET, the channel region and the source/drain region **100** in the semiconductor layer **20** are formed of silicon; and the source/drain extension region **140** is formed of silicon germanium.

[**0083**] However, if the source/drain region **100** is also formed of silicon germanium, irregularity is formed in the boundary between the silicide and the source/drain region **100**, which causes a problem of the abnormal growth of silicide to generate a junction leakage current. Whereas, according to the first embodiment, while improving the mobility of carriers, the abnormal growth of silicide and the generation of junction leakage current can be suppressed.

[**0084**] Also according to the first embodiment, silicon germanium can be evenly formed from the upper portion to the bottom portion of the fin **130**, and thereby, the mobility of carriers can be improved evenly from the upper portion to the bottom portion of the channel region.

[**0085**] Also according to the first embodiment, by forming the fin **130** higher and wider than the fin **20**F, the parasitic resistance can be reduced.

[**0086**] Also according to the first embodiment, when a part of the fin **20**F in the semiconductor layer **20** is removed, the disappearance of all silicon in the source/drain forming region including the contact region **20**C can be prevented, and thereby, impossibility of the epitaxial growth of silicon germanium can be avoided.

[**0087**] Further according to the first embodiment, since the source/drain region **100** that requires a high-temperature heating step is formed before the source/drain extension region **140**, change in the impurity concentration distribution of the source/drain extension region **140** can be suppressed.

(2) Second Embodiment

[**0088**] FIGS. **11** to **18** illustrate the method for manufacturing a FinFET according to the second embodiment of the present invention. In the case of the second embodiment, a method for manufacturing a FinFET having a plurality of fins will be described. The elements same as the elements shown in FIGS. **1** to **10** are denoted by the same numerals and characters, and the description thereof will be omitted.

[**0089**] As FIG. **11** shows, in the same manner as in the first embodiment, an SOI substrate wherein a buried insulating film **10** and a semiconductor layer **20** sequentially laminated on a semiconductor substrate (not shown) is prepared. After depositing a mask material **30** composed, for example, of a silicon nitride (SiN) film having a thickness of about 70 nm on the semiconductor layer **20**, the mask material **30** and the semiconductor layer **20** are sequentially patterned by lithography and RIE, to form a convex semiconductor layer consisting of three fins **20**F and a contact region **20**C.

[**0090**] As FIG. **12** shows, in the same manner as in the first embodiment, a gate insulating film (not shown) is formed on each of a pair of facing sides of the fin **20**F. After depositing a gate electrode material **40** as a first layer using CVD or the like, the gate electrode material **40** is planarized by CMP using the mask material **30** as a stopper.

[**0091**] After depositing a gate electrode material **50** as a second layer using CVD or the like, a mask material **180** composed, for example, of a silicon oxide ($SiO_2$) film is deposited on the gate electrode material **50**. The mask material **180** and the gate electrode materials **50** and **40** are sequentially patterned using lithography and RIE to form a gate electrode **70**.

[**0092**] Thereafter, a first gate electrode sidewall material composed, for example, of a silicon oxide film of a thickness of about 7 nm is deposited on the entire surface, and the first gate electrode sidewall material is etched using RIE to form first gate electrode sidewalls **190** on the sides of the gate electrode **70** and the mask material **180**.

[**0093**] As FIG. **13** shows, after depositing a second gate sidewall material composed, for example, of a silicon nitride film whose etching rate is high, having a thickness of about 40 nm is deposited on the entire surface, the second gate electrode sidewall material is etched using RIE, to form second gate electrode sidewalls **200** on the sides of the first gate electrode sidewalls **190**.

[**0094**] At this time, in the same manner as in the first embodiment, in the semiconductor layer **20**, the mask material **30** formed on the source/drain forming region is removed, and the film thickness of the mask material **180** formed on the gate electrode **70** reduced to about 40 nm.

[**0095**] Thereafter, in the same manner as in the first embodiment, by performing ion implantation into the semiconductor layer **20**, a source/drain region **100** having a deep junction depth in the lateral direction in the drawing is formed in the contact plug forming region **20**C and a part of the fin **20**F in the semiconductor layer **20**. Then, a silicide (not shown), is formed on the surface portion of the source/drain region **100**. As FIG. **14** shows, after depositing a thick insulating film **110** composed, for example, of a TEOS film, the insulating film **110** is planarized using CMP.

[**0096**] As FIG. **15** shows, the insulating film **110**, the mask material **180**, and the first gate electrode sidewalls **190** are etched by RIE to expose the upper surface of the second gate electrode sidewalls **200**.

[**0097**] By wet etching using hot phosphoric acid, the second gate electrode sidewalls **200** composed of the silicon nitride film having higher etching rate than the silicon oxide film and the TEOS film is selectively removed to expose a part of the fin **20**F. As FIG. **16** shows, in the same manner as in the first embodiment, the exposed fin **20**F is etched off by RIE.

[**0098**] As FIG. **17** shows, by vapor-phase growth or solid-phase growth, silicon germanium is epitaxially grown using the sides of the fin **20**F exposed on the sides of the first gate electrode sidewalls **190** and the insulating film **110** as

seeds to form a silicon germanium layer **210**. At this time, the fins **20**F adjoining each other are connected by the silicon germanium layer **210**.

[**0099**] Next, an impurity, such as boron (B), is ion-implanted into the silicon germanium layer **210** to form a source/drain extension region **220**, having a shallow junction depth in the lateral direction in the drawing and sharp impurity concentration distribution, in the silicon germanium layer **210**.

[**0100**] As FIG. **18** shows, in the same manner as in the first embodiment, an insulating film is deposited, and the insulating film is planarized using CMP to form an interlayer insulating film **150**. Then, contact plugs **160** are formed in the interlayer insulating film **150**, and wiring steps are conducted to fabricate a FinFET **230**, which is a PMOSFET.

[**0101**] As FIG. **18** shows, the FinFET **230**, which is a PMOSFET fabricated using the above-described methods, is formed so that a plurality of adjoining fins **20**F are connected by the silicon germanium layer **210**.

[**0102**] As described above, according to the second embodiment, in the same manner as in the first embodiment, while improving the mobility of carriers, the abnormal growth of suicide and the generation of junction leakage current can be suppressed.

[**0103**] Also according to the second embodiment, in the same manner as in the first embodiment, the silicon germanium layer **210** can be evenly formed from the upper portion to the bottom portion, and thereby, the mobility of carriers can be improved evenly from the upper portion to the bottom portion of the channel region.

[**0104**] Also according to the second embodiment, by connecting a plurality of adjoining fins **20**F by the silicon germanium layer **210**, the parasitic resistance can be further reduced compared with the first embodiment.

[**0105**] Also according to the second embodiment, in the same manner as in the first embodiment, when a part of the fin **20**F in the semiconductor layer **20** is removed, the disappearance of all silicon in the source/drain forming region including the contact plug forming region **20**C can be prevented, and thereby, impossibility of the epitaxial growth of silicon germanium can be avoided.

[**0106**] Further according to the second embodiment, in the same manner as in the first embodiment, since the source/drain region **100** that requires a high-temperature heating step is formed before the source/drain extension region **220**, change in the impurity concentration distribution of the source/drain extension region **220** can be suppressed.

(3) Third Embodiment

[**0107**] FIGS. **19** to **28** illustrate the method for manufacturing a FinFET according to the third embodiment of the present invention. In the case of the third embodiment, an ordinary semiconductor substrate is prepared, and a FinFET is formed on the semiconductor substrate. Here, the same steps as in the first embodiment are implemented on the ordinary semiconductor substrate. The elements same as the elements shown in FIGS. **1** to **10** are denoted by the same numerals and characters, and the description thereof will be omitted.

[**0108**] First, as FIG. **19** shows, an ordinary semiconductor substrate **240** is prepared. After depositing a mask material **30** composed, for example, of silicon nitride film on the semiconductor substrate **240**, the mask material **30** is patterned using lithography or RIE.

[**0109**] Further, the semiconductor substrate **240** is etched to a depth of about 70 nm using the mask material **30** as a mask to form a convex semiconductor layer **260** composed of a fin **260**F and a contact plug forming region **260**C.

[**0110**] After depositing an element isolating insulating film **270** composed for example of a silicon oxide film on the entire surface using high-density plasma (HDP) CVD, the upper surface of the mask material **30** is exposed by planarizing the element isolating insulating film **270** by CMP using the mask material **30** as a stopper. The element isolating insulating film **270** is etched by RIE using the mask material **30** as a mask to reduce the thickness of the element isolating insulating film **270** to about 30 nm.

[**0111**] Thereafter, by implementing steps shown in FIGS. **20** to **28**, which are same as the steps shown in FIGS. **2** to **10** of the first embodiment, a FinFET **280**, which is a PMOSFET, is manufactured.

[**0112**] In the third embodiment, as FIG. **25** shows, when the exposed fin **260**F is removed, the fin **260**F is exposed not only on the first gate electrode sidewalls **80** and the sides of the insulating film **110**, but also on the upper surface of the element isolating insulating film **270**.

[**0113**] In this case, a fin **130** which is higher and wider than the fin **260**F is formed by the epitaxial growth of silicon germanium by vapor-phase growth or solid-phase growth using the fin **260**F exposed on the first gate electrode sidewalls **80** and the sides of the insulating film **110**, and the upper surface of the element isolating insulating film **270** as the seed.

[**0114**] At this time, if the fin **260**F is etched so that the upper surface of the fin **260**F is ten-odd nanometers lower than the upper surface of the element isolating insulating film **270**, a silicon germanium can be formed evenly from the upper portion to the bottom of the fin **130**.

[**0115**] As described above, according to the third embodiment, in the same manner as in the first embodiment, while improving the mobility of carriers, the abnormal growth of silicide can be suppressed and the generation of junction leakage current can be suppressed.

[**0116**] Also according to the third embodiment, in the same manner as in the first embodiment, a silicon germanium can be formed evenly from the upper portion to the bottom of the fin **130**, and thereby, the mobility of carriers can be improved evenly from the upper portion to the bottom of the channel region.

[**0117**] Also according to the third embodiment, in the same manner as in the first embodiment, parasitic resistance can be reduced by forming a fin **130** higher and wider than the fin **260**F.

[**0118**] Also according to the third embodiment, in the same manner as in the first embodiment, the complete disappearance of silicon in the source/drain forming region including the contact plug forming region **260**C can be prevented when a part of the fin **260**F of the semiconductor

layer **260** is removed, and thereby, the impossibility of epitaxial growth of silicon germanium can be avoided.

[**0119**] Further according to the third embodiment, in the same manner as in the first embodiment, since the source/drain region **100** that requires a high-temperature heating step is formed before the formation of the source/drain extension region **140**, change in the impurity concentration distribution of the source/drain extension region **140** can be suppressed.

(4) Fourth Embodiment

[**0120**] FIGS. **29** to **33** illustrate the method for manufacturing a FinFET according to the fourth embodiment of the present invention. Since the steps of FIGS. **19** and **20** of the third embodiment are identical to the steps in the fourth embodiment, the description thereof will be omitted.

[**0121**] In the structure shown in FIG. **29**, by the ion implantation of an impurity, such as boron (B), into the fin **260**F before forming the second gate electrode sidewalls **90**, a source/drain extension region (not shown) having a shallow junction depth in the lateral direction in FIG. **29** and a sharp impurity concentration distribution is formed on the fin **260**F.

[**0122**] Then, after depositing a second gate electrode sidewall material on the entire surface, the second gate electrode sidewall material is etched by RIE to form second gate electrode sidewalls **90** on the sides of the first gate electrode sidewalls **80**.

[**0123**] At this time, the mask material **30** formed on the source/drain forming region where a source/drain region will be subsequently formed is removed, and the thickness of the mask material **60** formed on the gate electrode **70** is made to be about 50 nm.

[**0124**] As FIG. **30** shows, the exposed semiconductor layer **260** (source/drain forming region consisting of the contact plug forming region **260**C and a part of the fin **260**F) is etched off by RIE.

[**0125**] At this time, as FIG. **31** shows, if the semiconductor layer is etched so that the upper surface of the semiconductor **260** is ten-odd nanometers lower than the upper surface of the element isolating insulating film **270**, a silicon germanium layer can be formed evenly from the upper portion to the bottom of the fin **260**F.

[**0126**] As FIG. **32** shows, by vapor-phase growth or solid-phase growth, a silicon germanium layer **290** is formed by the epitaxial growth of silicon germanium using the semiconductor layer **260** exposed on the sides of the second gate electrode sidewalls **90** and the upper surface of the element isolating insulating film **270** as seeds.

[**0127**] Thereafter, by the ion implantation into the silicon germanium layer **290**, the source/drain region **300** having a deep junction depth in the lateral direction in FIG. **32** is formed on the silicon germanium layer **290**.

[**0128**] As FIG. **33** shows, in the same manner as in the first embodiment, by sequentially forming the interlayer insulating film **150** and contact plugs **160** and performing a wiring step, a FinFET **310**, that is a PMOSFET, is manufactured.

[**0129**] As described above, according to the fourth embodiment, the mobility of carriers can be improved.

[**0130**] Also according to the fourth embodiment, in the same manner as in the first embodiment, a silicon germanium layer **290** can be formed evenly from the upper portion to the bottom of the fin **260**F, and thereby, the mobility of carriers can be improved evenly from the upper portion to the bottom of the channel region.

[**0131**] Also according to the fourth embodiment, in the same manner as in the first embodiment, parasitic resistance can be reduced by forming the silicon germanium layer **290** higher and wider than the fin **260**F.

[**0132**] Also according to the fourth embodiment, even if the exposed semiconductor layer **260** (source/drain forming region consisting of the contact plug forming region **260**C and a part of the fin **260**F) is removed, silicon germanium can be epitaxially grown using the semiconductor layer **260** exposed on the sides of the second gate electrode sidewalls **90** and the upper surface of the element isolating insulating film **270** as seeds.

[**0133**] The above-described embodiments are examples, and do not limit the present invention. For example, by the epitaxial growth of silicon carbide (SiC) in place of silicon germanium, an NMOSFET can be formed as a FinFET.

What is claimed is:

**1**. A semiconductor device comprising:

convex semiconductor layers formed on a semiconductor substrate via an insulating film;

gate electrodes formed on a pair of facing sides of the semiconductor layers via a gate insulating film;

a channel region formed of silicon between the gate electrodes in the semiconductor layers;

a source extension region and a drain extension region formed of silicon germanium or silicon carbon on both sides of the channel region in the semiconductor layers; and

a source region formed of silicon so as to adjoin to the opposite side of the channel region in the source extension region, and a drain region formed of silicon so as to adjoin to the opposite side of the channel region in the drain extension region in the semiconductor layers.

**2**. The semiconductor device according to claim 1, wherein the semiconductor layers are formed so that the surface of the source extension region and the drain extension region is located outside the surface of the channel region.

**3**. The semiconductor device according to claim 1, wherein the source extension region and the drain extension region are formed of the silicon germanium or the silicon carbon evenly from the upper portion to the bottom portion of the semiconductor layers.

**4**. The semiconductor device according to claim 1, wherein the semiconductor layers have a plurality of fins in each of which the channel region, the source extension region and the drain extension region is formed, and

the plurality of fins are formed so as to be connected by the silicon germanium or silicon carbon.

5. The semiconductor device according to claim 1, wherein the semiconductor layers are formed on the semiconductor substrate so as to be connected to the semiconductor substrate and to penetrate the insulating film.

6. The semiconductor device according to claim 5, wherein the silicon germanium or the silicon carbon is formed to a location lower than the upper surface of the insulating film.

7. The semiconductor device according to claim 1, wherein the source region and the drain region are formed of the silicon germanium or the silicon carbon.

8. A method for manufacturing a semiconductor device comprising:

depositing a mask material on a first semiconductor layer formed of silicon on a semiconductor substrate via a buried insulating film, and patterning the mask material and the first semiconductor layer, to form a first semiconductor layer having a convex shape;

forming gate insulating films on a pair of facing sides of the semiconductor layer;

depositing a gate electrode material on the buried insulating film, the gate insulating films, and the mask material, and pattering the gate electrode material, to form a gate electrode on the pair of facing sides and the upper surface of the first semiconductor layer via the gate insulating films and the mask material;

forming gate electrode sidewalls on the sides of the gate electrode, and removing the mask material formed on the first semiconductor layer and not coated by the gate electrode and the gate electrode sidewalls;

forming a source region and a drain region by the ion implantation of a predetermined impurity into the first semiconductor layer using the gate electrode and the gate electrode sidewalls as masks;

forming an insulating film on the buried insulating film, the first semiconductor layer, the gate electrode, and the gate electrode sidewalls;

forming a mask having a pattern wherein the upper surfaces of the gate electrode sidewalls are opened on the insulating film;

exposing a part of the first semiconductor layer by etching the insulating film and the gate electrode sidewalls using the mask;

removing the mask, and etching off the exposed first semiconductor layer;

forming a second semiconductor layer composed of silicon germanium or silicon carbide on the removed region; and

forming a source extension region and a drain extension region by the ion implantation of a predetermined impurity into the second semiconductor layer using the gate electrode and the insulating film as masks.

9. The method for manufacturing a semiconductor device according to claim 8, wherein the second semiconductor layer is formed so that the surface of the second semiconductor layer is positioned outside the surface of the first semiconductor layer.

10. The method for manufacturing a semiconductor device according to claim 8, wherein the second semiconductor layer is formed by the epitaxial growth of the silicon germanium or the silicon carbide using vapor-phase growth or solid-phase growth using the sidewall of the first semiconductor layer exposed on the sidewalls of the insulating film as seeds.

11. The method for manufacturing a semiconductor device according to claim 8, wherein the first semiconductor layer is formed so as to have a plurality of fins.

12. The method for manufacturing a semiconductor device according to claim 11, wherein the second semiconductor layer is formed so as to connect the plurality of fins.

13. A method for manufacturing a semiconductor device comprising:

depositing a mask material on a first semiconductor layer formed of silicon on a semiconductor substrate via a buried insulating film, and patterning the mask material and the first semiconductor layer, to form a first semiconductor layer having a convex shape;

forming gate insulating films on a pair of facing sides of the first semiconductor layer;

depositing a gate electrode material on the buried insulating film, the gate insulating films, and the mask material, and pattering the gate electrode material, to form a gate electrode on the pair of facing sides and the upper surface of the first semiconductor layer via the gate insulating films and the mask material;

forming gate electrode sidewalls on the sides of the gate electrode, and removing the mask material formed on the first semiconductor layer and not coated by the gate electrode and the gate electrode sidewalls;

forming a source region and a drain region by the ion implantation of a predetermined impurity into the first semiconductor layer using the gate electrode and the gate electrode sidewalls as masks;

forming an insulating film on the buried insulating film, the first semiconductor layer, the gate electrode, and the gate electrode sidewalls;

planarizing the insulating film, and selectively removing the gate electrode sidewalls by wet etching to expose a part of the first semiconductor layer;

removing the mask, and etching off the exposed first semiconductor layer;

forming a second semiconductor layer composed of silicon germanium or silicon carbide on the removed region; and

forming a source extension region and a drain extension region by the ion implantation of a predetermined impurity into the second semiconductor layer using the gate electrode and the insulating film as masks.

14. The method for manufacturing a semiconductor device according to claim 13, wherein the gate electrode sidewalls which has a higher etching rate than the etching rate of the insulating film is formed.

15. The method for manufacturing a semiconductor device according to claim 14, wherein when a part of the first semiconductor layer is exposed, the gate electrode sidewalls are selectively removed by wet etching using hot phosphoric acid.

**16**. The method for manufacturing a semiconductor device according to claim 13, wherein the second semiconductor layer is formed so that the surface of the second semiconductor layer is positioned outside the surface of the first semiconductor layer.

**17**. The method for manufacturing a semiconductor device according to claim 13, wherein the second semiconductor layer is formed by the epitaxial growth of the silicon germanium or the silicon carbide using vapor-phase growth or solid-phase growth using the sidewall of the first semiconductor layer exposed on the sidewalls of the insulating film as seeds.

**18**. The method for manufacturing a semiconductor device according to claim 13, wherein the first semiconductor layer is formed so as to have a plurality of fins.

**19**. The method for manufacturing a semiconductor device according to claim 18, wherein the second semiconductor layer is formed so as to connect the plurality of fins.

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