FORM 1

609284

SPRUSON & FERGUSON

COMMONWEALTH OF AUSTRALIA

PATENTS ACT 1952

APPLICATION FOR A STANDARD PATENT

NEC Corporation, incorporated in Japan, of 33-1, Shiba 5-chome, Minato-ku, Tokyo 108, JAPAN, hereby apply for the grant of a standard patent for an invention entitled:

Data Processing Apparatus

which is described in the accompanying complete specification.

Details of basic application(s):-

Basic Applic. No:	Country:	Application Date:
100249/'88	JP	25 April 1988

PATENT SUB OFFICE
19 APR 1989
SYDNEY

The address for service is:-

Spruson & Ferguson
Patent Attorneys
Level 33 St Martins Tower
31 Market Street
Sydney New South Wales Australia

DATED this NINETEENTH day of APRIL 1989

NEC Corporation

By:

Registered Patent Attorney

TO: THE COMMISSIONER OF PATENTS
OUR REF: 93394
S&F CODE: 64259

ACCEPTED AND AMENDMENTS
ALLOWED 25-11-91

5845/3

prùson & Ferguson

AUSTRALIA
CONVENTION
STANDARD
& PETTY PATENT
DECLARATION
SFP4

COMMONWEALTH OF AUSTRALIA

THE PATENTS ACT 1952

DECLARATION IN SUPPORT OF A CONVENTION APPLICATION FOR A PATENT

In support of the Convention Application made for a patent for an invention entitled:

Title of Invention: Data Processing Apparatus

I/~~We~~ Susumu Uchihara

Full name(s) and address(es) of Declarant(s): ~~of~~ c/o NEC Corporation of 33-1, Shiba 5-chome, Minato-ku, Tokyo, Japan

do solemnly and sincerely declare as follows:–

Full name(s) of Applicant(s): ~~I am/We are the applicant(s) for the patent~~

(or, in the case of an application by a body corporate)

1. I am/~~We are~~ authorised by NEC CORPORATION

the applicant(s) for the patent to make this declaration on its/~~their~~ behalf.

2. The basic application(s) as defined by Section 141 of the Act was/~~were~~ made

Basic Country(ies): in Japan

Priority Date(s): on the 25th April, 1988

Basic Applicant(s): by NEC CORPORATION

Full name(s) and address(es) of inventor(s): ~~I am/We are the actual inventor(s) of the convention referred to in the basic application(s)~~

(or where a person other than the inventor is the applicant)

3. HIROTAKA NAKANO

~~of~~ c/o NEC Corporation of 33-1, Shiba 5-chome, Minato-ku, Tokyo, Japan

~~(respectively)~~,

is/~~are~~ the actual inventor(s) of the invention and the facts upon which the applicant(s) is/~~are~~ entitled to make the application are as follows:

Set out how Applicant(s) derive title from actual inventor(s) e.g. The Applicant(s) is/are the assignee(s) of the invention from the inventor(s)

The said applicant is the assignee of the actual inventor.

4. The basic application(s) referred to in paragraph 2 of this Declaration was/~~were~~ the first application(s) made in a Convention country in respect of the invention(s) the subject of the application.

Declared at Tokyo, Japan this 23rd day of March, 1989.

NEC CORPORATION

Susumu Uchihara

Signature of Declarant(s)

Susumu Uchihara
General Manager, Patents Division

P4

To: The Commissioner of Patents

11/81

(12) PATENT ABRIDGMENT (11) Document No. AU-B-33191/89
(19) AUSTRALIAN PATENT OFFICE (10) Acceptance No. 609284

(54) Title
COUNTING INSTRUCTIONS EXECUTED IN A DATA PROCESSING SYSTEM

International Patent Classification(s)
(51)[4] **G06F 009/32**
(51)[5] **G06F 009/06 G06F 011/34**

(21) Application No. : **33191/89** (22) Application Date : **19.04.89**

(30) Priority Data

(31) Number (32) Date (33) Country
63-100249 **25.04.88** **JP JAPAN**

(43) Publication Date : **26.10.89**

(44) Publication Date of Accepted Application : **26.04.91**

(71) Applicant(s)
NEC CORPORATION

(72) Inventor(s)
HIROTAKA NAKANO

(74) Attorney or Agent
SPRUSON & FERGUSON, GPO Box 3898, SYDNEY NSW 2001

(56) Prior Art Documents
EP 205122

(57) Claim

1. A data processing apparatus including segment and page descriptors as a control structure for realizing a logical address, comprising:

a step counter to be incremented or decremented every time a machine instruction is executed; and

count control means for causing said step counter to count or stop counting in accordance with data in said segment or page descriptor of a segment or page in which a machine instruction to be executed is present.

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S & F Ref: 93394

FORM 10

COMMONWEALTH OF AUSTRALIA

PATENTS ACT 1952

COMPLETE SPECIFICATION

(ORIGINAL)

FOR OFFICE USE:

Class Int Class

Complete Specification Lodged:
Accepted:
Published:

Priority:

Related Art:

Name and Address of Applicant:

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33-1, Shiba 5-chome
Minato-ku
Tokyo 108
JAPAN

Address for Service:

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Sydney, New South Wales, 2000, Australia

Complete Specification for the invention entitled:

Data Processing Apparatus

The following statement is a full description of this invention, including the best method of performing it known to me/us

Abstract of the Disclosure

A data processing apparatus includes segment and page descriptors as a control structure for realizing a logical address, a step counter, and a count control means. The step counter is incremented or decremented every time a machine instruction is executed. The count control means causes the step counter to count or stop counting in accordance with data in the segment or page descriptor of a segment or page in which a machine instruction to be executed is present.

Background of the Invention

The present invention relates to count control of a step counter for a data processing apparatus.

Recently, as the application field of digital computers has been greatly extended, users' demands for functions have been diversified. Consequently, operating systems for software have become very complicated. For this reason, structural analysis of an operating system cannot be performed only by desk work. As a means for performing this structural analysis, a step counter for counting a dynamic execution number of machine instructions is sometimes incorporated in a data processing apparatus.

In such a conventional data processing apparatus, a step counter counts machine instructions in units of processes. However, since a program for software generally has a hierarchical structure using subroutines, when minute analysis such as structural analysis of a specific subroutine is to be performed, a count control instruction for causing a step counter to count or stop counting is inserted in the program for software in advance.

Since the above-described conventional step counter counts machine instructions in units of processes, when minute structural analysis is to be performed, a count

control instruction for causing a step counter to count or stop counting must be inserted in a program for software in advance. Therefore, the conventional step counter has poor flexibility, and the processing speed is decreased.

Summary of the Invention

The present invention has been made in consideration of the above situation, and has as its object to provide a data processing apparatus which can flexibly specify an object to be measured without degrading the performance of the apparatus.

In order to achieve the above object, there is provided a data processing apparatus including segment and page descriptors as a control structure for realizing a logical address, comprising a step counter to be incremented or decremented every time a machine instruction is executed, and count control means for causing the step counter to count or stop counting in accordance with data in the segment or page descriptor of a segment or page in which a machine instruction to be executed is present.

Brief Description of the Drawing

Fig. 1 is a block diagram showing an arrangement of a data processing apparatus according to an embodiment of the present invention.

Detailed Description of the Preferred Embodiment

Fig. 1 shows an arrangement of a data processing apparatus according to an embodiment of the present invention. Referring to Fig. 1, reference numeral 1 denotes

a logical address, 2, a segment descriptor; 3, a page descriptor; 4, a physical space; 5, a TLB (Translation Look-aside Buffer); 6, a flip-flop (F/F); 7, an AND gate; and 8, a step counter (STPC).

The data processing apparatus of this embodiment comprises the segment and page descriptors 2 and 3 as a control structure for realizing the logical address 1. Count control data 21 for causing the step counter 8 to count or stop counting is included in the segment descriptor 2.

Translation of the logical address 1 into a physical address is performed by an address translating section of the data processing apparatus through the control structure constituted by a "table" consisting of the segment and page descriptors 2 and 3 and the like which are present in a main storage. The TLB 5 is arranged in the apparatus in order to perform this translation at high speed.

The data 21 in the segment descriptor 2 is count control data for causing the step counter 8 to count or stop counting, and is stored in the TLB 5 as data 51. When program read is performed in response to a program read signal a, the data 51 is stored in the flip-flop 6 and is supplied to the AND gate 7 as one input data b. When a machine instruction start signal c is supplied to the AND gate 7, if data stored in the flip-flop 6 is "ON" data, the step counter 8 is incremented or decremented. If the stored data is "OFF" data, incrementation or decrementation of the

step counter 8 is not performed. Count control of the step counter 8 is performed by data in the segment descriptor 2 in this manner.

In this embodiment, count control data for causing the step counter 8 to count or stopping counting is present in the segment descriptor 2. However, the present invention can be equally applied to a case wherein this data is present in the page descriptor 3.

As has been described above, according to the present invention, count control for causing a step counter (which is incremented or decremented every time a machine instruction is executed) to count or stop counting is performed by using data in a segment or page descriptor. Therefore, an object to be measured can be flexibly specified, and the present invention can be easily used for, e.g., structural analysis of an operating system without degrading the performance of the apparatus.

~~What is claimed is:~~
The claims defining the invention are as follows:

1. A data processing apparatus including segment and page descriptors as a control structure for realizing a logical address, comprising:

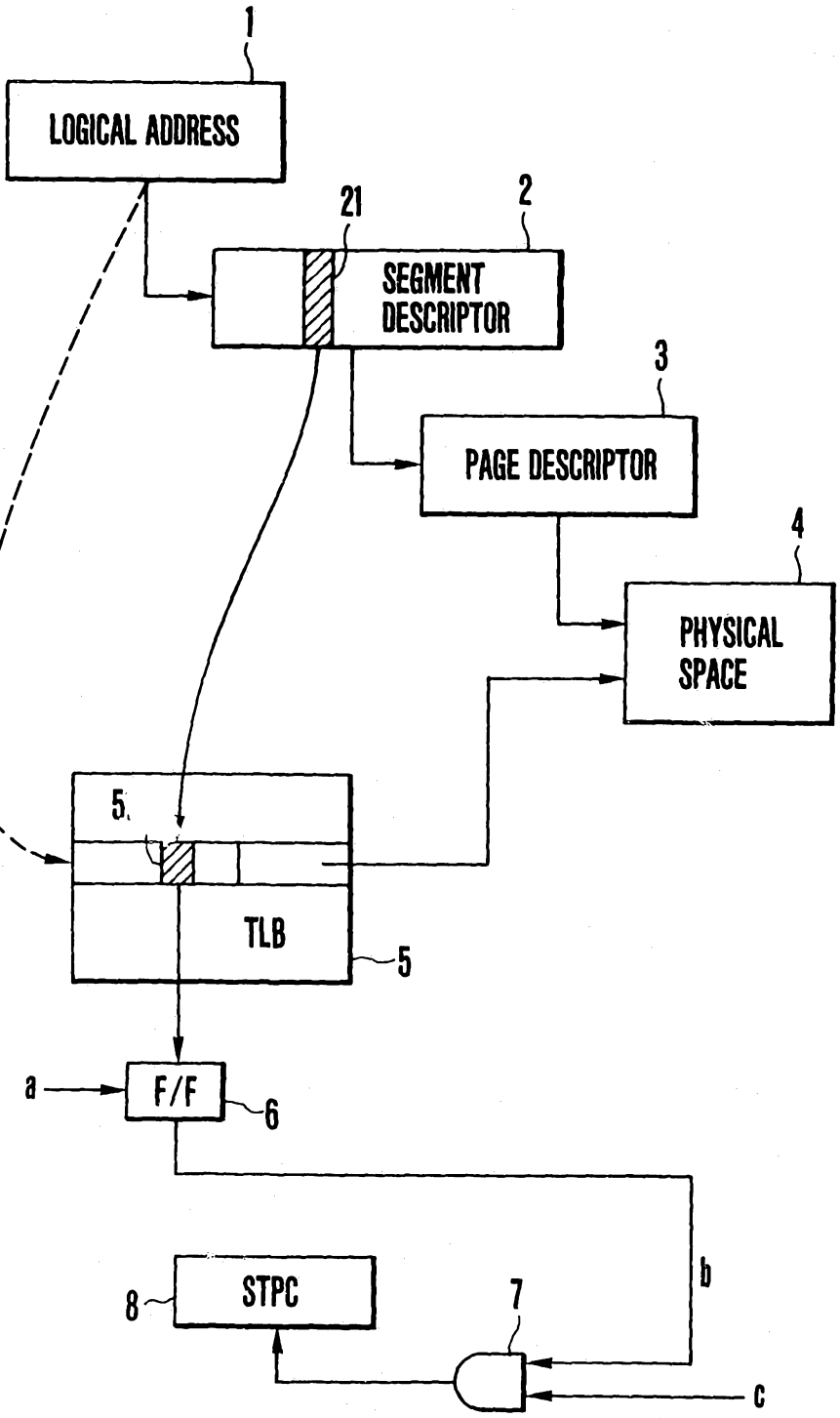
a step counter to be incremented or decremented every time a machine instruction is executed; and

count control means for causing said step counter to count or stop counting in accordance with data in said segment or page descriptor of a segment or page in which a machine instruction to be executed is present.

DATED this EIGHTEENTH day of APRIL 1989

NEC Corporation

Patent Attorneys for the Applicant
SPRUSON & FERGUSON


1
LOGICAL ADDRESS
21
2
SEGMENT DESCRIPTOR
3
PAGE DESCRIPTOR
4
PHYSICAL SPACE
5
TLB
5
a
F/F
6
b
8
STPC
7
c