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(72) Inventors MUTSUO SUGAWARA KEIJI NAMIMOTO

(54) POWER SUPPLY CONTROL IN A MEMORY SYSTEM

(71) We, TOKYO SHIBAURA ELECTRIC COMPANY LIMITED, a Japanese corporation, of 72 Horikawa-cho, Saiwai-ku, Kawasaki-shi, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement: —

The present invention relates to power supply control in a memory system in which a power supply voltage for the read/write operation is applied only to a selected memory chip in which the read/write operation is to be executed.

Generally, one type of memory unit includes at least one chip of random access memory (RAM) and/or read only memory (ROM). When in use, the power is always supplied to the memory chips or chips of the memory unit. Such power is used, for example, for sustaining the information stored in the memory and for enabling the read/write operation with the related memory.

By convention, the power is constantly, supplied to the memory chip or chips when the memory unit is used, thus resulting in superfluous power consumption. In the case where the stored data is kept in the memory for a long time, a counter measure taken in the past for such a problem is to stop the power supply for the read/write operation in the case of a RAM, or to stop all the power supply to the memory chip in the case of a ROM.

However, this countermeasure brings about poor results of power consumption reduction. It is for this reason that most of the power in the memory unit is consumed in the read/write operation with the related memory chip or chips. Accordingly, the conventional way for the power consumption reduction is ineffective in the case of frequent repetition of the read/write operations. In this specification, the term read/write operation is defined as follows. That is, the read/write operation means a read operation for reading out data from a memory and/or a write operation for writing data into the memory. The symbol V_D means not only a read/write power terminal but read/write power as well.

Another object of the present invention ns to provide a memory system in which power is supplied to the memory chip selected for the read and write operation execution only when the read and write operations are executed.

Accordingly, the primary object of the present invention is to provide a memory system having a power supply control system for controlling the power supply to the memory.

Another object of the present invention is to provide a memory system in which the power necessary for a read/write operation is supplied when data is read and written from and into the memory, thereby resulting in a great reduction of power consumption.

Still another object of the present invention is to provide a memory system having a power supply control system for a memory unit having a plurality of memory chips in which the power is supplied only to the memory chip selected for the read/write operation to be executed.

According to the present invention, there is provided a memory system comprising a semiconductor memory chip having an address terminal to which an address signal is applied to designate a memory location, a data terminal to which is applied a data signal which is written into the designated memory location or is read out of the designated memory location, a chip enable terminal to which is applied a chip enable signal during which a read operation or write operation is executed, a memory con-

tent holding power supply terminal to which a power supply voltage is applied to hold memorized contents of said memory chip and a read/write power supply terminal to which a power supply voltage necessary for read/write operation is applied; a power supply connected to said memory content holding power supply terminal of said memory chip; application means for applying an address signal and a chip enable signal to said address terminal and said chip enable terminal of said memory chip, respectively, to initiate a read or write cycle of said memory chip; and coupling means responsive to initiation of said read or write cycle of said memory chip to couple said power supply to said read/write power supply terminal of said memory chip during a predetermined period of time in said read or write cycle.

The invention will now be described, by way of example, with reference to the accompanying drawings, in which: —

Fig. 1 shows a block diagram of a circuit for illustrating the principle of a power supply control system used in the present invention;

Fig. 2 shows a block diagram of a computer system into which an embodiment of the memory system of the present invention is incorporated;

Fig. 3 is a circuit diagram of the memory control unit in the Fig. 2 system;

Fig. 4A is a circuit diagram of the power control unit of the Fig. 2 system;

Fig. 4B is a circuit diagram of a modification of the power control unit of the Fig. 2 system;

Fig. 5A is a time-chart for explaining the operations of the power supply control system of Fig. 2;

Fig. 5B is a time-chart for explaining the operations of the power supply control system when the power control unit of Fig. 4B is used;

Fig. 6 shows a block diagram of another embodiment of the memory system of the present invention;

Fig. 7 is a circuit diagram of the memory control unit and the power control unit of the Fig. 6 system;

Fig. 8 is a time-chart for explaining the operations of the power supply control system of Fig. 6;

Fig. 9 is a block diagram of a part of the power supply memory system which is another embodiment of the present invention;

Fig. 10 is a block diagram of the power supply control system employing an n-channel MOS-IC memory chip;

Fig. 11 is a block diagram of a system using a read only memory into which the memory system of the present invention is incorporated;

Fig. 12 is a power supply control circuit circuit using both a random access memory and a read only memory;

Fig. 13 is a block diagram of still another embodiment of the memory system of the present invention;

Fig. 14 is a circuit diagram of the memory control unit and power control unit of Fig. 12; and

Fig. 15 is a time-chart for explaining the operations of the Fig. 12 system.

Referring now to Fig. 1, there is shown a circuit diagram useful in explaining the principle of a power supply control system used in the present invention. In this circuit, a memory chip 11 is comprised of a random access memory (RAM) of P channel MOS-IC (metal oxide semiconductor integrated circuit) type. The power terminal at the source side (common power terminal) of the memory chip 11, is designated by V_{SS}, and the power terminals at the drain side thereof are designated by V_D and V_{DD}. The terminal V_D is used for read or write, while the terminal V_{DD} is used for memory sustaining. To these terminals, V_{SS}, V_D and V_{DD}, power is supplied from a power source 12, having the polarity as shown in the figure. A power control unit 13 includes a high speed bipolar type transistor Q. In the read/write operations for reading and writing the data from and into the memory chip 11, the power control unit 13, upon receipt of a control signal, permits electric power from the power source 12 to be supplied to the read/write power terminal V_D. The memory chip 11 further includes a read/write data terminal D, an address terminal A, a read/write terminal W, and a chip enable terminal C. Write data is applied to the read/write data terminal D. The read data read out of the memory chip 11 is delivered to a data line 14 via the terminal D. Thet address terminal A receives a read/write address selection signal via an address line 15. The read/write address selection signal is used to designate any one of the memory locations of the memory chip 11. To the read/write terminal W a read/write instruction signal is applied for designating the data write instruction or the data read instruction, via an instruction line 16. The chip enable terminal C receives a chip enable signal enabling the read or write operation of the memory chip 11 via a chip enable line 17 for performing the chip selection.

Incidentally, when the memory chip 11 is a read only memory (ROM), the read/write control line is unnecessary so that it is omitted. In this specification, the power source necessary for the read/write operation means the read-out or write-in power source required for the read or write operation.

When no control signal is applied to the base of the transistor Q of the power control unit 13, the transistor Q is turned OFF, with the result that the read/write power terminal V_D is disconnected from the power line V_2. Therefore, the memory chip 11 fails to execute the read/write operation. On the contrary, when the control signal is applied to the base of the transistor Q, the transistor Q is turned ON so that the read/write power terminal V_D of the memory chip 11 is connected with the power line V_2. The result is that the read/write operaitons are executed.

Turning now to Fig. 2, there is shown a computer system using the power supply control circuit of Fig. 1. This is the case where the read/write operation of a RAM comprising memory chips 11_1 and 11_3 is controlled by the power supply control circuit. More than two memory chips may be used for the memory. In Fig. 2, like reference numbers are used to designate like components in Fig. 1.

In Fig. 2, the processor 18 is known in the computer field. Upon receipt of an operation mode instruction the processor 18 issues first and second data transfer control signals C_1 and C_2 of the same level but different in pulse width as will be referred to in Fig. 5. The processor 18 also receives the program instruction or data fed from an input/output unit or a memory unit (not shown), through a bus 19 and an interface bus 20. On the basis of this information, the processor 18 executes an ordinary arithmetic logic operation and then transfers the result of the calculation again to the bus 19 through the interface bus 20. The operation mode instruction includes, for example, the commands of machine run and machine halt. The processor 18 feeds data transfer control signals C_1 and C_2 to the memory control unit 21. Upon receipt of signals C_1 and C_2 and an address signal fed from the address line 22, the memory control unit 21 feeds commonly to the memory chips 11_1 and 11_2 various signals necessary for the read/write operation, a signal for designating the address in either one of the memory chips 11_1 and 11_2 (an address lower part), a chip enable signal enabling the memory chips and a read/write signal for designating the read or write operation mode. The memory control unit 21 delivers only an address upper part for selecting one of the memory chips 11_1 and 11_2 in the address signals fed through the address line 23, to the power control unit 13.

Fig. 3 is a circuit diagram of the memory control unit 21. The memory control unit 21 is comprised of an exclusive OR gate 211, an inverter 212, an AND gate 213 and an address register 214. The exclusive OR gate 211 receives the first and second data transfer control signals C1 and C2 and outputs the chip enable signal. The inverter 212 inverts the first data transfer control signal C1. The AND gate 213 is ANDed by the output of the inverter 212 and the second data transfer control signal C2 and outputs the read/write signal. The address register 214 stores the address signal fed through the address line 22 therein at the rising edge of the first data transfer control signal C1, and outputs the address signal (for example, consisting of 12 bits) in the divided fashion; an upper part signal of 5 bits, for example, and a lower part signal of 7 bits, for example. The address lower part signal is applied to address terminal A of each of the memory chips 11_1 and 11_2. The address upper part signal is applied to the power control unit 13, via the address line 23. A chip enable signal $\overline{CE}$ is fed to the chip enable terminals C of the respective memory chips.

In response to the first and second data transfer control signals C1 and C2, the power control unit 13 selects the first or second memory chip 11_1 or 11_2 to permit the power necessary for the read and write operation to be fed from the power source 12 to the selected memory chip, via the power lines 24 and 25 respectively.

Fig. 4A illustrates in detail the circuit of the power control unit 13. The power control unit 13 includes an OR gate 131, an address decoder 132, an AND gate 133, an AND gate 134, and first and second high speed bipolar transistors 135 and 136. The OR gate 131 ORs the first and second data transfer control signals C1 and C2. The address decoder 132 receives an address upper part signal for memory chip selection fed through the address line 23 from the memory control unit 21, and decodes the address upper part signal to produce first and second decode signals D1 and D2 corresponding to the first and second memory chips 11_1 and 11_2. The first AND gate 133 is ANDed by the first decode signal D1 and the output of the OR gate 131. The second AND gate 134 is ANDed by the second decode signal D2 and the OR gate 131 output. The bipolar transistors 135 and 136 are provided corresponding to the first and second AND gates and the memory chips 11_1 and 11_2 respectively. With such an arrangement, these transistors control the power supply for the read and write operations to the corresponding memory chips. As shown, the output of the AND gate 133 is fed to the base of the transistor 135, while the output of the AND gate 134 is fed to the base of the transistor 136. The emitters of these transistors 135 and 136 are connected commonly to a common terminal V2 of the power source 12. The

output of the first transistor 135 is connected to the read/write power terminal V_D of the first memory chip 11_1 through the power line 24, while the output of the second transistor 136 is connected to the read/write power terminal V_D of the second memory chip 11_2 via the power line 25. The respective power terminals V_{DD} and V_{SS} of the memory chips 11_1 and 11_2 are coupled commonly with the corresponding terminals of the power source 12.

Reference will be made to FIG. 5A illustrating a set of timing diagrams useful in explaining the operations of the power supply control system shown in Fig. 2. Upon depression of a key, an operator mode instruction for the machine run is given to the processor 18. Then the processor 18 issues the first and second data transfer control signals C1 and C2 of which the levels are equal and the pulse width are different, as shown in Figs. 5A(a) and (b). The data transfer of read or write is made between the respective memory chips 11_1 and 11_2 and the processor 18 is controlled by the first and second data transfer control signals C1 and C2. As shown in Fig. 5A(c), the bus 19 receives an address information ADDRESS for designating the read and write addresses of the memory chip and a data information DATA for read and write data from and into the memory chip.

The memory control unit 21 receives the data transfer control signals C1 and C2 shown in Figs. 5A(a) and (b) and only the ADDRESS signal of the ADDRESS and DATA signals shown in Fig. 5A (c), and then issues designating signals necessary for the read/write operations of the respective memory chips. In the memory control unit shown in Fig. 3, the first and second data transfer control signals C1 and C2 are inputted into the exclusive OR gate 211 which in turn outputs the chip enable signals (Fig. 5A(f)) enabling the memory chip to be operable only during the time period where the read and write operations are executed. In Fig. 5A(f) the chip enable signal is labelled as an inverted chip enable signal $\overline{CE}$. The first data transfer control signal C1 is inverted in the inverter 212 and then fed to one of the input terminals of the AND gate 213. The second data transfer control signal C2 is fed to the other input terminal of the AND gate 213. Thus, the AND gate 213 outputs the read/write signal as shown in Fig. 5A(e) for designating the read operation or write operation. For addressing the memory chip, the ADDRESS signal of, for example, 12 bits is set in the address register 214 at the rising edge of the first data transfer cotnrol signal C1, as shown in Fig. 5A(d). The lower significant bits of, for example, 7 bits of the address register 214 are applied as the address lower part signal to the chips, while the upper significant bits of, for example, 5 bits are applied as the address upper part signal to the power control unit 13. The address lower part signal is used to designate the address in the memory chip and the address upper part signal for selecting the memory chip.

At the rising edges of the control signals C1 and C2, i.e. at the time when these signals rise from the logical level "0" to "1", the address signal exists on the bus 19. When the first control signal C1 is "1" and the second control signal C2 is "0", i.e. during the periods of time, T1 and T3, the read operation in which the data is read from the memory chips to the processor 18 is executed. During the period of time T2 when the first control signal C1 is "0" and the second control signal C2 is "1", the data is written into the memory chips from the processor 18.

It is noted that the first and second data transfer control signals C1 and C2 rise from the logical level "0" to "1" substantially at the same time, and no read and write operation is executed when the control signals are both in "0" level. The read/write signal W designates the write operation only when the first control signal C1 is "0" and the second control signal C2 is "1". The chip enable signal $\overline{CE}$ is fed to all the memory chips.

On the other hand, the power control unit 13 receives the address upper part signal from the memory control unit 21 and decodes it in the decoder 132. The decoder 132 outputs the first decode signal D1 when the address upper part signal designates the memory chip 11_1, and outputs the second decode signal D2 when the address upper part signal designates the memory chip 11_2. The decode signals D1 and D2 are ANDed by the AND gates 133 and 134, respectively, together with the output of the OR gate 131 which receives the first and second control signals C1 and C2. The outputs of the AND gates 133 and 134 are applied to the bases of the first and second transistors 135 and 136. By this application, the transistors 135 and 136 are conductive with the result that the transistor 135 permits the voltage V2 of the power source 12 to be applied to the read/write power terminal V_D of the memory chip 11_1, while the transistor 136 permits the voltage V2 of the power source 12 to be applied to the read/write power terminal V_D of the memory chip 11_2.

In Fig. 5A, the time period t1 to t2 indicates the read cycle of the memory chip 11_1, the time period t2 to t3 indicates the write cycle of the memory chip 11_1 and the time period t3 to t4 the read cycle

of the memory chip 11_2. Accordingly, during the period t1 to t3, the memory chip 11_1 is selected and, as shown in Fig. 5A(g), the power is applied to the power terminal V_D of the memory chip 11_1 only during the shadowed periods. During the period t3 to t4, the memory chip 11_2 is selected and, as shown in Fig. 5A(a), the power is applied to the power terminal V_D of the memory chip 11_2 oniy during the shadowed period. When both the control signals C1 and C2 are "0", no voltage is applied to the power terminals V_D of the memory chips 11_1 and 11_2. In the above mentioned embodiment of the present invention, one of the features of the power supply control system resides in that, through the operation of the power control unit 13, the memory chip corresponding to the address information is selected and supplied with the power for read/write operations to the selected memory chip, and another feature is that the power is not applied when the control signals C1 and C2 are both "0" during the read/write cycle of the selected memory chip. Therefore, power consumption of the memory unit is greatly reduced.

The power control unit 13 shown in Fig. 2 may be constructed as the circuit shown in Fig. 4B. As seen from the figure, OR gate 131 and AND gate 133 and 134 are removed from the circuit of Fig. 4A. The address upper part signal through the address line 23 is applied to the address decoder 132 where it is decoded and the address decoder produces predetermined decode signals D1 or D2. Each decode signal makes the transistor to be selected conductive thereby to supply the power to the memory chip selected for read/write operation.

Fig. 5B is a set of timing charts for explaining the operation of the power control system using the power control unit of Fig. 4B. As shown in Figs. 5B(g) and (h), when the memory chip 11_1 is selected, the power is applied to the memory chip 11_1, while, when the memory chip 11_2 is selected, the power is applied to the memory chip 11_2. In other words, the power supply control system using the power control unit shown in Fig. 4B supplies the power to only the memory chip selected in the memory unit having a plurality of memory chips, the power being necessary for the read and write operation.

Referring now to Fig. 6, there is shown a computer system using another embodiment of the necessary system according to the present invention. In the figure, like numbers are used to designate like portions in Fig. 2, of which the explanation will be omitted. The first difference of the example from the Fig. 2 embodiment is that the memory control unit 21 issues the first and second chip enable signals $\overline{CE}1$ and $\overline{CE}2$ which in turn are applied to the first and second memory chips 11_1 and 11_2 via the first and second chip enable lines 26 and 27, thereby selecting the memory chip for which the read/write operation is to be performed. The second difference is that the power control unit 13 permits the read/write power from the power source 12 to be applied commonly to the read/write power terminals V_D of the memory chips 11_1 and 11_2, through the power line 28.

Fig. 7 shows a detail of the memory control unit 21 and the power control unit 13 shown in Fig. 6. As shown in Fig. 7, the memory control unit 21 is comprised of an address register 214, an address decoder 215, a timing pulse generator 216, first and second NAND gate circuits 217 and 218, an inverter 212, and an AND gate 213. The address register 214 stores a signal for designating the address of the memory chip at the rising edge of the first data transfer control signal C1 and produces the address lower part signal for designating the address of the memory chip and the address upper part signal for selecting a memory chip. The address decoder 215 decodes the address upper part signal fed from the address register 214 and produces the first and second decode signals D1 and D2 corresponding to the memory chips 11_1 and 11_2. The timing pulse generator 216 receives the first and second data transfer control signals C1 and C2 and generates timing pulses for designating the timing of the chip enabling signal generation. The first and second NAND gates 217 and 218 are connected respectively to the first and second decode signals D1 and D2 together with the timing pulses from the timing pulse generator 216 to produce the chip enable signals $\overline{CE}1$ and $\overline{CE}2$ corresponding to the memory chips 11_1 and 11_2. The inverter 212 inverts the first data transfer control signal C1. The AND gate 213 makes the logical product of the output of the inverter 212 and the second data transfer control signal C2 to produce the read/write signal.

The power control unit 13 comprises an OR gate 131 connected to receive the first and second data transfer control signals C1 and C2, and a high speed bipolar transistor 137, responsive to the output of the OR gate 131, for supplying the voltage necessary for the read/write operation from the power source 12 commonly to the respective memory chips 11_1 and 11_2.

Fig. 8 is a set of timing charts for illustrating the operation of the power supply control system of Fig. 6. The period t1 to t2 corresponds to the read cycle of the memory chip 11_1, the time period t2 to t3

to the write cycle of the memory chip 11_1, and the time period t3 to t4 to the read cycle of the memory chip 11_2. The address signal fed via the address line 22 is stored in the address register 214. The upper significant bits (address upper part) of the address register 214 is decoded in the decoder 215 to produce either decode signal D1 or D2. Assuming now that the decoder 215 produces the decode signal D1, the decode signal D1 is fed to the NAND gate 217, and NAND gate 217 is enabled when it receives the timing pulse from the timing pulse generator 216, and then the NAND gate 217 produces the chip enable signal $\overline{CE1}$ as shown in Fig. 8(f). The chip enable signal $\overline{CE1}$ is applied to the memory chip 11_1 through the first chip enable line 26, with result that the memory chip 11_1 is conditioned operable. On the other hand, in the power control unit 13, the transistor 137 is made conductive by the first and second data transfer control signals C1 and C2 through the OR gate 131. As a result, the voltage V2 from the power source 12 is applied commonly to the memory chips 11_1 and 11_2 through the power line 28 only during the period of time when the logical sum of the control signals C1 and C2 is "1" (the shadowed portion of Fig. 8(h)). Accordingly, during the period T1, the data is read out from the memory chip 11_1 addressed to be transferred to the bus 19 through the data line 14. During the period T2, since the read/write signal is "1" as shown in Fig. 8(e), the data from the processor 18 is loaded into the memory chip 11_1 addressed, through the bus 19. During the period T3, since the chip enable signal $\overline{CE2}$ is produced as shown in Fig. 8(g), the data is read out of the memory chip 11_2. As shown in Fig. 8(h), the read/write power V_D is supplied from the power source 12 to the memory chips 11_1 and 11_2 only during the shadowed portions, i.e. when the first and second data transfer control signals C1 and C2 are "1". Consequently, in the power supply control system in Fig. 6, no power is supplied to the memory chip when the read/write operation is not performed in the read/write cycle of the memory chip with the result that the power consumption is considerably reduced.

While the examples of Figs. 2 and 6 use two memory chips, similar power supply control is applied to the power supply control system with one or three or more memory chips by using the power lines or the chip enabling lines corresponding to the number of memory chips used. In this case, if the bit number of one chip is less than the bit number of each word of the memory, the bit number of the memory may be increased by connecting a plurality of memory chips in parallel, as shown in Fig. 9. In this case, the power line 25 is connected to the memory chips 11_1, and the power line 24 is connected to the memory chips 11_2. In this way, as in the previous case, the power supply control may be performed to each triplet of memory chips.

Turning now to Fig. 10, there is shown another example of an embodiment of the present invention in which the memory chip of N channel MOS-IC is used. In this case, inversion of the polarity of the power source 12 and the conductivity type of transistor 13 is needed for obtaining the same power supply control. While a RAM is used in the above-mentioned examples, a ROM may also be used for the power supply control system of the present invention. The programmable read only memory (PROM) also may be used likewise. The example using the ROM is shown in Fig. 11. In the cases using the ROM and PROM, the data holding power source V_{DD} is unnecessary; however, when the data is read out of the memory chip, the read-out power V_D is necessary. Thus, as in the previous cases, the power supply control may be performed by the power control unit 13. As shown in Fig. 12, the present invention is applicable to the memory unit including RAM and ROM. The memory may be arranged with at least one memory unit including a plurality of memory chips.

The power control unit is not limited to the circuits shown in Figs. 2 and 6, but may be constituted by the circuit comprising transistor transistor logic (TTL).

The high speed bipolar transistor circuit so used in the power control unit 13 is such that, in a high speed read/write operation, connection or disconnection of the power V_D may be made smoothly. The power control circuit is not limited to such bipolar transistor circuit, if the circuit is operable at a high speed. The data transfer control signals C1 and C2 shown in Figs. 2 and 6 may be substituted by the address designating signal ADR, the read signal READ, and the write signal WRITE each with a different frequency, as shown in Fig. 13. In the figure, like reference numerals designate like parts in the previous cases. The processor 18 produces the address designating signal ADR and the read/write signal. The memory control unit 21 and the power control unit 13 may be constructed by the circuit as shown in Fig. 14. The timing charts of this circuit are shown in Fig. 15. As shown in Fig. 15(a), when the ADR signal is "1", the address information from the processor 18 appears on the bus 19. As shown in Fig. 15(b), when the read signal is "1", the memory chip

11_1 delivers the read data on the bus 19. When the write signal is "1" as shown in Fig. 14(c), the processor 18 outputs the write data on the bus 19. If both the address designating signal and the read/write signal are present, the power for the read/write operation is supplied to the memory chip selected by the address designating signal.

WHAT WE CLAIM IS:—

1. A memory system comprising a semiconductor memory chip having an address terminal to which an address signal is applied to designate a memory location, a data terminal to which is applied a data signal which is written into the designated memory location or is read out of the designated memory location, a chip enable terminal to which is applied a chip enable signal during which a read operation or write operation is executed, a memory content holding power supply terminal to which a power supply voltage is applied to hold memorized contents of said memory chip and a read/write power supply terminal to which a power supply voltage necessary for read/write operation is applied; a power supply connected to said memory content holding power supply terminal of said memory chip; application means for applying an address signal and a chip enable signal to said address terminal and said chip enable terminal of said memory chip, respectively, to initiate a read or write cycle of said memory chip; and coupling means responsive to initiation of said read or write cycle of said memory chip to couple said power supply to said read/write power supply terminal of said memory chip during a predetermined period of time in said read or write cycle.

2. A memory system as claimed in Claim 1, in which said memory chip as a Mos-IC chip.

3. A memory system as claimed in Claim 1 or Claims 2, in which said memory chip includes a random access memory.

4. A memory system as claimed in Claim 1 or Claim 2, in which said memory chip includes a read only memory.

5. A memory system as claimed in any preceding Claim, in which said coupling means comprises a high-speed bi-polar transistor.

6. A memory system as claimed in any preceding Claim, further comprising processor means for producing first and second data transfer control signals, each taking successively a first voltage level and a second voltage level and specifying a first memory addressing state in which the first and second control signals are at the first voltage level, a second read/write operation execution state in which one of the first and second control signals is at the first voltage level and the other is at the second voltage level and a third idle state in which the first and second control signals are at the second voltage level, said states following in succession during the read or write cycle.

7. A memory system as claimed in Claim 6, wherein said application means are responsive to the first state of the first and second control signals to apply the first part of a received address signal to the address terminal of said memory chip and responsive to the second state of the control signals to apply the chip enable signal and the read/write control signal respectively to the chin enable terminal and the read/write control terminal of said memory chip.

8. A memory system as claimed in Claim 7, wherein said coupling means are actuated by the first and second states of the first and second control signals and the second part signal of said received address signal only during the first and second states of the first and second control signals.

9. A memory system as claimed in Claim 7, wherein said coupling means are actuated by the second part signal of said received address signal during the first, second and third states of the control signals during a read or write cycle.

10. A memory system as claimed in Claim 7, wherein said coupling means are actuated by the first and second states of first and second control signals.

11. A memory system as claimed in any preceding Claim, wherein at least one further similar memory chip is provided.

12. A memory system substantially as hereinbefore described, with reference to the accompanying drawing.

MARKS & CLERK.

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1574058 COMPLETE SPECIFICATION
15 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1

FIG. 1

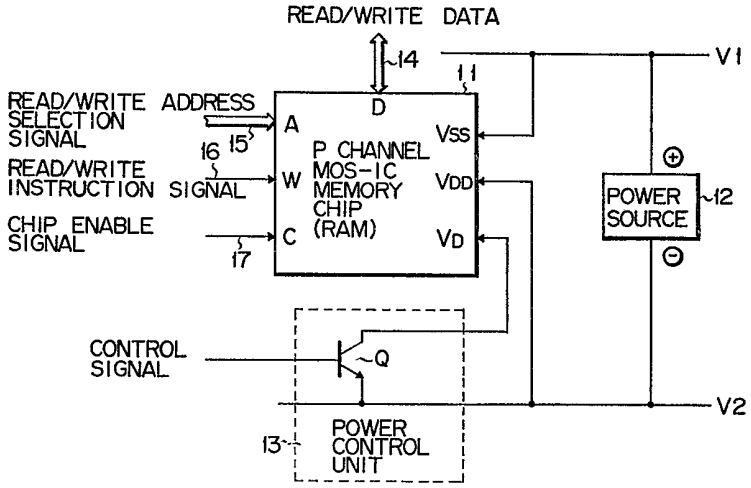
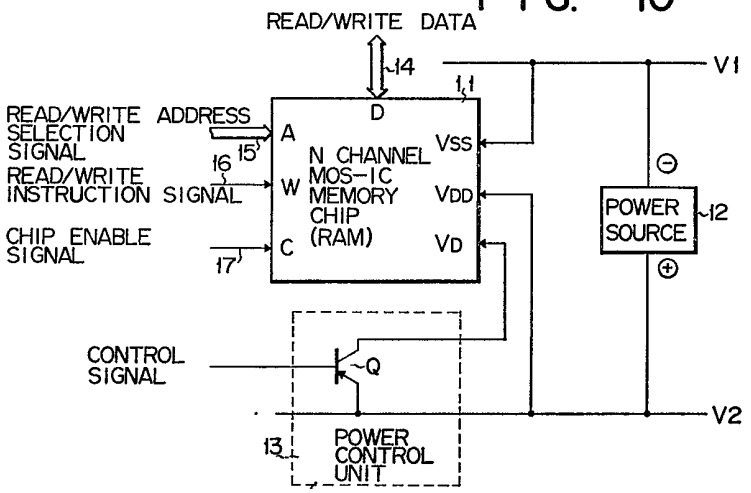


FIG. 10



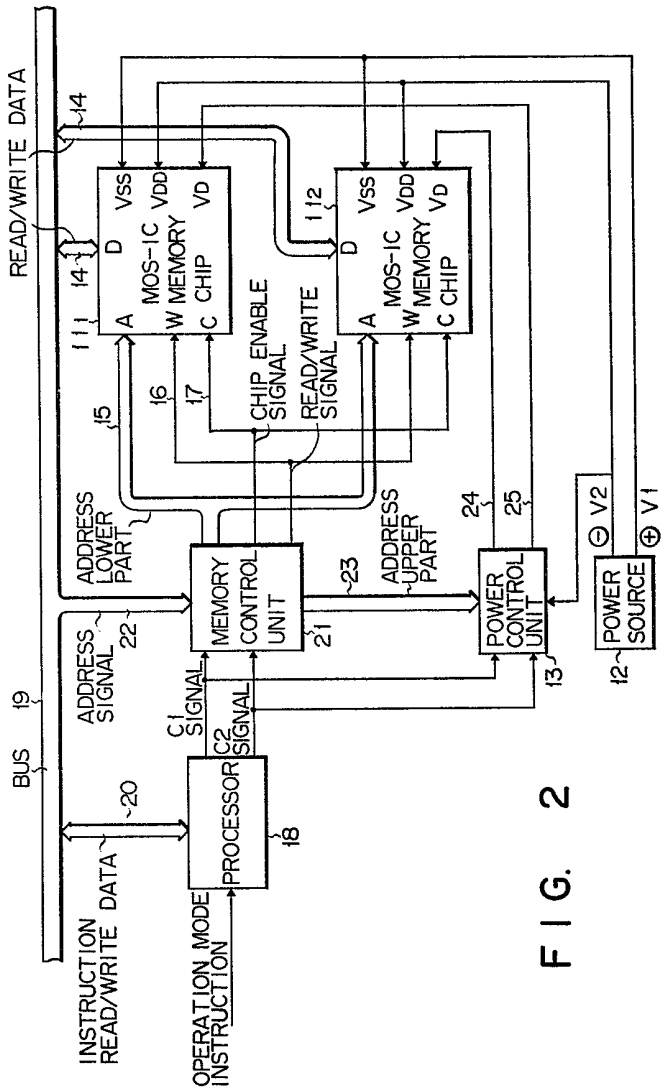

READ/WRITE DATA
14
MOS-IC MEMORY CHIP
D
A
W
C
VSS
VDD
VD
111
112
14-1
CHIP ENABLE SIGNAL
READ/WRITE SIGNAL
15
16
17
ADDRESS LOWER PART
ADDRESS UPPER PART
MEMORY CONTROL UNIT
21
22
23
POWER CONTROL UNIT
24
25
13
POWER SOURCE
12
⊖ V2
⊕ V1
BUS
19
ADDRESS SIGNAL
C1 SIGNAL
C2 SIGNAL
PROCESSOR
18
20
INSTRUCTION READ/WRITE DATA
OPERATION MODE INSTRUCTION

FIG. 2

FIG. 3

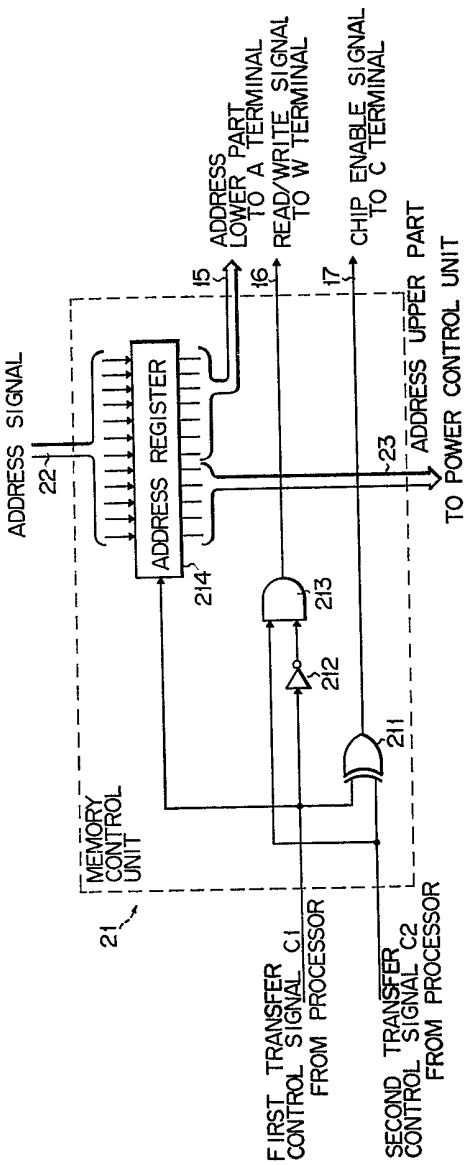

ADDRESS SIGNAL
22
ADDRESS REGISTER
214
MEMORY CONTROL UNIT
21
15
ADDRESS LOWER PART TO A TERMINAL
16
READ/WRITE SIGNAL TO W TERMINAL
17
CHIP ENABLE SIGNAL TO C TERMINAL
23
ADDRESS UPPER PART TO POWER CONTROL UNIT
213
212
211
FIRST TRANSFER CONTROL SIGNAL C1 FROM PROCESSOR
SECOND TRANSFER CONTROL SIGNAL C2 FROM PROCESSOR

FIG. 4A

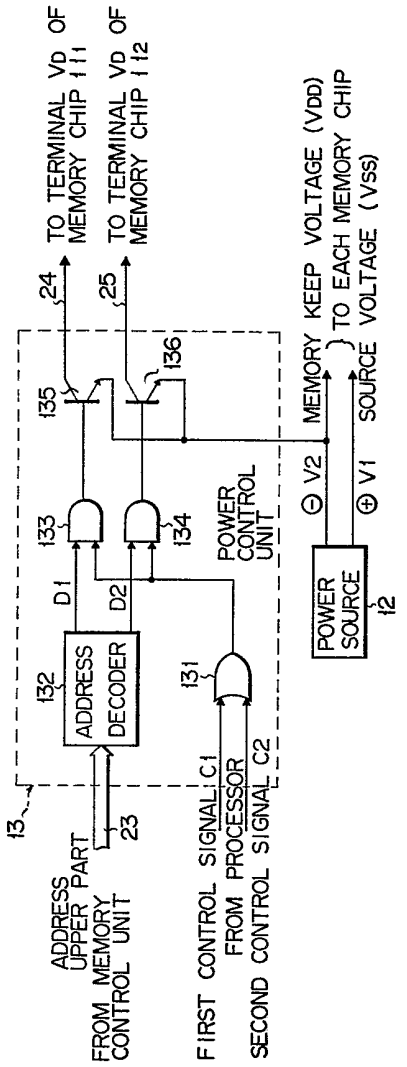
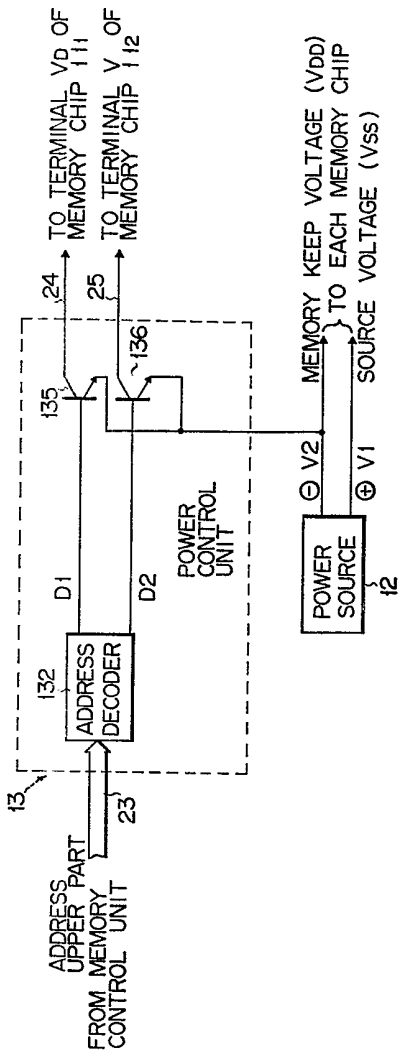

TO TERMINAL VD OF MEMORY CHIP 111
TO TERMINAL VD OF MEMORY CHIP 112
24
25
135
136
133
134
D1
D2
132
ADDRESS DECODER
131
POWER CONTROL UNIT
13
23
ADDRESS UPPER PART FROM MEMORY CONTROL UNIT
FIRST CONTROL SIGNAL C1 FROM PROCESSOR
SECOND CONTROL SIGNAL C2
⊖ V2 MEMORY KEEP VOLTAGE (VDD)
TO EACH MEMORY CHIP
⊕ V1 SOURCE VOLTAGE (VSS)
POWER SOURCE
12

FIG. 4B


TO TERMINAL VD OF MEMORY CHIP 111
TO TERMINAL V OF MEMORY CHIP 112
MEMORY KEEP VOLTAGE (VDD) TO EACH MEMORY CHIP
SOURCE VOLTAGE (Vss)
24
25
136
135
V2
V1
POWER SOURCE
12
POWER CONTROL UNIT
D1
D2
132
ADDRESS DECODER
13
23
ADDRESS UPPER PART FROM MEMORY CONTROL UNIT

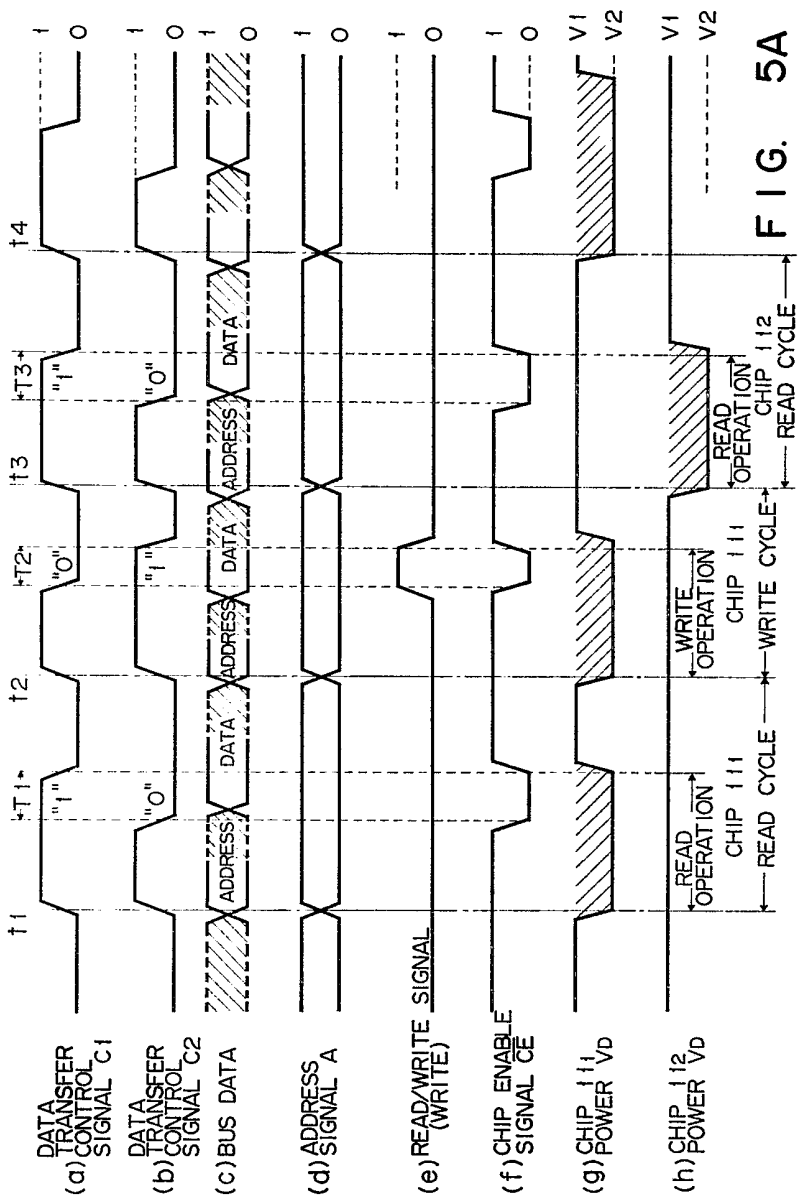

t1
T1
t2
T2
t3
T3
t4
"1"
"0"
ADDRESS
DATA
(a) DATA TRANSFER CONTROL SIGNAL C1
(b) DATA TRANSFER CONTROL SIGNAL C2
(c) BUS DATA
(d) ADDRESS SIGNAL A
(e) READ/WRITE (WRITE) SIGNAL
(f) CHIP ENABLE SIGNAL CE
(g) CHIP 111 POWER VD
(h) CHIP 112 POWER VD
V1
V2
READ OPERATION CHIP 111
READ CYCLE
WRITE OPERATION CHIP 111
WRITE CYCLE
READ OPERATION CHIP 112
READ CYCLE

FIG. 5A

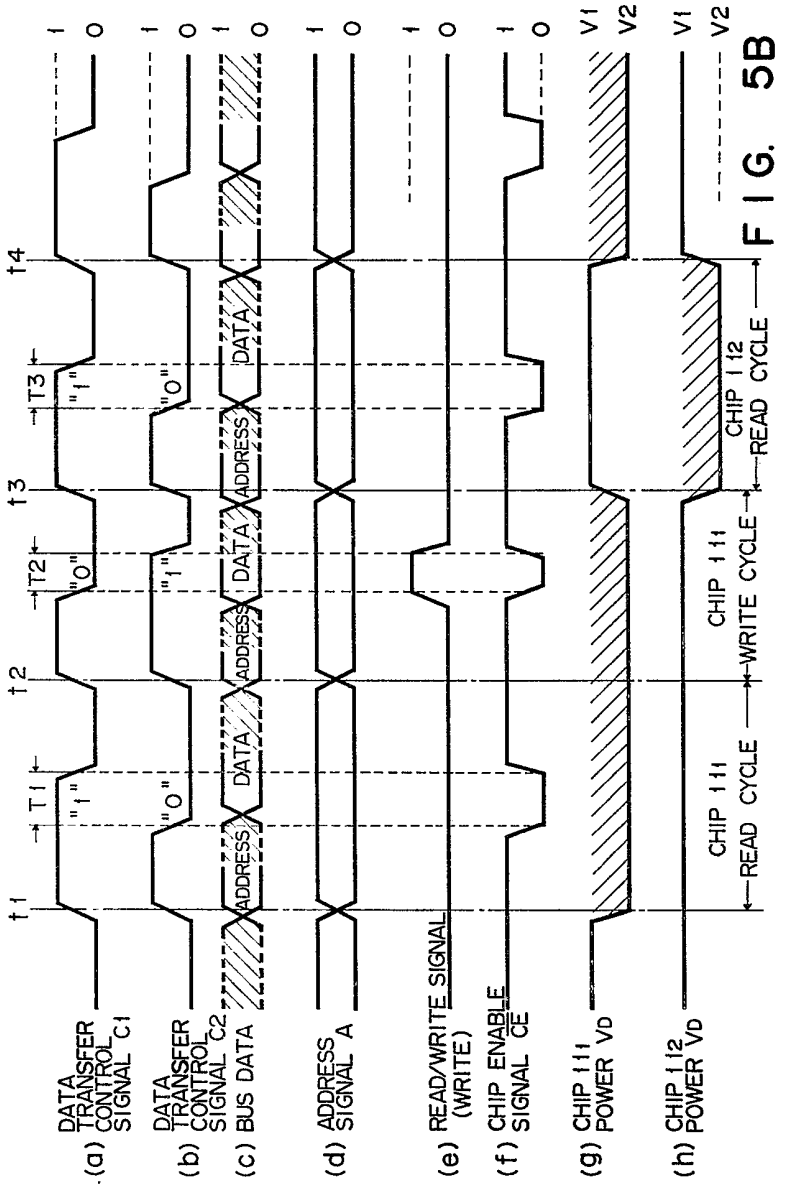

t1
t2
t3
t4
T1
T2
T3
"1"
"0"
DATA
ADDRESS
(a) DATA TRANSFER CONTROL SIGNAL C1
(b) DATA TRANSFER CONTROL SIGNAL C2
(c) BUS DATA
(d) ADDRESS SIGNAL A
(e) READ/WRITE SIGNAL (WRITE)
(f) CHIP ENABLE SIGNAL CE
(g) CHIP 111 POWER VD
(h) CHIP 112 POWER VD
V1
V2
CHIP 111 READ CYCLE
CHIP 111 WRITE CYCLE
CHIP 112 READ CYCLE

FIG. 5B

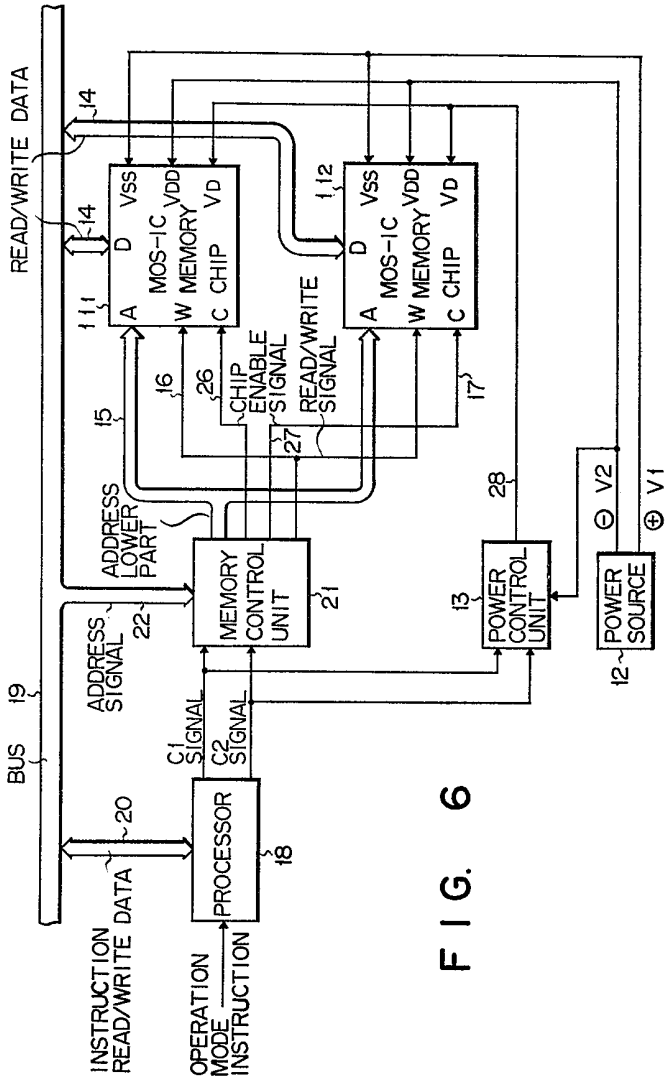
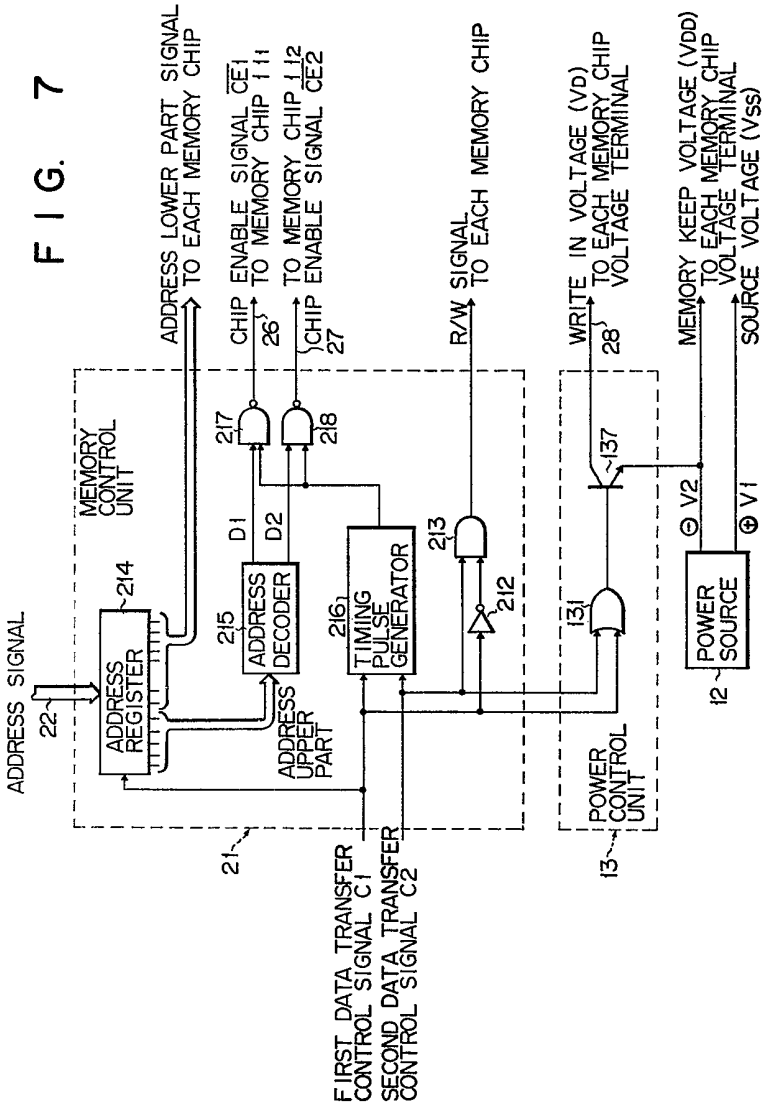

READ/WRITE DATA
14
MOS-IC MEMORY CHIP
D
A
W
C
Vss
VDD
VD
111
112
15
16
17
26
27
CHIP ENABLE SIGNAL
READ/WRITE SIGNAL
ADDRESS LOWER PART
ADDRESS SIGNAL
22
MEMORY CONTROL UNIT
21
28
13
POWER CONTROL UNIT
POWER SOURCE
12
⊖ V2
⊕ V1
BUS
19
C1 SIGNAL
C2 SIGNAL
20
PROCESSOR
18
INSTRUCTION READ/WRITE DATA
OPERATION MODE INSTRUCTION

FIG. 6

FIG. 7


ADDRESS SIGNAL
22
ADDRESS REGISTER
214
MEMORY CONTROL UNIT
ADDRESS LOWER PART SIGNAL TO EACH MEMORY CHIP
CHIP ENABLE SIGNAL CE1 TO MEMORY CHIP 111
26
TO MEMORY CHIP 112 ENABLE SIGNAL CE2
27
217
218
D1
D2
215
ADDRESS DECODER
ADDRESS UPPER PART
216
TIMING PULSE GENERATOR
213
212
R/W SIGNAL TO EACH MEMORY CHIP
WRITE IN VOLTAGE (VD) TO EACH MEMORY CHIP VOLTAGE TERMINAL
28
131
137
POWER CONTROL UNIT
13
MEMORY KEEP VOLTAGE (VDD) TO EACH MEMORY CHIP VOLTAGE TERMINAL
⊖ V2
⊕ V1
SOURCE VOLTAGE (Vss)
POWER SOURCE
12
21
FIRST DATA TRANSFER CONTROL SIGNAL C1
SECOND DATA TRANSFER CONTROL SIGNAL C2

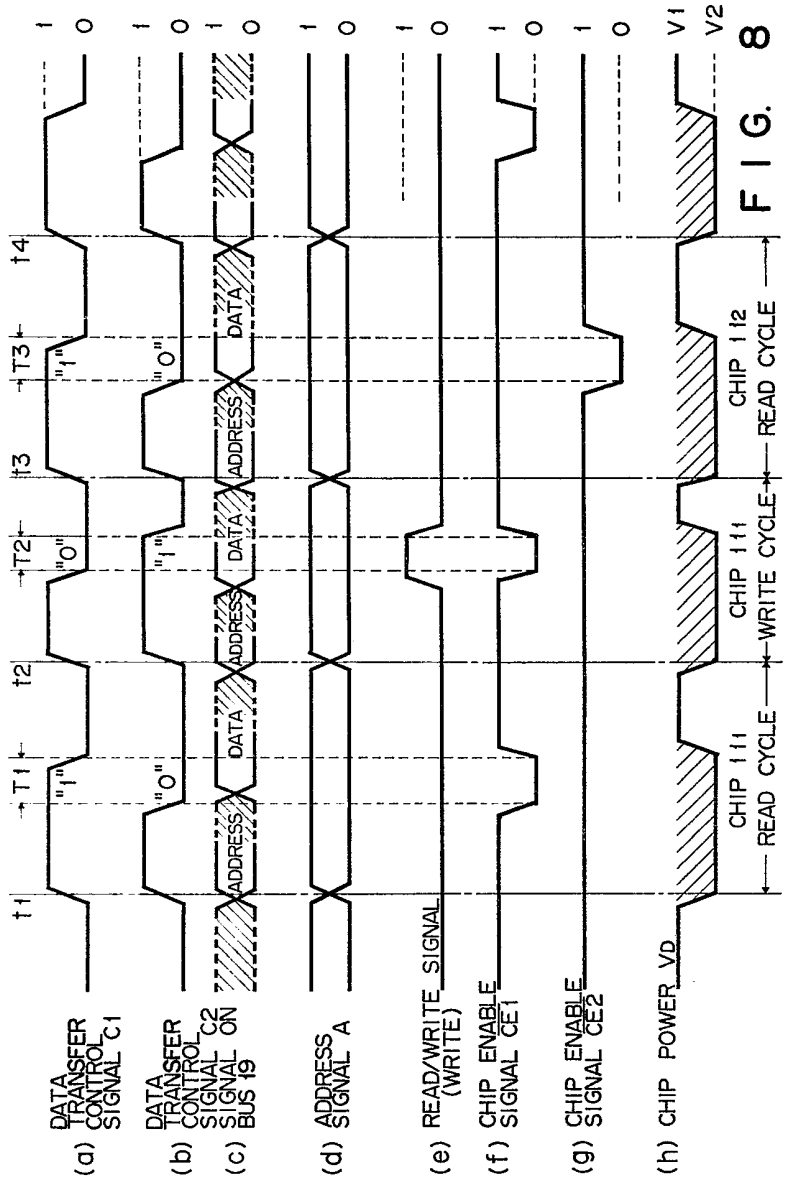

t1
t2
t3
t4
T1
T2
T3
"1"
"0"
ADDRESS
DATA
CHIP 111
READ CYCLE
WRITE CYCLE
CHIP 112
V1
V2
(a) DATA TRANSFER CONTROL SIGNAL C1
(b) DATA TRANSFER CONTROL SIGNAL C2
(c) SIGNAL ON BUS 19
(d) ADDRESS SIGNAL A
(e) READ/WRITE SIGNAL (WRITE)
(f) CHIP ENABLE SIGNAL CE1
(g) CHIP ENABLE SIGNAL CE2
(h) CHIP POWER VD

FIG. 8

FIG. 9

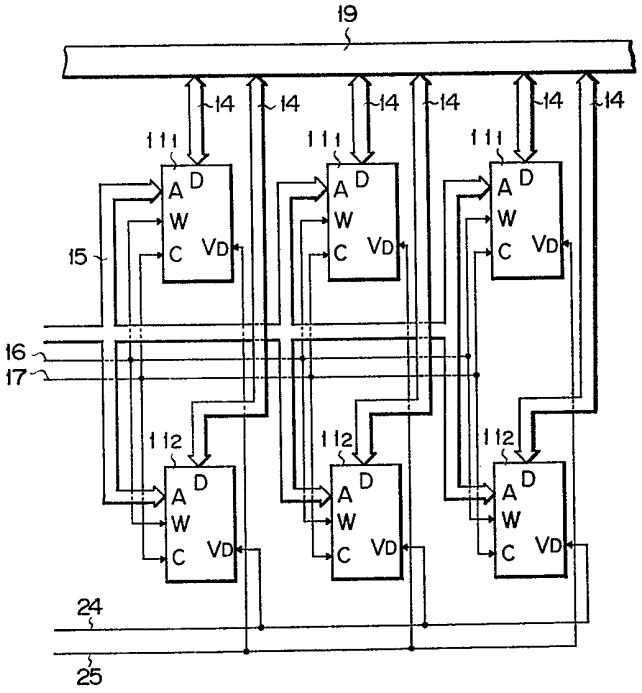


FIG. 11

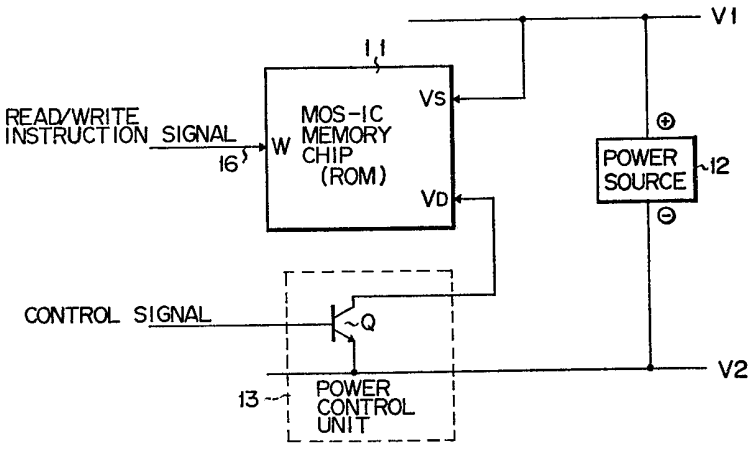
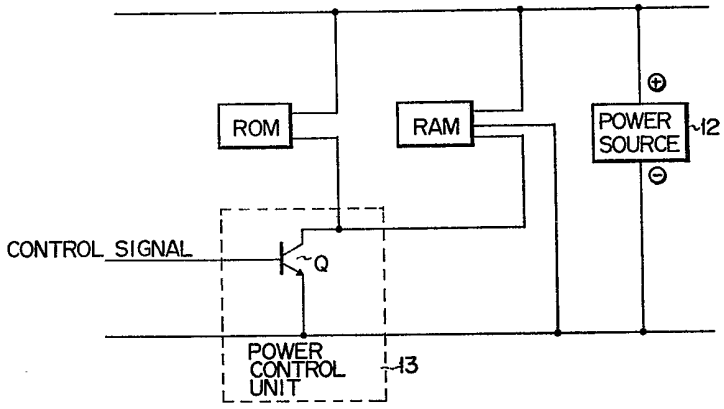

V1
11
READ/WRITE INSTRUCTION SIGNAL
16
W
MOS-IC MEMORY CHIP (ROM)
Vs
VD
POWER SOURCE
12
CONTROL SIGNAL
Q
V2
13
POWER CONTROL UNIT

FIG. 12


ROM
RAM
POWER SOURCE
12
CONTROL SIGNAL
Q
POWER CONTROL UNIT
13

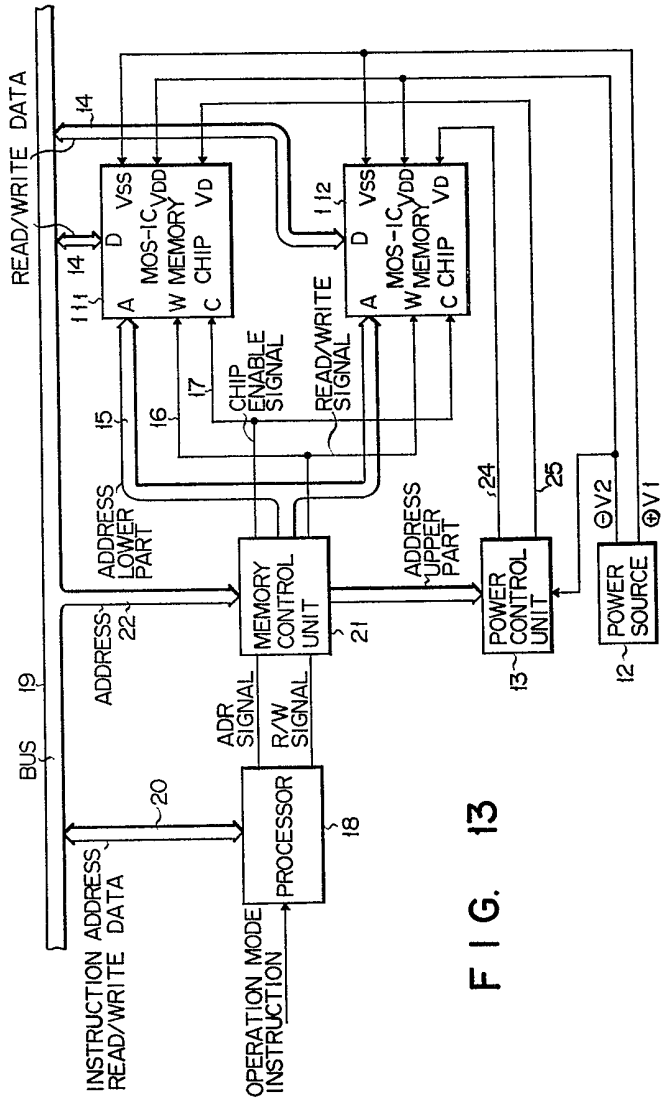

READ/WRITE DATA
14
MOS-IC MEMORY CHIP
D
Vss
VDD
VD
A
W
C
111
112
CHIP ENABLE SIGNAL
READ/WRITE SIGNAL
15
16
17
ADDRESS LOWER PART
ADDRESS UPPER PART
24
25
⊖V2
⊕V1
MEMORY CONTROL UNIT
21
ADDRESS
22
POWER CONTROL UNIT
13
POWER SOURCE
12
BUS
19
ADR SIGNAL
R/W SIGNAL
20
PROCESSOR
18
INSTRUCTION ADDRESS DATA
READ/WRITE
OPERATION MODE INSTRUCTION

FIG. 13

FIG. 14

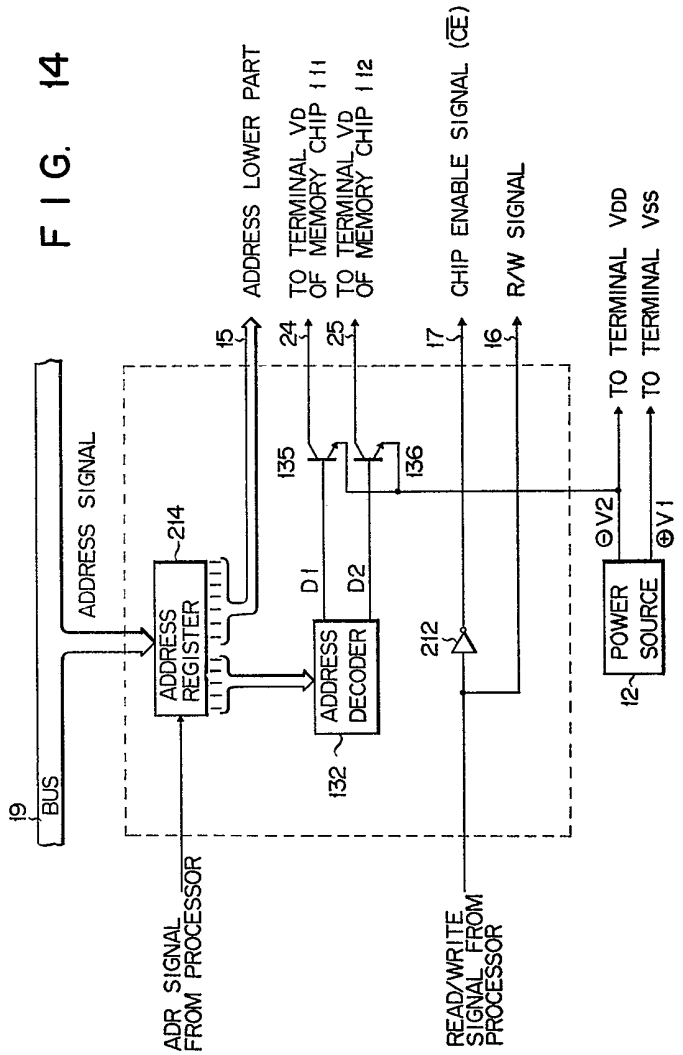
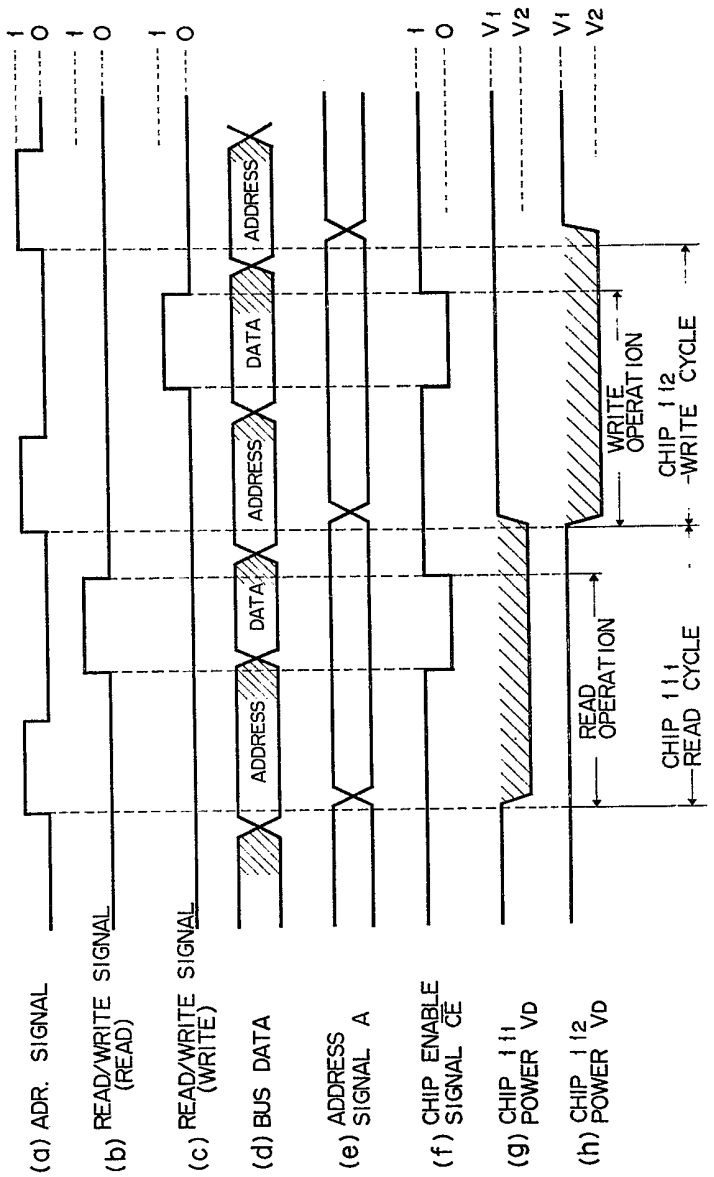

19
BUS
ADDRESS SIGNAL
214
ADDRESS REGISTER
ADDRESS DECODER
132
D1
D2
135
136
212
15
ADDRESS LOWER PART
24
TO TERMINAL VD OF MEMORY CHIP 111
25
TO TERMINAL VD OF MEMORY CHIP 112
17
CHIP ENABLE SIGNAL (CE)
16
R/W SIGNAL
⊖V2
⊕V1
POWER SOURCE
12
TO TERMINAL VDD
TO TERMINAL VSS
ADR SIGNAL FROM PROCESSOR
READ/WRITE SIGNAL FROM PROCESSOR

FIG. 15


(a) ADR. SIGNAL
(b) READ/WRITE SIGNAL (READ)
(c) READ/WRITE SIGNAL (WRITE)
(d) BUS DATA
(e) ADDRESS SIGNAL A
(f) CHIP ENABLE SIGNAL CE
(g) CHIP 111 POWER VD
(h) CHIP 112 POWER VD
1
0
ADDRESS
DATA
V1
V2
READ OPERATION
WRITE OPERATION
CHIP 111 READ CYCLE
CHIP 112 WRITE CYCLE