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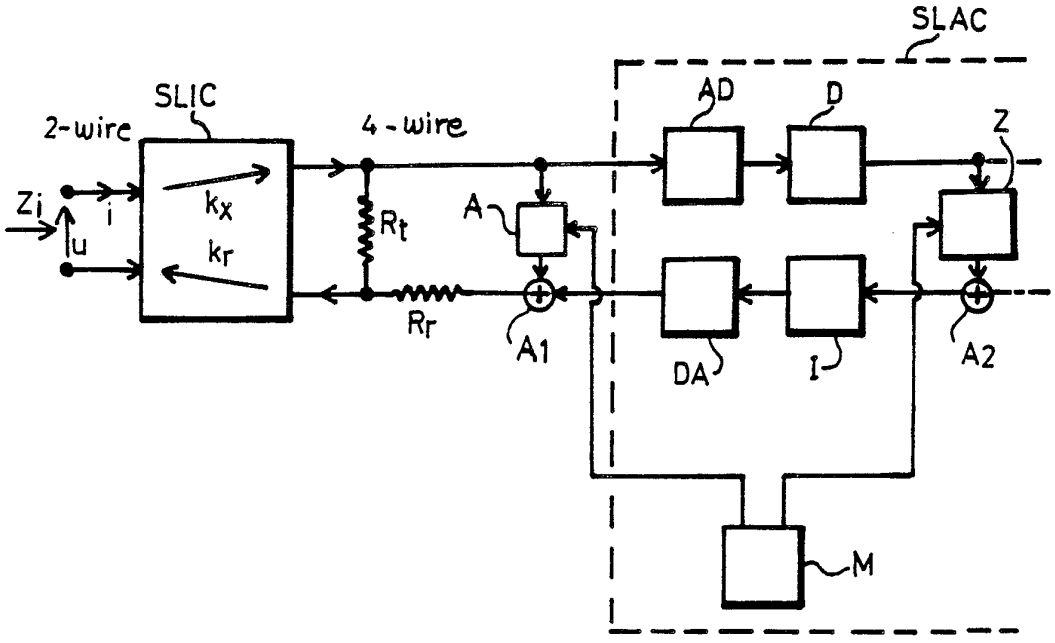
(54) Title: APPARATUS FOR ACHIEVING A CONTROLLABLE LINE TERMINATION IMPEDANCE



(57) Abstract

Circuit apparatus included in a subscriber line circuit for creating a variable line connection impedance for the subscriber line circuit. This comprises a two wire-four wire converter, i.e. a subscriber line interface circuit (SLIC) and a subscriber line audio processing circuit (SLAC). In the latter there is conventionally included a controllable impedance (Z) comprising a digital filter. A resistor (R_T) which can be controllable, or a controllable amplifier (Za) is connected across the four wire side of the SLIC to form the resistive part of the termination impedance (Zi) while the already available digital filter in the SLAC forms the reactive part. An adding circuit (A1) superposes the current contribution from the resistive onto the reactive part.

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APPARATUS FOR ACHIEVING A CONTROLLABLE LINE TERMINATION IMPEDANCE.

TECHNICAL FIELD

The present invention relates to an apparatus for providing a controllable line termination impedance for a subscriber line circuit. The subscriber line circuit comprises two units, a two wire-four wire converter, i.e. a so-called subscriber line interface circuit (SLIC) and a subscriber line adapting circuit, i.e. a so-called subscriber line audio processing circuit (SLAC).

BACKGROUND ART

The general task of subscriber line circuits is to connect and form the interface for a telephone line towards a telephone exchange. Optionally, the line circuit can serve several telephone lines to the exchange. Incoming two wire connection to the subscriber are converted in the SLIC circuit to a four wire connection towards the following SLAC circuit, where analogue-digital conversion and recoding to PCM is carried out. In the SLAC circuit there are furthermore a balancing impedance and an impedance filter. This impedance filter should have a value such that the impedance, which from the subscriber line is "seen" towards the line circuit, meets the requirements which are placed on it inter alia by the telephone authorities. A prior art line circuit with the above mentioned SLIC and SLAC circuits is described in the EP-B-54024, for example.

A line circuit with a complex impedance for adapting to a subscriber line is described in the US-B-4,558,185. This known line circuit includes a complex impedance with capacitive character for adapting the impedance of the line circuit to the side tone characteristic of the subscriber apparatus, apart from adapting the subscriber line to the two wire-four wire junction, i.e. the SLIC circuit.

DISCLOSURE OF INVENTION

The present invention intends, as well as the above mentioned line circuit according to US-B-4,558,185, to provide a complex impedance in the line circuit for simulating a desired input impedance seen from the two wire side. In accordance with the invention, the impedance filter included in the SLAC circuit is utilized to form the complex part in the input impedance, which is furthermore made controllable by controlling the filter coefficients included in the digital impedance filter. In addition, there is included an analogue part in the form of an analogue feedback provided before the analogue-digital and digital-analogue interface in the SLAC circuit. With the aid of the apparatus in accordance with the present invention there can be achieved a flexible setting of a complex line termination impedance in accordance with the requirements made by telephone authorities for the transmission between subscriber and telephone exchange.

The object of the present invention is thus to provide a complex line termination impedance for a telephone line circuit, the impedance properties of which can be controlled in accordance with the requirements placed on the transmission between subscriber and line circuit without needing to resort to any alteration in the hardware.

The apparatus in accordance with the invention is characterized by the disclosures in the accompanying claims.

BRIEF DESCRIPTION OF DRAWINGS

The invention will now be described in more detail with reference to the accompanying drawings, where Figure 1 illustrates a simple circuit diagram of an impedance, Figures 2a-2d are different diagrams of the voltage and current in the diagram according to Figure 1, Figure 3 is a block diagram of an apparatus in accordance with the invention, together with closely associated circuits, Figure 4 is a block diagram of an impedance filter and contiguous blocks included in the block diagram according to Figure 3, Figures 5a-5f are the current diagrams for the impedance filter according to Figure 4.

BEST MODE FOR CARRYING OUT THE INVENTION

Figures 1 and 2a-2d are referred to for more closely explaining the idea and advantages of the invention. Figure 1 is a schematic diagram of an impedance Zi. When a voltage pulse U of a sinusoidal configuration according to Figure 2a occurs across the impedance Zi a current pulse is obtained through it. If Zi is real (resistive) the current pulse has the same appearance as the voltage pulse U_1, see Figure 2b. If Zi is complex the current pulse will be changed.

Figures 2c, 2d illustrate the current pulse i when the impedance Zi consists of a resistance-capacitance network. Positive and negative pulses of different appearances are obtained according to Figures 2c and 2d, depending on how the capacitance in Zi is connected, and on the values of the respective resistance and capacitance. The current may be said to comprise a part (the positive part) which does not have any delay and a part (the negative part) which is given a given delay relative to the applied voltage pulse U. The apparatus in accordance with the invention is intended to simulate this when Zi is the input impedance to a line circuit seen from the two wire side.

Figure 3 shows a block diagram of the proposed arrangement, together with contiguous circuit blocks in the line circuit. A two wire-four wire converter SLIC has a two wire input across which the voltage U occurs. The voltage U gives rise to a current i. An outgoing four-wire connection (ground is not shown) together with an incoming four wire connection connects the SLIC block to a SLAC circuit. Between the two four wire connections there has been connected an analogous block A with the transfer function Ha. The output of the block A is connected to a resistor R_r in the second four-wire connection via an adding circuit A1 The block A can comprise a controllable voltage divider or a controllable amplifier for enabling variation of the amplitude of the voltage which is sent to the adding circuit A1. A resistor R_t is connected between both four-wire branches. There is thus obtained greater freedom for selecting Z_i, since the resistor R_r is already fixed to a given value for maintaining prescribed signal levels in the SLAC circuit and across the input to the SLIC circuit.

The block, inclosed by dashed lines in Figure 3 and designated SLAC, is known per se, and is described in detail in the above-mentioned EP-B-54024. For the

sake of simplicity there are only shown in Figure 3 the analogue-digital converter AD, the decimation filter D in one four wire path, with the interpolation filter I and digital-analogue converter DA in the other four wire path. The impedance filter Z and the adding circuit A2 are also included in the known SLAC circuit, but at the same time they are a part of the present apparatus together with the block A in the way described hereinafter. A coefficient memory M, e.g. a RAM, for storing the coefficients to the impedance filter Z is included in the SLAC circuit, but is extended for also being able to store the values for controlling the block A, as described hereinafter.

Let it now be assumed that the SLIC circuit has a voltage amplification =kx from the two wire side to the four wire side and a current amplification =kr from the four wire side to the two wire side. Let it also be assumed that the impedance filter Z has a transfer function H_Z. If it is further assumed that the transfer functions of the units AD, D, I and DA are H_{AD}, H_D, H_I and H_{DA}, respectively, the input admittance Yi is obtained as

$$Yi = \frac{I}{Zi} = \frac{I}{U} = \frac{kx \cdot kr}{R_t} + \frac{kx \cdot kr}{R_r} (Ha + Hk\,Hz), \text{ where } Hk =$$

$H_{AD} \cdot H_D \cdot H_I \cdot H_D$ is only dependent on the frequency and where I and U are the complex values of i and u respectively.

The input admittance Yi to the SLIC-SLAC circuit thus comprises two parts. A first part, which does not give any delay and which is proportional to Ha and $1/R_t$, and a second part which is dependent on Z. The part which does not give any delay comprises an uncontrollable part proportional to $1/R_t$ and a controllable part proportional to Ha, c.f. Figures 5a and 5b. By varying (controlling) the block A there is obtained control of the part which corresponds to Figure 5B, and by controlling Z there is obtained control of the delayed part according to Figures 5c-5f. Since the impedance filter Z is already in the block SLAC, there is only required an addition of the block A and possibly the resistance R_k, which are analogue components and are relatively easy to implement.

Figure 4 shows in more detail the design of the controllable impedance filter Z in the case where it comprises a four-tap filter. The filter Z is implemented conventionally with three delay units DL1-DL3, four controllable multipliers Mo-M3 and an adding circuit A3. The input signal to the filter Z is connected to the input of the multiplier MO and to the delay unit DL1. The delay units DL1-DL3 have a delay equal to τ and have their outputs connected to inputs of the mulitpliers M1-M3. The adding circuit A3 sums the output signals from the multipliers M0-M3 and sends an output signal to one input of the adding circuit A2, this output signal then being led further to the subsequent units I and DA and towards the SLIC circuit.

Figures 5a-5f illustrate the current pulses obtained when a sinusoidal voltage pulse is applied to the line circuit input, c.f. Figure 2. From the output of block A, which in this case has the transfer function $H_a = k_a$, there is obtained according to Figure 5b a current pulse which is not delayed, the amplitude of which is proportional to k_a/R_r. From the respective multiplier output in the filter Z are obtained, according to Figures 5c-5f, delayed current pulses with amplitudes responsive to the coefficients $Z_0 - Z_3$ of the multipliers M0-M3 and which are mutually delayed by a time interval = τ .

It is apparent from Figures 5c-5f that when the coefficients Z_0-Z_3 are varied between positive and negative values, various positive and negative curve forms can be obtained in the delayed current pulses, and thereby various desired curve forms can be obtained in the output signal coming from the adding circuit A3. After superposition of the undelayed current pulse according to Figure 2a in the adding circuit A1 there is thus obtained a current comprising an undelayed part and delayed parts, where the appearance of the current can be changed within desired limits. The proposed apparatus which achieves this comprises two feed back circuits between both four-wire branches, namely an analogue feed back (A) and a digital feed back (Z). Control of the analogue and digital feedbacks can take place in the coefficient memory M of the SLAC circuit. In relation to the known SLAC circuit according to the EP-B-54024 mentioned herein before, the memory space in the coefficient memory M only needs to be added by a space for controlling the analogue feedback A, since the digital feedback is already available.

In the embodiment form above, the block A is a voltage converter. The block A can be a voltage-current converter in the form of a controllable resistance, however. In such a case the adder A_1 sums the currents from the SLAC circuit and from the block A.

CLAIMS

1 Apparatus for providing a controllable complex line termination impedance for a subscriber line circuit comprising a two wire-four wire converter (SLIC) and a subscriber line audio processing circuit (SLAC), which apart from a digital balance filter includes a controllable digital impedance filter (Z) as well as a control unit (M) for controlling the impedance filter (Z) so that a current quantity from the subscriber line circuit is obtained which is delayed relative an incoming voltage quantity (u), an analogue circuit block (A) on the four wire side of the converter being connected between both four-wire outputs of the converter, characterized in that the analogue circuit block (A) is controllable from said control unit (M) for obtaining a variable undelayed current quantity (Figure 5b) from the subscriber line circuit (SLIC) in relation to said incoming voltage magnitude (u), and by an adding circuit (A1) for superposing said delayed on said undelayed current quantity.

2 Apparatus as claimed in claim 1, characterized by a resistance (R_t) being connected between both four-wire connections on the output of the two wire-four wire converter.

3 Apparatus as claimed in claims 1 or 2, characterized in that said block (A) comprises a voltage converter for achieving an undelayed current quantity.

4 Apparatus as claimed in claims 1 or 2, characterized in that said block (A) for providing an undelayed current quantity comprises a current-voltage converter.

5 Apparatus as claimed in claims 1-4, characterized in that said controllable filter (Z) comprises a digital filter (DL1-DL3, M0-M3, A3) included in the said filter having a plurality of ports and associated controllable coefficient multipliers (M0-M3) for controlling the value and delay ($\tau, 2\tau, \ldots$) of said delayed current quantity.

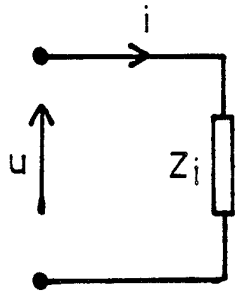
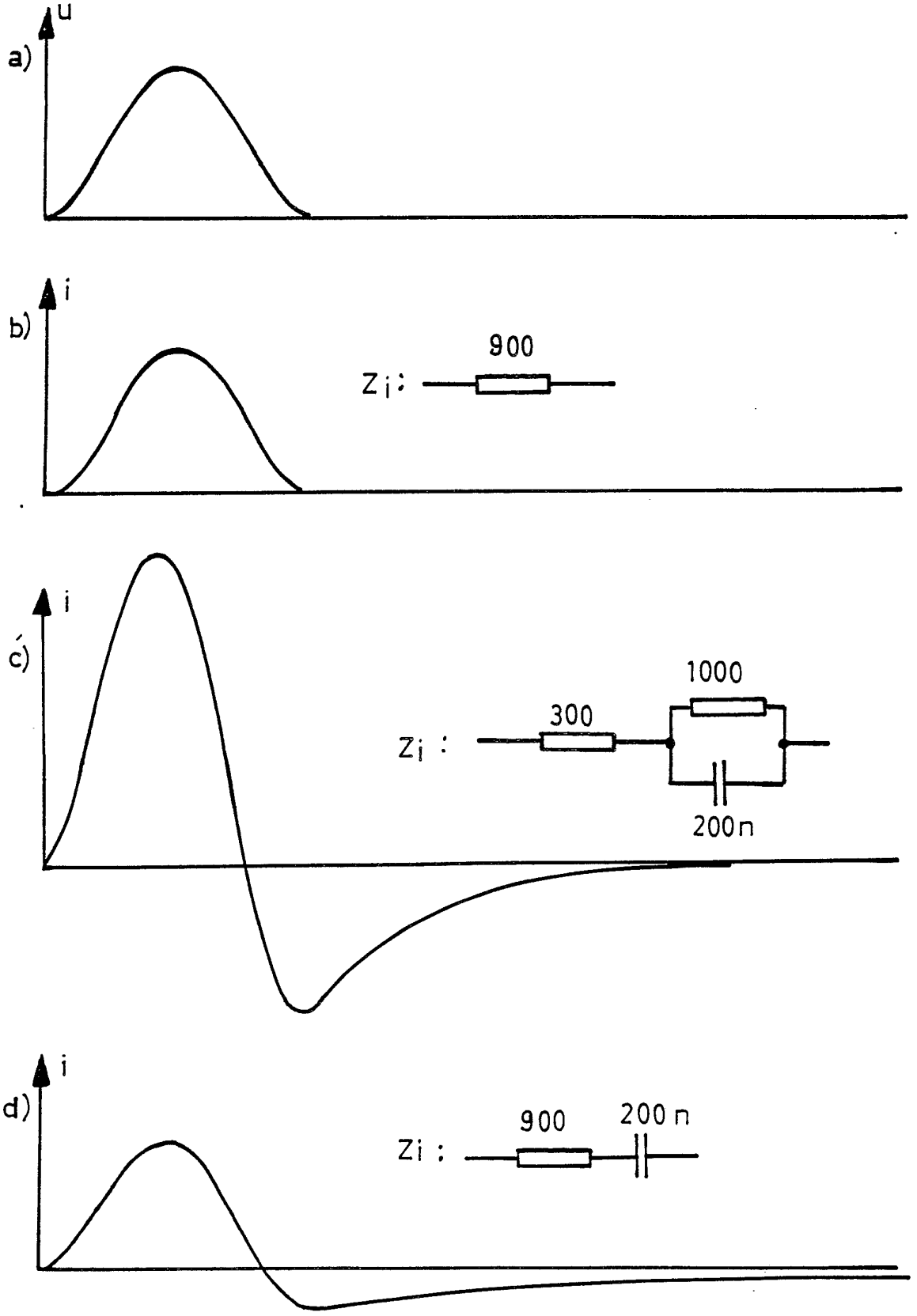


Fig.1

Fig.2a-d



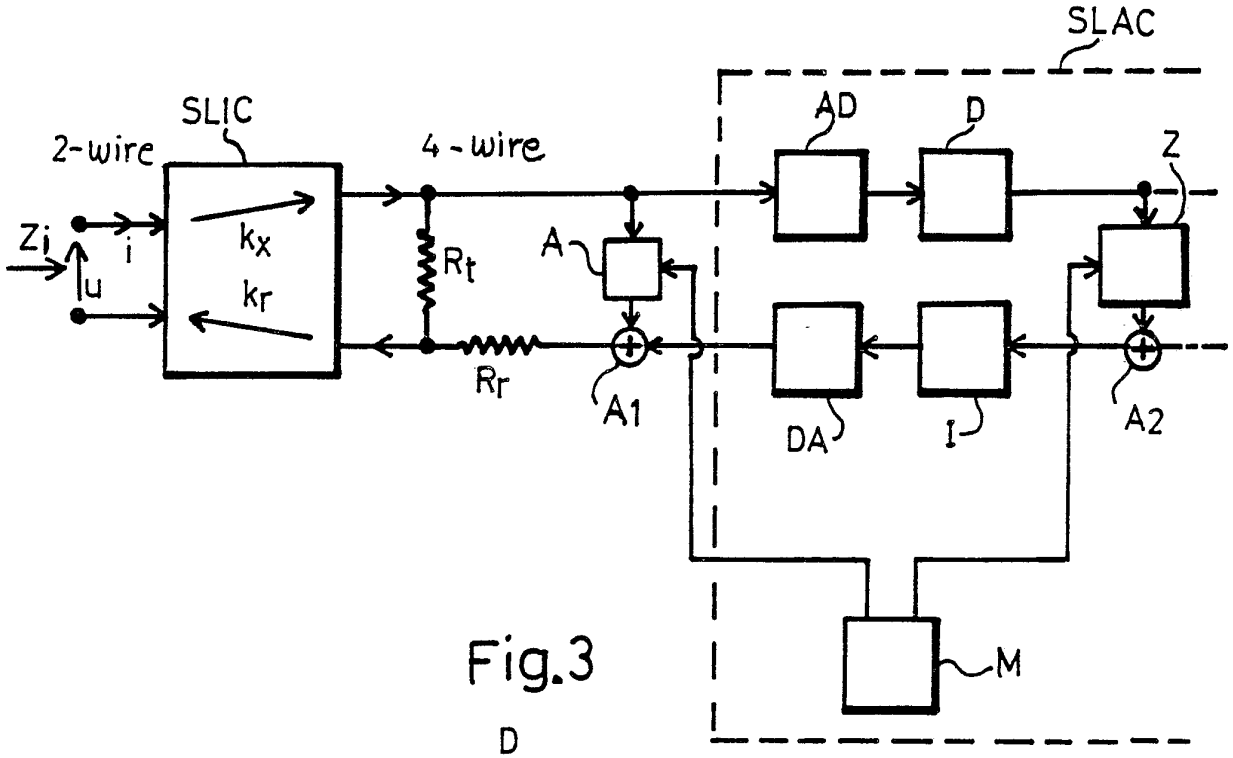

SLAC
SLIC
2-wire
4-wire
AD
D
Z
Zi
i
u
kx
kr
Rt
Rr
A
A1
DA
I
A2
M

Fig.3

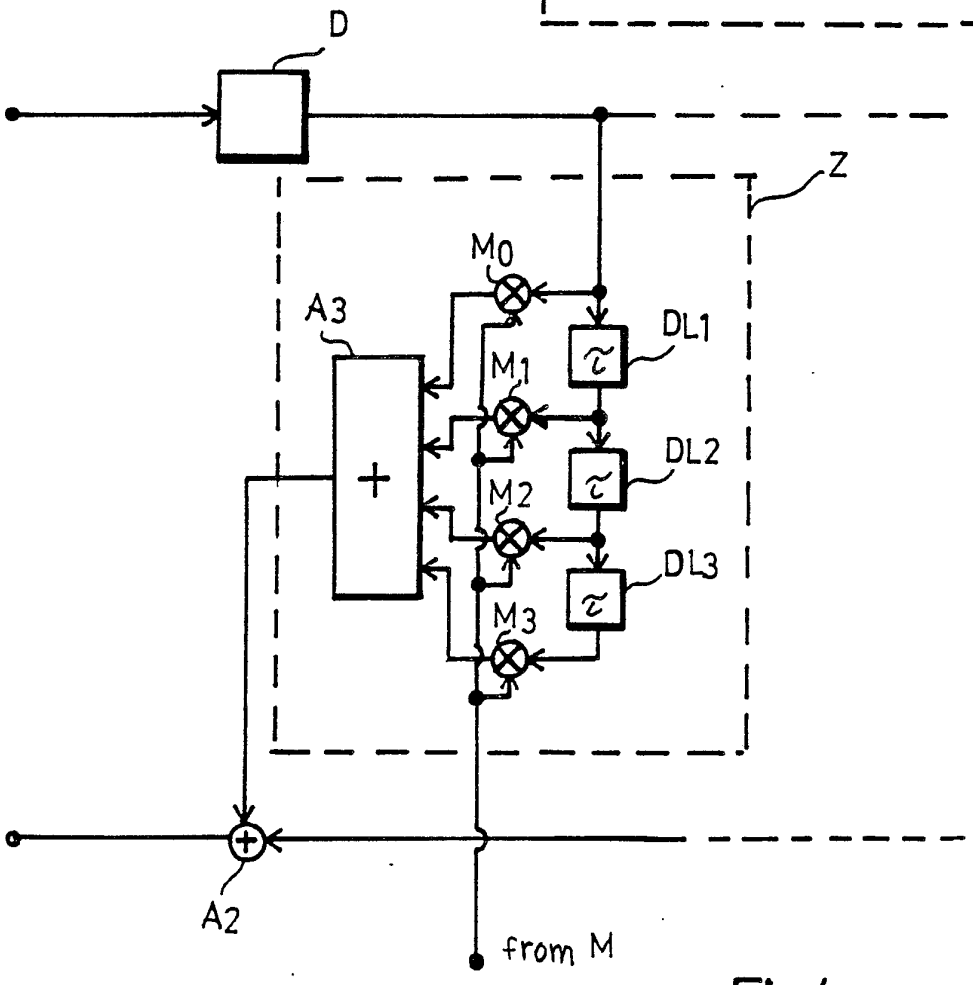
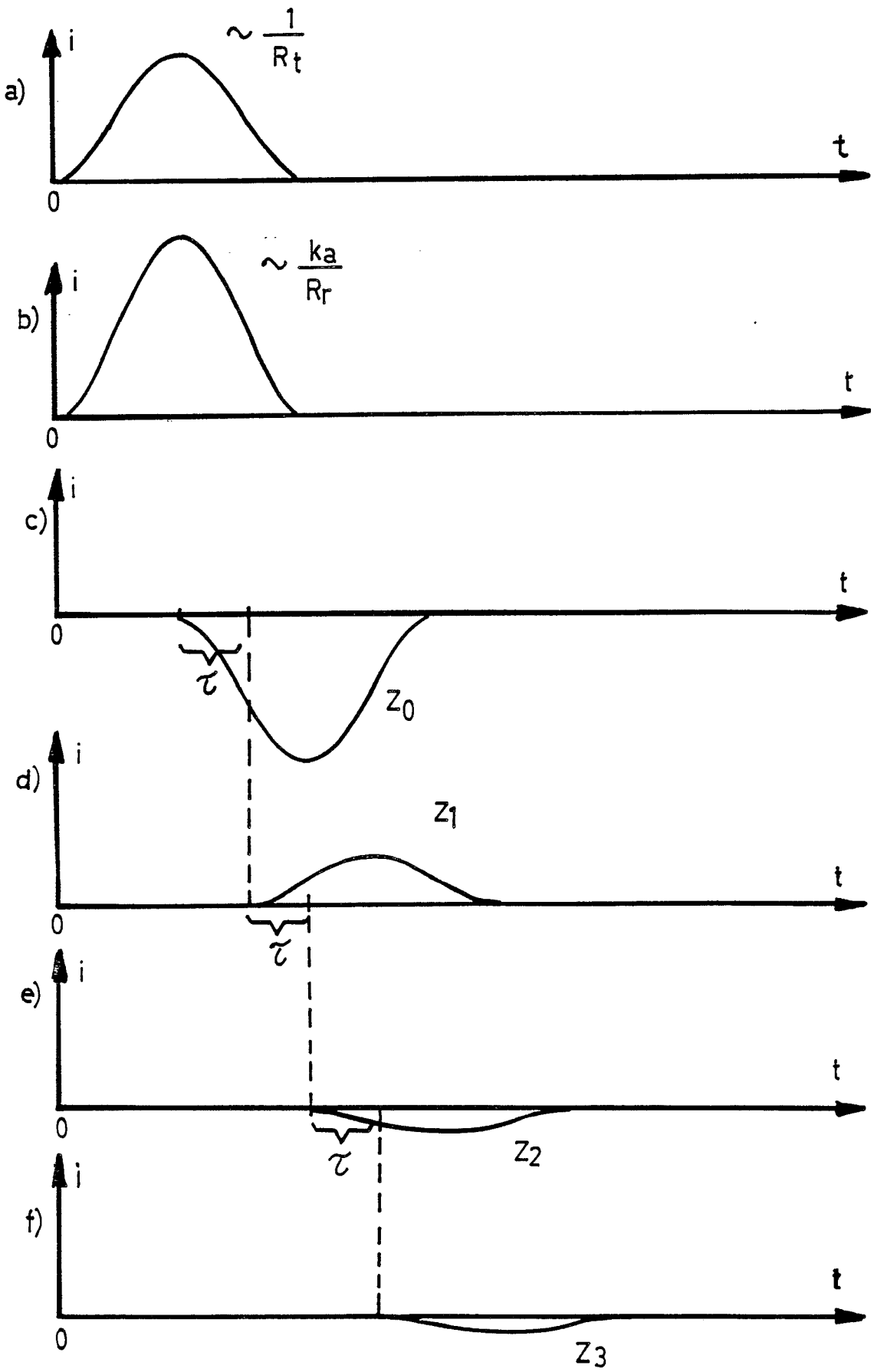

D
Z
M0
A3
DL1
M1
DL2
M2
DL3
M3
A2
from M

Fig.4

Fig 5 a-f


a)
i
$\sim \frac{1}{R_t}$
t
0
b)
i
$\sim \frac{ka}{R_r}$
t
0
c)
i
t
0
τ
z_0
d)
i
z_1
t
0
τ
e)
i
t
0
τ
z_2
f)
i
t
0
z_3

INTERNATIONAL SEARCH REPORT

International Application No PCT/SE88/00254

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC 4

H 04 B 3/03

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC 4	H 04 B 1/58, 3/02-/03, /20, /23; H 04 M 1/76; H 04 Q 3/24
National cl	21a^2:36/03
US Cl	179:16F, 170, 170.2, 170.6, 170.8; .../...

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

SE, NO, DK, FI classes as above

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	WO, A1, 81/03728 (ADVANCED MICRO DEVICES INC ET AL) 24 December 1981 See page 20, line 27 to page 21, line 6 and figure 1A	1-5
A	US, A, 4 558 185 (MORIKAWA ET AL) 10 December 1985 See column 1, line 40 to column 2, line 14, column 2, line 59 to column 3, line 36 and column 5, lines 51-56	1-5
A	EP, A2, 0 163 298 (HITACHI LTD) 4 December 1985 See page 3, line 19 to page 6, line 16, page 15, lines 14 to 19 and figure 1	1-5

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
1988-08-23	1988 -09- 02
International Searching Authority	**Signature of Authorized Officer**
Swedish Patent Office	Roland Landström Roland Landström

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

II Fields searched (cont)

364:724, 825;

370:24, 27;

379:345, 398, 400-411

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [1]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers....., because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claim numbers....., because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out specifically:

3. ☐ Claim numbers....., because they are dependent claims and are not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [2]

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.