A process for fabricating a circuit board with an embedded passive component is provided. An electrode-patterned layer having electrodes is formed on a surface of a conductive layer. A passive component material is filled in the intervals between the electrodes. The conductive layer and the electrode-patterned layer are laminated to a dielectric layer, wherein the electrode-patterned layer is embedded in the dielectric layer. The conductive layer is patterned to form a circuit layer.
FIG. 1A (PRIOR ART)

FIG. 1B (PRIOR ART)

FIG. 1C (PRIOR ART)
FIG. 1D (PRIOR ART)

FIG. 1E (PRIOR ART)
FABRICATING PROCESS OF CIRCUIT BOARD WITH EMBEDDED PASSIVE COMPONENT
CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a divisional of an application Ser. No. 11/626,379, filed on Jan. 24, 2007, now allowed, which claims the priority benefit of Taiwan application serial no. 95102753, filed on Jan. 25, 2006. The entirety of each of the above-mentioned patent applications is hereby incorporated by reference herein and made a part of this specification.

BACKGROUND OF THE INVENTION

[0002] 1. Field of Invention
[0003] The invention relates to a circuit board and a fabricating process thereof. More particularly, the invention relates to a circuit board with an embedded passive component and a fabricating process thereof.
[0004] 2. Description of Related Art
[0005] Due to the increasingly greater degree of integration of electronic products, circuit layers of circuit boards applied in highly integrated electronic products have changed from single or double layers to six layers, eight layers, or even more than ten layers, so that electronic devices can be mounted more densely on circuit boards. However, with the increase of layer counts of circuit boards and the density of the lines, influences to electrical signals transmitted in circuit boards caused by resistance-capacitance delay (RC delay) or crosstalk become more and more obvious. Therefore, additional passive components must be disposed in limited areas of circuit boards to improve the electrical properties thereof.
[0006] As described above, besides passive components, various electronic devices are further arranged in limited layout areas of circuit boards. However, the specified passive components with particular electrical values may not completely meet a particular given circuit design. Therefore, it is practical to fabricate passive components directly in circuit boards. Moreover, passive components in circuit boards can also adjust the electrical values thereof depending on layout design, circuit board material selection, and the like.

[0007] FIGS. 1A-1E show schematic sectional views of a conventional process for fabricating a circuit board with an embedded passive component. As shown in FIG. 1A, a first copper foil layer 110 is provided, and a capacitive material is coated on the overall first copper foil layer 110, so as to form a capacitive material layer 120. In FIG. 1B, a second copper foil layer 130 is formed on the capacitive material layer 120 in a laminating manner. In FIG. 1C, the second copper foil layer 130 in FIG. 1B undergoes a lithographic process and an etching process to form a second circuit layer 131. In FIG. 1D, the capacitive material layer 120 in FIG. 1C undergoes a patterning process, for example, including a lithographic process and an etching process, to form a patterned capacitive material layer 120'. A multilayer circuit board L and a dielectric layer 140 are provided, and the structure formed by the above processes, the multilayer circuit board L, and the dielectric layer 140 are laminated, wherein the patterned capacitive material layer 120' and the second circuit layer 131 are embedded in the dielectric layer 140. Further, referring to FIG. 1E, the first copper foil layer 110 undergoes the patterning process, for example, including a lithographic process and an etching process, to form a first circuit layer 110'. A plurality of conductive vias (not shown) is formed in the structure formed by the above processes to electrically connect the multilayer circuit board L and the first circuit layer 110'.

[0008] However, only single layer capacitance devices can be fabricated through conventional circuit board processes, and just one kind of passive component (referred to as a capacitance device herein) can be embedded in the single layer. Moreover, each capacitance device occupies a large area, such that the area for accommodating other integrated circuit devices is relatively reduced.

SUMMARY OF THE INVENTION

[0009] In view of the above, the invention is directed to a process for fabricating a circuit board with an embedded passive component for reducing the area occupied by the passive components.
[0010] Moreover, the invention is directed to a circuit board with an embedded passive component that occupies a small space.
[0011] In the invention, a process for fabricating a circuit board with an embedded passive component is provided. The process includes following steps. An electrode-patterned layer is formed on a first surface of a conductive layer, wherein the electrode-patterned layer has a plurality of electrodes. A passive component material is filled in the intervals between the electrodes. The conductive layer and the electrode-patterned layer are laminated to a dielectric layer, wherein the electrode-patterned layer is embedded in the dielectric layer. The conductive layer is patterned to form a first circuit layer.

[0012] According to an embodiment of the invention, the step of forming the electrode-patterned layer comprises forming a patterned photosist layer on the first surface of the conductive layer; then performing an electroplating process to form the electrode-patterned layer; and then removing the patterned photosist layer.

[0013] According to an embodiment of the invention, the step of forming the first circuit layer comprises forming a patterned photosist layer on a second surface of the conductive layer; next performing an electroplating process to form the first circuit layer; then removing the patterned photosist layer; and then removing a part of the conductive layer, such that the electrodes are electrically insulated.

[0014] According to an embodiment of the invention, after forming the first circuit layer, it further comprises forming a patterned dielectric layer on the first circuit layer, wherein the patterned dielectric layer exposes a part of the first circuit layer, and then, forming a second circuit layer on the patterned dielectric layer, wherein the second circuit layer is electrically connected to the first circuit layer.

[0015] In the invention, a circuit board with an embedded passive component is provided. The circuit board includes a dielectric layer, an electrode-patterned layer, a passive component material, and a first circuit layer, wherein the electrode-patterned layer is embedded in the dielectric layer, and the electrode-patterned layer has a plurality of electrodes. Moreover, a passive component material is filled in the intervals between the electrodes. Furthermore, the first circuit layer is disposed on the dielectric layer and the electrode-patterned layer, and the first circuit layer is electrically connected to the electrode-patterned layer.
According to an embodiment of the invention, the thickness of the electrode-patterned layer falls in the range of, for example, 10 μm to 100 μm.

According to an embodiment of the invention, the electrodes are, for example, plate-shaped, and the electrodes are approximately perpendicularly embedded in the dielectric layer.

According to an embodiment of the invention, the thickness of the passive component material is, for example, smaller than or equal to that of the electrode-patterned layer.

According to an embodiment of the invention, the circuit board with an embedded passive component further comprises, for example, a second circuit layer and a patterned dielectric layer disposed between the first circuit layer and the second circuit layer, wherein the first circuit layer is electrically connected to the second circuit layer.

According to an embodiment of the invention, the dielectric layer is, for example, a prepreg or core layer.

According to an embodiment of the invention, the passive component material is, for example, resistive or inductive material.

Based on the above, in the invention, a passive component is embedded in a dielectric layer (e.g. prepreg or core layer), and the electrodes of the passive component are substantially perpendicular to the dielectric layer, thus the space occupied by the passive component is significantly reduced. Moreover, circuit boards fabricated with the circuit board fabricating process of the invention have high reliability and low variance.

In order to make aforementioned and other features and advantages of the invention comprehensible, embodiments accompanied with figures are described in detail below.

It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A-1E show schematic sectional views of a conventional process for fabricating a circuit board with an embedded passive component.

FIGS. 2A-2I show schematic sectional views of a process for fabricating a circuit board with an embedded passive component according to the first embodiment of the invention.

FIG. 3 shows a schematic top view of a part of means of the circuit board with an embedded passive component according to the first embodiment of the invention.

FIGS. 4A-4B show schematic sectional views of a process for fabricating a circuit board with an embedded passive component according to the second embodiment of the invention.

DESCRIPTION OF EMBODIMENTS

First Embodiment

FIGS. 2A-2I show schematic sectional views of a process for fabricating a circuit board with an embedded passive component according to the first embodiment of the invention. The fabricating process for the circuit board of the invention comprises the following steps. In FIG. 2A and FIG. 2B, a conductive layer 210 is provided, and the conductive layer 210 is a copper foil or another kind of metal film. A patterned photosist layer P1 is formed on a first surface 212 of the conductive layer 210, wherein the step of forming the patterned photosist layer P1 comprises forming a photosist material layer (not shown) on the conductive layer 210 by adhering a photosist dry film or coating a liquid photosist. The photosist material layer is patterned to form a patterned photosist layer P1, wherein the patterning process comprises an exposing process and a developing process.

An electroplating process is performed to form an electroplating layer 220 on the area without being covered by the patterned photosist layer P1, wherein the electroplating layer 220 has a plurality of electrodes 222, and the electrodes 222 are substantially perpendicular to the conductive layer 210. The patterned photosist layer P1 is removed, wherein the patterned photosist layer P1 is removed by, for example, cleaning with an organic solution or an inorganic solution.

However, the method of forming the electroplated patterned layer 220 on the conductive layer 210 is not limited to the above process. For example, a thick conductive layer (not shown) can be first provided, and then a part of the thick conductive layer is removed to form the electroplated patterned layer 220.

Referring to FIG. 2C, a passive component material 224 is filled in the intervals between the electrodes 222, wherein the method for filling the passive component material 224 may be screen printing. Moreover, the filled passive component material 224 can be a resistive material, a capacitive material, or an inductive material.

Referring to FIGS. 2D-2E, a dielectric layer 230 is provided, wherein the dielectric layer 230 is, for example, a core layer or a prepreg, and in the present embodiment, the dielectric layer 230 is a core layer. Then, the conductive layer 210 and the electroplated patterned layer 220 are laminated to the dielectric layer 230, wherein the electroplated patterned layer 220 is embedded in the dielectric layer 230.

Referring to FIG. 2F, a patterned photosist layer P2 is formed on a second surface 240 of the conductive layer 210, wherein the method of forming the patterned photosist layer P2 is similar to that of forming the patterned photosist layer P1 on the first surface 212. Referring to FIG. 2G, an electroplating process is performed to form a first circuit layer 240 on the area without being covered by the patterned photosist layer P2. Referring to FIG. 2H, the patterned photosist layer P2 is removed, wherein the method of removing the patterned photosist layer P2 is similar to that of removing the patterned photosist layer P1. Referring to FIG. 2I, a part of the conductive layer 210 is removed such that the electrodes 222 are electrically insulated, wherein the method of removing a part of the conductive layer 210 is, for example, performing an etching process for the conductive layer 210. Thus, the process of fabricating the circuit board 200 is substantially completed.

However, after FIG. 2E, a part of the conductive layer 210 can be directly removed to form the first circuit layer 240 and make the electrodes 222 electrically insulated from one another. Moreover, when the dielectric layer 230 is a core layer, after forming the first circuit layer 240, other circuits can be formed by a build-up or lamination method. The build-up method is illustrated as an example herein below.
Referring to FIGS. 2J-2K, the schematic sectional views of a process for fabricating a second circuit layer according to the first embodiment of the invention are shown. After forming the first circuit layer 240, other circuits are formed with the build-up method. Referring to FIG. 2J, more particularly, a patterned dielectric layer 250 is formed on the first circuit layer 240, wherein the patterned dielectric layer 250 exposes a part of the first circuit layer 240. Moreover, the method of forming the patterned dielectric layer 250 includes, for example, forming a dielectric material layer (not shown) on the first circuit layer 240 by spin coating, and then performing a patterning process (e.g., including a lithographic and etching process) to form the patterned dielectric layer 250.

Referring to FIG. 2K, a conductive material layer (not shown) is formed on the patterned dielectric layer 250, wherein the conductive material layer can be formed by sputtering or other metal deposition process. Then, a patterning process (e.g., including a lithographic process and an etching process) is performed on the conductive material layer to form a second circuit layer 260, wherein the second circuit layer 260 is electrically connected to the first circuit layer 240.

It shall be noted that the above second circuit layer 260 is formed by a build-up method; however, a laminating method or other methods can be used. Moreover, other circuit layers can be sequentially formed on the second circuit layer 260 in accordance with the requirements of design, and the forming method of the circuit layers is described above. The structure of the circuit board with an embedded passive component will be described in detail below.

FIG. 3 shows a schematic top view of a part of means of the circuit board with an embedded passive component according to the first embodiment of the invention. Referring to FIG. 2I and FIG. 3, the circuit board with an embedded passive component 200 comprises a dielectric layer 230, an electrode-patterned layer 220, a passive component material 224, and a first circuit layer 240. The electrode-patterned layer 220 is embedded in the dielectric layer 230, and the electrode-patterned layer 220 has a plurality of electrodes 222. It can be seen from FIG. 3 that the electrode patterns 220 of the invention take the electrode pattern of a capacitance device. However, the electrodes 222 can also be the electrode pattern of an inductance device or a resistance device. Moreover, the thickness of the electrode-patterned layer 220 falls in the range of, for example, 10 μm to 100 μm, and the thickness of the electrode-patterned layer 220 is, for example, larger than the thickness of the first circuit layer 240.

The passive component material 224 is disposed in the intervals between the electrodes 222, and the thickness of the passive component material 224 is, for example, smaller than or equal to the thickness of the electrode-patterned layer 220. Moreover, the first circuit layer 240 is disposed on the dielectric layer 230 and the electrode-patterned layer 220, and the first circuit layer 240 is electrically connected to the electrode-patterned layer 220. When the dielectric layer 230 is a prepreg, the structure as shown in FIG. 2I is regarded as a single layer circuit board.

Further, when the dielectric layer 230 is a core layer, the circuit board with an embedded passive component of the invention further comprises, for example, a second circuit layer 260 and a patterned dielectric layer 250 disposed between the first circuit layer 240 and the second circuit layer 260, and the first circuit layer 240 is electrically connected to the second circuit layer 260.

Since the electrode-patterned layer 220 is embedded in the dielectric layer 230, i.e., in the core layer or prepreg, and the electrode 222 is substantially perpendicular to the dielectric layer 230, compared with the conventional technology, the area occupied by the passive component of the invention can be reduced. Moreover, since the passive component occupies a smaller area, the circuit board of the invention can be integrated with other electronic devices or passive components. Further, compared with the conventional technology, the circuit board of the invention has high reliability and low variance.

Second Embodiment

FIGS. 4A-4B show the schematic sectional views of a process for fabricating a circuit board with an embedded passive component according to a second embodiment of the invention. Referring to FIG. 4A, when the dielectric layer 230 is a prepreg, a circuit board 200 is regarded as a single layer circuit board. Therefore, the circuit board 200 is laminated with other circuit boards. Then, a circuit unit L and a dielectric layer 350 are provided, wherein the circuit unit L is a dual-layer circuit board or a multilayer circuit board, and the circuit unit L has a circuit layer 360 disposed on the two opposite surfaces thereof respectively.

Referring to FIG. 4B, the circuit board 200 and the circuit unit L are laminated, and the dielectric layer 350 is disposed between the circuit board 200 and the circuit unit L. Then, the first circuit layer 240 is electrically connected to the circuit layer 360 of the circuit unit L. For example, a plurality of conductive vias (not shown) is formed in the structure after lamination to electrically connect the first circuit layer 240 and the circuit layer 360 of the circuit unit L.

To sum up, the circuit board with an embedded passive component of the invention at least has the following advantages.

1. In the invention, the electrodes of the passive component are embedded in the dielectric layer, i.e., in the core layer or prepreg, and the electrodes of the passive components are substantially perpendicular to the dielectric layer. Therefore, compared with the conventional technology, the space occupied by the passive component of the invention is significantly reduced.

2. The circuit board fabricated by the circuit board fabricating process of the invention has high reliability and low variance, thus the manufacturing cost can be reduced.

3. Various passive components (e.g., resistors, capacitors, or inductors) can be formed in a single layer of the circuit board of the invention in accordance with the requirements of the design, which is more flexible in design compared with the conventional technology.

4. It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.
What is claimed is:

1. A process for fabricating a circuit board with the embedded passive component, the process comprising:
   forming an electrode-patterned layer on a first surface of a conductive layer, wherein the electrode-patterned layer has a plurality of electrodes;
   filling a passive component material in the intervals between the electrodes;
   laminating the conductive layer and the electrode-patterned layer to a dielectric layer, wherein the electrode-patterned layer is embedded in the dielectric layer; and
   patterning the conductive layer to form a first circuit layer.

2. The process for fabricating the circuit board with the embedded passive component as claimed in claim 1, wherein the step of forming the first circuit layer comprises:
   forming a patterned photoresist layer on the first surface of the conductive layer;
   performing an electroplating process to form the electrode-patterned layer; and
   removing the patterned photoresist layer.

3. The process for fabricating the circuit board with the embedded passive component as claimed in claim 1, wherein the step of forming the first circuit layer comprises:
   forming a patterned photoresist layer on a second surface of the conductive layer;
   performing an electroplating process to form the first circuit layer;
   removing the patterned photoresist layer; and
   removing a part of the conductive layer, such that the electrodes are electrically insulated.

4. The process for fabricating the circuit board with the embedded passive component as claimed in claim 1, after forming the first circuit layer, further comprising:
   forming a patterned dielectric layer on the first circuit layer, wherein the patterned dielectric layer exposes a part of the first circuit layer; and
   forming a second circuit layer on the patterned dielectric layer, wherein the second circuit layer is electrically connected to the first circuit layer.