(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 June 2017 (29.06.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/112819 A1

(51) International Patent Classification:
H03B 29/00 (2006.01) *H03L 7/085* (2006.01)

(21) International Application Number:
PCT/US2016/068132

(22) International Filing Date:
21 December 2016 (21.12.2016)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
62/270,515 21 December 2015 (21.12.2015) US
15/385,859 20 December 2016 (20.12.2016) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 15/385,859 (CON)
Filed on 20 December 2016 (20.12.2016)

(71) Applicant: **TEXAS INSTRUMENTS INCORPORATED** [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(71) Applicant *(for JP only)*: **TEXAS INSTRUMENTS JAPAN LIMITED** [JP/JP]; 24-1, Nishi-shinjuku 6-chome, Shinjuku-ku, 160-8366 (JP).

(72) Inventor: **FINN, Steven, Ernest**; 2633 Mural Drive, Atlanta, GA 30341 (US).

(74) Agents: **DAVIS, Michael, A., Jr.** et al.; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

[Continued on next page]

(54) Title: LOOP FILTER WITH ACTIVE DISCRETE-LEVEL LOOP FILTER CAPACITOR IN VCO

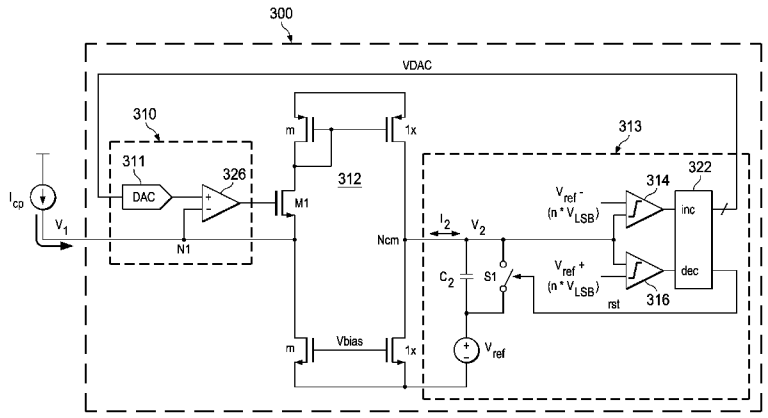


FIG. 3

(57) Abstract: In described examples, a loop filter with an active discrete-level loop filter capacitor (300) can be used in a VCO (such as for CDR). In described examples, a loop filter capacitor function is simulated by sensing input loop filter current (such as with a current mirror (312) and source follower (Ml) in an input leg), and forcing back a loop filter (VCO) control voltage (VI at Nl). Loop filter voltage control is provided using a VDAC (311) with a discrete-level VDAC feedback voltage (VDAC), incremented/decremented (314, 316, 322) based on the sensed loop filter current (12). In one embodiment, the VDAC voltage (311) is provided as the non-inverting input to an amplifier (326), with the inverting input providing the control voltage (VI at Nl), forced to the VDAC feedback voltage. The VDAC feedback voltage can be provided by increment/decrement comparators (314, 316) based on a voltage deviation on a C2 capacitor (from a reference voltage) that receives the sensed loop filter current (effectively multiplying the C2 capacitance to provide a simulated loop filter capacitance).

WO 2017/112819 A1

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

Loop filter with active discrete-level loop filter capacitor in VCO

[0001] This relates generally to filter circuits, and more particularly to loop filter circuits used in phase-locked loop (PLL) circuits, such as for clock data recovery.

BACKGROUND

[0002] Analog phase-locked loop control systems include a VCO (voltage or current controlled oscillator) with a frequency/phase control loop including a phase (or phase/frequency) detector PD/PFD, and a loop filter. The PD/PFD compares the phase of an input signal and a VCO feedback signal, and generates an phase error output, which is low pass filtered by the loop filter to provide a VCO control voltage to phase lock the VCO output signal with the input signal.

[0003] FIG. 1 illustrates a PLL 10 with a VCO 12 and a phase/frequency detector (PFD) 14, and an example charge pump loop filter 20 driven by the PFD. Loop filter 20 includes a loop filter capacitor C1, and an optional secondary filter (smoothing) capacitor C2. Loop filter 20 low pass filters the PDF phase error output to provide a VCO control voltage V1.

[0004] One application of phase-locked loop control systems is for clock data recovery. In an integrated CDR, the loop filter capacitor can use 25% or more of the die area. Alternative design approaches to reducing this die area penalty are to use an external loop filter cap, or to replace an analog PLL/CDR design with a digital PLL/CDR.

SUMMARY

[0005] Described examples include apparatus and methods for a loop filter with an active discrete-level loop filter capacitor (e.g., for use in a voltage controlled oscillator), such as for clock data recovery.

[0006] In at least one example, the loop filter capacitor function is simulated by: (a) sensing an input loop filter current, and providing a corresponding sensed loop filter current; and (b) providing a VCO control voltage by generating a discrete-level VDAC feedback voltage that is incremented and decremented based on the sensed loop filter current, generating a VDAC control voltage using a VDAC (voltage digital to analog converter) based on the discrete-level VDAC feedback voltage, providing the VDAC control voltage to a non-inverting input to an

amplifier, and generating the VCO control voltage at a loop filter output node coupled to an inverting input to the amplifier, the VCO control voltage based on the VDAC feedback voltage, which is based on the sensed loop filter current.

[0007] According to other examples, the discrete-level VDAC feedback voltage can be generated by: incrementing and decrementing the VDAC feedback voltage based on a deviation of a voltage V2 on C2 from a voltage reference Vref based in the sensed loop filter current; and resetting the V2 voltage on C2 to Vref after each increment and decrement of the VDAC feedback voltage; such that an effective loop filter capacitance of the loop filter circuitry is a multiplication of a capacitance of C2. According to other examples, the input loop filter current is sensed using: a current mirror with a mirror input leg including a mirror input node coupled to receive the input loop filter current, and a mirror output leg including a mirror output node to provide the sensed loop filter current, the mirror output node coupled to the VDAC feedback circuitry; and a source follower transistor included in the mirror input leg, and controlled by the VDAC circuitry to sense the input loop filter current, which is mirrored as the sensed loop filter current to the mirror output leg based on a pre-defined mirror-ratio.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1 illustrates a PLL with a VCO and phase/frequency detector, and an example charge pump loop filter, including a loop filter capacitor.

[0009] FIG. 2 is a functional illustration of replacing a loop filter capacitor with an active discrete-level loop filter capacitor according to example embodiments.

[0010] FIG. 3 illustrates an example embodiment of a loop filter with an active discrete-level loop filter capacitor for replacing a component loop filter capacitor, using VDAC circuitry to approximate the loop filter capacitor function, including sensing input loop filter current (Icp), and forcing back the appropriate VCO control voltage generated by the VDAC circuitry.

[0011] FIG. 4 illustrates an example implementation of a loop filter with an active discrete-level loop filter capacitor, including VDAC circuitry, current sense circuitry and VDAC feedback circuitry.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0012] Described examples include a loop filter with active discrete-level loop filter capacitor. An example application is a loop filter for VCOs (voltage or current controlled oscillators), such as for clock data recovery systems.

[0013] The terminology active discrete-level loop filter "capacitor" means an active circuit design for loop filter capacitance function that can be used to replace a component capacitor, such as illustrated in FIG. 1 (C1).

[0014] In brief overview a loop filter with an active discrete-level loop filter capacitor can be used in a VCO (such as for CDR). A loop filter capacitor function is simulated by sensing input loop filter current (such as with a current mirror and source follower in the input leg), and forcing back a loop filter (VCO) control voltage. Loop filter voltage control is provided using a VDAC with a discrete-level VDAC feedback voltage, incremented/decremented based on the sensed loop filter current. In one embodiment, the VDAC voltage is provided as the non-inverting input to an amplifier, with the inverting input providing the control voltage, forced to the VDAC feedback voltage. The VDAC feedback voltage can be provided by increment/decrement comparators based on a voltage deviation on a C2 capacitor (from a reference voltage) that receives the sensed loop filter current (effectively multiplying the C2 capacitance to provide a simulated loop filter capacitance).

[0015] FIG. 2 is a functional illustration of replacing a component loop filter capacitor C1 with an active discrete-level loop filter capacitor (30) according to example embodiments.

[0016] As described hereinabove, as used in this description, the terminology active discrete-level loop filter "capacitor" means an active circuit design for loop filter capacitance function that can be used to replace a component capacitor, as described in connection with FIGS. 3 and 4. Accordingly, the active loop filter capacitor design creates, in effect a "pseudo" capacitor that provides the loop capacitor functionality, as an alternative analog capacitor design, without adopting a full digital loop filter.

[0017] FIG. 3 illustrates an example embodiment of a loop filter with an active discrete-level loop filter capacitor 300. The active discrete-level loop filter capacitor design uses VDAC (voltage digital-to-analog converter) voltage control circuitry 310, 311, 313 to approximate the loop filter capacitor function.

[0018] The loop filter capacitor function is simulated by sensing (312) input loop filter current Icp received at an input node N1, and forcing back the appropriate VCO control voltage V1 at node N1 with the VDAC voltage control circuitry. The VDAC voltage control circuitry includes VDAC circuitry 310, including a VDAC 311, and VDAC feedback circuitry 313.

[0019] Current sense circuitry 312 senses input loop filter current Icp (received through N1), and provides a corresponding sensed loop filter current I2. Current sense circuitry includes a current mirror with a source follower NMOS M1 in the mirror input leg.

[0020] The current mirror includes an input leg coupled to node N1, and a mirror (output) leg with an output node Ncm. Source follower M1 in the current mirror input leg is source-coupled to node N1, receiving the input loop filter current Icp.

[0021] The low-output impedance source follower M1 is controlled by the VDAC circuitry as described below. Source follower M1 senses the input loop filter current Icp at its drain, which is mirrored to the mirror output leg (based on a pre-defined mirror ratio, such as 10:1), and output through Ncm as the sensed loop filter current I2.

[0022] The VDAC voltage control circuitry 310, 313 generates the VCO control voltage V1 (N1) based on a VDAC feedback voltage, which is based on the sensed loop filter current generated by current sense circuitry 312. VDAC voltage control circuitry includes VDAC circuitry 310, including VDAC 311, and VDAC feedback circuitry 313.

[0023] VDAC feedback circuitry 313 generates a discrete-level VDAC feedback voltage that is incremented and decremented based on the sensed loop filter current, and input to the VDAC 311.

[0024] VDAC feedback circuitry 313 includes increment and decrement comparators 314 and 316 responsive to a voltage based on the sensed loop filter current I2 output from current sense circuitry 312 at the mirror output node Ncm. Increment/decrement comparators respectively generate increment/decrement signals input to INC/DEC logic 322. INC/DEC logic 322 is responsive to the increment/decrement signals from comparators 314/316 to generate the discrete-level VDAC feedback voltage.

[0025] VDAC feedback circuitry includes a capacitor C2 coupled between the current mirror output node Ncm, and a reference voltage Vref. The increment/decrement comparators generate the increment/decrement signals based on a deviation of a voltage V2 on C2 from Vref. INC/DEC logic 322 provides a reset signal to switch S1 to reset V2 to Vref after each increment and decrement signal. Effectively, the loop filter capacitance of the loop filter circuitry 300 is a multiplication of the capacitance of C2.

[0026] VDAC circuitry 310 includes an amplifier 326 to provide a control input to the source follower M1 in current sense circuitry (current mirror) 322. Amplifier 326 has a noninverting

input coupled to receive the VDAC feedback voltage, and an inverting input coupled to node N1, the VCO control voltage V1. Amplifier 326 forces the VCO control voltage V1 at the inverting input to be substantially equal to the VDAC feedback voltage at the non-inverting input.

[0027] Thus, the low-output impedance provided by source follower M1 (1/(Av*gm)) at the input node N1 effectively provides a "pseudo" loop filter capacitor. The capacitor function simulated by the VDAC voltage control function, including VDAC 311 and amplifier 326 providing a control voltage to source follower M1. Loop filter input current Icp is sensed by the source follower M1, and mirrored to provide the sensed loop filter current I2 output from Ncm. The sensed loop filter current I2 is applied across the secondary capacitor C2 (such as approximately 1pF). Increment/decrement comparators 314/316 sense the deviation of V2 relative to Vref, and provide corresponding increment/decrement signals to the INC/DEC logic 322. When a positive edge of the increment/decrement signals is sensed, the INC/DEC control logic increments/decrements by 1x LSB (such as approximately 1mV) the VDAC feedback voltage controlling the VCO control voltage V1.

[0028] The loop filter with an active discrete-level loop filter capacitor 300 effectively provides capacitance multiplication of C2 by two factors: (a) $n = V_{trig}/V_{LSB}$ where V_{trig} is the delta voltage accumulated on the small capacitor C_2; and (b) the current mirror ration m. An example value of C_2 1pF yields approximately 1000x reduction from 1nF (a representative value for a component loop filter capacitor):

$$I_{cp} = C_1 \frac{dV_1}{dt} \Rightarrow \left(\frac{I_{cp}}{m}\right) = \left(\frac{C_1}{n \cdot m}\right) \frac{n \cdot dV_1}{dt} \Rightarrow I_2 = C_2 \frac{dV_2}{dt}$$

[0029] FIG. 4 illustrates an example implementation of a loop filter with an active discrete-level loop filter capacitor 400, including VDAC circuitry 410, current sense circuitry 412 and VDAC feedback circuitry 413. VDAC feedback circuitry 413 is shown deconstructed as comparators 414, 416, and INC/DEC control logic 422, together generating the VDAC feedback voltage.

[0030] The loop filter with an active discrete-level loop filter capacitor according to this description can be designed as a un-clocked digital block that is low power and low current consumption (such as approximately 1mA total). It is based on a VDAC VCO voltage control architecture including approximately a 10bit VDAC, inc/dec comparators, and a current-mirror.

For an example CDR application with integrated loop filter capacitor, die area is significantly reduced.

[0031] In summary, a loop filter, such as for use in a VCO, is based on an active discrete-level loop filter capacitor that includes: current sense circuitry to sense an input loop filter current, and provide a corresponding sensed loop filter current; and VDAC voltage control circuitry. The VDAC control circuitry includes: VDAC circuitry including a VDAC (voltage digital-to-analog converter), and VDAC feedback circuity to generate a discrete-level VDAC feedback voltage that is incremented and decremented based on the sensed loop filter current; the VDAC circuitry to generate the VCO control voltage based on the VDAC feedback voltage, which is based on the sensed loop filter current. The VDAC circuitry can include an amplifier to provide a control input to the current sense circuitry; the amplifier having a noninverting input coupled to receive the VDAC feedback voltage, and an inverting input coupled to the VCO control voltage; such that the VCO control voltage is substantially equal to the VDAC feedback voltage. The VDAC feedback circuitry can include increment and decrement comparators responsive to a voltage based on the sensed loop filter current to respectively generate increment and decrement signals; and inc/dec logic responsive to the increment and decrement signals to generate the discrete-level VDAC feedback voltage. The VDAC feedback circuitry can further include: a capacitor C2 coupled between the output node, and a reference voltage Vref; the increment and decrement comparators to generate the increment and decrement signals based on a deviation of a voltage V2 on C2 from Vref; and reset circuitry coupled to C2 and responsive to a reset signal from the inc/dec logic to reset V2 to Vref after each increment and decrement signal; such that an effective loop filter capacitance of the loop filter circuitry is a multiplication of a capacitance of C2. The current sense circuitry can include: a current mirror with a mirror input leg including a mirror input node coupled to receive the input loop filter current, and a mirror output leg including a mirror output node to provide the sensed loop filter current, the mirror output node coupled to the VDAC feedback circuitry; and a source follower transistor included in the mirror input leg, and controlled by the VDAC circuitry to sense the input loop filter current, which is mirrored as the sensed loop filter current to the mirror output leg based on a pre-defined mirror-ratio.

[0032] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A circuit, comprising:

a VCO (voltage controlled oscillator); and

loop filter circuitry to provide a low-pass filtered VCO control voltage to the VCO, including:

current sense circuitry to sense an input loop filter current, and provide a corresponding sensed loop filter current; and

VDAC voltage control circuitry, including: VDAC circuitry including a VDAC (voltage digital-to-analog converter); and VDAC feedback circuity to generate a discrete-level VDAC feedback voltage that is incremented and decremented based on the sensed loop filter current; the VDAC circuitry to generate the VCO control voltage based on the VDAC feedback voltage, which is based on the sensed loop filter current.

2. The circuit of claim 1, wherein the VDAC circuitry comprises:

an amplifier to provide a control input to the current sense circuitry, the amplifier having: a noninverting input coupled to receive the VDAC feedback voltage; and an inverting input coupled to the VCO control voltage; such that the VCO control voltage is substantially equal to the VDAC feedback voltage.

3. The circuit of claim 2, wherein the VDAC feedback circuitry comprises:

increment and decrement comparators responsive to a voltage based on the sensed loop filter current to respectively generate increment and decrement signals; and

inc/dec logic responsive to the increment and decrement signals to generate the discrete-level VDAC feedback voltage.

4. The circuit of claim 3, wherein the current sense circuitry outputs the sensed loop filter current at an output node coupled to the increment and decrement comparators, and wherein the VDAC feedback circuitry further comprises:

a capacitor C2 coupled between the output node, and a reference voltage Vref;

the increment and decrement comparators to generate the increment and decrement signals based on a deviation of a voltage V2 on C2 from Vref; and

reset circuitry coupled to C2 and responsive to a reset signal from the inc/dec logic to reset V2 to Vref after each increment and decrement signal;

such that an effective loop filter capacitance of the loop filter circuitry is a multiplication of a capacitance of C2.

5. The circuit of claim 1, wherein the current sense circuitry comprises:

a current mirror with a mirror input leg including a mirror input node coupled to receive the input loop filter current, and a mirror output leg including a mirror output node to provide the sensed loop filter current, the mirror output node coupled to the VDAC feedback circuitry; and

a source follower transistor included in the mirror input leg, and controlled by the VDAC circuitry to sense the input loop filter current, which is mirrored as the sensed loop filter current to the mirror output leg based on a pre-defined mirror-ratio.

6. The circuit of claim 5, wherein the VDAC circuitry comprises:

an amplifier to provide a control input to the source follower transistor, the amplifier having: a noninverting input coupled to receive the VDAC feedback voltage; and an inverting input coupled to the VCO control voltage; such that the VCO control voltage is substantially equal to the VDAC feedback voltage.

7. The circuit of claim 6, wherein the VDAC feedback circuitry further comprises:

a capacitor C2 coupled between the mirror output node, and a reference voltage Vref;

the VDAC feedback circuity to generate the discrete-level VDAC feedback voltage, incremented and decremented based on a deviation of a voltage V2 on C2 from Vref, corresponding to the sensed loop filter current; and

reset circuitry coupled to C2 and responsive to a reset signal from the inc/dec logic to reset V2 to Vref after each increment and decrement of the VDAC feedback voltage;

such that an effective loop filter capacitance of the loop filter circuitry is a multiplication of a capacitance of C2 based on the deviation in V2 and the mirror-ratio.

8. The circuit of claim 1, wherein the loop filter circuitry comprises a charge pump loop filter.

9. A circuit, comprising:

a phase detector coupled to receive an input signal at an input frequency and phase, and generate a PD phase detect signal based on a VCO feedback signal;

a VCO (voltage controlled oscillator) responsive to a VCO control voltage to generate a VCO output signal phase aligned with the input signal, the VCO feedback signal corresponding to the VCO output signal; and

loop filter circuitry coupled to receive the PD phase detect signal, and to provide a low-pass filtered VCO control voltage to the VCO, including:

current sense circuitry to sense an input loop filter current, and provide a corresponding sensed loop filter current; and

VDAC voltage control circuitry, including: VDAC circuitry including a VDAC (voltage digital-to-analog converter); and VDAC feedback circuity to generate a discrete-level VDAC feedback voltage that is incremented and decremented based on the sensed loop filter current; the VDAC circuitry to generate the VCO control voltage based on the VDAC feedback voltage, which is based on the sensed loop filter current.

10. The circuit of claim 9, wherein the VDAC circuitry comprises:

an amplifier to provide a control input to the current sense circuitry, the amplifier having: a noninverting input coupled to receive the VDAC feedback voltage; and an inverting input coupled to the VCO control voltage; such that the VCO control voltage is substantially equal to the VDAC feedback voltage.

11. The circuit of claim 10, wherein the VDAC feedback circuitry comprises:

increment and decrement comparators responsive to a voltage based on the sensed loop filter current to respectively generate increment and decrement signals; and

inc/dec logic responsive to the increment and decrement signals to generate the discrete-level VDAC feedback voltage.

12. The circuit of claim 11, wherein the current sense circuitry outputs the sensed loop filter current at an output node coupled to the increment and decrement comparators, and wherein the VDAC feedback circuitry further comprises:

a capacitor C2 coupled between the output node, and a reference voltage Vref;

the increment and decrement comparators to generate the increment and decrement signals based on a deviation of a voltage V2 on C2 from Vref; and

reset circuitry coupled to C2 and responsive to a reset signal from the inc/dec logic to reset V2 to Vref after each increment and decrement signal;

such that an effective loop filter capacitance of the loop filter circuitry is a multiplication of a capacitance of C2.

13. The circuit of claim 9, wherein the current sense circuitry comprises:

a current mirror with a mirror input leg including a mirror input node coupled to receive

the input loop filter current, and a mirror output leg including a mirror output node to provide the sensed loop filter current, the mirror output node coupled to the VDAC feedback circuitry; and

a source follower transistor included in the mirror input leg, and controlled by the VDAC circuitry to sense the input loop filter current, which is mirrored as the sensed loop filter current to the mirror output leg based on a pre-defined mirror-ratio.

14. The circuit of claim 13, wherein the VDAC circuitry comprises:

an amplifier to provide a control input to the source follower transistor, the amplifier having: a noninverting input coupled to receive the VDAC feedback voltage; and an inverting input coupled to the VCO control voltage; such that the VCO control voltage is substantially equal to the VDAC feedback voltage.

15. The circuit of claim 14, wherein the VDAC feedback circuitry further comprises:

a capacitor C2 coupled between the mirror output node, and a reference voltage Vref;

the VDAC feedback circuity to generate the discrete-level VDAC feedback voltage, incremented and decremented based on a deviation of a voltage V2 on C2 from Vref, corresponding to the sensed loop filter current; and

reset circuitry coupled to C2 and responsive to a reset signal from the inc/dec logic to reset V2 to Vref after each increment and decrement of the VDAC feedback voltage;

such that an effective loop filter capacitance of the loop filter circuitry is a multiplication of a capacitance of C2 based on the deviation in V2 and the mirror-ratio.

16. The circuit of claim 9, wherein the loop filter circuitry comprises a charge pump loop filter.

17. The circuit of claim 9, wherein the circuit comprise one of a phase-locked loop system, and a clock data recovery system.

18. A method suitable for simulating a loop filter capacitor function in a VCO (voltage controlled oscillator), comprising:

sensing an input loop filter current, and providing a corresponding sensed loop filter current; and

providing a VCO control voltage by: generating a discrete-level VDAC feedback voltage that is incremented and decremented based on the sensed loop filter current; generating a VDAC control voltage using a VDAC (voltage digital to analog converter) based on the discrete-level VDAC feedback voltage; providing the VDAC control voltage to a non-inverting input to an

amplifier; and generating the VCO control voltage at a loop filter output node coupled to an inverting input to the amplifier, the VCO control voltage based on the VDAC feedback voltage, which is based on the sensed loop filter current.

19. The method of claim 18, wherein the voltage based on the sensed loop filter current is generated using:

a capacitor C2 coupled to receive the sensed loop filter current;

incrementing and decrementing the VDAC feedback voltage based on a deviation of a voltage V2 on C2 from a voltage reference Vref; and

resetting the V2 voltage on C2 to Vref after each increment and decrement of the VDAC feedback voltage;

such that an effective loop filter capacitance of the loop filter circuitry is a multiplication of a capacitance of C2.

20. The method of Claim 18, where the input loop filter current is sensed using:

a current mirror with a mirror input leg including a mirror input node coupled to receive the input loop filter current, and a mirror output leg including a mirror output node to provide the sensed loop filter current, the mirror output node coupled to the VDAC feedback circuitry; and

a source follower transistor included in the mirror input leg, and controlled by the VDAC circuitry to sense the input loop filter current, which is mirrored as the sensed loop filter current to the mirror output leg based on a pre-defined mirror-ratio.

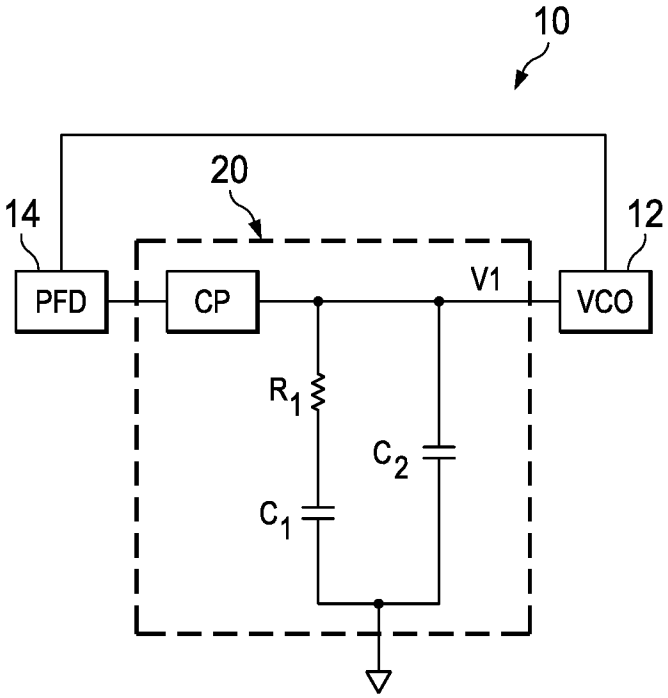

10
20
14
12
PFD
CP
V1
VCO
R1
C2
C1

FIG. 1

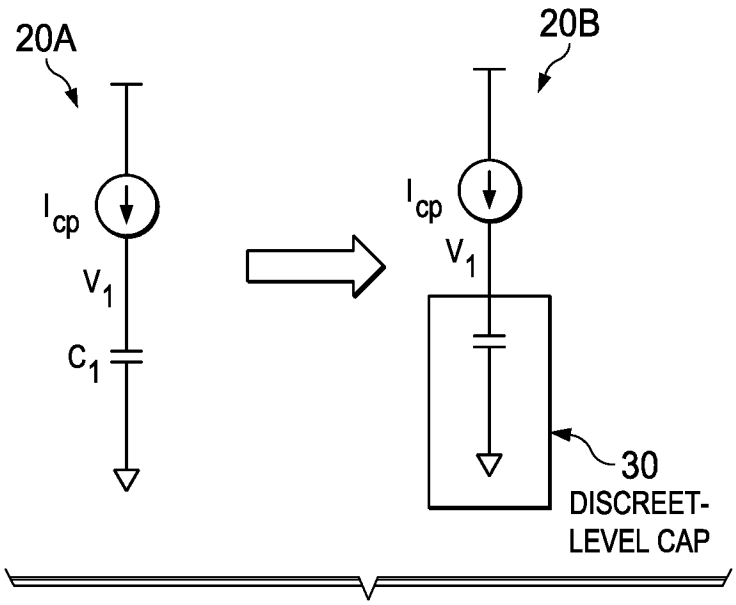

20A
20B
Icp
V1
C1
Icp
V1
30
DISCREET-
LEVEL CAP

FIG. 2

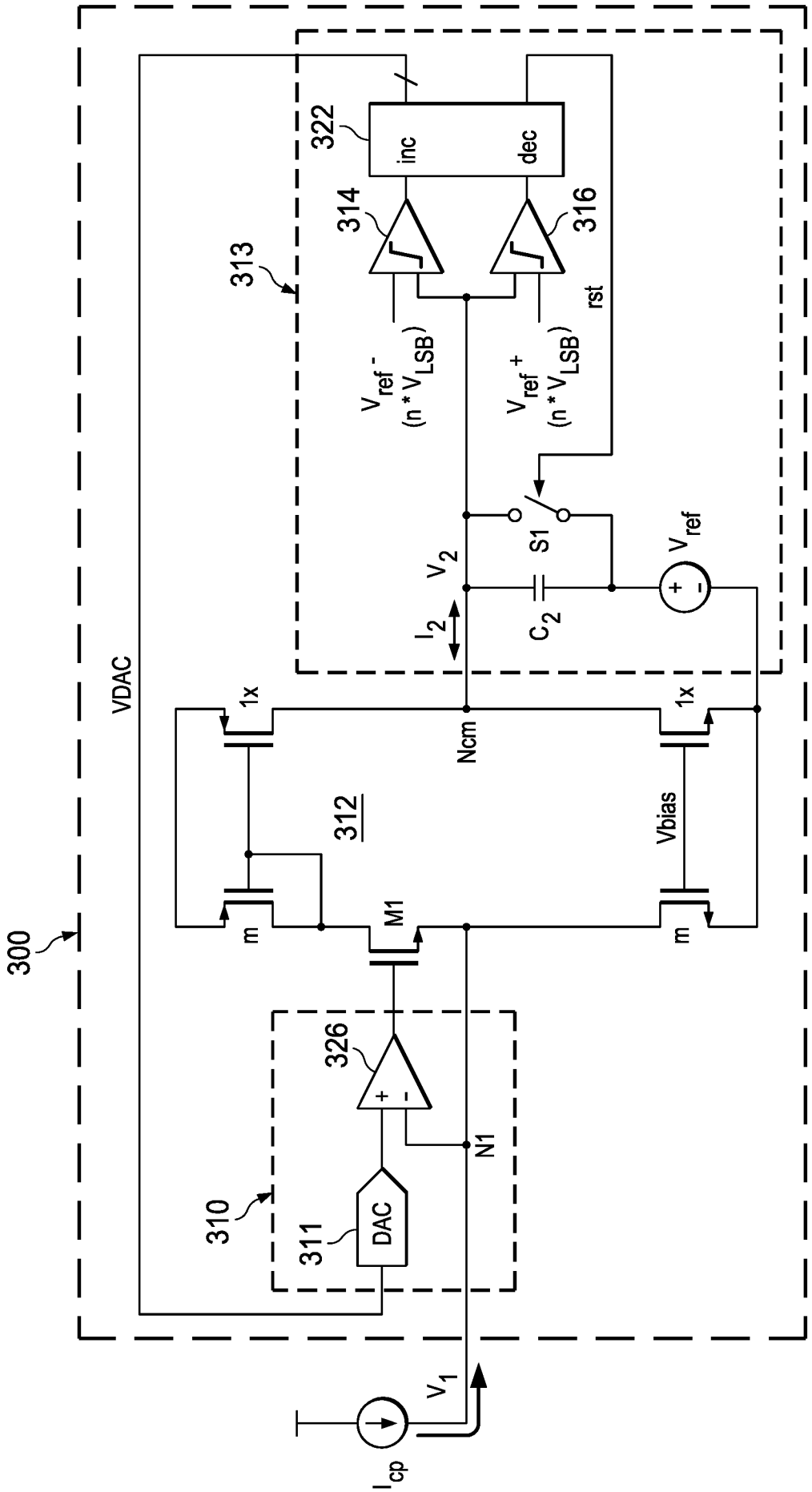

300
VDAC
313
322
inc
dec
314
316
rst
V_{ref}^{-} ($n*V_{LSB}$)
V_{ref}^{+} ($n*V_{LSB}$)
S1
V_{ref}
V_2
I_2
C_2
1x
Ncm
1x
312
Vbias
m
M1
m
326
N1
310
311
DAC
V_1
I_{cp}

FIG. 3

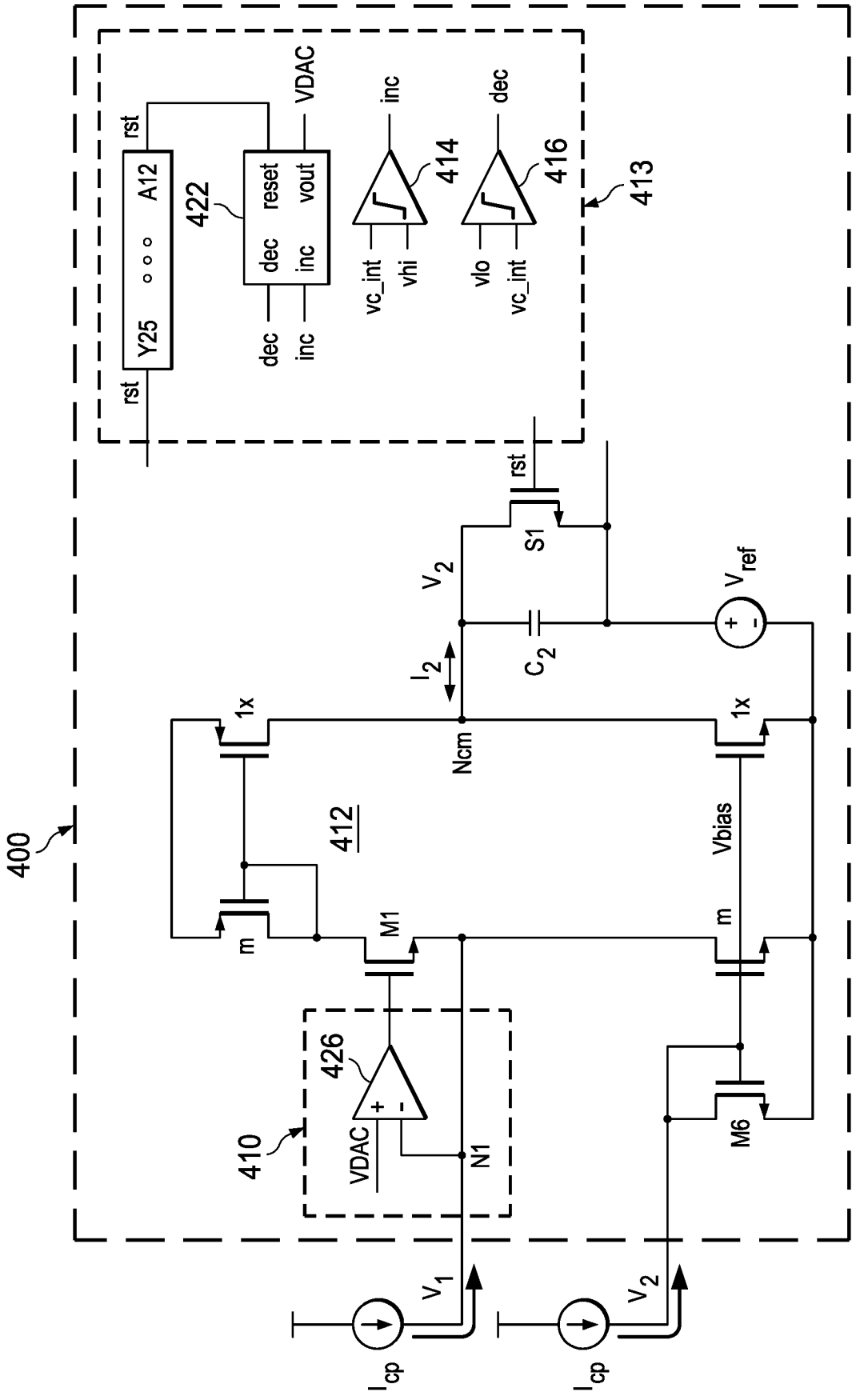

400
413
rst
A12
Y25
422
reset
vout
dec
inc
VDAC
414
416
vc_int
vhi
vlo
S1
V_2
V_{ref}
C_2
I_2
Ncm
1x
412
Vbias
m
M1
M6
426
410
VDAC
N1
V_1
I_{cp}

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2016/068132

A. CLASSIFICATION OF SUBJECT MATTER

H03B 29/00 *(2006.01)*
H03L 7/085 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03B 5/00 –29/00, H03L 7/00 –9/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, K-PION, Esp@cenet, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 8188798 B1 (CHI TAK (GERRY) LEUNG et al) 29.05.2012	1-20
A	US 6753738 B1 (REX T.BAIRD) 22.06.2004	1-20
A	US 8278984 B2 (PASQUALE LAMANNA et al) 02.10.2012	1-20
A	US 8781046 B2 (FRANCOIS GUILLOT et al) 15.07.2014	1-20
A	US 8154351 B2 (TADJPOUR SHAHRZAD) 10.04.2012	1-20
A	EP 1422822 A2 (MOTOROLLA, INC.) 26.05.2004	1-20
A	US 7583151 B2 (INTEL CORPORATION) 01.09.2009	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 April 2017 (13.04.2017)	20 April 2017 (20.04.2017)

Name and mailing address of the ISA/RU:
Federal Institute of Industrial Property,
Berezhkovskaya nab., 30-1, Moscow, G-59,
GSP-3, Russia, 125993
Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37

Authorized officer

L. Ptentsova

Telephone No. (499) 240-25-91