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(19)

(54) IMPROVEMENTS IN OR RELATING TO ELECTRICAL CHECKING CIRCUITS

(71) We, STANDARD TELEPHONES AND CABLES LIMITED, a British Company of 190 Strand, London W.C.2, England, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to a majority logic circuit, also known as a voting circuit, and to checking arrangements in which such circuits are used.

In electronic systems, such as data processing and telecommunication systems, in the interest of system security it is common practice for control equipments to be triplicated. The three control equipments operate simultaneously and in parallel and their outputs are constantly checked for discrepancies. If a discrepancy is detected an alarm is given and the faulty equipment disabled. In such case the fault indication is given when one equipment's output differs from that of the other two, when the output from the other two is assumed to be correct. Often, especially where intelligence is conveyed parallel-wise, a number of majority logic circuits are needed, so that relatively simple circuits of this type are needed.

Accordingly it is an object of the invention to provide a simple and economical majority logic circuit.

According to the present invention there is provided a majority logic circuit, which includes a full adder module having three inputs to which the three signals to be compared are applied and two outputs, wherein when the electrical conditions on the three inputs all have the same binary condition both of said outputs have the same binary condition, wherein when the electrical condition of one of the inputs differs from that of the other two inputs one of the outputs is at binary 0 and the other of said outputs is at binary 1, wherein the output condition of at least one of said outputs is used to give a majority of logic indication, and wherein the two outputs of the adder are applied to a monitoring device which gives an alarm indication if the conditions of the two outputs differ, indicating that the electrical condition of one of the inputs differs from that of the other two inputs.

As will be seen later, the principles set out above for a 2-out-of-3 majority logic circuit are extendable to give a 3-out-of-5 logic circuit.

Thus, according to a further embodiment of the invention there is provided a circuit for the provision of a three-out-of-five majority logic circuit, which includes a four-bit parallel binary full adder, in which three of the inputs are connected to the carry-in terminal and the two bit input terminals of the first stage of the adder, in which the sum output of the first stage provides one output for a three-out-of-five logic operation based on the first three logic inputs, in which the sum output of the second stage provides the other and voting output for said three inputs and is also connected to both bit inputs of the second stage of the adder, in which the fourth and fifth logic inputs are connected to the bit inputs of the third stage, in which the sum outputs of the first and second stages of the adder are also connected respectively to the bit inputs of the fourth stage, in which the carry output from the fourth stage provides the three-out-of-five majority logic voting output, and in which the outputs of the adder go to a monitoring device which gives an alarm indication in respect of discrepancies between the three outputs.

Embodiments of the invention will now be described with reference to the drawings of which Figs. 1 to 4 accompanied the Provisional Specification while Figs. 5 and 6 are the accompanying drawings. In these drawings,

Fig. 1 is a majority logic circuit embodying the invention.

Fig. 2 shows how a commercially available four-bit adder integrated circuit unit can be used to provide the comparison functions for two circuits embodying the invention.

Fig. 3 shows the application of a number of circuits such as Fig. 1 in a "three-level" logic system.

Fig. 4 is explanatory of certain checking

functions which can be performed with circuits such as Fig. 1.

Fig. 5 shows how a commercially available four-bit adder integrated circuit unit can be used to give a 3-out-of-5 majority logic circuit.

Fig. 6 is a monitoring circuit for use with the circuit of Fig. 5.

Fig. 1 shows a full adder FA, which is preferably an integrated circuit unit having three inputs A, B and CI, of which inputs A and B usually receive the two numbers to be added, and input CI is the Carry-in input. As used in a majority decision circuit the outputs of three triplicated but similar equipments X, Y and Z are connected to the three inputs.

The adder has two outputs, a sum output Σ and a carry-out output CO, which form the S (Sum) and V (Vote) inputs respectively to a monitoring circuit MC. The operation of the full adder FA is such that if all three inputs X, Y and Z are at binary 0, then both outputs S and V are at binary 0, while if all three inputs X, Y and Z are at binary 1 then both outputs S and V are at binary 1. That is, as long as the three triplicated equipments being monitored continue to produce identical outputs, the condition of the two inputs to MC are identical. MC is a simple monitoring device which compares its two inputs and gives a first output if they are identical and a second output if they differ. Such a circuit could be an EXCLUSIVE OR gate or a half adder. Whichever is used the circuit MC gives one output when all three inputs to the adder are the same, and a different output if there is any discrepancy between the inputs to the adder. In the second case, the discrepancy output acts as an alarm condition, and causes the monitored system to use as the effective output the condition which appears on two of the inputs X, Y, Z. At the same time an alarm is given to cause the faulty equipment to be identified, so that it can be replaced or repaired. The effective output from the full adder FA, which provides the output from the monitored equipments, and thus extends to the next system stage, comes from the V output.

Fig. 2 shows how a single integrated circuit package providing the four-bit addition function, e.g. that coded 7483, can be used to provide the comparison functions for two majority logic circuits. When such a circuit is used as a four-bit adder, the two four-bit binary adders are applied to A1—A2—A3—A4 inputs and B1—B2—B3—B4 inputs with the sum appearing at the $\Sigma 1$, $\Sigma 2$, $\Sigma 3$ and $\Sigma 4$ outputs. There is also a carry-in input C0, internal carry connections, and a fourth bit carry output C4. The first of these circuits uses A1, B1 and C0 inputs, which are the two least significant "data" inputs for the first stage, plus the carry-in input therefor, A2 and B2 are connected together and to earth (or other suitable reference potential), so that the Σ_2 output is equal to the carry-out from the first stage. Thus there is no effective carry-out from the second to the third stage of the four-bit adder. Hence the $\Sigma 1$ and $\Sigma 2$ outputs form the inputs to the monitoring circuit MC1 for the first of the majority decision circuits.

Inputs A3 and B3 are connected together and to X2 which ensures that the carry-out from the third stage into the fourth stage is equal to X2. The other inputs to the fourth stage are connected to Y2 and Z2, and the outputs which go to the second monitoring circuit MCII come from $\Sigma 4$ and C4, the latter being the carry-out from the fourth stage of the multi-bit adder.

One of the hazards of using a voting circuit is that an internal fault in the integrated circuit which does not appear at the terminals of the device during normal operation can combine with an additional fault external to the device to cause the system to fail. This risk is minimized by the use of full adders as described above since the use of two outputs from each full adder presents an additional checking facility. Thus when a dormant fault such as just mentioned occurs, the voltages of the two outputs S and V (Fig. 1) disagree. Under the no-fault condition, V and S agree, and by monitoring those two output terminals the probability of internal faults remaining undetected decreases.

The majority decision circuits such as described above can be used in the interfaces between security units, and Fig. 3 shows how three majority logic circuits ML1, ML2 and ML3 are used between the equipments of security unit n and $n+1$, each of which has three levels. Every level of each security unit is preceded by a majority logic circuit ML which receives inputs from the three levels of the preceding security unit. The correct output which is calculated by the majority logic circuit is presented to the next security unit, and preferably also to an alarm monitor such as MC, Fig. 1.

To increase the rate of data transfer between the units the interface usually consists of facilities for the passage of several signals in parallel, using several majority logic circuits. Thus it is important for the majority decisions to be performed efficiently and with a high degree of reliability. In this arrangement faults are contained within one level of one security unit, and overall system reliability is greatly increased.

To get the full benefit from the majority logic circuit used in a system such as Fig. 3, it is possible to monitor both outputs of the three logic levels, as will be described with reference to Fig. 4. This uses a process of comparison which in effect extends the principles used in the circuits MC. As shown in Fig. 4, the S and V outputs of all three

levels are scanned, which reveals some at least of the internal faults. Thus consider an open-circuit lead at Z_1, on level I. The output V_1I does not show this fault but output S_1I does, and by comparing S_1I, S_1II and S_1III the faults can be detected. Even when Z_1I and Z_1II are faulty, by monitoring the S outputs the fault is detected but not located. The same principles apply for faults on X_2, Y_2, Z_2. Thus the probability of undetected faults on the majority logic circuits is reduced, and in some cases it is possible to avoid the case of additional expensive circuits for monitoring the logic circuit to detect internal faults.

The principle on which the three-input majority logic are based can be extended, as will be described with reference to Fig. 5 to a three-out-of-five majority decision circuit, using the same type of four-bit adder as used in Fig. 2.

The first stage of the adder works as a 2-out-of-3 majority logic circuit, with inputs X—Y—Z to the adder's C0, A_1 and B_1 terminals. This gives the sum output Sxyz at Σ_1 and the vote output at the carry output of the first stage. With the Σ_2 outputs connected back to A_2 and B_2 terminals as shown, this carry output appears at Σ_2, as shown. The other two inputs V and W are connected to the A_3 and B_3 terminals, and Vxyz and Sxyz are also connected to the A_4 and B_4 terminals so that the final carry from C_4 gives a V_T voting output for the device.

When X, Y and Z are all at the same logic level, Vxyz and Sxyz are the same, and they cause the carry out from the fourth stage, V_T, to be the same as Vxyz.

When X, Y and Z are not all at the same logic level, Vxyz and Sxyz are different, and cause the carry-out from the fourth stage, V_T, to be the same as the carry-out for the third stage. As Vxyz is also fed to both second stage inputs, the carry-out from the second stage is the same as Vxyz.

When the inputs V and W to the third stage are not the same, the carry-out from that stage, and hence V_T, becomes the same as the carry-out of the second stage, Vxyz, i.e. 1-out-of-2 plus 2-out-of-3=3-out-of-5.

When the inputs to the third stage V and W are the same the carry-out from the third stage, and hence V_T is the same as V and W, i.e. 2-out-of-2 plus 2-out-of-3 or 1-out-of-3=3 or 4-out-of-5.

The above logical combinations are detailed in the following truth tables.

W	V	Z	Y	X	Vxyz	Sxyz	V_T
0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0
0	0	0	1	0	0	1	0
0	0	0	1	1	1	0	0
0	0	1	0	0	0	1	0
0	0	1	0	1	1	0	0
0	0	1	1	0	1	0	0
0	0	1	1	1	1	0	0
0	1	0	0	0	0	0	0
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	1	0
0	1	1	0	1	1	0	1
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1	0	1	1	1	1	1	1
1	1	0	0	0	0	0	0
1	1	0	0	1	0	1	1
1	1	0	1	0	0	1	1
1	1	0	1	1	1	0	1
1	1	1	0	0	0	1	1
1	1	1	0	1	1	0	1
1	1	1	1	0	1	0	1
1	1	1	1	1	1	1	1

Fig. 6 shows one example of a monitoring circuit for use in conjunction with a 3-out-of-5 device such as that of Fig. 5. Here we have two EXCLUSIVE OR gates, one for Vxyz and Sxyz to indicate discrepancy between X, Y, Z and the other for Σ_3 and Σ_4 to indicate discrepancy between V, W and Vxyz when there is no discrepancy between X, Y and Z. These two in their turn feed an OR device, as shown.

WHAT WE CLAIM IS:—

1. A majority logic circuit, which includes a full adder module having three inputs to which the three signals to be compared are applied and two outputs, wherein when the electrical conditions on the three inputs all have the same binary condition both of said outputs have the same binary condition, wherein the electrical condition of one of the inputs differs from that of the other two inputs one of the outputs is at binary 0 and the other of said outputs is at binary 1, wherein the output condition of at least one of said outputs is used to give a majority logic indication, and wherein the two outputs of the adder are applied to a monitoring device which gives an alarm indication if the conditions of the two outputs differ, indicating that the electrical condition of one of the inputs differs from that of the other two inputs.

2. A circuit for the provision of two separate majority logic circuits each as claimed in claim 1 are provided by the use of a four-bit parallel binary full-adder, in which the adder's carry-in input and its first bit place inputs are used as the three inputs for the first majority logic circuit, in which the first and second sum outputs are

used as two outputs of the first majority logic circuit in which the two second bit place inputs are grounded, in which the two third place bits are connected together and to one of the inputs of the second majority logic circuit, the two fourth place bits providing the other two inputs of the second majority logic circuit, in which the outputs of the second majority logic circuit are provided by the fourth bit sum output and the fourth bit carry output, and in which the two majority logic circuits each has its own monitoring device.

3. A circuit for the provision of a three-out-of-five majority logic circuit, which includes a four-bit parallel binary full adder, in which three of the inputs are connected to the carry-in terminal and the two bit input terminals of the first stage of the adder, in which the sum output of the first stage provides one output for a three-out-of-five logic operation based on the first three logic inputs, in which the sum output of the second stage provides the other and voting output for said three inputs and is also connected to both bit inputs of the second stage of the adder, in which the fourth and fifth logic inputs are connected to the bit inputs of the third stage, in which the sum outputs of the first and second stages of the adder are also connected respectively to the bit inputs of the fourth stage, in which the carry output from the fourth stage provides the three-out-of-five majority logic voting output, and in which the outputs of the adder go to a monitoring device which gives an alarm indication in respect of discrepancies between the three outputs.

4. A circuit as claimed in claim 3, and in which said monitoring device includes a first EXCLUSIVE-OR gate to the inputs of which are applied the sum outputs of the first two stages of the adder, a second EXCLUSIVE-OR gate to the inputs of which are applied the sum outputs of the last two stages of the adder, and an OR gate to the inputs of which are applied the outputs of the two EXCLUSIVE-OR gates.

5. A majority logic circuit substantially as described with reference to Figs. 1, 2, or 5 and 6 of the drawings.

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For the Applicants.

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1560243 PROVISIONAL SPECIFICATION
1 SHEET This drawing is a reproduction of the Original on a reduced scale

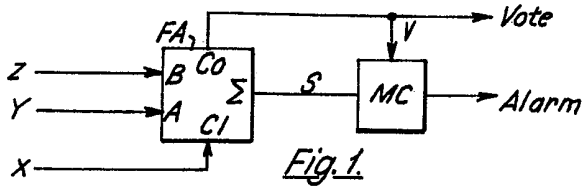


Fig.1.

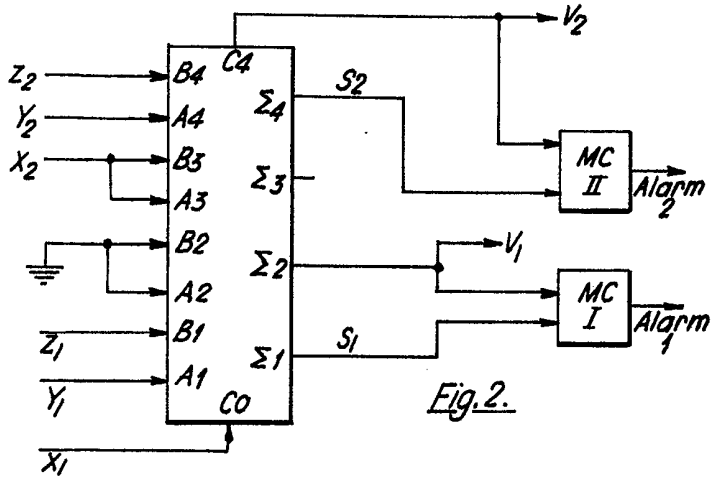


Fig.2.

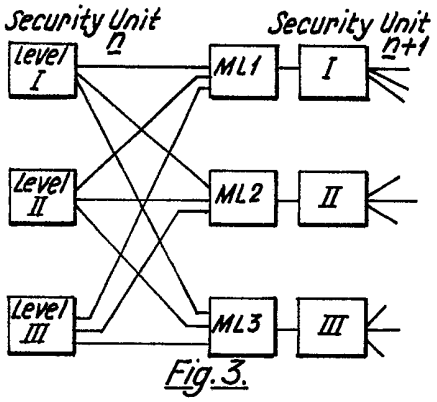


Fig.3.

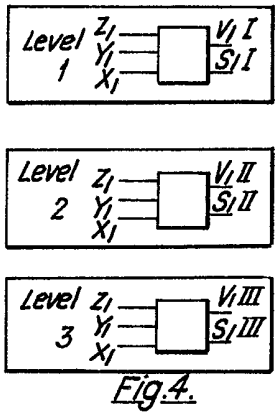
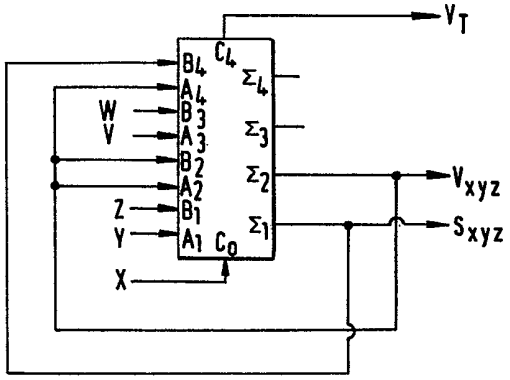


Fig.4.

Fig.5.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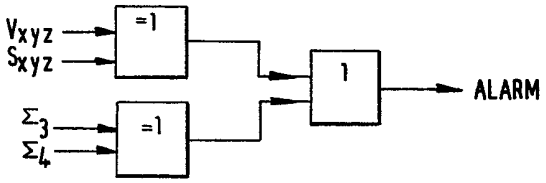
C_4
B_4
A_4
W
V
B_3
A_3
B_2
A_2
Z
Y
B_1
A_1
C_0
X
Σ_4
Σ_3
Σ_2
Σ_1
V_{xyz}
S_{xyz}

Fig.6.


V_{xyz}
S_{xyz}
=1
Σ_3
Σ_4
=1
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ALARM