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(71) Applicant: **MILLENNIAL NET, INC.** [US/US]; One Canal Park, Cambridge, MA 02141 (US).

(72) Inventors: **SOKWOO, Rhee**; 25 Webster Avenue, #305, Sommerville, MA 02143 (US). **SHENG, Liu**; 615 Green Street, Cambridge, MA 02139 (US).

(74) Agents: **KAMERER, Bruce, E.** et al.; Iandiorio & Teska, 260 Bear Hill Road, Waltham, MA 02451-1018 (US).

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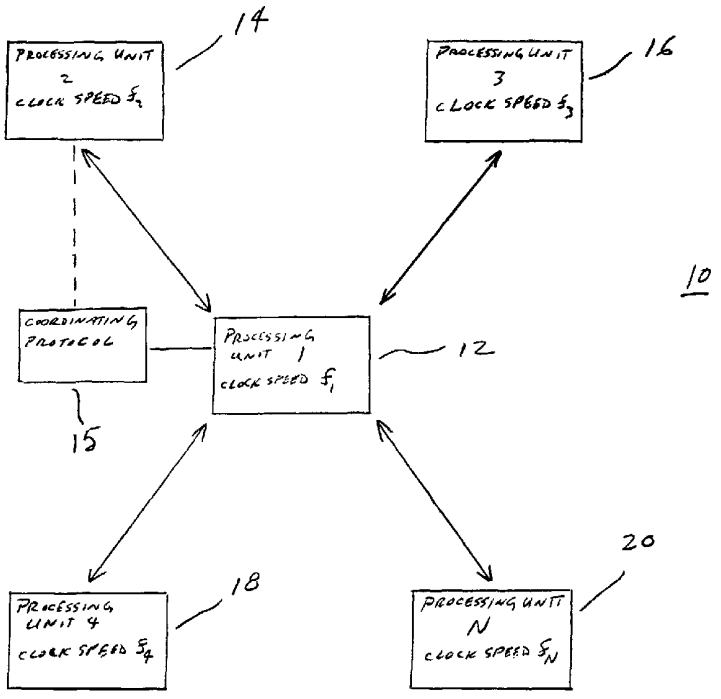
(54) Title: NETWORKED PROCESSING SYSTEM WITH OPTIMIZED POWER EFFICIENCY



(57) Abstract: A multi-processor computing system (10) including a plurality of processing units (12, 14, 16, 18, 20) is provided in which each of the plurality of processing units operates at a clock frequency and a coordinating protocol (15) is used to assign tasks and operations to any of the plurality of processing units in a manner such that the power efficiency of the system is optimized.

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NETWORKED PROCESSING SYSTEM WITH OPTIMIZED POWER EFFICIENCY

FIELD OF THE INVENTION

This invention relates to a networked processing system with an optimized power efficiency.

RELATED APPLICATIONS

This application claims benefit of U.S. Provisional Application Serial No. 60/244,502 filed October 31, 2000 and entitled I-BEAN: AN INTEGRATED WIRELESS COMMUNICATION AND COMPUTING DEVICE USING NOVEL POWER SAVING ALGORIGHMS FOR MINIMAL ENERGY OPERATIONS.

BACKGROUND OF THE INVENTION

Power efficiency and minimizing power usage are important issues in networked systems, such as communications systems and computing systems. Programs which monitor the usage of various components of a computer system and shut down or minimize some of those components have been used in the past.

However, one area in which such power conservation has not been utilized is with respect to processing units. Whether in networked computer systems or communications systems, optimizing the power efficiency of processing units has not been previously addressed. For example, computer systems with multiple processors operate all processors in parallel at the same time to improve overall system performance without consideration to the power usage involved.

In multiple processor systems, specific tasks such as disk operations, display operations and keyboard input may be assigned to each processor. Another method of improving performance is to assign specific programs, such as word processing and spreadsheet programs, to separate processors. What these systems fail to address is the power used when the processor units are idling. Even when idling, processors are using power with every tick of the processor clock. For high speed processors, this can result in a substantial power usage.

This problem is particularly evident in portable units where the power is limited to that which is available from batteries. One solution used in laptop computers is to slow the processor speed when the laptop computer is running on battery. For example, a processor chip may operate at 1GHz when the computer is connected to an AC power outlet and at 500MHz when running on the internal battery. This results in a significant impact on the performance of the system.

Likewise, communications systems such as cellular phones experience considerable idle time during which power continues to be used in order to keep the system ready to transmit or receive signals. This use of power even when idling causes portable, battery-powered units to require frequent recharging.

SUMMARY OF THE INVENTION

It is therefore an object of this invention to provide a networked processing system in which power usage is minimized.

It is a further object of this invention to provide a networked processing system in which performance is optimized.

It is a further object of this invention to provide a multi-tasking, multiple

processor system in which the power efficiency is optimized.

It is a further object of this invention to provide a self-contained, miniaturized computer with a built in power source, flash memory, digital I/O interface and radio frequency (RF) transceiver for bi-directional communication.

The invention results from the realization that, in a multi-tasking, multi-processor environment, the power efficiency of the system can be optimized by coordinating the usage of processing units such that tasks are run on the appropriate speed processing unit and unused processing units are placed in sleep mode.

This invention features a networked computing system with improved power consumption comprising a plurality of processing units including at least first and second processing units. A coordinating protocol is operative on the first and second processing units and controls the operation of the system such that the power consumption of the system is minimized.

In a preferred embodiment, the first and second processing units are interconnected. The first processing unit operates at a first clock frequency, and the second processing unit operates at a second clock frequency. The first clock frequency may be lower than the second clock frequency.

The first processing unit assigns a task to the first or second processing units based on the clock frequency required to run the task such that the minimum power is used. The first processing unit may instruct the second processing unit to enter a minimum power usage mode. The first processing may activate the second processing unit from the minimum power usage mode when a task is to performed by the second processing unit. The first processing unit may transfer the coordinating protocol to the second processing unit.

The processing units may be communications device which may be bi-directional communications devices. The first processing unit may instruct the second processing unit to enter a minimum power usage mode for a preprogrammed time. The second processing unit may poll the first processing unit after the preprogrammed time. The preprogrammed time may be variable.

This inventions also provides a multiple processor computer system comprising a plurality of processing units, each of the plurality of processing units operating at a clock frequency. A first processing unit operates at a clock frequency lower than the remaining processing units. A coordinating protocol is operable on the first processing unit and coordinates the operation of the system such that the power efficiency is optimized.

In a preferred embodiment, each of the plurality of processing units operates at a different clock frequency. The first processing unit may transfer the coordinating protocol to a second processing unit of the plurality of processing units. The second processing unit may transfer the coordinating protocol to any of the plurality of processing units.

This invention also features a wireless communication system comprising a base unit and a plurality of terminal units in communication with the base unit. Each of the plurality of terminal units has a duty cycle. The base unit controls the duty cycle of each of the plurality of terminal units to optimize the power efficiency of the system.

In a preferred embodiment, the base unit may instruct at least one of the terminal units to enter a minimum power consumption mode for a preprogrammed time. The base unit and the plurality of terminal units may be bi-directional. The

terminal unit may poll the base unit after the preprogrammed time.

This invention also features a method for optimizing the power efficiency of a multi-processor computer system including the steps of providing a plurality of processing units including at least first and second processing units, each processing unit operating at a clock frequency, and operating a coordinating protocol on the first processing unit. The coordinating protocol is operative to receive a request to perform a task, determine to which of the processing units to assign the task, and assign the task to one of the plurality of processing units. The coordinating protocol determines which processing unit to which a task is to be assigned based on optimizing the power efficiency of the system.

The method may also include the steps of transferring the coordinating protocol from the first processing unit to the second processing unit based on the speed required to run the coordinating protocol. The coordinating protocol may be further transferred from the second processing unit to any of the plurality of processing units based on the speed required to run the coordinating protocol.

This invention also features a self-contained, miniaturized computer system including first and second processing units, the first processing unit including a coordinating protocol operable to coordinate the operation of the first and second processing units, a power source, a flash memory module and a RF transceiver, wherein the coordinating protocol assigns tasks to the first and second processing units to optimize the power efficiency of the system.

In a preferred embodiment, the first processing unit operates at a clock frequency of 32 kHz and the second processing unit operates at a clock frequency of 4 MHz. The power source may be a battery.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features and advantages will occur to those skilled in the art from the following description of a preferred embodiment and the accompanying drawings, in which:

Fig. 1 is a schematic diagram of a networked processing system according to the subject invention;

Fig. 2 is a block diagram of a bi-directional wireless communication system according to the subject invention;

Fig. 3 is a timing diagram illustrating the transfer of the coordinating protocol among processing units according to the subject invention;

Fig. 4 is a block diagram of the method of the subject invention; and

Figs. 5A, 5B and 5C are block schematic diagrams of a self-contained computer according to the subject invention.

PREFERRED EMBODIMENT

Networked processing system 10, Fig. 1, includes a number of interconnected processing units 12, 14, 16, 18, and 20. There should be at least two interconnected processing units, and there may be any number N of these processing units in system 10. Each processing unit operates at a given clock frequency, f_1, f_2, f_3, f_4,...f_N, respectively. The clock frequencies may all be the same, one or more of the clock frequencies may be the same, or all of the clock frequencies may be different. In a preferred embodiment, each processing unit operates at a different clock frequency, with $f_1<f_2<f_3<f_4<...f_N$.

Processing units 12, 14, 16, 18 and 20 may be central processing units (CPUs) used in many desktop and portable computers today. These processing units may be networked externally, i.e., one or more processing unit may be located in a separate enclosure, or they may be networked internally, i.e., the processing units may be located on a single circuit board or interconnected via an internal data bus in the same computer enclosure.

In operation, processing unit 12 includes a coordinating protocol 15 which is used to control the operation of system 10 by assigning tasks and operations to various processing units based upon the speed required to perform a given task of function. Coordinating protocol 15 is designed to assign tasks to the various processing units with the result being the optimization of the power efficiency of system 10.

For example, the coordinating protocol will allow processing unit 12 to assign a given task or operation to itself or to any other processing unit 14, 16, 18 or 20 based upon the speed requirements of the task or operation and the clock frequencies of the various processing units. Tasks and operations which require lower clock frequencies, which may include such tasks as refreshing a display or operations such as processing keyboard entries, will be assigned to processing units with lower clock frequencies. Because those processing units operate at lower clock frequencies, the power efficiency of the system as a whole will be optimized. When the task load of the system is low enough, processing units may even be shut off or placed into a "sleep" mode to further optimize the power efficiency of the system. One processing unit will always need to remain active to run the coordinating protocol so it may reactivate any processing units which have been shut down.

In a preferred embodiment, the coordinating protocol may be transferred from one processing unit to another processing unit. As shown in Fig. 3, there are N processing units 50, 52, 54, each operating at a respective clock frequency of f_1, f_2,...f_N, with $f_1 < f_s < ... f_N$. Processing unit 50 is the "watchdog", i.e., the processing unit that runs the coordinating protocol, from time T_0 to time T_4. During that period, processing unit 50 activates processing unit 52 at time T_1, deactivates processing unit 52 at time T_2, and activates processing unit 54 at time T_3. At time T_4, processing unit 50 activates processing unit 52 and transfers the coordinating protocol to processing unit 52 which then becomes the "watchdog." Processing unit 52 deactivates processing units 50 and 54 at time T_5, reactivates processing unit 54 at time T_6, and reactivates processing unit 50 at time T_7. Processing unit 52 transfers the coordinating protocol back to processing unit 50 time at T_7, whereby processing unit 50 resumes the "watchdog" responsibility. Finally, processing unit 50 deactivates processing units 52 and 54 at time T_8.

Transferring the coordinating protocol between processing units is useful when the coordinating protocol itself requires a higher clock frequency than that of the lowest clock frequency available. For example, if the number of tasks requested is high enough, the coordinating protocol may require a clock frequency higher than that of the lowest clock frequency available to efficiently and effectively handle the assignment of the tasks to various processing units. Normally, the power efficiency is generally optimized when the coordinating protocol is run by the processing unit with the lowest clock frequency as this processing unit uses the minimum power when idling due to the low clock frequency.

One application of a computing system where this invention is particularly

useful is laptop, or other portable, computers. By using multiple processing units in a laptop combined with the coordinating protocol of this invention, it is possible to optimize the power consumption of the laptop computer such that the battery life is maximized.

In another embodiment, communications system 30, Fig. 2, includes base station 32 and at least one portable communications device 34. System 30 may include a plurality of M portable communications devices 34, 36, 38, 40, 42, and 44. Base station 32 is usually connected to a continuous power supply (not shown) such that the power efficiency of base station 32 is not relevant. However, portable communications device 34 (and 36, 38, 40, 42, and 44 in a multi-point system) are usually powered by batteries which have a finite amount of power. Therefore, optimizing the power efficiency of the system, and particularly of the portable communications device(s), is important. Even so, such optimization must also allow for the communications system to operate effectively, i.e., to be able to send and/or receive signals without significant delay.

In one embodiment, base station 32 is bi-directional and portable communications devices 34, 36, 38, 40, 42 and 44 are receive only devices. Base station 32 includes a coordinating protocol which controls the operation of the portable communications devices. For example, base station 32 controls the duty cycle of the portable communications devices by placing one or more of the portable communications devices in a minimum power usage mode for a preprogrammed time. After the preprogrammed time, the portable communications device automatically returns to the standby mode awaiting another signal. The minimum power usage mode uses less power than the standby mode. By placing a portable communications

devices into the minimum power usage mode, the power efficiency of that portable communications device is optimized.

The preprogrammed time may be variable. For example, if a particular portable communications device is required to be active very infrequently, the preprogrammed time is longer than for a portable communications device that is required to be used more frequently. This allows for the maximum efficiency in the power consumption of the system as a whole. Also, if a particular task is run less frequently, the preprogrammed time for a portable communications device on which that task is to be run may be longer than for a portable communications device on which a task that is run more frequently.

In another embodiment, portable communications devices 34, 36, 38, 40, 42, and 44 are also bi-directional. In this embodiment, base station 32 may put a portable communications device into minimum power mode for a preprogrammed time. However, because the portable communications device is bi-directional, after the preprogrammed time, the portable communications device may poll base station 32 to notify the base station that the portable communications device is once again in the standby mode. This allows base station 32 to transmit any signals which may have been queued up during the preprogrammed time.

In another embodiment, computer 60, Figs. 5A-5C, is a self-contained, miniaturized computer. Computer 60 includes first processing unit 62, RF transceiver 64, second processing unit 66 (Fig. 5B), low clock frequency crystal 68, high clock frequency crystal 70 and I/O connector 72 all mounted on circuit board 74. Power source 76, Fig. 5C, for example a battery, may be attached to circuit board 74.

The small size and low power consumption of computer 60 allows computer

60 to operate from battery 70 for its entire life span. In a preferred embodiment, first processing unit 62 operates at a clock frequency of 32 kHz, and second processing unit 66 operates at a clock frequency of 4 MHz. A coordinating protocol operates so that computer 60 may perform signal processing and RF transmission with optimum power efficiency. Such self-contained, miniaturized computers are useful in communications systems and locally networked computer systems.

A method for optimizing the power efficiency of a multi-processor computer system is also provided. Step 80 of providing a plurality of processing units, Fig. 4, includes providing at least first and second processing units. Each of the processing units operates at a clock frequency. In a preferred embodiment, the clock frequencies of each of the plurality of processing units is different, although this is not a necessary limitation. Step 82 of operating a coordinating protocol on the first processing unit includes receiving a request to perform a task, determining to which processing unit to assign the task, and assigning the task to a processing unit. In a preferred embodiment, step 84 of transferring the coordinating protocol from the first processing unit to the second processing unit may be included. In a further embodiment, step 86 of transferring the coordinating protocol from the second processing unit to any of the plurality of processing units may be included. Optional steps 84 and 86 provide for transferring the coordinating protocol based on the speed required to operate the coordinating protocol. For example, if the number of task requested is high, a higher clock speed processing unit may be required to run the coordinating protocol.

Although specific features of the invention are shown in some drawings and not in others, this is for convenience only as each feature may be combined with any

or all of the other features in accordance with the invention. The words "including", "comprising", "having", and "with" as used herein are to be interpreted broadly and comprehensively and are not limited to any physical interconnection. Moreover, any embodiments disclosed in the subject application are not to be taken as the only possible embodiments.

Other embodiments will occur to those skilled in the art and are within the following claims:

What is claimed is:

CLAIMS

1. A networked computing system with improved power consumption comprising:

a plurality of processing units including at least first and second processing units, said first processing unit including a coordinating protocol,

wherein the first processing unit utilizes the coordinating protocol to control the operation of the system such that the power consumption of the system is minimized.

2. The networked computing system of claim 1 wherein the first and second processing units are physically interconnected.

3. The networked computing system of claim 2 wherein the first processing unit operates at a first clock frequency and the second processing unit operates at a second clock frequency, the second clock frequency being higher than the first clock frequency.

4. The networked computing system of claim 3 wherein the first processing unit assigns a task to the first processing unit or the second processing unit based on the processing speed required by the task such that the minimum power is used to process the task.

5. The networked computing system of claim 3 wherein the first processing unit instructs the second processing unit to enter a minimum power usage

mode.

6. The networked computing system of claim 5 wherein the first processing unit activates the second processing unit from the minimum power usage mode when a task is to be performed by the second processing unit.

7. The networked computing system of claim 4 wherein the first processing unit switches the coordinating protocol from the first processing unit to the second processing unit.

8. The networked computing system of claim 1 wherein the first and second processing units are communications devices.

9. The networked computing system of claim 7 wherein the first processing unit coordinates the operation of the second processing unit to minimize power consumption of the system.

10. The networked computing system of claim 8 wherein the first processing unit instructs the second processing unit to enter a minimum power usage mode.

11. The networked computing system of claim 8 wherein the first and second processing units are bi-directional communications devices.

12. The networked computing system of claim 12 wherein the first processing unit coordinates the operation of the second processing unit to minimize the power consumption of the system.

13. The networked computing system of claim 13 wherein the first processing unit instructs the second processing unit to enter a minimum power consumption mode for a preprogrammed time.

14. The networked computing system of claim 14 wherein the second processing unit polls the first processing unit after the preprogrammed time.

15. The networked computing system of claim 13 wherein the preprogrammed time is variable.

16. A multiple processor computer system comprising:

a plurality of processing units, each of the plurality of processing units operating at a clock frequency, with at least a first processing unit operating at a clock frequency lower than the remaining processing units; and

a coordinating protocol operable on the first processing unit,

wherein the first processing unit coordinates the operation of the processing units such that the power efficiency of the computer system is optimized.

17. The multiple processor computer system of claim 16 wherein each of

the plurality of processing units operates at a different clock frequency.

18. The multiple processor computer system of claim 16 wherein the first processing unit transfers the coordinating function to a second processing unit of the plurality of processing units.

19. The multiple processor computer system of claim 18 wherein the second processing unit transfers the coordinating function to any of the plurality of processing units.

20. A wireless communication system comprising:

a base unit; and

a plurality of terminal units in communication with the base unit, each of the plurality of terminal units having a duty cycle,

wherein the base unit controls the duty cycle of the plurality of terminal units to optimize the power efficiency of the system.

21. The wireless communication system of claim 20 wherein the base unit instructs at least one of the terminal units to enter a minimum power consumption mode for a preprogrammed time.

22. The wireless communication system of claim 20 wherein the base unit and the terminal units are bi-directional.

23. The wireless communication system of claim 22 wherein the base unit instructs at least one of the terminal units to enter a minimum power consumption mode for a preprogrammed time.

24. The wireless communication system of claim 23 wherein at least one of the plurality of terminal unit polls the base unit after the preprogrammed time.

25. A method for optimizing the power efficiency of a multi-processor computing system comprising:

providing a plurality of processing units including at least a first and second processing unit, each of the plurality of processing units operating at a clock frequency; and

operating a coordinating protocol on the first processing unit, the first processing unit:

receiving a request to perform a task;

determining to which of the plurality of processing units to assign the task; and

assigning the task to one of the plurality of processing units.

26. The method of claim 25 wherein the first processing unit determines which processing unit to which a task is to be assigned based on optimizing the power efficiency.

27. The method of claim 25 further comprising the step of transferring the

coordinating protocol from the first processing unit to the second processing unit based on the speed required for the coordinating protocol.

28. The method of claim 27 further comprising the step of further transferring the coordinating protocol from the second processing unit to any of the plurality of processing units based on the speed required for the coordinating function.

29. A self-contained, miniaturized computer system comprising:

first and second processing units, the first processing unit including a coordinating protocol operable to coordinate the operation of the first and second processing units;

a power source;

a flash memory module; and

a RF transceiver,

wherein the first processing unit assigns tasks to the first and second processing units to optimize the power efficiency of the system.

30. The self-contained, miniaturized system of claim 29 wherein the first processing unit operates at a clock frequency of 32 kHz and the second processing unit operates at a clock frequency of 4 MHz.

31. The self-contained, miniaturized computer system of claim 30 wherein the power source is a battery.

32. The self-contained, miniaturized computer system of claim 30 wherein the first processing unit transfers the coordinating protocol from the first processing unit to the second processing unit.

33. The self-contained, miniaturized computer system of claim 32 wherein the second processing unit transfers the coordinating protocol from the second processing unit to the first processing unit.

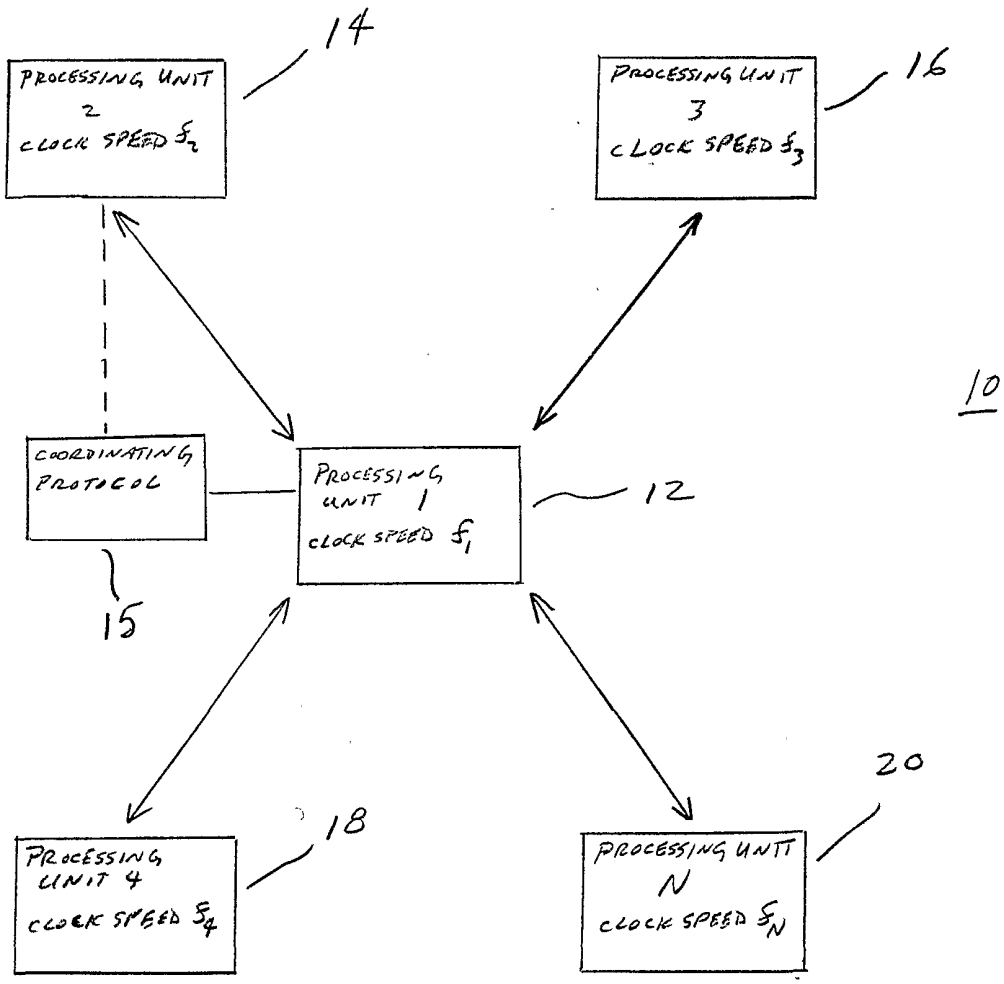

14
PROCESSING UNIT 2
CLOCK SPEED f_2
16
PROCESSING UNIT 3
CLOCK SPEED f_3
10
COORDINATING PROTOCOL
15
PROCESSING UNIT 1
CLOCK SPEED f_1
12
18
PROCESSING UNIT 4
CLOCK SPEED f_4
20
PROCESSING UNIT N
CLOCK SPEED f_N

FIG. 1

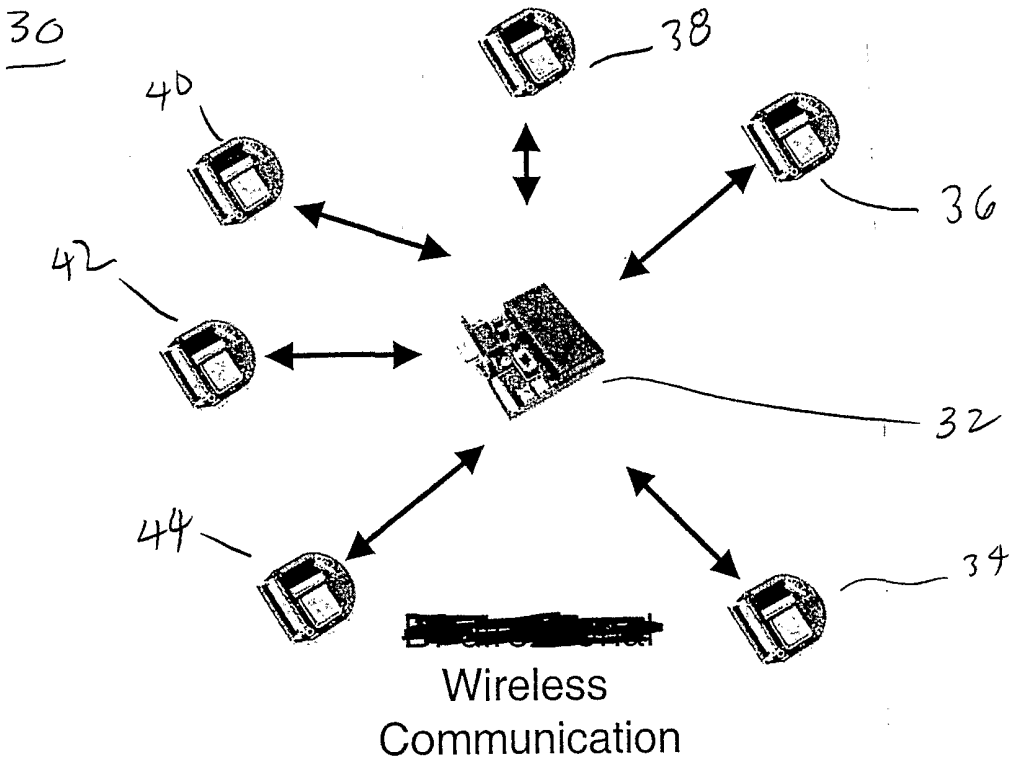
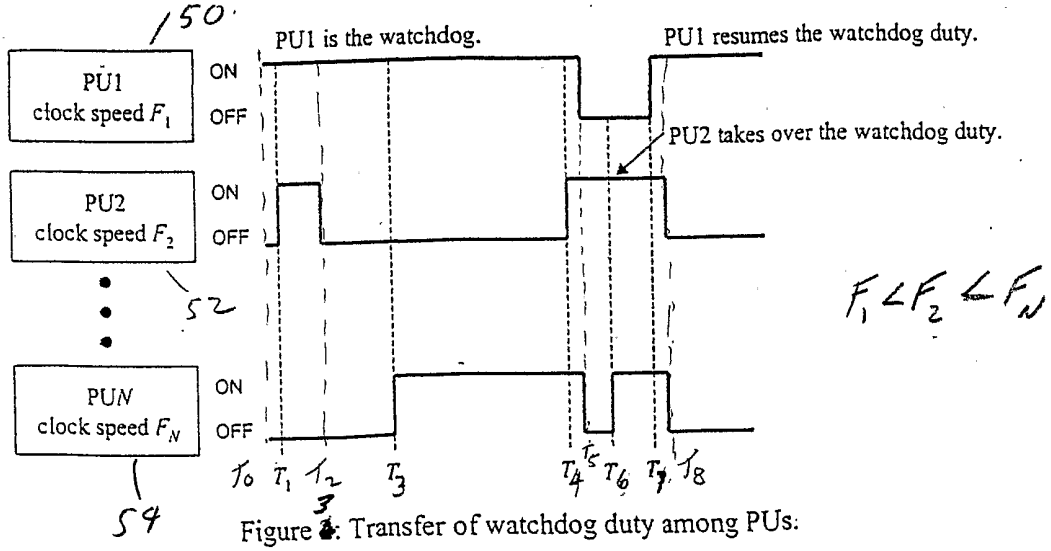


FIG. 2



$F_1 < F_2 < F_N$

Figure 3: Transfer of watchdog duty among PUs.

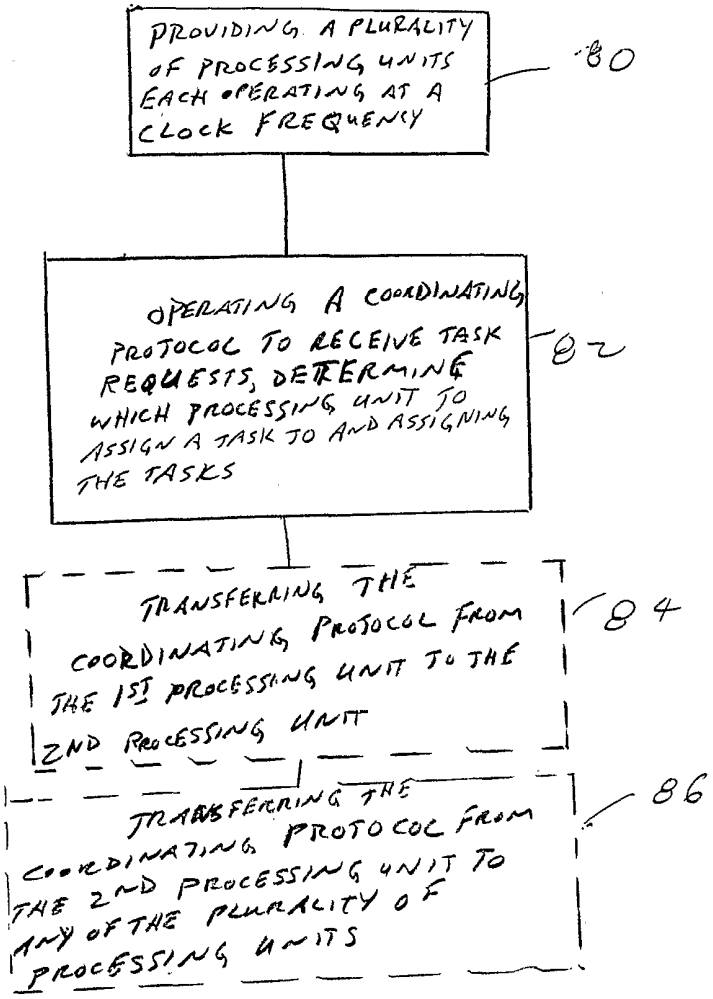

PROVIDING A PLURALITY OF PROCESSING UNITS EACH OPERATING AT A CLOCK FREQUENCY
80
OPERATING A COORDINATING PROTOCOL TO RECEIVE TASK REQUESTS, DETERMINE WHICH PROCESSING UNIT TO ASSIGN A TASK TO AND ASSIGNING THE TASKS
82
TRANSFERRING THE COORDINATING PROTOCOL FROM THE 1ST PROCESSING UNIT TO THE 2ND PROCESSING UNIT
84
TRANSFERRING THE COORDINATING PROTOCOL FROM THE 2ND PROCESSING UNIT TO ANY OF THE PLURALITY OF PROCESSING UNITS
86

FIG. 4

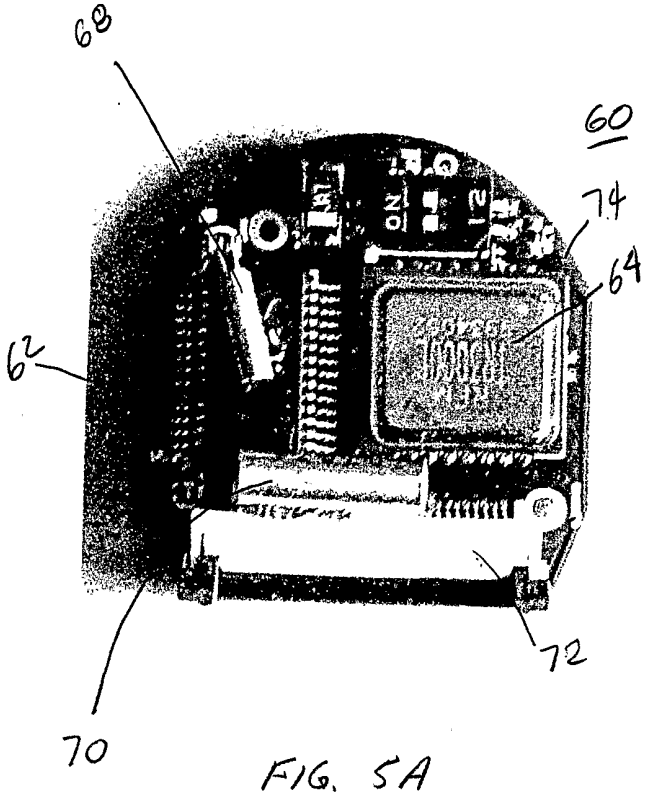


FIG. 5A

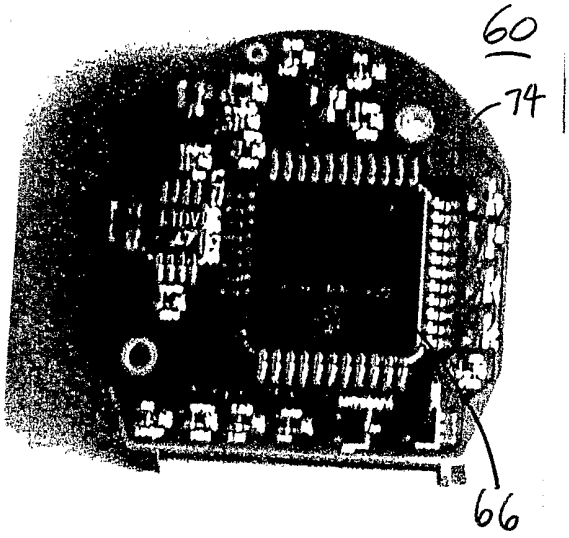


FIG. 5B

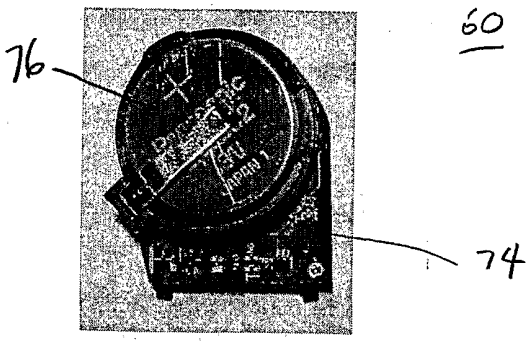


FIG. 5C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/50648

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : G06F 1/26, 1/32
US CL : 713/300, 320, 322, 323, 324

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 713/300, 320, 322, 323, 324

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,790,817 A (ASGHAR et al.) 4 August 1998 (04.08.1998), see the entire document especially column 5, line 56 through column 6, line 17.	1-33
Y,P	US 6,272,537 B1 (KEKIC et al.) 7 August 2001 (07.08.2001), column 82 line 51 through column 83 line 52	13, 14, 15, 23, and 24
Y	US 4,358,823 A (MCDONALD et al.) 9 November 1982 (09.09.1982), the entire document.	1-33
Y	US 5,194,860 A (JONES et al) 16 March 1993 (16.03.1993), column 3 line 59 through column 4 line 35.	5, 10 and 21
Y	US 5,257,372 A (FURTNEY et al) 26 October 1993 (26.10.1993), the entire document, especially column 4 line 50 through column 5 line 37.	6

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer Thomas Lee Telephone No. (703) 305-3900

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