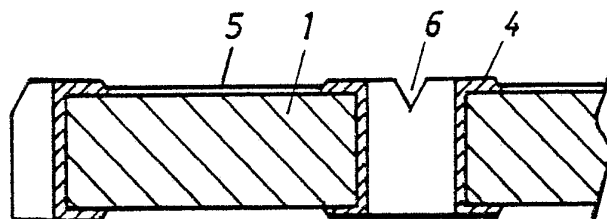




## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification <sup>3</sup> : H05K 13/00; H01C 1/16	A1	(11) International Publication Number: <b>WO 84/ 01259</b> (43) International Publication Date: 29 March 1984 (29.03.84)
<p>(21) International Application Number: PCT/SE83/00326</p> <p>(22) International Filing Date: 14 September 1983 (14.09.83)</p> <p>(31) Priority Application Number: 8205343-0</p> <p>(32) Priority Date: 17 September 1982 (17.09.82)</p> <p>(33) Priority Country: SE</p> <p>(71) Applicant (for all designated States except US): TELEFONAKTIEBOLAGET L M ERICSSON [SE/SE]; S-126 25 Stockholm (SE).</p> <p>(72) Inventors; and (75) Inventors/Applicants (for US only) : OLOFSSON, Lars, Anders [SE/SE]; Stallbacken 4, S-175 43 Järfälla (SE). BJÖRKLUND, Fritz, Lars, Gunnar [SE/SE]; Måndalsvägen 24, S-135 54 Tyresö (SE).</p> <p>(74) Agents: GAMSTORP, Bengt et al.; Telefonaktiebolaget L M Ericsson, S-126 25 Stockholm (SE).</p>	<p>(81) Designated States: DE (European patent), FR (European patent), GB (European patent), JP, US.</p> <p><b>Published</b> <i>With international search report.</i></p>	

(54) Title: A METHOD OF PRODUCING ELECTRONIC COMPONENTS



## (57) Abstract

Method of producing electronic components, e.g. resistors, capacitances, fuses and the like. The components consist of an insulating substrate with electrical connections, connected by layers or wires. In accordance with the invention, the components (5) and their connections are applied to a common substrate (1), which is provided with fractural impressions (6). The components lie in the areas between the impressions. The connections are produced by making holes in the substrate along certain of the fractural impressions (6), and the envelope surface of the holes being coated with conductive material (4), as well as an area about the holes on both sides of the substrate. The components (5) are connected to the connections, subsequent to which the substrate is divided into individual components along the fractural impressions. Certain components require adjustment in manufacture, e.g. by laser beam. This adjustment is carried out before the substrate is divided up.

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A METHOD OF PRODUCING ELECTRONIC COMPONENTS

## TECHNICAL FIELD

The invention relates to a method of producing electronic components (resistors, capacitances, fuses and the like) which includes an insulating substrate provided with layers or wires and electrical connections for the components.

## BACKGROUND ART

5 Microelectronic components have so small dimensions that difficulties occur in their manufacture. This applies to handling individual components in the manufacturing process itself, as well as their after treatment. One example of the former is fuses, of which the dimensions up to now must exceed a given minimum, because a reduction thereof would result  
10 in complicated time-consuming handling. An example of the latter is resistances which require adjustment after manufacture.

## DISCLOSURE OF INVENTION

The basic concept of the invention is to manufacture electronic components of the type mentioned in the introduction on a common substrate and to perform all operations before the substrate is divided up to  
15 individual components.

## PREFERRED EMBODIMENT

A preferred embodiment of the invention will now be described in conjunction with the figures where  
Figure 1 is a portion of the substrate provided with resistors  
Figure 2 is a portion of the substrate provided with wire fuses  
20 Figure 3 is a cross-section to a larger scale of a resistor with connections.

A non-conductive substrate 1, according to figure 1, is provided during the course of production with a first set of parallel fractural impressions 2, e.g. grooves, which define strips with the width of the ready



component. The substrate is then provided with uniformly spaced through holes 3 along the central lines of these strips, so that the holes form columns. The substrate is provided with a second set of parallel fractural impressions 6 passing through the holes 3. The impressions 6 are at right angles to the impressions 2 and define the length of the component. The inside of each hole, together with a minor area round the hole on both sides of the substrate, is coated with a metal paste 4 to form electrical connections for the component. A layer of electrically resistive material 5 is deposited in the form of squares in the areas defined by the fractural impressions, such that all squares will be separated from each other but each has contact with two electrical connections, the squares thus being connected in series in rows. The substrate with its resistors is heated to sinter the metal paste 4. After sintering, the individual resistances of the resistors are measured and the values adjusted e.g. by treatment with a laser beam, sandblasting or the like. The resistors are possibly coated with a protective layer, after which the substrate is broken into strips along the impressions 2, and the strips thus obtained are broken into individual components along the impressions 6 at the holes. In the latter case, the rupture line passes through the centres of the holes. The conductive coating of the holes is thus parted into two halves which constitute electrical connections for the individual components. Figure 2 illustrates a substrate 11, provided with fractural impressions 12, 16 and holes 13, in the same way as the embodiment of figure 1. The holes are provided with a conductive coating 14, which is sintered to provide electrical connections. A layer of electrically conductive material is applied, in the form of two mutually separated squares 17 and 18 within a field defined by the fractural impressions, such that these squares are each in electrical contact with a connection. In contradistinction to the method according to figure 1, metal wires 15, constituting fuse elements, are fastened between the squares 17 and 18, e.g. by thermo-compression or supersonic welding. A protective coating, e.g. of plastics, can be applied over the metal wires. In an alternative method of producing fusible fuses, a layer is applied between two connections in the manner apparent from the description applying to figure 1. These layers are electrically conductive in this application, and their thickness, width and length adapted to a given current strength



at which the layer fuses. The layer may be heatinsulated from the substrate with the aid of a glass coating, whereby its ability to withstand current is decreased. The final step in the manufacture of fusable fuses is performed in the same way as with the method according to figure 1, namely in that the individual components are obtained by the common substrate being ruptured along the fractural impressions. Figure 3 illustrates an electrical connection in cross-section. The metal paste is applied by impressing from one or two sides, according to need, subsequent to which the viscous material forms a coating on the inner wall of the hole. As will be seen, the conductive material constituting the coating of the hole, is in electrical contact with the layer 5. The method in accordance with the above signifies the advance in respect to the prior art residing in that the individual components can be processed in one operation during manufacture, while these are still in one continuous unit, where each unit embraces a number of components in the order of magnitude of 100, for example. Such operations are enabled since each component has a well-defined fixed location in the common substrate. An advantage is obtained if, in accordance with the invention, the electrical connections are made available from both of the substrate. This makes the ready components easy to assemble on a printed board assembly with the aid of so-called surface soldering.



CLAIMS

1. A method of producing electronic components (resistors, capacitances, fuses and the like) which includes an insulating substrate provided with layers or wires and electrical connections for the components, the components and their connections being applied to a common substrate  
5 within individual areas which are defined by fractural impressions, characterized in that the electrical connections are produced by holes being made in the insulating substrate along said fractural impressions, the envelope surface of the holes together with an area round the holes on  
10 both sides of the substrate being provided with a conductive coating, such that the components come into electrical contact with the coating in the hole, subsequent to which the substrate is divided up along the fractural impressions such that the respective halves of the envelope surface constitute connection surface for the contiguous component.
2. Method as claimed in claim 1, characterized in that in manufacture of components, having an electrical value that must be adjusted during manufacture, e.g. by treatment with a laser beam, sandblasting or the like, a measuring device is connected to the components defined by the  
5 fractural impressions for measuring their electrical value, and in that the adjustment is carried out before dividing up components along the fractural impressions.



Fig. 1

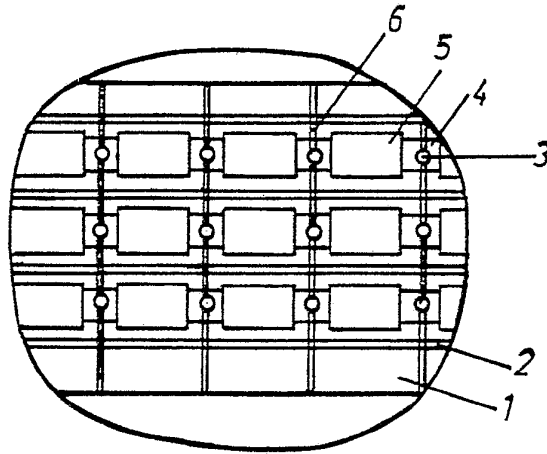


Fig. 2

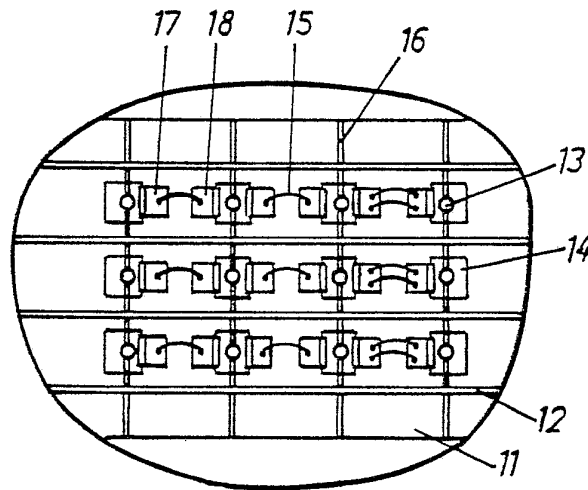
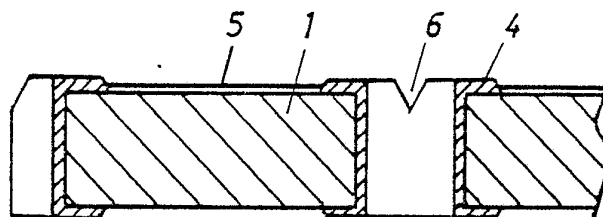



Fig. 3



# INTERNATIONAL SEARCH REPORT

International Application No PCT/SE83/00326

<b>I. CLASSIFICATION OF SUBJECT MATTER</b> (if several classification symbols apply, indicate all) <sup>3</sup>		
According to International Patent Classification (IPC) or to both National Classification and IPC <sup>3</sup>		
H 05 K 13/00, H 01C 1/16		
<b>II. FIELDS SEARCHED</b>		
Minimum Documentation Searched <sup>4</sup>		
Classification System	Classification Symbols	
IPC 3	H 05 K 13/00,04, 3/40,42, H 01 C 1/14,16,22,24	
US C1	<u>338</u> :195, 203; <u>29</u> : 621	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included In the Fields Searched <sup>6</sup>		
SE, NO, DK, FI classes as above		
<b>III. DOCUMENTS CONSIDERED TO BE RELEVANT</b> <sup>14</sup>		
Cat	Citation of Document, <sup>16</sup> with indication, where appropriate, of the relevant passages <sup>17</sup>	Relevant to Claim No. <sup>18</sup>
Y	DE, A1, 2 527 037 (OY PARAMIC AB) 8 January 1976 & FR 2 275 862 US 3 983 528 GB 1 481 933 JP 51 013 946 SE 7 506 920 SE 395 326	1
Y	SE, A, 8007792-8 (TELEFON AB L M ERICSSON) 6 May 1982	1
Y	GB, A, 2 086 139 (KOLLMORGEN TECHNOLOGIES CORPORATION) 6 May 1982 & DE 3 008 143 NL 8 101 050 FR 2 482 406 JP 56 162 899 US 4 374 868 SE 8 101 360	1
.../...		
<p><sup>15</sup> * Special categories of cited documents:</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p>		<p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>"&amp;" document member of the same patent family</p>
<b>IV. CERTIFICATION</b>		
Date of the Actual Completion of the International Search <sup>1</sup>	Date of Mailing of this International Search Report <sup>1</sup>	
1983-10-31	1983 -11- 2 2	
International Searching Authority <sup>1</sup>	Signature of Authorized Officer <sup>10</sup>	
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III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)		
Category *	Citation of Document, <sup>16</sup> with indication, where appropriate, of the relevant passages <sup>17</sup>	Relevant to Claim No <sup>18</sup>
Y	IMB Technical Disclosura Bulletin, vol 23, no 6, November 1980, p. 2256 W.L. UNDERKOFER: " Etchback of Insulation on Wire In A Multiwire Board"	
Y	AU, B, 59 996/69 (TECHNOGRAPH LIMITED) 4 March 1971	1
A	IBM Technical Disclosura Bulletin, vol 13 no 5, October 1970, p. 1105, A. Bross et al: "Modular Resistor Array"	
A	US, A, 4 228 418 (J.R. PIEDMONT ET AL) 14 October 1980	1
A	GB, A, 1 236 580 (N.G. WORSTER) 23 June 1971 & DE 1 816 067 FR 1 596 267 US 3 541 491	1
X	US, A, 4 032 881 (D.L.SINGLETON) 28 June 1977 especially figure 5	2