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(54) **Title:** A SYSTEM, METHOD, AND DEVICE TO DISTRIBUTE ACCURATE SYNCHRONIZATION TIMESTAMPS IN AN EXPANDABLE AND TIMING CRITICAL SYSTEM

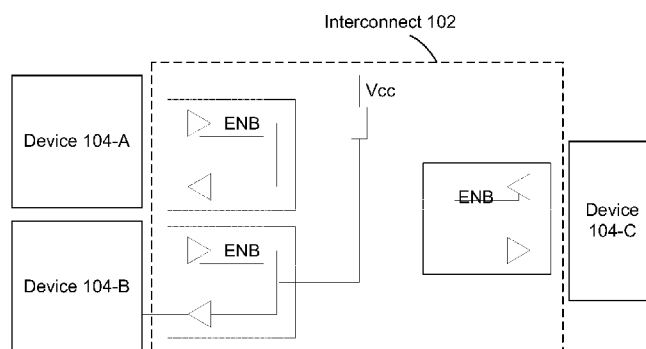


FIG. 1

(57) **Abstract:** Techniques are described to provide a device and network of devices that collect distributed coordinated timestamps from distributed time counters in a multi-module or multi-integrated circuit system. The interconnect between the modules can be a single-wire or a two-wire interconnect. The modules communicatively coupled to the interconnect can use a collision-avoidance protocol for triggering the broadcasting of timestamps among the modules as well for allowing all modules to transmit their timestamps. Timestamps from multiple clocks can be transmitted by all modules and then collected and compared to produce correction factors to clock signals of each module to potentially achieve distributed clock synchronization in multiple independent modules or integrated circuits.



**A SYSTEM, METHOD, AND DEVICE TO DISTRIBUTE
ACCURATE SYNCHRONIZATION TIMESTAMPS
IN AN EXPANDABLE AND TIMING CRITICAL SYSTEM**

FIELD

5 The subject matter disclosed herein relates generally to event time stamp generation and time stamp distribution in a system with a plurality of clocks to potentially achieve clock synchronization between a plurality of components in the system.

RELATED ART

10 Many digital devices use clocks to coordinate operations. When multiple digital devices inter-operate, it is desirable to have clock synchronization among the devices. For example, in media systems, it is desirable to synchronize operations of an audio decoder and a video decoder so that audio output is in synch with corresponding video. In multi-point data acquisition systems, data
15 samples must be taken with an accurate time relationship and associated timestamps are recorded on a recording device together with captured data. For example, in cable modems, the transmission in the upstream direction must be synchronized with the transmission opportunities communicated through the downstream.

20 When it is possible to specify use cases and the components are developed with this assumed use case in mind, the designer can provide a special interface and interconnect to coordinate synchronization. When the entire system is located on a single die (e.g., system-on-chip (SoC)), providing an interconnect is feasible as external device terminals are not constrained in the implementation.
25 However, if the time stamp coordination spans across multiple physical devices (in the form of integrated circuits or functional modules), it is desirable to reduce terminal count for synchronization to an absolute minimum. In some cases, what is needed is a low pin count interface suitable for heterogeneous coordinated time stamping and distribution of the corresponding timestamps between multiple
30 physical devices.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the present invention are illustrated by way of example, and not by way of limitation, in the drawings and in which like reference numerals

refer to similar elements. For evolving systems with the capability to add components, it is desirable to provide synchronization between added components.

FIG. 1 depicts an example of a system of devices where the devices are
5 communicatively coupled using an interconnect.

FIG. 2 depicts components used by a device to transmit time stamps to an interconnect and receive time stamps from the interconnect.

FIG. 3 depicts an example timing diagram in which devices attempt to transmit time stamps.

10 FIG. 4 depicts an example process in accordance with an embodiment.

FIG. 5 provides an example of a system in accordance with an embodiment.

DETAILED DESCRIPTION

Reference throughout this specification to “one embodiment” or “an
15 embodiment” means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearances of the phrase “in one embodiment” or “an embodiment” in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular
20 features, structures, or characteristics may be combined in one or more embodiments.

Various embodiments provide a device and network of devices that collect distributed coordinated timestamps from distributed time counters in a multi-module or multi-integrated circuit system. The interconnect between the modules
25 can be a single-wire or a two-wire interconnect. The modules communicatively coupled to the interconnect can use a collision-avoidance protocol for triggering the broadcasting of timestamps among the modules as well for allowing all modules to transmit their timestamps. The collision-avoidance protocol can be made compatible with I2C. Timestamps from multiple clocks can be transmitted
30 by all modules and then collected and compared to produce correction factors to clock signals of each module to potentially achieve distributed clock synchronization in multiple independent modules or integrated circuits.

For example, in the system, if CLK_B is variable, the desired ratio between clocks CLK_A and CLK_B can be expressed by the ratio M/N, and the

coordinated timestamps from these clocks at two different instances of time can be read as (TS_A1, TS_B1) and (TS_A2 and TS_B2) respectively. Then the equation $(TS_A2 - TS_A1) * M = (TS_B2 - TS_B1) * N$ holds if the clock frequencies are synchronized. The error signal $Err = (TS_A2 - TS_A1) * M - (TS_B2 - TS_B1) * N$ represents the difference between clock rates, and the tracking system can minimize the difference by adjusting the variable clock. The phase synchronization may be achieved by sending a command to reset the phase of oscillators at predefined time when the frequency synchronization is achieved. A digital or analog tracking loop may be utilized by the tracking system with the error signal as an input.

Accordingly, clock sources of multiple independent modules or integrated circuits may potentially achieve mutual or selected group synchronization. For example, the independent modules or integrated circuits can be wireless or wired network interfaces. Synchronization of distributed clock sources can be used for synchronization of a network clock and/or audio/video clocks of networked multimedia modules or for synchronization of media and transport clocks in wireless or wired video distribution systems.

Various embodiments provide a method for devices that are communicatively coupled to an interconnect to use the interconnect to communicate when one of the devices is going to capture a time stamp and also to invoke other devices to take a coordinated time stamp and communicate the time stamps using the interconnect without collision. One embodiment of an interconnect can have an open drain, open collector, or similarly wired-OR bi-directional interface transceiver configuration. To prevent collision of time stamps, devices that use the interconnect may implement an arbitration scheme that compares the data line while driving it with the desired data. If the data in the interconnect does not match the driven value, the transmitter stops driving data because another, higher priority unit is winning arbitration. In some cases, an I2C compatible interface can be used both to initiate the coordinated time stamping and to communicate the timestamps between units.

When every device attempts to transmit their device identifier on the interconnect, priority is given to the device with the lowest identifier. The number of bits in the identifier is based on the number of devices couplable to the

interconnect. For example, the number of bits could be two for a four device interconnect.

FIG. 1 depicts an example of a system of devices where the devices are communicatively coupled using an interconnect. Devices 104-A to 104-C can use interconnect 102. Interconnect 102 can include one or two conductive paths. In an embodiment where interconnect 102 is a single wire, an asynchronous communication method and bit timing can be based on universal asynchronous receiver/transmitter (UART). In another embodiment, interconnect 102 can use a two-wire system management bus (SMB) to initiate the transmission of time stamps and to arbitrate conflicts among transmissions of time stamps. SMB is described in SBS Implementers Forum, System Management Bus (SMBus) Specification, Version 2.0 (August 3, 2000).

As depicted, interconnect 102 uses an open drain, open collector, or similarly wired-OR bi-directional interface with each of devices 104-A to 104-C.

Interconnect 102 can use a conflict resolution technique similar to that of I2C when multiple devices attempt to transmit to interconnect 102 simultaneously. The conflict resolution technique of I2C is described in section 3.8 of I2C-Bus Specification and User manual, UM 10204 (2007). The interconnect makes it feasible to trigger a time stamping process on all connected devices within 20-100ns relative to each other and the timestamp initiator.

Devices 104-A to 104-C can be any type of device that uses a clock signal. For example, devices 104-A to 104-C can be any of wireless or wired network interfaces, real time process control or automation, audio encoders or decoders, or video encoders or decoders. Each of devices 104-A to 104-C can be implemented as an integrated circuit. For example, an event causes device 104-A to determine a time stamp of its clock and subsequently broadcast the time stamp using interface 102. The event that triggers time stamping can be the start of new video frame, vertical or horizontal synchronization pulse in TV, global timer tick, start of the audio sample block or a SYNC frame in MPEG transport stream, but is not limited to listed event types.

Device 104-A pulls the interconnect 102 to state zero to indicate a time stamp determining event ("TS Event") has occurred. Pulling interconnect 102 to state zero causes transmission of a zero for a bit signaling period. Device 104-A determines its time stamp. In addition, devices 104-B and 104-C recognize that a

TS Event has occurred and in response, devices 104-B and 104-C capture their own time stamp from their own timebase. A time base can include a local time source or clock and a time counter which monotonically increments or decrements its count on every period of the clock. At the same time, all devices 104-A to 104-
5 C attempt to use interconnect 102 to serially transmit their identifier assigned when the system was manufactured or assembled.

As all devices attempt to transmit their identifiers and simultaneously monitor the state of the interconnect, the arbitration process selects only one device which has the highest priority. Other devices will stop driving the
10 interconnect, and arbitrated device will remain active. The arbitration scheme permits the device with the lowest preamble number to subsequently transmit its time stamp value using interconnect 102. After the device with the lowest identifier transmits its time stamp, the devices that were not able to transmit their time stamp can retry the attempt to transmit their time stamp. Again, the device
15 with the lowest identifier wins. The process repeats until all devices transmit their time stamps.

Devices 104-A to 104-C can use the time stamps from other devices to synchronize their clock sources, where the device ID transmitted together with the timestamp is not only used for arbitration, but also identifies the unit to which the
20 timestamp belongs. For example, devices 104-B and 104-C can compare the received time stamp from device 104-A to their own locally clocked counter values to measure drift errors. The drift error values can be used to adjust oscillator frequency to synchronize clocks of devices 104-B and 104-C to a clock of device 104-A. One possible application of the method is to adjust the frequencies of
25 tunable display and audio clock (e.g., doppler phase locked loop) for synchronized and uninterrupted playback.

One of the transmitted time stamps is associated with a master clock signal. A device can indicate if its clock signal is the master clock signal. For example, IEEE 1588 specifies that devices can indicate their clock accuracy. The
30 clock with the highest accuracy can be the master clock. In some cases, a system wide transmission (e.g., broadcast) identifies the master clock. The transmission can be made using the interconnect.

In some cases, consumer electronic (CE) devices with clock sources can be communicatively coupled to a personal computer and the CE devices can use

the interconnect to synchronize their clocks with components of the personal computer or vice versa. CE devices with clock sources can be communicatively coupled to other CE devices and the CE devices can use the interconnect to synchronize their clocks with the other CE devices. Similarly, components can be added to a personal computer and use the interconnect to synchronize clocks with some components of the personal computer.

If all devices are trying to transmit their time stamps after a first TS Event and a device has another TS Event, the devices are free to select the time when each may want to trigger the coordinated time stamping. This potentially may lead to more than one device attempting to trigger a TS Event. In some cases, the first TS event leads to transmission of timestamps in the connected system, and once timestamp transmission has started, the other TS Events are cancelled and blocked. In the worst-case situation, two devices may not recognize the other's TS Event due to propagation delays in the interconnect and they may transmit inaccurate timestamp values, leading to a maximum error equal to propagation delay.

In some cases, the interface to the interconnect is a bidirectional optical interconnect system and communication of bits occurs by modulating optical radiation. Collision avoidance involves detecting monitoring optical signal intensity or phase to determine if a signal different from that transmitted by the interface is communicated by the interconnect.

FIG. 2 depicts components used by a device to transmit time stamps to an interconnect and receive time stamps from the interconnect. Time stamp generator logic 202 can determine time stamps of a clock source to a device. Time stamps can be determined using a time base, which can include a local time source or clock and a time counter which monotonically increments or decrements its count on every period of the clock. Outbound time stamp storage logic 204 can store the time stamp of the device for future transmission. The format of the time stamp can be [ID7, TS32], where ID7 is I2C standard IC address and TS32 is a 32-bit snapshot of the local time base counter in this device. Collision avoidance logic 206 can use a technique compatible with I2C to determine whether its device can transmit using the interconnect. Received time stamp storage logic 208 can store one or more time stamps from other devices that were received using the interconnect.

Clock adjuster logic 210 can compare received time stamps with the locally clocked time stamp to measure drift errors. The drift error values can be used to adjust oscillator frequency of the clock used by the device.

FIG. 3 depicts an example timing diagram in which devices attempt to
5 transmit time stamps. Before TS Event, some internal or external event in Device 1 tells Device 1 to generate its TS. The event causes Device 1 to determine its TS and transmit the TS on the interconnect. Device 1 pulls wire to zero to indicate a TS Event has occurred. The TS Event is “at will” in time and occurs when any device in the system wishes to issue a timestamp. Pulling down the wire causes
10 transmission of a “0” for one signaling period. The TS Event can be treated as the start of a first pulse, whose duration is assumed to be one bit interval. Other devices recognize the TS Event and in response, other devices determine their own time stamps regardless of whether there is an internal TS event. In the next signaling period after the TS Event, at approximately the same time, all devices
15 attempt to transmit their device identifier.

In asynchronous transmission mode (UART), the duration of the bit intervals is determined automatically, from the duration of the bits, using commonly known techniques called autobaud. When an I2C-compatible protocol is used by the interconnect, each transmitter uses a clock signal for timing
20 transmitted bits.

For example, an identifier can have two bits, b0 followed by bit b1. For a first bit b0, any device whose b0 is a 0 pulls the interconnect to zero which does not allow other devices with an identifier having a b0 of 1 to transmit. Next, for second bit b1, a b1 of 0 similarly only permits the device with the b0b1 of 00 to
25 transmit until the interconnect is freed. An identifier of b0b1 of 00 allows its device to transmit its time stamp first. A device that has an identifier b0b1 of 11 will transmit its time stamp last. Devices know that they do not pull a wire to zero because they have a receiver that detects a different level on the interconnect than that transmitted by the device. Devices that were not able to transmit their
30 time stamps go offline and store their time stamps in memory and subsequently transmit their identifiers again. The device with the lowest identifier is permitted to transmit its time stamp. The process repeats until the device with the highest identifier transmits its time stamp.

Referring again to the example of FIG. 3, at 250, device 1 and device 2 transmit their identifiers. Device 2 has the lowest device identifier and is permitted to transmit its time stamp before Device 1. While device 2 transmits its time stamp, device 1 goes offline and stores its time stamp to transmit later. After
5 device 2 transmits its time stamp, then at 251, device 1 transmits its identifier again and because device 1 has the lowest identifier value.

FIG. 4 depicts an example process in accordance with an embodiment. Block 302 includes a first device detecting a time stamp generation event. The event that triggers time stamping can be the start of new video frame, vertical or
10 horizontal synchronization pulse in TV, global timer tick, start of the audio sample block or a SYNC frame in MPEG transport stream, but is not limited to listed event types.

Block 304 includes the first device transmitting a zero on an interconnect to signify a time stamp sharing is to take place. The interconnect can include one or
15 two wires. The interconnect can include an open drain, open collector, or similarly wired-OR bi-directional interface for interfacing with the first device and other devices.

Block 306 includes all devices communicatively coupled to the interconnect transmitting their device identifier to the interconnect. Synchronized transmission
20 of the identifiers causes a collision between the identifiers. A conflict resolution technique of I2C is used to determine which device is permitted to transmit. The device with the lowest device identifier value is permitted to transmit its time stamp using the interconnect.

Block 308 includes the device with the lowest device identifier value
25 transmitting its time stamp using the interconnect. Blocks 306-308 repeat until all devices on the interconnect have transmitted their time stamps. Devices are able to receive time stamps transmitted from other devices. Devices can use the received time stamps to synchronize their clock source using the received time stamps.

30 FIG. 5 provides an example of a system in accordance with an embodiment. The system can be used in a mobile station, user element, netbook, handheld computer, handheld phone, and so forth. Computer system 400 may include host system 402 and display 422. Computer system 400 can be implemented in a handheld personal computer, mobile telephone, set top box, or

any computing device. Any type of user interface is available such as a keypad, mouse, touch screen, and/or gesture or motion recognition. Host system 402 may include chipset 405, processor 410, host memory 412, storage 414, graphics subsystem 415, and radio 420. Chipset 405 may provide intercommunication
5 among processor 410, host memory 412, storage 414, graphics subsystem 415, and radio 420. For example, chipset 405 may include a storage adapter (not depicted) capable of providing intercommunication with storage 414.

An interconnect between devices is shown as a dotted line. Each device can include features described herein to perform time stamp
10 generation and synchronization.

Processor 410 may be implemented as Complex Instruction Set Computer (CISC) or Reduced Instruction Set Computer (RISC) processors, x86 instruction set compatible processors, multi-core, or any other microprocessor or central processing unit.

15 Host memory 412 may be implemented as a volatile memory device such as but not limited to a Random Access Memory (RAM), Dynamic Random Access Memory (DRAM), or Static RAM (SRAM). Storage 414 may be implemented as a non-volatile storage device such as but not limited to a magnetic disk drive, optical disk drive, tape drive, an internal storage device, an attached storage device, flash
20 memory, battery backed-up SDRAM (synchronous DRAM), and/or a network accessible storage device.

Graphics subsystem 415 may perform processing of images such as still or video for display. An analog or digital interface may be used to communicatively couple graphics subsystem 415 and display 422. For example, the interface may
25 be any of a High-Definition Multimedia Interface, DisplayPort, wireless HDMI, and/or wireless HD compliant techniques. Graphics subsystem 415 could be integrated into processor 410 or chipset 405. Graphics subsystem 415 could be a stand-alone card communicatively coupled to chipset 405.

Radio 420 may include one or more radios capable of transmitting and
30 receiving signals in accordance with applicable wireless standards such as but not limited to any version of IEEE 802.11 and IEEE 802.16. For example, radio 420 may include at least a physical layer interface and media access controller. Radio 420 can include a baseband processor to perform techniques described herein.

The graphics and/or video processing techniques described herein may be implemented in various hardware architectures. For example, graphics and/or video functionality may be integrated within a chipset. Alternatively, a discrete graphics and/or video processor may be used. As still another embodiment, the graphics and/or video functions may be implemented by a general purpose processor, including a multicore processor. In a further embodiment, the functions may be implemented in a consumer electronics device.

Embodiments of the present invention may be implemented as any or a combination of: one or more microchips or integrated circuits interconnected using a motherboard, hardwired logic, software stored by a memory device and executed by a microprocessor, firmware, an application specific integrated circuit (ASIC), and/or a field programmable gate array (FPGA). The term "logic" may include, by way of example, software or hardware and/or combinations of software and hardware.

Embodiments of the present invention may be provided, for example, as a computer program product which may include one or more machine-readable media having stored thereon machine-executable instructions that, when executed by one or more machines such as a computer, network of computers, or other electronic devices, may result in the one or more machines carrying out operations in accordance with embodiments of the present invention. A machine-readable medium may include, but is not limited to, floppy diskettes, optical disks, CD-ROMs (Compact Disc-Read Only Memories), and magneto-optical disks, ROMs (Read Only Memories), RAMs (Random Access Memories), EPROMs (Erasable Programmable Read Only Memories), EEPROMs (Electrically Erasable Programmable Read Only Memories), magnetic or optical cards, flash memory, or other type of media / machine-readable medium suitable for storing machine-executable instructions.

The drawings and the forgoing description gave examples of the present invention. Although depicted as a number of disparate functional items, those skilled in the art will appreciate that one or more of such elements may well be combined into single functional elements. Alternatively, certain elements may be split into multiple functional elements. Elements from one embodiment may be added to another embodiment. For example, orders of processes described herein may be changed and are not limited to the manner described herein.

Moreover, the actions of any flow diagram need not be implemented in the order shown; nor do all of the acts necessarily need to be performed. Also, those acts that are not dependent on other acts may be performed in parallel with the other acts. The scope of the present invention, however, is by no means limited by

5 these specific examples. Numerous variations, whether explicitly given in the specification or not, such as differences in structure, dimension, and use of material, are possible. The scope of the invention is at least as broad as given by the following claims.

CLAIMS:

What is claimed is:

1. A device comprising:
 - an interface to an interconnect system;
 - 5 a time base comprising a clock and a time counter which increments or decrements its count each period of the clock;
 - a time stamp generator to capture a count of the time base associated with the device, the time stamp generator to use the interface to transmit a time stamp event indicator to the interconnect system and also to transmit a device identifier
 - 10 to the interconnect system, wherein the interface is to transmit signals to simultaneously initiate a time stamping event in one or more other devices and to trigger transmission by the one or more other devices of device identifiers and timestamps to the interconnect system; and
 - collision avoidance logic to determine whether the device is permitted to
 - 15 transmit its time stamp using the interconnect system, wherein the time stamp generator is to wait for a period of time and transmit the device identifier to the interconnect system again in response to the device not being permitted to transmits its time stamp.
2. The device of claim 1, wherein the interface is configured in one of: an
- 20 open collector, open drain, and a wired-OR configuration.
3. The device of claim 1, wherein the interface comprises a bidirectional optical interconnect system and communication of bits occurs by modulating optical radiation and wherein collision avoidance logic is to detect collisions by monitoring optical signal intensity or phase to determine if a signal different from
- 25 that transmitted by the interface is communicated by the interconnect system.
4. The device of claim 1, wherein the time stamp event indicator is to trigger at least one other device communicatively coupled to the interconnect system to determine its time stamp, to transmit its device identifier to the interconnect system, and to transmit its coordinated time stamp to the interconnect system if its
- 30 device identifier is the lowest value.
5. The device of claim 1, wherein the collision avoidance logic is to determine that the time stamp generator is permitted to transmit its time stamp using the interface if the associated device identifier is the lowest value.

6. The device of claim 1, wherein the collision avoidance logic is utilize a collision-avoidance protocol compliant with I2C.
7. The device of claim 1, further comprising:
in response to the again transmitted device identifier being the lowest value,
- 5 the time stamp generator is to transmit the time stamp associated with the device identifier to the interconnect system using the interface.
8. The device of claim 1, further comprising:
time stamp storage to store any time stamp received from the interconnect system.
- 10 9. The device of claim 1, wherein the interconnect system comprises a single or two wire hardware interconnect.
10. The device of claim 1, further comprising:
a clock adjuster logic to compare received time stamps with the time stamp of the device to measure drift errors and to adjust an oscillator frequency of a
- 15 clock used by the device to synchronize with one of the received time stamps.
11. A method comprising:
each of at least two devices coupled to an interconnect receiving an indication to determine its time stamp;
each of the at least two devices determining its time stamp;
- 20 each of the at least two devices transmitting its identifier to the interconnect;
a device with the lowest identifier transmitting its time stamp to the interconnect;
each of the at least two devices, other than the device with the lowest
- 25 identifier, receiving the time stamp;
each of the at least two devices, other than the device with the lowest identifier, transmitting its identifier to the interconnect; and
a second device with the second lowest identifier transmitting its time stamp to the interconnect.
- 30 12. The method of claim 11, wherein each of the at least two devices that receives a time stamp from another device synchronizes its clock to a clock of one of the devices.

13. The method of claim 11, wherein each of the at least two devices that receives a time stamp from another device synchronizes its clock to a network or multi-media clock of one of the devices.

14. The method of claim 11, wherein each of the at least two devices is an independent module or integrated circuit.

15. The method of claim 11, wherein each of the at least two devices are selected from among a wireless or wired network interface, an audio encoder, an audio decoder, a video encoder, and a video decoder.

16. A system comprising:

- 10 a network medium;
- a network interface communicatively coupled to the network medium;
- an interconnect;
- a plurality of devices communicatively coupled to the interconnect,
- 15 wherein each of the devices comprises:
 - an interface to the interconnect;
 - a time base comprising a clock and a time counter which increments or decrements its count each period of the clock;
 - a time stamp generator to capture a count of the time base
 - 20 associated with the device, the time stamp generator to use the interface to transmit a time stamp event indicator to the interconnect and also to transmit a device identifier to the interconnect, wherein the interface is to transmit signals to simultaneously initiate a time stamping event in one or more other devices and to trigger
 - 25 transmission by the one or more other devices of device identifiers and timestamps to the interconnect; and
 - collision avoidance logic to determine whether the device is permitted to transmit its time stamp using the interconnect, wherein the time stamp generator is to wait for a period of time and transmit
 - 30 the device identifier to the interconnect again in response to the device not being permitted to transmits its time stamp.

17. The system of claim 16, wherein the interface is configured in one of: an open collector, open drain, and a wired-OR configuration.

18. The system of claim 16, wherein the time stamp event indicator is to trigger at least one other device communicatively coupled to the interconnect to determine its time stamp, to transmit its device identifier to the interconnect, and to transmit its coordinated time stamp to the interconnect if its device identifier is

5 the lowest value.

19. The system of claim 16, wherein the interconnect comprises a single or two wire hardware interconnect.

20. The system of claim 16, wherein each of the devices further comprises:
a clock adjuster logic to compare received time stamps with the time stamp

10 of the device to measure drift errors and to adjust an oscillator frequency of a clock used by the device to synchronize with one of the received time stamps.

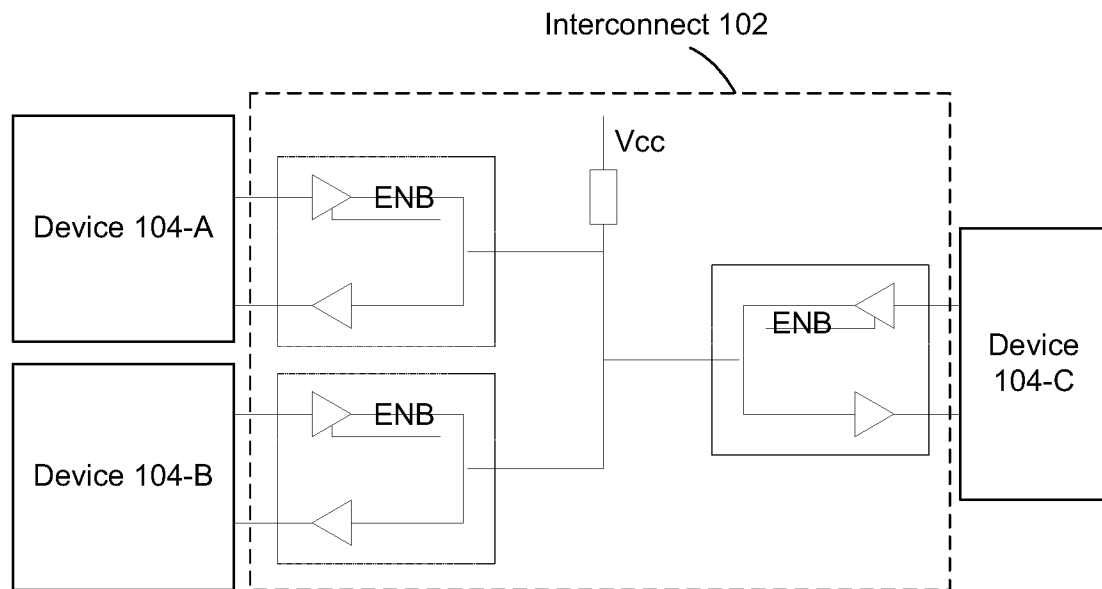


FIG. 1

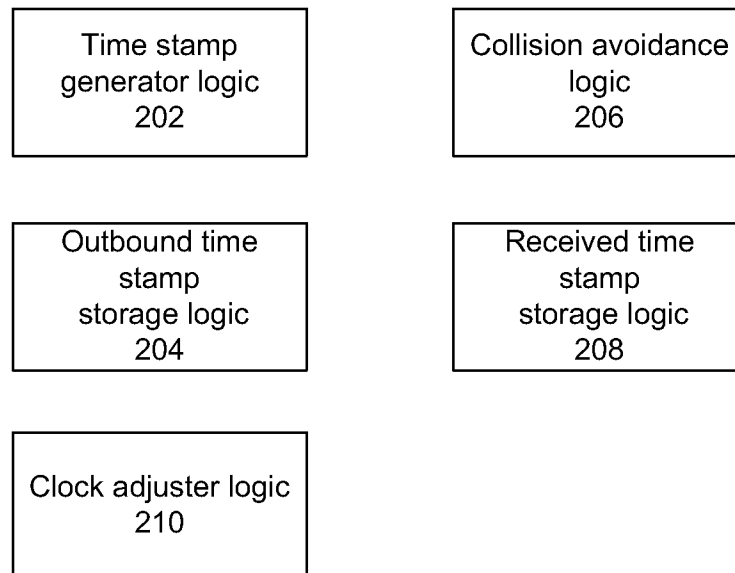


FIG. 2

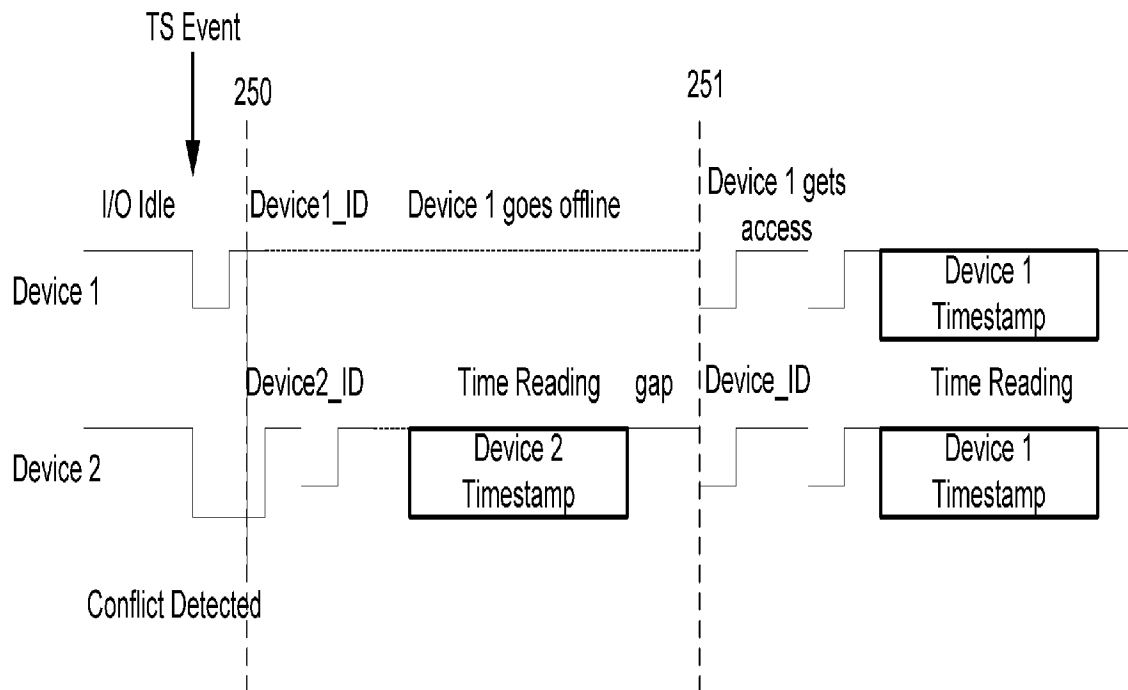


FIG. 3

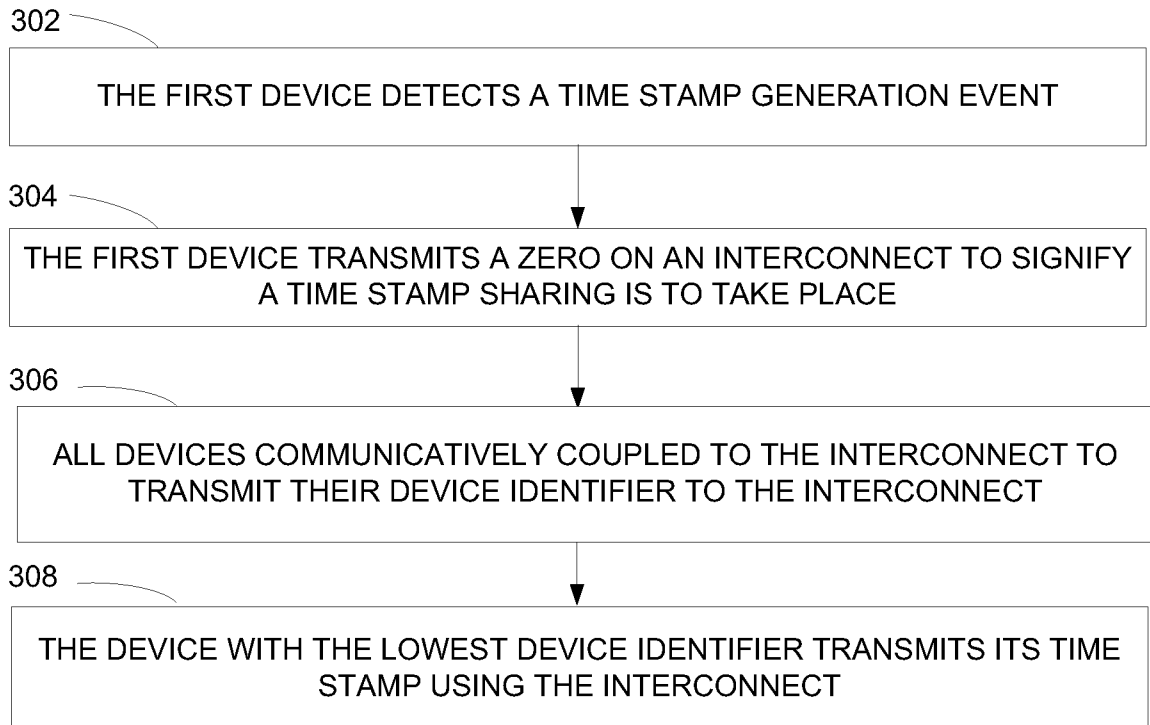


FIG. 4

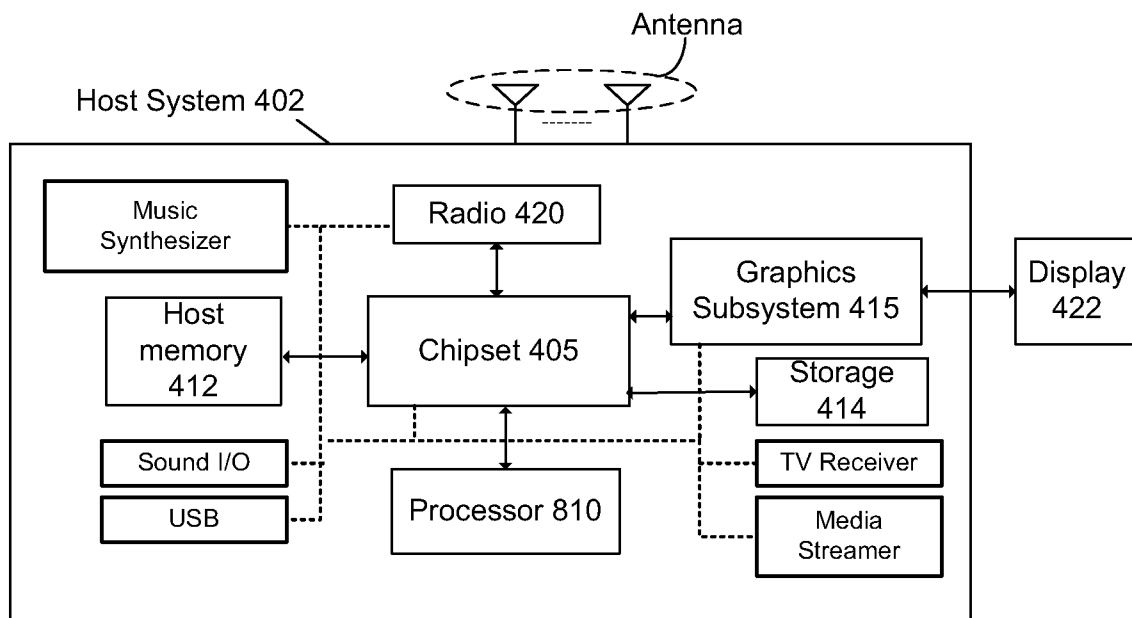


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/067603**A. CLASSIFICATION OF SUBJECT MATTER****G06F 1/04(2006.01)i, G06F 13/38(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 1/04; G06F 15/16; G06F 12/16; H04J 14/08; H03K 5/15

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: "TIMESTAMP" , "CLOCK" , "SYNCH" , "IDENTIFIER"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2009-0142062 A1 (HARRISON STEVEN ANTHONY BERNARD et al.) 04 June 2009 See abstract, paragraphs [0027]-[0057] and figure 3	1-20
A	US 2008-0243950 A1 (WEBMAN EREZ et al.) 02 October 2008 See abstract, paragraphs [0023]-[0049] and figure 1	1-20
A	US 2011-0035511 A1 (BIEDERMAN DANIEL) 10 February 2011 See abstract, paragraphs [0013]-[0049] and figure 1	1-20
A	US 2002-0073228 A1 (YVES COGNET et al.) 13 June 2002 See abstract, paragraphs [0036]-[0070] and figure 2	1-20

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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Date of the actual completion of the international search

12 JULY 2012 (12.07.2012)

Date of mailing of the international search report

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2011/067603

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