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(54) RANGE DETECTING METHOD AND APPARATUS

(71) We, CANON KABUSHIKI, KAISHA, a Japanese company of 30—2, 3-chome, Shimomaruko, Ohta-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a range detecting method and apparatus, and more particularly, it is concerned with a range detecting method and apparatus in which the range of an object is measured by electrically detecting a relative displacement between two images of the object using the distance measurement principle of a base line double-image coincidence type range finder. In the methods and devices to be described herein image signals concerning the two images are obtained by scanning the two images, the relative displacement between the two images being detected by processing these image signals.

There have previously been proposed various types of electric double-image coincidence detection type range detecting method and apparatus as outlined above, or automatic focus adjusting devices for photographic cameras, etc. using such range finding devices. More particularly various known range finding devices operate to form two images of an object with a relative displacement according to the object distance upon photo-electric light receiving means, the displacement, or positional difference, between these two images is determined from outputs of the light receiving means thereby permitting calculation of the distances to the object for the range finding.

For example, according to Japanese Patent Publication No. 48-5733, there is proposed a range detecting method and apparatus in the form of an automatic focus adjusting device, wherein a pair of photo-conductive elements which are so constructed that their resistance values may vary in accordance with positional changes in an image on the light receiving surfaces thereof are juxtaposed, and then images of the one and the same object are formed on these elements by means of a range finding optical system comprising a pair of focussing lenses fixedly disposed at a certain separation on the base line so that a distance to the object may be detected by measuring the difference between the resistance values of these two elements by utilizing the principle that a relative displacement of the image forming position on each element corresponds to a distance to the object.

In this disclosed device, however, the photo-conductive element per se is of a very specific structure, and accordingly the use of a pair of such elements presents a difficulty in the matching of the response characteristics of both such elements. As a result the precision of detection is impaired by an increased error signal, and inaccurate distance measurement will arise since coincidence of the resistance values in both elements does not accurately represent a correspondence of the positions of the images on the respective elements.

With a view to overcoming this problem, there has been proposed a range detecting device, or an automatic focus adjusting device, in which image signals concerning the two images are obtained by scanning them using a photo-electric light receiving means, and then the relative displacement is measured using the two image scanning signals, and the object distance is calculated, or the focus of the objective lens system in a camera is automatically adjusted using the data concerning this relative displacement.

For example, U.S. Patent No. 3,898,676, teaches an automatic focus adjusting device of a construction, wherein arrays of photo-sensors are used as the photo-electric light receiving means for receiving the two images, and, by driving these photo-sensor arrays simultaneously, photo-electric outputs of the photo-sensors in the arrays one obtained in a timed sequence to thereby

scan the two images simultaneously in a purely electrical manner, and image signals thus obtained on these two images are converted to continuous waveform signals by low pass filters. Such wave form signals are introduced into a phase discriminator to detect a phase difference between these image scanning signals, and a servo-motor is actuated by an output from the phase discriminator to cause the objective lens system to shift along its optical axis, in association with which one of the two images is shifted with respect to the other, whereby the "in-focus position" of the objective lens system to the object is indicated when the phase difference between the image scanning signals for the two images becomes zero, in other words, a point where the relative displacement between the two images on the respective photosensor arrays becomes zero.

Also, according to Laid-Open Japanese Patent Application No. 51-45556 there is proposed a method and an apparatus for detecting the range of an object, in which self-scanning image sensors (a kind of photo-sensor array) are utilized as the photo-electric light receiving means for receiving light from two images of the object, then the two images are repeatedly scanned by these image sensors, the time of commencement of scanning of one of the image sensors being varied by a variable delay circuit relative to the time of commencement of the scanning of the other image sensor, while coincidence and non-coincidence of the image signals concerning the two images obtained from the image sensors is detected by means of a coincidence detection circuit, and the relative displacement of the two images, i.e. representative of the object distance, is determined directly from the period between the start times of the scans by the two image sensors in a scanning operation during which coincidence is detected by the abovementioned coincidence detection circuit.

In the methods and devices as disclosed in these U.S. Patent No. 3 898 676 and Laid-Open Japanese Patent Application No. 51-45556, the two images of an object to be formed by the range finding optical system are scanned purely electrically using photo-sensor arrays or image sensors known as, in particular, Photo-Diode Array, CCD (Charge Coupled Device), or BBD (Bucket Brigade Device), and so on, and the image scanning signals concerning the two images to be obtained at this time are used for the distance detection or focus detection. In particular, since the image is scanned in a purely electrical manner utilizing the photo-sensor arrays or image sensors, accurate signal corresponding exactly to the image pattern can be used, on account of which further improvement in precision of the distance detection or the focus detection can be expected.

However, these methods and apparatuses as have heretofore been proposed contain therein many problems still to be solved such as, for example, concrete method for processing the abovementioned image scanning signals as one aspect, hence their reduction in practice is far-reaching.

For example, in the device proposed in the above-described U.S. Patent No. 3,898,676, as already mentioned above, the image scanning signals are converted to the waveform signals by causing them to pass through low pass filters, after which the waveform signals are introduced into the phase discriminator, where detection is conducted to detect any phase difference between the two signals. In this case, since the phase discriminator deals with the waveform signals, in particular, the device becomes complicated in construction, and hence unreliable in operation, and it is not possible accurately to detect small phase differences. Accordingly the operation of the phase discriminator as the automatic focussing device is unavoidably inaccurate.

Also, in the device as proposed in the above-discussed Laid-Open Japanese Patent Application No. 51-45556, there is merely adopted a differential amplifier or a combination of the differential amplifier and a comparator as the circuit for detecting coincidence and non-coincidence of the two image scanning signals. In view, however, of the fact that the signals which the circuit deals with are time-sequential output signals from the image sensors, it is almost impossible to carry out detection of the coincidence and non-coincidence of the image scanning signals with such simple circuit construction.

Furthermore, in the method and apparatus as proposed in this Japanese application, the scanning start timing of one of the image sensors it caused to vary with respect to the scanning start timing of the other image sensor by the use of a variable delay circuit, and a period between the scanning start timings for these two image sensors is taken as the object distance. However, as has so far been well recognized, in utilizing the self-scanning type image sensors such as the photo-diode array of the charge accumulation type, CCD, or BBD, etc., if the scanning start timing, i.e., the timing for imparting the start pulse, is varied, the integration time, i.e., the effective light receiving time, also varies with the result that the level of the output signal varies. Accordingly, in the proposed method and device, since the scanning start timing of one of the image

sensors is caused to vary by the variable delay circuit with respect to the scanning start timing of the other image sensor, the two image scanning signals obtained are subject to variation in level so that a proper comparison of these two image scanning signals for detection of coincidence, cannot be made. Accordingly, the accuracy of the distance information obtained, or of the focusing operation so performed is in question.

According to the present invention there is provided a method of detecting the range of an object, comprising the steps of:—

deriving first and second mutually spaced images of the object from radiation passing from the object along different optical paths;

deriving quantized data concerning each of N successive elements of the first image and quantized data concerning each of M successive elements of the second image, wherein M is greater than N; and

detecting, on the basis of the quantized data concerning the N successive elements of the first image and the quantized data concerning the M successive elements of the second image, a location, within the M successive elements of the second image, of one set of N successive elements which is most similar to the N successive elements of the first image, the said location being indicative of the said range of the object, the quantized data deriving step comprising the steps of:—

electrically sensing the elements of the first and second images to produce an electrical representation of each of the elements;

setting the value of a variable quantization standard on the basis of at least a portion of the electrical representations produced by a previous said sensing step, and

quantizing, on the basis of the quantization standard so set, each of the electrical representations produced by the sensing step to produce the said quantized data.

According to the invention there is also provided a device for detecting the range of an object, comprising:—

optical means arranged to form first and second mutually spaced images of the object from radiation passing from the object along different optical paths;

image sensing means arranged for sensing the first and second images to produce an electrical representation of each of successive elements of the first and second images;

quantization standard setting means for setting the value of a variable quantization standard on the basis of at least a portion of the electrical representations produced by the sensing means;

quantization means for quantizing each of the electrical representations produced by the sensing means on the basis of the quantization standard previously set by the quantization standard determination means to produce quantized data concerning each of the elements of the first and second images; and

a detection system for receiving the quantized data from the quantization means and for detecting, on the basis of quantized data concerning N successive elements of the first image and quantized data concerning M successive elements of the second image, where M is greater than N, a location, within the M successive elements of the second image, of one set of N successive elements which is most similar to the N successive elements of the first image, the said location being indicative of the range of the object.

The value of said variable quantization standard may be derived from the electrical representations, produced by said previous sensing step, of the N elements of the said first image only. This value may be derived from that electrical representation having the greatest magnitude out of said at least a portion of electrical representations.

The variable quantization standard may comprise a threshold level determined by a preset proportion of said greatest magnitude.

The quantization step may comprise comparing each of the electrical representations with the quantization standard so as to produce as the quantized data, binary data on each element of said first and second images.

The quantized values are, in devices described herein, stored, as inputs, in first and second storage means where coincidence and non-coincidence of the quantized data signals stored therein are detected by coincidence detection means, while one of the sets of quantized data signals is caused to shift bit by bit relative to the other, and the shift bit quantity required until the quantized data signals of the same bit numbers concerning these first and second images become optimumly coincided are counted, thereby determining object distance from this shift bit quantity.

Preferred embodiments of the invention will now be described by way of example with reference to the accompanying drawings, in which:—

Figure 1 is a schematic diagram for explanation of the principle of the range detection according to the present invention;

Figure 2 is a combination chart of Figures 2A and 2B which are block diagrams

showing one embodiment of the circuit construction of the present invention;

Figures 3A to 3Q show various output waveforms of the outputs from the principal part of the circuit block diagram shown in Figure 2;

Figure 4 is a circuit construction diagram showing one concrete example of the pulse generating circuit in the circuit construction shown in Figure 2;

Figure 5 is a circuit construction diagram showing one concrete example of the slice level setting circuit in the circuit construction shown in Figure 2;

Figure 6 is a circuit construction diagram showing one concrete example of the control circuit in the circuit construction shown in Figure 2;

Figure 7 is a circuit diagram of one concrete example of the coincidence detecting circuit in the circuit construction shown in Figure 2;

Figures 8A to 8G show various output waveforms of the outputs from the principal part of the circuit block diagram in the coincidence detecting circuit of Figure 7;

Figure 9 is a circuit diagram showing another concrete example of the coincidence detecting circuit in the circuit construction shown in Figure 2;

Figure 10 is a schematic diagram showing another embodiment of the present invention, in particular, the optical layout of the device;

Figure 11 is a block diagram of an electrical circuit used in the construction of Figure 10 showing the construction of the principal elements different from the circuit construction shown in Figure 2;

Figure 12 is a circuit construction diagram showing one concrete example of the slice level setting circuit shown in Figure 11;

Figure 13 is a circuit construction diagram showing another concrete example of the control circuit applicable to the circuit shown in Figure 11;

Figure 14 is a block diagram of still another embodiment of the present invention showing a construction of the main elements different from that shown in Figure 2 or 11;

Figure 15 is a circuit construction diagram showing one concrete example of the control circuit when the circuit construction shown in Figure 14 is applied to the embodiment shown in Figure 2;

Figures 16A to 16K show various output waveforms of the outputs from each circuit block diagram in the control circuit shown in Figure 15;

Figure 17 is a circuit construction diagram showing one concrete example of the control circuit when the circuit construction shown in Figure 14 is applied to the embodiment shown in Figure 11;

Figures 18A to 18Q show various waveforms of the outputs from various circuit blocks in the control circuit shown in Figure 17;

Figure 19 is a circuit construction diagram showing one concrete example of the pulse generating circuit, in which the light receiving time of the sensor arrays may be automatically adjusted in accordance with brightness of an object to be detected;

Figures 20A to 20I show various output waveforms of the outputs from the principal circuit in the range detecting device shown in Figure 2 or 11 as well as in the pulse generating circuit shown in Figure 19;

Figure 21 is a circuit construction diagram showing one concrete example of the automatic resetting circuit applicable to the pulse generating circuit shown in Figure 19;

Figures 22A to 22K show various output waveforms of the outputs from the principal circuit blocks in the automatic resetting circuit shown in Figure 21, the range detecting device shown in Figure 2 or 11 as well as the pulse generating circuit shown in Figure 19;

Figure 23 is a schematic diagram showing a general construction of one embodiment, in which the range detecting device shown in Figure 2 or 11 is applied to the automatic focus adjusting system in optical apparatuses and appliances such as photographic cameras, etc.;

Figure 24 is a perspective view of a principal mechanical construction of one concrete example, in which the range detecting device shown in Figure 2 is applied to the automatic focus adjustment system in a photographic camera;

Figure 25 is a schematic circuit diagram showing a general construction of one embodiment of the display circuit for displaying termination of the range detecting operation in the automatic focus adjustment system shown in Figure 24; and

Figure 26 is a schematic diagram showing a general construction of other embodiment, in which the range detecting device shown in Figure 2 is applied to the automatic focus adjustment system in optical apparatuses and appliances such as cameras, etc.

Referring first to Figure 1, the principle of the present invention will be explained. In the drawing, reference numerals 11 and 13 designate a pair of focusing lenses for range finding which are fixedly disposed at a certain spacing defining a base line length, and numerals 12 and 14 refer to photo-sensor arrays fixedly disposed in correspondence to the focusing lenses 11 and 13. The sensor array 12 consists of N

numbers of very small photo-sensors 12_1, 12_2, ..., 12_N disposed linearly and regularly. The other sensor array 14 is of such a construction that M (where M is a number sufficiently larger than N) photo-sensors 14_1, 14_2, ..., 14_M of the same configuration as those photo-sensors 12_1, 12_2, ..., 12_N in the sensor array 12 are arranged linearly and regularly in the same manner.

In such constructional arrangement, an image of an object *O* is focussed on the sensor arrays 12 and 14 by the focussing lenses 11 and 13, respectively. In this case, the set of the lens 11 and the sensor array 12 is used for collimating the object *O*, hence the image I_1 of the object *O* formed by the lens 11 can always be focussed on a substantially fixed position on the sensor array 12 due to the optical axis of the lens 11 being made to coincide with the object *O*. In contrast to this, the image I_2 of the object formed by the lens 13 is at a relatively displaced position on the sensor array 14 with respect to the focussing position of the image I_1 on the abovementioned sensor array 12 by an amount according to the distance upto the object *O*. The relative displacement of the focussing position of the image I_2 on the sensor array 14 with respect to the focussing position of the image I_1 on the sensor array 12 can be converted to a displacement variable *x* of the image of the object *O* from its focussing position on the sensor array 14 (this being designated by I'_2 in the drawing) when the object is at infinity and the optical axis of the lens 13 intersects the object *O*, whereby a distance *D* to the object *O* can be detected from this displacement variable *x*.

In more detail, if the base line length between the lenses 11 and 13 is *d* and their focal length is *f*, the distance *D* up to the object *O* is represented from the abovementioned displacement variable *x* of the image position, as follows:—

$$D=d.f/x$$

The displacement variable *x* can be determined from the size of the photosensors 14_1, 14_2, ..., 14_M in the sensor array 14 and from the number of photosensors covering this displacement.

In order to determine this displacement variable *x*, the apparatus disclosed herein is so constructed that trains of image element signals are taken out time-sequentially from the photo-sensor arrays 12 and 14, respectively, in equal numbers (for example, N) and thereafter, these image element signal trains are consecutively converted into quantized, e.g. binary signals to be introduced as inputs into separate storage means. The quantized image element signal trains from the sensor array 12 are stored in one of the storage means, while the quantized image element signal trains from the sensor array 14 are sequentially shifted bit-by-bit, for example, by clock pulses, etc. in the other storage means. The stored signals are examined for coincidence between one storage means and the other every time a shifting takes place, and, count values obtained by counting the clock pulses used for shifting the quantized image element signal trains in the other storage means until the stored values in both storage means become most similar to each other, from the start of the shifting of the quantized image element signal trains from the sensor array 14 are used to determine the value of the abovementioned displacement variable *x*, and thus also the distance to the object *O*.

In the following, one physical embodiment of the present invention will be explained bearing in mind the general principle described in the forgoing.

In Figure 2, which is composed of Figures 2A and 2B and which shows one embodiment of the present invention, the optical layout is exactly same as that shown in Figure 1 with the exception that self-scanning type sensor arrays are used as the photo-sensor arrays 12 and 14. In the drawing, a reference numeral 16 designates a pulse generating circuit which generates reference clock pulses required for driving the abovementioned sensor arrays 12 and 14 as well as sequential controls of the circuit elements to be described in the following. The circuit is so constructed that it may generate first reference clock pulses (output *a*) shown in Figure 3(A), second reference clock pulses (output *b*) shown in Figure 3(B) at a frequency determined by dividing the frequency of the first reference clock pulses by a factor $M+\beta$, and, further, third reference clock pulses (output *c*) shown in Figure 3(C) at frequency determined by dividing the frequency of the second reference clock pulses by K (where: K is a number sufficiently larger than the number M of the sensors in the sensor array 14). A reference numeral 15 designates a driver for driving the abovementioned sensor arrays 12 and 14 based on the abovementioned second and third reference clock pulses to be generated as outputs from the pulse generating circuit 16. In this embodiment, the driver is so constructed that it may produce a start pulse $\emptyset_s$ as shown in Figure 3(D) based on the third reference clock pulse (output c) and a drive clock $\emptyset_c$ as shown in Figure 3(E) based on the second reference clock pulse (output b), and that, by applying these signals to the sensor arrays 12 and 14, it may output time-sequentially the image element signals from each

of the photo-sensors $12_1 \ldots 12_N$ and $14_1 \ldots 14_M$ in the sensor arrays 12 and 14, respectively, as shown in Figures 3(F) and (G). Incidentally, a four or two phase drive clock $\emptyset_c$ is in practice used to drive the photosensor arrays. For the sake of ready understanding, however, the explanation herein will be made with reference to a drive clock having a single phase.

Reference numerals 17 and 18 designate sample and hold circuits which are connected respectively to the sensor arrays 12 and 14, and which, by being applied from a sampling pulse feeding circuit 19 with sampling pulses occurring simultaneously with the image element signals output from the sensor arrays 12 and 14 introduce thereinto the image element signal outputs from the sensor arrays 12 and 14 and hold them until subsequent sampling pulse is applied. Consequently, pulse-shaped image scanning signals from the sensor arrays 12 and 14 as shown in Figure 3(F) and (G) are converted by these sample and hold circuits 17 and 18 into continuous 100% duty signals, as shown in Figure 3(h) and (i), respectively. The abovementioned sampling pulse feeding circuit 19 is so constructed that it may introduce the second reference clock pulses (output b) from the pulse generating circuit 16 as the input thereinto where the clock pulses are shaped into pulses coincided with the output timing of the image element signals from the sensor arrays 12 and 14, after which the thus shaped pulses are applied to the sample and hold circuits 17 and 18 as the sampling pulses, whereby the sample and hold circuits 17 and 18 become able to capture and hold a peak in the rising (or a trailing) of the image element signals from the sensor arrays 12 and 14. Incidentally, where there is used a photo-sensor device such as a combination of photo-diode arrays and CCD, in which the continuous 100% duty signals, are directly obtainable, the sample and hold circuits 17 and 18 are not required.

Numerals 20 and 21 refer to comparators for binary conversion, by comparing each of the output signal levels from the sensors $12_1 \ldots 12_N$ and $14_1 \ldots 14_M$ in the sensor arrays 12 and 14 after the sampling and holding by the sample and hold circuits 17 and 18 with a slice level set in a slice level setting circuit 22 to produce an output "high" level signal when the signal level is higher than the slice level, and an output "low" level signal when the signal level is lower than the slice level. By these comparators 20 and 21, each of the output signals from each of the sensors $12_1 \ldots 12_N$ and $14_1 \ldots 14_M$ of the sensor arrays 12 and 14 after the sampling and holding operations by the abovementioned sample and hold circuits 17 and 18 are converted into binary quantized signals as shown in Figure 3(J) and (K). The slice level to be established in the slice level setting circuit 22 is automatically determined on the basis of the outputs from sensor array 12 so as to produce optimum binary signal trains for comparison. The manner of predetermining the slice level will be described in greater detail later herein.

Reference numerals 23 and 24 respectively designate serial-in-parallel-out type shift registers for storing the respective quantized image element signal trains (cf. Figure 3, (J) and (K)) output from the respective comparators 20 and 21. In this embodiment, the shift registers are of N-bit ($A_1 \ldots A_N$ and $B_1 \ldots B_N$) construction in correspondence to the number of sensors in the sensor array 12, and are driven by the second referenc clock pulse (output b) from the pulse generating circuit 16 at the same clock speed in conformity with the emission speed of the image element signals from the sensor arrays 12 and 14. Accordingly, these shift registers function in such a manner that each of the quantized image element signals output by the comparators 20 and 21 is sequentially stored, while shifting the signals bit-by-bit for every clock pulse, and the thus stored quantized values can be produced as parallel outputs.

A reference numeral 25 designates a control circuit which controls feeding of the clock pulse for shifting to the shift register 23, feeding of the second reference clock pulse (output b) from the abovementioned pulse generating circuit 16 to a counter 28 which counts the number of second reference clock pulses (output b), and, further, operations of a coincidence detecting circuit to be described later. The control circuit is so constructed that is introduces as the inputs thereinto both the second reference clock pulse (output b) and the third reference clock pulse (output c) from the abovementioned pulse generating circuit 16, then applies to an "AND" gate 26 provided for controlling feeding of the shift clock pulse to the shift register 23 a signal (output d) as shown in Figure 3(L) which maintains a high level during a period from the generation of the third reference clock pulse (output c) upto the generation of the α+Nth pulse of the second reference clock pulse (output b) in the pulse generating circuit 16, and maintains a low level during a period from the generation of the α+Nth pulse of the second reference clock pulse (output b) upto the generation, again, of the third reference clock pulse (output c), and applies to an "AND" gate 29 provided for controlling feeding of the abovementioned second reference clock pulse (output b) to

the abovementioned counter 28 a signal which is the complement of the abovementioned output *d*, i.e., a signal (output e) which maintains a low level during a period from the generation of the third reference clock pulse (output c) upto the generation of the α+Nth pulse of the second reference clock pulse (output b) and maintains a high level during a period from the generation of the α+Nth pulse of the second reference clock pulse upto the generation, again, of the third reference clock pulse (output c), as shown in Figure 3(M), and applies to the coincidence detecting circuit 27 a signal (output f) which maintains a low level during a period from the generation of the third reference clock pulse (output c) upto the generation of the α+N−1st pulse of the second reference clock pulse (output b) and maintains a high level during a period from the generation of the α+N−1st pulse of the second reference clock pulse upto the generation, again of the third reference clock pulse, as shown in Figure 3(N).

Accordingly, the shift register 23 is to be fed with only the first to α+Nth pulses of the second reference clock pulse (output b) through the "AND" gate 26 after generation of the third reference clock pulse (output c) as shown in Figure 3(O), on account of which it is caused to stop its shifting operation at the time of completion of the storage of the quantized image element signals from all of the sensors 12_1 ... 12_N in the sensor array 12, and then to hold these stored values. In contrast to this, the shift register 24, is shift-connected so far as the second reference clock pulse (output b) from the pulse generating circuit 16 is imparted thereto, so that the stored signals in the register 24 are shifted bit-by-bit once every clock pulse (output b) with respect to the stored signals in the shift register 23 by the pulses after the α+N+st. As a result, sets of N quantized image element signals, each set being displaced for one bit, (14_1 ... $14_N \rightarrow 14_2$ ... $14_{N+1} \rightarrow 14_3$ ... $14_{N+2} \rightarrow$ ...) are produced in parallel as the outputs upon successive shifting operations.

Further, since the "AND" gate 29 permits the abovementioned second reference clock pulse (output b) to pass therethrough only during the period when the output *e* from the control 25 is at the high level as shown in Figure 3P, the counter 28 receives at its clock input CK, those pulses after the α+N+1st of the second reference clock pulse (output b), and counts the these pulses, i.e., it counts the number of shifts of the quantized image element signals in the shift register 24 after stoppage of the shifting operations in the abovementioned shift register 23, or, more particularly, number of relative shifts between the quantized image element signal trains from the sensor 14 and the quantized image element signal trains from the sensor array 12. Incidentally, the contents of the counter 28 can be cleared by application of the abovementioned third reference clock pulse (output c) to its clear terminal CLR.

Incidentally, it will be understood from Figures 3(B) to 3(G) that the value of "α" corresponds to a delay between the first pulse of the second reference clock (output b) from the pulse generating circuit upon generation of the third reference clock pulse (output c) and the start of output of image element signals from the sensor arrays 12 and 14. This number "α" may be arbitrarily selected in conformity to this delay from the abovementioned first pulse until the output image element signals from the sensor arrays commences in accordance with the mode of driving by the driver as well as the characteristics of the sensor array to be employed.

A reference numeral 27 designates a coincidence detecting circuit which detects coincidence and non-coincidence of the N stored quantized signals in both shift registers 23 and 24. In this embodiment, the circuit 27 is so constructed that it may produce an output coincidence signal as shown in Figure 3(Q) when it has detected the optimumly coincided state, if not a perfect coincidence of the signals in the corresponding stages of the shift registers. This coincidence detecting circuit 27 is also controlled by the output *f* (Figure 3N) from the control circut 25 in such a manner that it may conduct the coincidence detection between the stored signals in the shift registers 23 and 24 only during the period when the output *f* is at the high level, the details of which will be explained later.

A numeral 30 refers to a register which reads thereinto a counted value of the abovementioned counter 28, in response to the coincidence output signal from the coincidence detecting circuit 27, at the time when the detection circuit 27 has detected the maximum coincidence between the stored signals in both shift registers 23 and 24. The abovementioned coincidence detecting circuit 27 is so connected that the coincided signal therefrom may be applied to a load terminal LD of the register 30.

A numeral 31 refers to a latching circuit which takes thereinto for latching the recorded values in the abovementioned register 30 in response to the third reference clock pulse (output c) from the pulse generating circuit 16, i.e., at every time the scanning of the object images by the sensor arrays 12 and 14 commences. This latching circuit is so connected that the third

reference clock pulse (output c) may be applied thereto through an inverter 32.

A reference numeral 33 designates a D/A converter which is so constructed that it may receive as an input thereto a latched value in the abovementioned latching circuit 31, and may process this input value in accordance with the equation for determining the distance, i.e., D=f.d/x which has been explained in relation to Figure 1, to produce an output signal (e.g., a voltage value) denoting the distance D. A reference numeral 34 designates a meter as an indicating device to indicate the distance upto the object for the range detection, and is connected to an output terminal 33a of the D/A converter 33.

In the above-described construction, the set of the lens 11 and the sensor array 12 are collimated with respect to the object for the range detection, and an image to be a reference of the object is focussed by the lens 11 on a substantially fixed position on the sensor array 12. On the other hand, when the second and third reference clock pulses as shown in Figure 3B and 3C are generated from the pulse generating circuit 16 with the object image being formed on the sensor array 14 at a relatively displaced position thereon depending on the distance to the object, the driver 15 is actuated, whereby the image element signals are output time-sequentially from the sensors in the sensor arrays 12 and 14 (Figure 3F and G). These image element signals are then converted into continuous wave signals as shown in Figure 3H and I by means of the sample and hold circuits 17 and 18, after which these full wave signals are compared by the comparators 20 and 21 with the slice level established in the slice level setting circuit 22, and then applied to the shift registers 23 and 24, while being converted to quantized signals.

At this time, the control circuit 25 applies the high level signal (output d) to the "AND" gate 26 as shown in Figure 3L in response to the third reference clock pulse (output c) from the pulse generating circuit 16. Accordingly, the shift registers 23 and 24 sequentially store the quantized image element signal trains to be output from the abovementioned comparators 20 and 21 while being driven by the second reference clock pulse (output b) from the pulse generating circuit 16, and shifting bit-by-bit, and produce these stored signals in the form of parallel outputs.

In this sequence operation, the control circuit 25 applies to the "AND" gate 29 the low level signal (output e) as shown in Figure 3(M), so that feeding of the second reference clock pulse (output b) from the pulse generating circuit 16 to the counter 28 is interrupted (vide Figure 3 (P)). When the α+Nth pulse output of the second reference clock pulse (output b) from the pulse generating circuit 16 is produced, the control circuit 25 at this time instant applies to the "AND" gate 26 the low level signal (output d) as shown in Figure 3(L) to interrupt feeding of the second reference clock pulse (output b) from the pulse generating circuit 16 to the shift register 23 to thereby stop the shifting operation (accordingly, the shift register 23 holds the quantized image element signal trains from the whole sensors $12_1 \ldots 12_N$ in the sensor array 12 (vide Figure 3(O)) and to apply to the "AND" gate 29 the high level signal (output e) as shown in Figure 3(M) to cause feeding of the second reference clock pulse (output b) from the pulse generating circuit 16 to the counter 28 to start (vide Figure 3(P)). Accordingly, the shifting operation of the shift register 24 alone is continued with respect to the pulses commencing at the α+N+1st of the second reference clock pulse (output b), and counting of the second reference clock pulse (output b) by the counter 28 commences at the α+N+1st pulse of this second reference clock pulse.

On the other hand, the coincidence detecting circuit 27 starts the coincidence detection of the recorded values in both shift registers 23 and 24 at the moment when the quantized image element signals from all of the sensors 12_1 to 12_N in the sensor array 12 are stored in the shift register 23 by the output *f* of the abovementioned control circuit 25, the signal level of which changes from low to high when the α+N−1st output pulse of the second reference clock pulse (output b) from the pulse generating circuit 16 is produced as shown in Figure 3(N) and, at the same time, the quantized image element signals from the first N sensors, i.e. sensors 14_1 to 14_N, of the sensor array 14 have been recorded in the shift register 24, and, in the course of the shift register 24 alone being subjected to the bit-by-bit shifting operations by the pulses commencing with the α+N+1st pulse of the second reference clock pulse (output b) and the train of N quantized image element signals stored therein being shifted sequentially such as to represent, successively, image elements 14_1 to 14_N, then 14_2 to 14_{n+1}, then 14_3 to 14_{N+2} and so on, when the circuit 27 detects a state of coincidence or substantial coincidence between the quantized signals stored in the registers 23 and 24 it produces an output coincidence signal 30 as shown in Figure 3(Q) to the register 30. The register 30, the load terminal LD of which has been applied with the coincidence signals from the coincidence detecting circuit 27 then reads thereinto counted values of the abovementioned counter 28. Accordingly,

the recorded values of the register 30 at this moment become the distance information to the object. Thereafter, the recorded values of the register 30 are latched by the latching circuit 31 in response to the third reference clock pulse output (output c) from the pulse generating circuit 16 at the start of the subsequent scanning operation of the object images, after which they are converted into, for example, voltage values, by means of the D/A converter 33. The output of the D/A converter drives the meter 34 which thereby indicates the distance information by the deflection of its indicator needle 34a, of the meter 34 being connected to an output terminal 33a of the converter 33. It may, of course, be possible to indicate digitally this information by the use of a digital indicating element in place of the analog indicating means as illustrated. In this case, the values latched by the latching circuit 33 are converted into digital codes for indication, based on which the abovementioned digital indicating element may be driven.

In the following practical examples of the pulse generating circuit 16, the slice level setting circuit 22, the control circuit 25, and the coincidence detecting circuit 27 in the circuit construction shown in Figures 2A and 2B will be described in detail.

First, the pulse generating circuit 16, may, for example, be of a construction as shown in Figure 4. In the drawing, a numeral 35 refers to an oscillator which, in this embodiment, has been so pre-adjusted as to generate the first reference clock pulse shown in Figure 3A. A numeral 36 refers to a first counter coupled to receive therein clock pulses from the oscillator 35 through its clock input terminal CK and to count these pulses. The counter 36 is so constructed that it may produce an output signal from its carry output terminal CY every time the count value reaches a carry value set in a first switching circuit 37 provided for setting the carry value. A reference numeral 38 designates a second counter which receives thereinto a carry signal from the first counter 36 through its clock input terminal CK and counts such carry signals. The counter 38 is so constructed that it may produce a carry output signal from its carry output terminal CY every time the count value arrives at a carry value, set in a second switching circuit 39 for setting the carry value for the counter 38. Also, a reference symbol Tr designates a transistor, to the collector side of which a voltage Vcc is applied, the emitter of which is connected to the earth, and the base of which is connected to the carry output terminal of the second counter 38.

According to such construction, the first reference clock pulses as shown in Figure 3A are produced as the output *a* from the oscillator 35; every time the count value in the first counter 36, produced by counting the first reference clock pulses (output a), reaches the value set by the first switch circuit 37, a pulse is generated in a signal line connected to the carry output terminal CY of the counter 36. Also, every time the count value in the second counter 38, produced by counting the carry signals from the first counter 36, reaches the value set by the second switch circuit 39, a pulse is generated in the signal line connected to the collector side of the transistor Tr due to its conduction or response to the carry output signal from the second counter. Here, if a constant $N+\beta$ is set by the combination of selective closure of the switches in the first switch circuit 37, and a constant K is set by the selective closure of the switches in the second switch circuit 39 in consideration of the abovementioned number α and the number M of the sensors in the sensor array 14, the second reference clock pulse (output b) as shown in Figure 3B can be obtained from the signal line connected to the carry output terminal CY of the first counter 36 at every time the first counter 36 counts $N+\beta$ first reference clock pulses (output a) from the oscillator 35, and also the third reference clock pulse (output c) shown in Figure 3C can be obtained from the signal line connected to the collector side of the abovementioned transistor Tr the third reference as the output *c* at every time the second counter 38 counts K carry signals from the first counter 36. Incidentally, each of the carry signals of the counters 36 and 38 is fed back to the respective load terminal LD thereof through the respective inverters 67 and 68. This feed back operation is for causing these counters 36 and 38 to introduce thereinto the values set in the switch circuits 37 and 39 respectively as the respective carry values when the counters 36 and 38 have completed counting upto the values already set in the switch circuits 37 and 39.

Next, the slice level setting circuit 22, may, for example, be of a construction as shown in Figure 5. In the drawing, a reference numeral 40 designates a peak hold circuit which holds sequentially the output peak values from the abovementioned sample and hold circuit 17. This peak hold circuit 40 consists of a differential amplifier 41, a capacitor Co to hold the peak values, and a diode Do for prevention of back flow. A numeral 42 refers to a sample and hold circuit which is so connected as to sample and hold the peak values held in the capacitor Co in the abovementioned peak hold circuit 40 in response to the third reference clock pulse from the abovementioned pulse generating

circuit 16 by its application to the clock input terminal CK through an inverter 47. A reference numeral 43 designates an operational circuit for determining a slice level on the basis of an output from the sample and hold circuit 42. This operational circuit consists of an operational amplifier 44 and a variable resistor VR for setting a constant to determine the slice level, wherein an output from the operational amplifier 44 is imparted to the abovementioned comparators 20 and 21 as the slice level. A numeral 45 refers to an analog switch for clearing the peak values held in the peak hold circuit 40. This analog switch is so constructed that it is connected to the capacitor Co in the peak hold circuit 40 and becomes conductive by application of the third reference clock pulse (output c) from the abovementioned pulse generating circuit 16 to its control terminal *c* through the inverter 47 and a shift register 46 to clear the values held in the capacitor Co. The shift register 46 is provided for delaying a timing to render the analog switch 45 to be conductive after a predetermined time τ from the generation of the third reference clock pulse (output c) in the pulse generating circuit 16. In this embodiment, this shift register 46 is so constructed that, after the third clock pulse (output c) is introduced as an input thereinto at its input terminal in through the inverter 47, this third clock pulse may be applied to the control terminal *c* of the analog switch 45 at the time when a number, corresponding to the bit construction number, of second reference clock pulses (output b) as shown in Figure 3B have been applied to its clock input terminal CK, whereby the value held in the capacitor Co becomes cleared or response to the third reference clock pulse (output c) but with the abovementioned time delay τ after the completion by the abovementioned sample and hold circuit 42 of the sampling and holding of the values held in the capacitor Co. The bit construction number of the shift register 46 in this case may be kept below the number α as already explained in connection with Figure 2.

According to such construction, the peak values of the output from the sample and hold circuit 17 (i.e., the peak values of the output from the sensor array 12) are first held in the capacitor Co in the peak hold circuit 40 at the time of scanning of the object image by the sensor array 12, and, after termination of the scanning operations, when the third reference clock pulse output (output c) as shown in Figure 3C is generated from the pulse generating circuit 16 at the start of the subsequent scanning operation, the sample and hold circuit 42, in response to this subsequent scanning, takes thereinto the peak values held in the abovementioned capacitor Co, and applies the values to the operational circuit 43. In the operational circuit 43 which has received the output from the sample and hold circuit 42, the operational amplifier 44 determines the slice level on the basis of the output from the sample and hold circuit 42, i.e., the peak value of the output from the sample and hold circuit 17 during the previous scanning of the object image and a slice level determining constant set in the variable resistor VR, and then forwards the thus determined slice level, as the output, to the comparators 20 and 21 for use in the quantizing operation, whereby both comparators 20 and 21 convert the outputs from the sample and hold circuits 17 and 18 into quantized signals on the basis of the slice level determined by the operational circuit 43.

As stated in the foregoing, the capacitor Co in the abovementioned peak hold circuit 40 is cleared of the hold values in the previous scanning by the analog switch 45 to become conductive in response to the output from the shift register 46 after lapse of the abovementioned delay time τ since the sample and hold circuit 42 has sampled and held the values held in the capacitor Co. Thereafter, the capacitor Co starts holding the peak values of the output from the sample and hold circuit 17 during the subsequent scanning of the object image by the sensor array 12.

Thus, in the construction of the slice level setting circuit 22 shown in Figure 5, the slice level at the time of a current scanning operation of the object image is automatically established upon the basis of the peak value of the output from the sensor array obtained during the previous scanning operation of the object image.

For the slice level determining constant to be set in the variable resistor VR in the abovementioned operational circuit 43, experiments have revealed that a constant of from 0.6 to 0.8 or so, i.e., a value which renders the output level from the operational amplifier 44 to be 60% to 80% of the peak level of the output from the sensor array 12 is preferable.

Thirdly, the control circuit 25 may, for example, be of a construction as shown in Figure 6. In the drawing, a reference numeral 48 designates a counter which introduces the second reference clock pulse (output b) as shown in Figure 3B from the pulse generating circuit 16 as the input thereto through its clock input terminal CK to be counted thereby, and which is cleared of its contents by the third reference clock pulse (output c as shown in Figure 3C). A numeral 49 refers to a first comparator which compares the counted value of the

counter 48 with a value set by a first constant setting switch circuit 50, and produces a coincided signal output when the counted value of the counter 48 becomes coincided with the value set by the first switch circuit 50. A numeral 51 refers to a first J—K type flip-flop which introduces into its clock input terminal CK the coincided signal from the first comparator 49 through an inverter 52. A reference numeral 53 designates a second comparator which compares the count value of the counter 48 with a value established by a second constant setting switch circuit 54, and produces a coincided signal output when the count value of the counter 48 becomes coincided with the value set by the second switch circuit 54. A reference numeral 55 denotes a second J—K type flip-flop which introduces the coincided signal from the second comparator 53 as an input into its clock input terminal CK through an inveter 56. Each of the abovementioned first and second flip-flops 51 and 55 is of such a construction that a voltage Vcc is applied to its input terminal J, its input terminal K is connected to the earth, and its clear terminal CLR receives the third reference clock pulse (output c) from the pulse generating circuit 16 as is the case with the abovementioned counter 48.

In this construction, outputs Q and $\overline{Q}$ of the first flip-flop 51 are first considered. In the state wherein the first flip-flop 51 is cleared by the third reference clock pulse (output c) from the pulse generating circuit 16, the output $\overline{Q}$ is at a "high" level, while the output Q is at a "low" level. When the counter 48 starts its counting operation from the first pulse of the second reference clock pulse (output b) after it is cleared by the third reference clock pulse (output c), and its count value has reached the value set by the first switch circuit 50, a coincided signal output is produced from the first comparator 49, whereby the first flip-flop 51 which receives this coincided signal through the inverter 52 is inverted, with the result that the output $\overline{Q}$ changes from the "high" level to the "low" level, and the output Q changes from the "low" level to the "high" level. Subsequently, when cleared again by the abovementioned third reference clock pulse (output c), the output $\overline{Q}$ reinstates its level from "low" to "high", and the output q from "high" to "low". Consequently, when a constant α+N is set by the selective closure of the switches in the first switch circuit 50, the first flip-flop 51 will become inverted at the time that the count value of the counter 48 reaches α+N. On account of this the outputs $\overline{Q}$ and Q take the "high" level and the "low" level, respectively, during the period from the generation of the third reference clock pulse (output c) from the pulse generating circuit 16 to the generation of the α+Nth pulse of the second reference clock pulse (output b). Thereafter, the outputs $\overline{Q}$ and Q, respectively take the "low" level and the "high" level until the third reference clock pulse (output c) is again generated in the subsequent stage. As the result, the output $\overline{Q}$ of the first flip-flop 51 can be utilized as the output *d* shown in Figure 3L for controlling the "AND" gate 26, and the output Q can be utilized as the output *e* shown in Figure 3M for controlling the "AND" gate 29.

Considering now the output Q from the second flip-flop 55, it shows the same change as the output Q of the first flip-flop 51, as is apparent from the foregoing explanations. Accordingly, when the constant α+N−1 is set by the selective closure of the switches in the second switch circuit 54, the second flip-flop 55 is inverted when the count value of the counter 48 reaches α+N−1. On account of this, the output Q thereof is at the "low" level during the period from the generation of the third reference clock pulse (output c) from the pulse generating circuit 16 to the generation of the α+N−1st pulse of the second reference clock pulse (output b), thereafter, it takes "high" level until the third reference clock pulse (output c) is again generated subsequently. As the result, the output Q of this flip-flop 55 can be utilized as the output *f* shown in Figure 3N for controlling the coincidence detecting circuit 27.

Lastly, the coincidence detecting circuit 27, may, for example, be of a construction as shown in Figure 7 or in Figure 9.

Here, a particular point should be mentioned. In the coincidence detection between the recorded values in the shift registers 23 and 24, it is ideal that coincidence is signified between recorded values in the shift registers 23 and 24 when all of the outputs from the corresponding bits in these shift registers 23 and 24 are perfectly coincident. However, it occurs from time to time that when the outputs from each of the sensors 12_1 to 12_N and 14_1 to 14_M in the respective sensor arrays 12 and 14 are converted into quantized signals by comparing them with the slice level set in the slice level setting circuit 22 through the comparators 20 and 21, those output signals which are very close to the slice level are determined in some cases as being at the "high" level, and in other cases as being at the "low" level. Accordingly, since probability of the perfect coindence between the recorded values in the shift registers 23 and 24 becomes extremely low in practice, it is more practical to adopt

such a method that satisfactory coincidence is considered to have been attained, if the recorded values in the corresponding bits coincide at a predertermined ratio.

Explaining first the embodiment shown in Figure 7, the construction of the coincidence detecting circuit 27 is such that coincidence between the recorded values in the shift registers 23 and 24 is signified at the time instant when quantized image element signals recorded in the mutually corresponding bits A_1—B_1, A_2—B_2, ..., A_N—B_N in the shift registers 23 and 24 are coincided at and above a predetermined ratio.

In the drawing, a reference numeral 57 designates a group of gates consisting of exclusive "NOR" gates 57_1 to 57_N (i.e., in number corresponding to the bit numbers in the shift registers 23 and 24, or N numbers). In this construction, the outputs from the mutually corresponding bits A_1—B_1, ..., A_N—B_N in the shift registers 23 and 24 are introduced as the inputs into their respectively corresponding exclusive "NOR" gates 57_1 to 57_N, and the gates produce "high" level output signals when the recorded values in mutually corresponding bits A_1—B_1, ..., A_N—B_N are equal, and "low" level output signals when they are different.

A numeral 58 refers to a shift register of N-bit construction which receives and stores the outputs from each of the exclusive "NOR" gates 57_1 to 57_N in the group of gates 57 in the respective bits 1 to N corresponding thereto at every time the second reference clock pulse (output b shown in Figure 3B) and Figure 8B from the pulse generating circuit 16 is applied to its load terminal LD through an "AND" gate 59. The "AND" gate 59 has been supplied with the output *f* from the control circuit 25 (as shown in Figure 3N and Figure 8C), and the shift register 58 is, accordingly, supplied with pulses after the α+Nth pulse of the abovementioned second reference clock pulse (output b) as shown in Figure 8E, whereby the outputs from the gates 57 are introduced from the time instantly when the N quantized image element signals from the first N sensors 14_1 to 14_N in the sensor array 14 are recorded in the shift register 24, and thereafter the outputs from the gates 57 are repeatedly introduced at every shifting of the shift register 24.

A reference numeral 61 designates an "AND" gate which imparts the first reference clock pulse (output *a* as shown in Figure 3A and Figure 8A) from the pulse generating circuit 16 to the clock input terminal CK of the shift register 58. Further, outputs (Figure 8D) from the "AND" gate 59 are imparted to this "AND" gate 61 with the phase being inverted by an inverter 60 as shown in Figure 8E. Accordingly, as shown in Figure 8F, the first reference clock pulse (output a) is applied to the shift register 58 only when the output from the "AND" gate 59 is at the low level, i.e., with a timing which does not carry out shifting in the shift register 24, whereby the recorded values of each bit in the shift register are produced sequentially and in series as the outputs.

A reference numeral 62 denotes an "AND" gate which takes an "AND" between the output of the shift register 58 and the first reference clock pulse (output a) to produce only "high" level signal outputs among those outputs from the shift register 58. A reference numeral 63 designates a counter which counts the number of the "high" level signal outputs from the "AND" gate 62. This counter is so controlled that it is cleared by the signals (Figure 8E) from the inverter 60 at every time the second reference clock pulse (output b) trails, (i.e., the output of the inverter 60 rises) and that it counts the output numbers from the "AND" gate 62 only when the second reference clock pulse (output b) is at the low level, (i.e., when the output from the inverter 60 is at the "high" level). Accordingly, the counted values of the counter 63 denote the coincided numbers of the recorded values in the mutually corresponding bits A_1—B_1, ..., A_N—B_N of the shift registers 23 and 24.

According to the abovementioned construction, the instant at which the count value of the counter 63 becomes N corresponds to the time when the recorded values in both shift register 23 and 24 are in the perfect coincidence. However, the determination of the coincidence of the recorded values in both shift registers 23 and 24 as the time when the count values of the counter 63, have become N is not realistic in view of the practical considerations described in the foregoing. In this embodiment, therefore, there is adopted such a circuit construction that imparts outputs of arbitrary bits in the counter 63 (the more significant bits may preferably be included) to the "AND" gate 64 together with the first reference clock pulse (output a), and produces high level signal output (Figure 8G) from the "AND" gate 64 when the preselected bit outputs in the counter 63 are all at the high level.

According to such construction, when the counted values of the counter 63 have become greater than a value previously established by the selection of the aforesaid arbitrary bits, in other words, when the recorded values in the mutually corresponding bits A_1—B_1, ..., A_N—B_N in the shift registers 23 and 24 have become coincided at a predetermined ratio and

above, "high" level signal outputs are produced from the "AND" gate 64, and these "high" level signals can be utilized as the coincided signals as already mentioned in the foregoing.

In the construction of the coincidence detecting circuit 27 shown in Figure 7, the coincided signals (Figure 3Q) are obtained in the form of $N+\beta-1$ pulses corresponding to the first pulse to the $N+\beta-1$st pulse in the first reference clock pulse (output a), as shown in Figure 8G. However, as will be understandable from Figure 8A to 8G and the foregoing explanations, since these $N+\beta-1$ coincided pulses are all generated within a pulse-to-pulse time duration of the second reference clock pulse (output b), they may safely be applied as the load signals to the register 30 in the form in which they are generated. Also, when the construction as shown in Figure 7 is used as the coincidence detecting circuit 27, the latching circuit as shown in Figure 2 may be dispensed with.

The embodiment shown in Figure 9 is a modification of that shown in Figure 7, which is so constructed that coincidence between the recorded values in the shift registers 23 and 24 is detected by detecting the time instant when the count value of the counter 63 is at a maximum, in other words, when the numbers of coincidence between the recorded values in the mutually corresponding bits A_1—B_1, . . ., A_N—B_N of the shift registers 23 and 24 have become maximum. In the drawing, the same elements and signals as those in Figure 7 are designated with the same reference symbols.

In the drawing, a reference numeral 65 designates a magnitude comparator which is capable of determining the relative magnitude of the recorded values in a register 66 and the counted values in the counter 63. The comparator is so constructed that it may produce "high" level signal outputs when the counted values C of the counter 63 is greater than the recorded values R of the register 66 ($C>R$), and that, while the "high" level signals from the comparator 65 are applied to the load terminal LD of the register 66 as the load signals, they may also be applied to the load terminal LD of the register 30 in Figure 2. Accordingly, these registers 66 and 30 are able to introduce thereinto the counted values of the counters 63 and 28 at that instant in response to the high level signal outputs from the comparator 65 when such are produced.

According to such construction, so far as the high level signal outputs are continuously produced from the comparator 65, the registers 66 and 30 introduce thereinto the counted values of the counters 63 and 28 at every time and in response to such output signals produced. On account of this, at the termination of one scanning operation of the object image, the values recorded in these registers 66 and 30 will be the maximum counted values of the counter 63 and the counted values of the counter 28 at the instant when the counted values of the counter 63 have become maximum, respectively. Consequently, as explained above in connection with Figure 2, if the recorded values of the register 30 are latched by the latching circuit 31 at the start of the subsequent scanning, the output from the latching circuit 31 at this time represents the shift numbers of the shift register 24 which have been spent until the recorded values in the shift registers 23 and 24 become optimumly coincided, i.e., the so-called object distance.

As is apparent from the foregoing explanations, no coincided signals as shown in Figure 3Q can be obtained with the construction of the coincidence detecting circuit 27 shown in Figure 9, but the counted values of the counter 28 at the instant when the recorded values in the shift registers 23 and 24 have become optimumly matched may be accurately recorded in the register 30.

In the following, another embodiment of the range detecting method and apparatus according to the present invention will be explained in reference to Figures 10 and 11. This embodiment differs from the embodiment shown in Figure 2 in that a single photo-sensor array is utilized in place of a pair of photo-sensor arrays 12 and 14. Accordingly, the relevant figures of drawing show only the construction of those main parts which particularly differs from that of the afore-described embodiment, and in which the similar component elements to those in the previous embodiment are designated by the same reference symbols, and the explanations will be directed to those parts alone which differ from the previous embodiment.

In Figure 10, reference numerals 11 and 13 designate a pair of focussing lenses fixedly disposed at a definite spacing defining a base line length *d*, as in the previous embodiment.

In this embodiment, the optical layout of the component elements is such that a single photo-sensor array 69 consisting of L photo-sensors 69_1 to 69_L (where: L is a number sufficiently larger than 2N such as, for example, $L=N+M$ in view of the embodiment in Figure 2) may be disposed in confrontation to these lenses 11 and 13 so as, on the one hand, to constantly focus an image I_1 of an object for the range detection formed by the lens 11 at a substantially definite position on a first sensor region 69a

containing the initial N numbers of sensors 69_1 to 69_N of the sensor array 69 by way of an obliquely fixed mirror 70 and a reflecting surface 72a of a reflecting prism 72 (hence the combination of the lens 11 and the first sensor region 69a may be applied for collimation to the object for the range detection, same as described in the foregoing), and, on the other hand, to focus an image I_2 of the object formed by the lens 13 at a position corresponding to a distance to the object on a second sensor region 69b containing (L—N) sensors, namely sensors 69_{N+1} to 69_L, by way of an obliquely fixed mirror 71 and another reflecting surface 72b of the reflecting prism 72.

According to such construction, if it is assumed that the object is at infinity, the image thereof to be formed by the lens 13 is focussed at a position designated by a reference symbol I'_2 (within a range of the sensors 69_{N+1} to 69_{2N}) in the drawing along a route shown by a dash line. Contrary to this, when the object is at a finite distance, the object image is focussed at a position designated by a reference symbol I_2 along a route shown by a solid line in the drawing.

Accordingly, when the value of a relative displacement variable x of the focussing position of the image I_2 to the focussing position I'_2 of the image of the object at infinity is determined the distance to the object can be ascertained. In order to measure this displacement variable x the embodiment of the present invention shown in Figure 10 operates in such a manner that quantized image element signal trains from the N numbers of the sensors 69_1 to 69_N in the first sensor region 69a are first introduced as the input into first storage means at the time when the image element signals are time sequentially taken out of each of the sensors 69_1 to 69_L in the sensor array 69, then quantized image element signal trains from the sensors of the same numbers in the second sensor region 69b as the output are introduced into the second storage means as the input thereto to cause the quantized image element signal trains in this second storage means to sequentially shift relative to the signals in the first storage means. In this way, the degree of shifting during a period from the start of the relative shifting operation up to a time when the stored values in both storage means can be considered as being substantially coincided with each other is determined, by counting individual shifts, and the shift count value is converted into the above-mentioned displacement quantity x i.e., the distance information of the object for the range detection.

The physical circuit construction of the embodiment shown in Figure 10 will now be explained in more detail in reference to Figure 11.

In the drawing, a reference numeral 22' designates a slice level setting circuit corresponding to the slice level setting circuit 22 in Figure 2. In this circuit construction, the slice level setting circuit 22' is so designed that it may set the slice level based on the peak value of the outputs from the first sensor region 69a of the sensor array 69 in correspondence to the slice level setting circuit 22 in Figure 2, the details of which will be described later. Similarly, a numeral 25' refers to a control circuit which corresponds to the control circuit 25 in Figure 2. This control circuit 25' is so constructed that, in conformity with changes in the sensor array, it may first impart to the "AND" gate 29 a signal, as an output e', which maintains a low level during a period from the generation of the third reference clock pulse output (output c shown in Figure 3C) from the pulse generating circuit 16 upto termination of the α+2Nth pulse output of the second reference clock pulse (output b shown in Figure 3B), and, thereafter, maintains a high level upto a time when the third reference clock pulse output (output c) is again produced, that is, a signal which causes the counter 28 to count pulses after the α+2N+1st pulse of the second reference clock pulse (output b); and, on the other hand, impart to the coincidence detecting circuit 27 a signal, as an output f', which maintains a low level during a period from the generation of the third reference clock pulse putput (output c) upto the termination of the α+2N−1st pulse output of the second reference clock pulse (output b), and, thereafter, maintains a high level upto a time when the third reference clock pulse output (output c) is again produced, that is, a signal to start the coincidence detection at the time instant when the quantized image element signals from the initial N sensors (i.e. the sensors 69_{n+1} to 69_{2N}) in the second sensor region 69b of the sensor array 69 are recorded in the shift register 24 (the details of this operation will be described later).

Incidentally, an "AND" gate 73 same as the "AND" gate 26 provided in the shift register 23 is also provided in the shift register 24 so that the control signal (output d shown in Figure 3L) to be imparted to the "AND" gate 26 from the control circuit 25' may also be imparted to the "AND" gate 73 through an inverter 74. According to this construction, of the second reference clock pulse outputs (output b) from the pulse generating circuit 16, the first to the α+Nth pulses alone are fed to the shift register 23, while the α+N+1st to the Kth pulses alone are fed to the shift register 24. Accordingly even if the data lines to the quantizing

comparator 20 in both shift registers 23 and 24 are common, the quantized image element signal trains from the N numbers of the sensors 69_1 to 69_N in the first sensor region 69a are introduced as input into the shift register 23 alone, while the quantized image element signal trains from the N sensors in the second sensor region 69b are introduced as input into the shift register 24 alone. Moreover, in the shift register 24, there is carried out the sequential shifting of the quantized image element signal trains by the clock pulses after the $\alpha+2N+1$st. Accordingly, the circuit construction shown in Figure 11 performs the same distance detecting operations as in the circuit construction shown in Figure 2.

The slice level setting circuit 22' has a circuit construction as shown, for example, in Figure 12. The illustrated construction, besides the construction shown in Figure 5, is further added with a construction which restricts feeding of the sensor output to the peak hold circuit 40 to an output from the first sensor region 69a in the sensor array 69 alone.

In the drawing, a reference numeral 75 designates a counter which counts the second reference clock pulse (output b) from the pulse generating circuit 16; 76 refers to a comparator which compares the counted values in the counter 75 with a constant set in a constant setting switch circuit 77, and produces an output coincidence signal when the counted values have become coincided with the constant set in the switch circuit 77; 78 refers to a J—K type flip-flop which is so connected in the circuit construction that it may be set by receiving in its input terminal J the third reference clock pulse (output c) from the pulse generating circuit 16 through the inverter 47, and in that set state produce from its output terminal Q the input J as an output in synchronism with the second reference clock pulse (output b) received at its clock terminal C, and that it may be reset by receiving a coincided signal from the comparator 76 in its input terminal K; and 79 designates an analog switch which is so circuit-connected that it may receive the output Q from the flip-flop 78 in its control terminal, and, when the output Q assumes the "high" level, become conductive in response thereto to enable the output from the sample and hold circuit 17 to be imparted to the peak hold circuit 40.

According to such circuit construction, the flip-flop 78 is in a set condition during a period from the generation of the third reference clock pulse (output c) upto coincidence of the counted values in the counter 75 with the constant already set in the switch circuit 77; during this set condition, the flip-flop produces as an output its input J (which is a high level signal) from its output terminal Q with a timing corresponding to the second reference clock pulse (output b), whereby the analog switch 79 is rendered on-and-off with this output Q with a timing corresponding to the second reference clock pulse. Accordingly, while the flip-flop 78 is in the set condition, an output from the sample and hold circuit 17 is applied to the peak hold circuit 40 with a timing corresponding to the sampling operation at this sample and hold circuit 17, whereby the slice level is determined by the operational circuit 43 on the basis of the hold value in the peak hold circuit 40, i.e., the peak value of the output from the sample and hold circuit 17, through the process as already discussed in connection with Figure 5.

Accordingly, whenever the constant $\alpha+N$ is set by the switch circuit 77, the flip-flop 78 is kept at its set condition during a period of from generation of the third reference clock pulse (output c) up to the termination of the output of all of image element signals the first sensor region 69a in the sensor array 69. Accordingly, only the outputs from the first sensor region 69a of the sensor 69 are supplied to the peak hold circuit 40. As the result, the slice level is set on the basis of the peak values in the outputs from the first sensor region 69a of the sensor array 69.

The abovementioned control circuit 25' has a construction as shown in Figure 13, for example. The illustrated circuit construction, besides the construction shown in Figure 6, is further added with a third constant setting switch circuit 81 which alters the constant set by the second switch circuit 54 from $\alpha+N-1$ to $\alpha+2n-1$, and further has another constant $\alpha+2N$ set therein; a third comparator 80 which compares the counted value of the counter 48 with the value set in this third switch circuit 81 to produce a coincided signal output when the counted value has become coincided with the set value; and a third J—K type flip-flop 82 of the same construction and same circuit-connection as those of the first and second flip-flops 51 and 55, which receives the coincided signal from the third comparator 80 in its clock input terminal CK through an inverter 83.

According to such construction, there can be obtained from the output terminal Q of the second flip-flop 55 a signal which maintains the low level during a period from generation of the third reference clock pulse (output c) from the pulse generating circuit 16 upto the termination of generation of the $\alpha+2N-1$st pulse in the second reference clock pulse (output b), and, thereafter, maintains the high level until the third reference clock pulse (output c) is again generated, i.e., an output f' to be

applied to the abovementioned coincidence detecting circuit 27; also, there can be obtained from the output terminal Q of the third flip-flop 82 a signal which maintains the low level during a period from generation of the third reference clock pulse (output c) upto termination of generation of the α+2Nth pulse in the second reference clock pulse (output b), and, thereafter, maintains the high level until the third reference clock pulse (output c) is again generated, i.e., an output e' to be applied to the abovementioned "AND" gate 29. Incidentally, there is no change at all as to the output *d* from that shown in Figure 6.

In the above-described embodiment, the serial-in-parallel-out type shift register has been used as the means for storing the quantized image element signal trains from each sensor array or each sensor region. In the following, explanations will be given in reference to Figure 14 as to a case wherein a serial-in-serial-out recirculation type shift register is used as the recording means.

The circuit construction shown in Figure 14 may be applied either to the embodiment shown in Figures 1 and 2 or to the embodiment shown in Figures 10 and 11. First of all the case wherein this type of shift register is applied to the embodiment shown in Figures 1 and 2 will be explained.

In the drawing which shows only the principal portions which differ from the construction in Figure 2, reference numerals 84 and 85 designate serial-in-serial-out recirculation type shift registers of an N-bit construction to store therein the quantized image element signal trains from the respective comparator 20 and 21, each output line of which is fed back to each input line.

A reference numeral 86 designates an exclusive "NOR" gate which produces a high level output signal when the stored values between the mutually corresponding bits in registers 84 and 85 are coincident, and produces a low level output signal when they are different.

A reference numeral 87 designates a counter which counts the number of the high level signals from the exclusive "NOR" gate 86, and which is so constructed that it may be cleared of its counted values by application of the second reference clock pulse (output b as shown in Figure 3B and Figure 16B) from the pulse generating circuit 16 through an inverter 90.

A numeral 88 refers to a magnitude comparator which determines the relative magnitude of the count values C of the counter 87 and the stored value R in a register 89 coupled to store therein the count values of the counter 87. This comparator produces a high level output signal when the count value C is larger than the recorded value R(C>R).

The abovementioned register 89 is so constructed that it may store therein, in response to the high level output signal from the magnitude comparator 88, the counted values before the counter 87 is cleared of its contents i.e., the count values associated with the stored contents of the shift register 85, these contents being shifted relative to the contents of the register 84 by one bit for each output of an image element signal from the sensor array 14 commencing with the 14_{N+1}th bit.

A reference numeral 25" designates a control circuit corresponding to the control circuit 25 shown in Figure 2, which is so constructed that it may receive thereinto the first, second and third reference clock pulses (outputs a, b, and c) shown in Figures 3A, 3B and 3C and Figures 16A, 16B and 16C, from the pulse generating circuit 16 as the inputs, based on which the mode change and drive control of the shift registers 84 and 85 as well as the feed control of the second reference clock pulse (output b) to the counter 28 may be effected.

Although the details of this circuit construction will be explained later, it is constructed generally as follows. That is, the shift register 84 is supplied with a mode control signal (output g shown in Figure 16F) for setting the shift register 84 in a "WRITE MODE" (a mode for recording the outputs from the quantizing comparator 20 during a period from generation of the third reference clock pulse (output c) from the pulse generating circuit 16 upto generation of the α+Nth pulse of the second reference clock pulse (output b), and for setting the same in a "RECIRCULATION MODE" (a mode for recirculating the recorded contents through the feed back line) during the other period than the abovementioned; and driving pulses (output h shown in Figure 16J) which cause the shift register 84 to take therein the outputs from the abovementioned comparator 20 in synchronism with the second reference clock pulse (output b) when the register is in the state of being set in the "WRITE MODE", and subject the recorded contents to one recirculation during non-generating period of the second reference clock pulse (output b) (more accurately, during a period of from trailing of the second reference clock pulse to its rising once again) when the shift register 84 is in the state of being set in the "RECIRCULATION MODE". On the other hand, to the shift register 85 there are applied a mode control signal (output i shown in Figure 16G) for setting the shift register 85 in the "WRITE MODE" during a period of from generation of the abovementioned third reference

clock pulse (output c) upto generation of the α+Nth pulse of the second reference clock pulse (output b), and, thereafter, during a period of from rising of the second reference clock pulse to its trailing at every generation of the second reference clock pulse (output b), and for setting the same in the "RECIRCULATION MODE" during a period other than the abovementioned; and driving pulses (output j shown in Figure 16K) which cause the shift register 85 to take therein the outputs from the comparator 21 in synchronism with the second reference clock pulse (output b) when the register is in the state of being set in the "WRITE MODE", and subject the recorded contents to one recirculation when the shift register is set in the "RECIRCULATION MODE". By the way, a control signal (output e shown in Figure 16E) is applied to the "AND" gate 29 to control feeding of the reference second clock pulse (output b) to the counter 28, as is the case with the control circuit 25 shown in Figure 2.

The other construction is exactly same as the circuit shown in Figure 2, with the exception that the register 30 is so made as to take thereinto the counted values of the counter 28 during that period in response to the high level signal from the comparator 88. The arrangement of the above-described counter 87, comparator 88, and register 89 is the same as that of counter 63, comparator 65, and register 66, respectively, shown in Figure 9.

In the above-described construction, when the third reference clock pulse (output c) is produced as an output from the pulse generating circuit 16, the control circuit 25", in response to this output, sets the shift registers 84 and 85 in their respective "WRITE MODES" with the outputs *g* and *i* (Figures 16F and 16G), after which it applies to both shift registers the driving pulses (output h and j shown in Figures 16J and 16K) in accordance with the second reference clock pulse (output b). Accordingly, the shift registers 84 and 85 begin to take thereinto the outputs from the comparators 20 and 21 in response to the driving pulses *h* and *j*. When the α+Nth pulse of the second reference clock pulse (output b) is produced from the pulse generating circuit 16, and, accordingly, the shift register 84 completes taking thereinto of the quantized signals of the outputs from the whole sensors 12_1 to 12_N, and the shift register 85 also completes taking thereinto of the quantized signals of the outputs from the initial N numbers of the sensors 14_1 to 14_N in the sensor array 14, the control circuit 25", at this point, sets the respective shift registers 84 and 85 in their "RECIRCULATION MODES" with the outputs *g* and *i*, and applies the N driving pulses (outputs h and j shown in Figures 16J and 16K) during a period until the α+N+1st pulse of the second reference clock pulse (output b) will be generated. Accordingly, the shift registers 84 and 85 subject the stored contents therein, i.e., the quantized signals of the outputs from the sensors 12_1 to 12_N and the quantized signals of the outputs from the sensors 14_1 to 14_N, to one recirculation. At the time of recirculation of the stored values in these shift registers 84 and 85, the exclusive "NOR" gate 86 detects coincidence and non-coincidence of the recorded values between the mutually corresponding bits. If the recorded values are coincident, i.e., both recorded values are either "1" or "0", a high level signal or match signal output is produced, and the match signal from the exclusive "NOR" gate 86 at this time is counted by the counter 87. Incidentally, the control circuit 25", at this point, causes the "AND" gate 29 to begin feeding of the second reference clock pulse (output b) to the counter 28 with the output *e* (Figure 16E). Accordingly, as in the case of the embodiment shown in Figure 2, the counter 28 begins to count the second reference clock pulse (output b) from its α+N+1st pulse. Then, when the α+N+1st pulse of the second reference clock pulse (output b) is produced from the pulse generating circuit 16, the control circuit 25" sets the shift register 85 in the "WRITE MODES" during the period of from rising of the second reference clock pulse (output b) to its trailing, with the shift register 84 being set in the "RECIRCULATION MODE", as shown in Figures 16F and 16G), and applies the driving pulses (output j) to the shift register 85, as shown in Figure 16K in synchronism with the second reference clock pulses (output b). Accordingly, the shift register 85, while it is causing the stored contents i.e., quantized signals of the outputs from the sensors 14_1 to 14_N, to shift by one bit (at which time the quantized signal of the output from the sensor 14_1 is discarded), begins to take thereinto the output from the comparator 21, i.e., the quantized signal of the output from the sensor 14_{N+1}, whereby the stored contents become changed from "the quantized signals of the outputs from the sensors 14_1 to 14_N" to "the quantized signals of the outputs from the sensor 14_2 to 14_N.". During this period, the control circuit 25" does not apply the driving pulse to the shift register 84, as shown in Figure 16J, and hence the shift register 84 is in stoppage with the quantized signals of the outputs from the sensors 12_1 to 12_N being maintained therein. When the α+N+1st pulse of the second reference clock pulse (output b) begins to trail, the control circuit

25", sets the shift register 85 in the "RECIRCULATION MODE" by the output *i* as shown in Figure 16G, and applies the N driving pulse (outputs h and j) to both shift registers 84 and 85, respectively, as shown in Figures 16J and 16K), during a period upto generation of the α+N+2nd pulse of the second reference clock pulse (output b) so as to cause the stored contents therein, i.e., the quantized signals of the outputs from the sensors 12_1 to 12_N and the quantized signals of the outputs from the sensors 14_2 to 14_{N+1}, to perform one recirculation. At this recirculation of the stored contents, the matched numbers in the stored contents of both shift registers 84 and 85 are counted by the counter 87 through the exclusive "NOR" gate 86, as mentioned in the foregoing. The same operations will be repeated thereafter until the Kth pulse of the second reference clock pulse (output b) will be produced from the pulse generating circuit. On the other hand, processing of the counted values of the counter 87 and the counted values of the counter 28 as well during this period can be performed in the same manner as mentioned in connection with Figure 9. Therefore, the recorded values in the register 30 at the instant when the shift register 85 has stored the quantized signals of the outputs from the sensors 14_{M-N-1} to 14_M and subjected the same to one recirculation amount to the maximum count value of the counter 28, i.e., relative shift numbers of the shift register 85 which have been spent during a period of from commencement of the relative shifting of the recorded contents as to attainment of optimum matching of the contents of the registers. After all, as already stated in connection with Figure 2, when the recorded values of the register 30 are latched by the latching circuit 31 by the third reference clock pulse (output c) generated from the pulse generating circuit 16, at the start of the subsequent scanning of the object images, the output from the latching circuit 31 represents the object distance.

As stated in the foregoing, the detection of the object distance with the circuit construction shown in Figure 14 is carried out by the use of the serial-in-serial-out recirculation type shift registers 84 and 85.

In the following, one example of the control circuit 25" will be explained in detail in reference to Figures 15 and 16A to 16K.

In Figure 15, a numeral 91 refers to a counter to count the second reference clock pulse (output b) shown in Figure 16(b) from the pulse generating circuit 16 through an "and" gate 96; 92 designates a comparator which compares the counted values by the counter 91 with a constant α+N set by a constant setting switch circuit 93 and produces a coincided signal output (Figure 16D) when the counted values have become coincided with the constant α+N; and 94 refers to a J—K type flip-flop which receives the coincided signal output from the comparator 92 in its clock input terminal CK through an inverter 101. The counter 91, the comparator 92, the switch circuit 93, and the flip-flop 94 exactly correspond to the first counter 48, the first comparator 49, the first switch circuit 50, and the first flip-flop 51, respectively, as shown in Figure 6 or 13. The flip-flop 94 is so constructed that the input terminal J may be applied with a voltage Vcc, the input terminal K thereof may be connected to the earth, and the clear terminal CLR thereof may receive, along with the counter 97, the third reference clock pulse (output c shown in Figure 16C) from the pulse generating circuit 16 as the clear signal. The "AND" gate 96 is arranged so as to receive the output $\bar{Q}$ (Figure 16F) of the flip-flop 94, and the output thereof is as shown in Figure 16H. A reference numeral 95 designates an "OR" gate which receives therein the output $\bar{Q}$ of the flip-flop 94 and the second reference clock pulse (output b), the output from this gate being as shown in Figure 16G. A numeral 97 refers to an "AND" gate which receives the first reference clock pulse (output a shown in Figure 16A) from the pulse generating circuit 16, the second reference clock pulse (output b) inverted by an inverter 98, and the output Q of the flip-flop 94. By taking "AND" of these three input signals, the gate permits the first reference clock pulse (output a) to pass therethrough, only when the output Q of the flip-flop 94 is at the high level, and the second reference clock pulse (output b) is at the low level (hence the output of the inverter 98 is at the high level), as shown in Figure 16I. Incidentally, as shown in Figures 16A and 16B, the frequency of the first reference clock pulse (output a), and the sustaining time and number β of the second reference clock pulse (output b) are so set in this gate that the β pulses out of the N+β first reference clock pulse (output a) may be covered by the second reference clock pulses (output b). In other words, when the "AND" is taken between the first reference clock pulse (output a) and the second reference clock pulse (output b) inverted by the inverter, the N first reference clock pulses (output a) can be obtained within a period when the second reference clock pulse is at the low level. A reference numeral 99 designates an "OR" gate which receives an output from the "AND" gate 96 and an output from the "AND" gate 97, these outputs being as shown in Figure 16J. A numeral 100 refers to an "OR" gate which receives the output

from the "OR" gate 97 and the second reference clock pulse (output b), the outputs from this gate 100 being as shown in Figure 16K.

According to such construction, the output Q of the flip-flop 94 (Figure 16E) can be utilized as the output *e* for controlling the "AND" gate 29, as is the case with the control circuit 25 in Figure 6. On the other hand, the output $\bar{Q}$, complementary to the output Q, as shown in Figure 16 (f), maintains the high level during a period of from generation of the third reference clock pulse (output c) from the pulse generating circuit 16 upto generation of the α+Nth pulse of the second reference clock pulse (output b), and maintains the low level during a period, thereafter, until the third reference clock pulse (output c) is again generated. Accordingly, if the shift registers 84 and 85 are of a type which assumes the "WRITE MODE" when the mode control signal to be imparted to the mode control terminal of the registers is at the high level, and which assumes the "RECIRCULATION MODE" when the mode control signal is at the low level, this output $\bar{Q}$ can be utilized as the output *g* for controlling the mode of the shift register 84. Also, the output from the "OR" gate 95 is a further addition of the second reference clock pulse (output b) to the output $\bar{Q}$ of the flip-flop 94, as shown in Figure 16G, so that the output therefrom can be utilized as the output *i* for controlling the mode of the shift register 85. Further, as shown in Figure 16J, since the second reference clock pulse output (output b) is produced from the "OR" gate 99 during a period of from generation of the third reference clock pulse (output c) from the pulse generating circuit 16 upto generation of the α+Nth pulse of the second reference clock pulse (output b), and the first reference clock pulse (output a) is produced from the "OR" gate 99, only while the second reference clock pulse (output b) is at the low level, during a period, thereafter, until the third reference clock pulse (output c) will again be generated, the output from this "OR" gate 99 can be utilized as the output *h* for driving the shift register 84. Moreover, since the second reference clock pulse output (output b) is produced from the "OR" gate 100 throughout the whole period, as shown in Figure 16K, and the first reference clock pulse (output a) is produced therefrom, while the second reference clock pulse (output b) is at the low level, during a period of from generation of the α+Nth pulse of the second reference clock pulse (output b) upto generation of the third reference clock pulse (output c), the output from this "OR" gate 100 can be utilized as the output *j* for driving the shift register 85.

The circuit construction shown in Figure 14 may also be applied to the embodiments shown in Figures 10 and 11. In such a case, the mode of operations should be such that, as is apparent from the explanations in connection with Figures 11 and 10, the first sensor region of the sensor array 69, i.e., the quantized signals of the outputs from the sensors 69_1 to 69_N, are first taken into the shift register 84, then the quantized signals of the outputs from the initial N sensors in the second sensor region 69b are taken into shift register 85, and, at the termination of the signal taking operations, the stored contents in both shift registers 84 and 85 are subjected to one recirculation with a mutually same timing, before the quantized signal of the output from the subsequent sensor 69_{2N+1} is produced from the comparator 20, to thereby count the matched numbers between the stored contents in both shift registers by the counter 87_1 through the exclusive "NOR" gate 86, and, after termination of this one recirculation, the quantized signal of the output from the sensor 69_{2N+1} is taken into the shift register 85, as described above, and, at the termination of this signal taking operation, the stored contents of each of the shift registers 84 and 85 are subjected once again to one recirculation to count the matched numbers. Accordingly, the control circuit 25" should be such that the shift register 84 is set in the "WRITE MODE" during a period of from generation of the third reference clock pulse (output c) from the pulse generating circuit 16 upto generation of the α+Nth pulse of the second reference clock pulse (output b), is set in the "RECIRCULATION MODE" during a period, thereafter, until the third reference clock pulse (output c) is again generated, and, in the state of the "WRITE MODE", it applies the first to α+Nth pulses of the second reference clock pulse (output b) for taking thereinto of the quantized signals of the outputs of the sensors 69_1 to 69_N produced from the comparator 20, and, in the state of the "RECIRCULATION MODE", it does not apply any driving pulse until the α+2Nth pulse of the second reference clock pulse (output b) is generated, and, after termination of this α+2Nth pulse, and only while the second reference clock pulse (output b) is at the low level, it applies the N pulses of the first reference clock pulse (output a) for the recirculation of the recorded contents therein. On the other hand, the shift register 85 should be set in the "WRITE MODE" every time the second reference clock pulse (output b) is generated during a period of from termination of the α+Nth pulse of the second reference clock pulse (output b)

upto generation of the α+2Nth pulse, and during a period, thereafter, until the third reference clock pulse (output c) will again be generated is set in the "RECIRCULATION MODE" during, a period other than the abovementioned, and, in the state of its being set in the "WRITE MODE", it applies the second reference clock pulse (output b) for taking thereinto the two-value signals of the outputs of the sensors 69_{N+1} to 69_1 produced from the comparator 20, and, in the state of its being set in the "RECIRCULATION MODE", it applies N pulses of the first reference clock pulse (output a) for the recirculation of the stored contents therein, only while the second reference clock pulse (out b) is at the low level during the remaining period except for the period of from generation of the third reference clock pulse (output c) to generation of the α+Nth pulse of the second reference clock pulse (output b) this period corresponds to a period, in which the shift register 84 is set in the "WRITE MODE". the physical circuit construction of the control circuit 25'' is, for example, as shown in Figure 17.

The construction shown in Figure 17 is a modification of the circuit construction shown in Figure 15 in accordance with the contents as explained in the foregoing. In the illustration, those component elements designated by the same reference symbols as in Figure 15 correspond to those elements in Figure 15. A reference numeral 102 designates a second comparator which compares the counted values of the counter 91 with a constant α+2N set in a second constant setting switch circuit 103, and produces a coincided signal output (Figure 18G) when this counted values become coincided with the constant α+2N. A numeral 104 refers to a second J—K type flip-flop which receives therein the coincided signal from the comparator 102 through an inverter 105, which is of the same circuit connection as that of the abovementioned flip-flop 94. Incidentally, the second comparator 102, the second switch circuit 103, and the second flip-flop 104 exactly correspond to the third comparator 80, the third switch circuit 81, and the third flip-flop 82, respectively, shown in Figure 13. 106 refers to an "AND" gate which receives the output Q (Figure 18E) of the flip-flop 94 and the output $\bar{Q}$ of the flip-flop 104, the output of this gate 106 being as shown in Figure 18J. 107 designates an "AND" gate which receives the output Q of the flip-flop 104 and the second reference clock pulse (output b) shown in Figure 18B to be generated at the pulse generating circuit 16, the output of this gate 107 being as shown in Figure 18K. By the way, the abovementioned "OR" gate 95 is so arranged in this embodiment that the outputs from these "AND" gates 106 and 107, may be received thereby, hence the output from this gate 95 is as shown in Figure 18L. A numeral 108 refers to and "AND" gate which receives the output Q of the flip-flop 94 and the second reference clock pulse (output b), the output of this gate 108 being as shown in Figure 18P. Incidentally, the "AND" gate 97 is so made here as to receive the output Q of the flip-flop 104, the output of this gate 97 being as shown in Figure 18N, hence the output from the "OR" gate 99 is as shown in Figure 18O. Also, the abovementioned "OR" gate 100 is arranged to receive the output from the "AND" gate 97 and the output from the "AND" gate 108, hence the output of this gate 100 is as shown in Figure 18Q.

As will be clearly understood from comparison of the signal waveforms shown in Figures 18F, 18L, 18O and 18Q with the foregoing explanations, the output $\bar{Q}$ of the flip-flop 94 can be used as the output *g* for controlling the mode of the shift register 84, the output of the "OR" gate 99 can be used as the output *h* for driving the shift register 84, the output of the "OR" gate 95 can be used as the output *i* for controlling the mode of the shift register 85, and the output of the "OR" gate 100 can be used as the output j for driving the shift register 85, respectively. Also, for the output *e* for controlling the counter 29, the output Q of the flip-flop 104 can be used as is the case with the construction shown in Figure 13.

The embodiments of the present invention described so far are so constructed that two images of an object formed by a range finding optical system are electrically scanned by the use of one or more photo-sensor arrays, then the analog data concerning these two images at this time are quantized into digital data signals, thereafter, these data signals are relatively shifted in the shift registers, and the relative shifting occurring until both stored sets of data signals become optimumly mutually coincided is used to determine the object distance or range.

Where a photo-sensor array or arrays are used, the following should be taken into consideration from the standpoint of the characteristics of the photo-sensors constituting the array. That is, of the abovementioned photo-sensor arrays, CCD or BBD, for example, consist of the charge accumulation type photosensors; this charge accumulation type photo-sensor, when subjected to light irradiation in a state of an electrically void layer being formed by application of a voltage to the electrode, accumulates electrical charge proportional to the incident light quantity (light intensity × time) at a rate in accordance with intensity

of the incident light. Generally, this accumulated charge is obtained as the image element signal during a period from discharge of the accumulated charge until the charge is again discharged at the subsequent scanning operation having been accumulated during that period in accordance with the integrated quantity of the light projected into the sensor (hence the abovementioned period is recognized as the charge accumulation time of each photo-sensor). At this time, however, the charge quantity which the photosensor can accumulate, i.e. the saturation level of the accumulated charge, is fixed previously, so that, when this saturation level is exceeded, excess charge will flow out thereafter, and this outflow charge would intrude into the void layer in another photo-sensor. This is the phenomenon known as the so-called "blooming phenomenon". When such phenomenon occurs, satisfactory image element signals can no larger be obtained.

Together with this, when the accumulated charge quantity in the photo-sensor is very small, an S/N ratio to dark current, etc., becomes extremely low, hence adequate image element signal cannot be obtained.

On the other hand, in the case of a self-scanning type photo-diode array, if it is used in the charge accumulation mode, the photo-diode constituting the array, when light is irradiated thereonto in a state of its having been charged until it is saturated in the capacitor of the pn junction, decreases its accumulated charge due to the charge proportional to the incident light quantity being discharged at a rate in accordance with intensity of the incident light (hence, in this case, the photo-diode functions as the charge accumulation and discharge type photo-sensor). In general, the charge is discharged in accordance with the integrated quantity of the incident light during a time period after the photosensor is charged to its saturation level until it is charged again to its saturaton level at the time of the subsequent scanning, so that, at the time of the re-charging, the flowing charge current may be obtained as the image element signal in a manner to fill up the portion of the charge decreased by the previous discharge (hence, the abovementioned time is recognised as the charge discharging time of each photo-diode). At this time, the capacity of each photo-diode is previously fixed, so that, if, for example, the integrated quantity of the incident light into the photo-diode exceeds the level of the integrated light quantity to be determined in correspondence to the photo-diode capacity, there only takes place discharge of the entire charge from this photo-diode which has been accumulated to the saturation level of this capacity, and no further discharge will occur. Therefore, the current to flow in the subsequent charging corresponds to the capacity of this photo-diode, and it does not correspond to the integrated quantity of the incident light into the photo-diode. As the result, the image element signal becomes unsatisfactory.

Further, when the discharge from the photo-diode is very small, the current flowing at the time of the charging becomes very weak with the result that the S/N ratio to the dark current, etc., becomes very low. Accordingly no adequate image element signal can be obtained.

Accordingly, when the photo-sensor array consisting of the charge accumulation type or charge accumulation and discharge type photo-sensors is used for the range detecting device, it is not possible to obtain highly precise range detection using such photo-sensor array, unless the light receiving quantity (light receiving time) of the photo-sensor is properly adjusted in accordance with brightness of the object so that the S/N ratio may become high, i.e., adequate image element signal may constantly be obtained, without accumulation or discharge of the charge in or from the photo-sensor arriving at the limited level.

From the above view point, one physical embodiment of the pulse generating circuit 16 which is so made as to be able to automatically adjust light receiving time of the photo-sensor arrays 12 and 14 or 69 in accordance with brightness of the object will be explained in reference to Figures 19 and 20.

In Figure 19, the pulse generating circuit in its entirety is designated by a reference numeral 16'. In this pulse generating circuit 16', the same circuit elements as those shown in Figure 4 will be designated by the same reference numerals. In the drawing, a numeral 121 deisgnates a reference voltage setting circuit, in which a voltage $V_{ref.1}$ slightly lower than the saturation level of each photo-sensor in the photo-sensor array 12 or 69 is established. 122 refers to a comparator which compares an output from the sample and hold circuit 17 with the reference voltage $V_{ref.1}$ set in the reference voltage setting circuit 121. This comparator is so set that, when the output from the sample and hold circuit 17 exceeds this reference voltage $V_{ref.1}$ (vide Figure 20F), it may produce a high level signal (figure 20G). 123 refers to an RS type flip-flop which produces a high level signal output (Figure 20H) from its output terminal Q by being set in response to the high level signal from the comparator 122. 123a designates

its reset terminal. A numeral 124 designates a D type flip-flop which produces a high level signal output (Figure 20I) from its output terminal Q in synchronism with a carry signal output from the counter 38, after receiving the high level signal input from the flip-flop 123.

A numeral 35' refers to an oscillating circuit corresponding to the oscillator 35 in Figure 4. In this embodiment, the oscillating circuit consists of an oscillator 125 which generates a reference clock pulse of a predetermined frequency F_1, a counter 126, or a frequency dividing circuit which divides the clock pulse from the oscillator 125 into a frequency F_2 lower than this clock pulse frequency, and "AND" gate 127 which produces the reference clock pulse output from the oscillator 125 when the output Q from the flip-flop 124 it receives assumes "high" level, and "AND" gate 128 which receives the output from the flip-flop 124, in the same manner as the gate 127, through an inverter 129, and produces the reference clock pulse output from the counter 126 when the output from the inverter 129 is at the high level, i.e., the output Q from the flip-flop 124 is at the low level, and an "OR" gate 130 which produces the outputs of these "AND" gates 127 and 128 as the first reference clock pulse (output a).

In the above-described construction, if no output from the photo-sensors in the photo-sensor arrays 12 or 69, exceeds the reference voltage $V_{ref.1}$ set in the reference voltage setting circuit 121 upon image scanning, the output of the comparator 122 is at the low level, hence the outputs Q of the flip-flops 123 and 124 are either at the low level. Accordingly in the oscillation circuit 35' the "AND" gate 128 is in the "on" state due to the "high" level output from the inverter 129 to produce, as the output *a*, the output from the counter 126 i.e., the first reference clock pulse of the frequency F_2, whereby the frequency f2 of the second reference clock pulse output (output b) from the counter 36 can be represented as $f_2=F_2/N+\beta$. As the result, there are applied to the driver 15 both the second reference clock pulse (output b) of the frequency f_2 and the third reference clock pulse output (output c) which is generated at every Kth number of the second reference clock pulse (output b) of the frequency f_2, so that the scanning operation is conducted at a relatively slow speed (accordingly, the charge accumulating time of each photo-sensor in the sensor array 12, 14 or 69 is prolonged due to the start pulse generating cycle period being long).

In contrast to this, as shown in Figure 20F, when the output from the sample and hold circuit 17 exceeds the reference voltage $V_{ref.1}$ in the course of image scanning, the output of the comparator 122 assumes a "high" level as shown in Figure 20G, in response to which the output Q of the flip-flop 123 assumes the high level, as shown in Figure 20H. On the other hand, the output Q of the flip-flop 124 which receives the high output from this flip-flop 123 assumes the high level in response to the carry signal output produced from the counter 38 at the start of the subsequent scanning, as shown in Figure 20I. Consequently, the output of the inverter 129 assumes the low level, on account of which the "AND" gate 128 becomes off and the "AND" gate 127 becomes on instead, whereby the output from the oscillator 125, i.e., the first reference clock pulse of the frequency F_1 is produced as the output *a*. Therefore, the second reference clock pulse output (output b) of the frequency f_1 ($f_1=F_1/N+\beta$) is produced from the counter 36, as shown in Figure 20A. Thus, both the second reference clock pulse (output b) of the frequency f_1 and the third reference clock pulse (output c) generating at every Kth number of the second reference clock pulse (output b) of the frequency f_1 are applied to the driver 15, whereby the scanning cycle period of the sensor array 12, 14, or 69 becomes short, and the charge accumulation time of the photo-sensor becomes curtailed. The ratio of the curtailment of the charge accumulation time at this time corresponds to the ratio of the frequency changes in the first reference clock pulse (output a) so that if $F_1=2F_2$, the ratio becomes 1/2, if $F_1=4F_2$, it is 1/4, and so on.

Thus, according to the pulse generating circuit 16' shown in Figure 19, when the object is particularly bright, the frequency of the second reference clock pulse (output b) to be applied to the driver 15 becomes higher, on account of which the pulse generating time interval of the third reference clock pulse (output c) becomes shorter, hence the scanning cycle period, i.e., the charge accumulation time of the photo-sensors in the photo-sensor array 12, 14, or 69 becomes shortened and the accumulated charge in the photo-sensors can be prevented in advance from reaching the saturation level.

In the embodiment of the pulse generating circuit shown in Figure 19, the adopted construction is such that the oscillation circuit 35' is composed of the oscillator 125 which generates the reference clock pulse of the frequency F_1 and the counter 126 which frequency-divides the reference clock pulse of the frequency F_1 to generate the reference clock pulse of the frequency F_2 so as to be able to utilize either

output from the oscillator 125 or the counter 126 depending on whether the output Q of the flip-flop 124 is at a "high" level or a "low" level. In particular, for this oscillation circuit 35', a V—F converter (Voltage-Frequency converter) which is known to produce a clock signal output of a frequency corresponding to the input voltage may be utilized. In this case, a first voltage generating circuit to generate a voltage V_1 suited for the abovementioned frequency F_1 and a second voltage generating circuit to generate a voltage V_2 suited for the frequency F_2 are connected to the input terminal of the V—F converter so that either output voltage from these first and second voltage generating circuits may be selected for application to the V—F converter in accordance with the level of the output Q of the flip-flop 124, i.e., "high" or "low" level. Also, the embodiment of the pulse generating circuit shown in Figure 19 is so constructed that the frequency of the second reference clock pulse (output b) and the pulse generating time interval of the third reference clock pulse (output c) may be varied by changing the frequency of the first reference clock pulse (output a) to thereby adjust the light receiving time of the sensor array 12, 14, or 69. Besides this, the adjustment of the light receiving time in the photo-sensor array 12, 14, 69 is possible even by varying the pulse generating time interval of the third reference clock pulse (output c) alone without changing whatsoever the frequency of the first and second reference clock pulse (outputs a and b). In other words, this is done by automatically changing the set value in the counted value setting switch circuit 39 for the counter 38 shown in Figure 19. For example, if the circuit is so constructed that some of the switches in the switch circuit 39 are removed, and instead the set value input terminals at the side of the counter 38 corresponding to these removed switches are connected to the Q output terminal of the flip-flop 124, so that the set counted value for the counter 38 may be K when the output Q of the flip-flop 124 is at the "low" level, and the set counted value may be K' (where:

$$K > K' \geqq \alpha + M$$

or

$$K > K' \geqq \alpha + L,$$

when the output Q is at the "high" level, the set counted value for the counter 38 assumes K or K' in accordance with the level of the output Q of the flip-flop 124, i.e., "low" or "high" level, on account of which the pulse generating time interval of the third reference clock pulse (output c) alone changes, while the frequency of the first and second reference clock pulse (outputs a and b) remains unchanged. As a result, the light receiving time of the sensor array 12, 14 or 69 becomes automatically adjusted.

For change-over of the frequency of the first reference clock pulse (output a) from the oscillation circuit 35' in the pulse generating circuit 16' shown in Figure 19 from F_1 back to the original F_2, a "high" level signal may be applied to the reset terminal 123a of the flip-flop 123. This change-over operation can can be done conveniently by being interlocked with, for example, shutter charging operation, etc., in case the range detecting device in question is applied to a focus detecting device or an automatic focus adjusting device for incorporation into a photographic camera. Or, there is another way, in which the frequency is automatically changed over to the original frequency F_2 in accordance with brightness of the object for the range detection, when it becomes dark. This will be explained in the following in reference to Figures 21 and 22.

In Figure 21, the automatic reset circuit in its entirety is designated by a reference numeral 131. 132 refers to a peak hold circuit which functions to sequentially hold peak values of the outputs from the sample and hold circuit 17 (Figure 22F). 133 designates a switch for clearing the peak values held by the peak hold circuit 132 (Figure 22G). This switch functions to clear the values held in the peak hold circuit 132 by being turned on in response to a control signal output from a shift register 134 after lapse of a certain delay time τ_1 (when the frequency of the second reference clock pulse is f_1) or τ_2 (when the frequency of the second reference clock pulse is f_2) from the generation of the third reference clock pulse (output c) shown in Figure 22B from the pulse generating circuit 16'. 135 refers to a sample and hold circuit for sampling and holding the output from the peak hold circuit 132, which is set as to take thereinto the output from the peak hold circuit 132 in response to the third reference clock pulse (output c) from the pulse generating circuit 16' and to hold this until the third reference clock pulse (output c) is again applied. 136 designates a reference voltage setting circuit, in which there is set a voltage $V_{ref.2}$ for determining the level to reinstate the pulse generating circuit 16' to the original state, i.e. to reset the frequency of the first reference clock pulse (output a) from the oscillation circuit 35' to the original state, i.e., from frequency F_1 to F_2. 137 designates

a comparator which compares the output from the sample and hold circuit 135 (Figure 22 (h)) with the reference voltage $V_{ref.2}$ set in the reference voltage setting circuit 136. The comparator is so set that it may produce a high level signal output, i.e., the reset signal output (Figure 22 (i)) to the reset terminal 123a of the flip-flop 123 in the pulse generating circuit 16', when the output of the sample and hold circuit 135 becomes lower than the reference voltage $V_{ref.2}$.

In this construction, when the hold value of the peak hold circuit 132 (Figure 22 (g)) is higher than the reference voltage $V_{ref.2}$ in the state of the frequency of the first reference clock pulse generated from the oscillation circuit 35' in the pulse generating circuit 16' being F_1, the output of the sample and hold circuit at this time (Figure 22H) is naturally higher than this reference voltage $V_{ref.2}$, even when the sample and hold circuit 135 takes thereinto the output of the peak hold circuit 132 at the start of the subsequent scanning operation and forwards it to the comparator 137 as the output. Accordingly the output of the comparator 137 (Figure 22I) assumes the "low" level and the pulse generating circuit 16' is not reset. In contrast to this, when the value held in the peak hold circuit 132 becomes lower than the reference voltage $V_{ref.2}$, as shown in Figure 22G, the sample and hold circuit 135 takes thereinto the output of the peak hold circuit 132 at the start of the subsequent scanning, as shown in Figure 22H, and produces it as the output therefrom, whereupon the output of the comparator 137 assumes the "high" level (i.e., the reset signal is generated), as shown in Figure 22I. Thus, as shown in Figure 22J, the flip-flop 123 is immediately reset in the pulse generating circuit 16', and the output Q thereof assumes the "low" level. The flip-flop 124 which receives this low level signal also assumes the low level in its output Q in response to the third reference clock pulse (output c) to be imparted thereto at the subsequent scanning operation, as shown in Figure 22K, whereby the "AND" gate 127 in the oscillation circuit 35' of the pulse generating circuit 16' is turned off, and, at the same time, the "AND" gate 128 is turned on to change-over the frequency of the first reference clock pulse (output a) from F_1 to F_2. As the result, the frequency of the second reference clock pulse (output b) to be imparted to the driver 15 is changed from f_1 to the original frequency f_2, as shown in Figure 22A.

As such, according to the combination of the pulse generating circuit 16' shown in Figure 19 and the automatic reset circuit 131 shown in Figure 21, even when brightness of the object varies during the range detecting operations, there can always be obtained an image scanning signal at an adequate level satisfactorily conforming to variations in the object brightness, so that it can be employed as the range detecting device with extreme advantage.

The range detecting method and device as has so far been explained in the foregoing can be applied to the automatic focus adjusting system in the optical apparatuses and appliances such as photographic camera, etc., and a detailed description will now be given as to this practical application of the method and apparatus.

Figure 23 shows schematically the principal part of a mechanism for servo-controlling a photographic lens in a camera utilizing of an object distance signal output from the D/A converter 33 in the above-described device shown in Figure 2.

In the drawing, 138 designates a photographic lens to be focussed to the object for the range detection; 139 refers to a drive motor for adjusting the photographic lens 138 along its optical axis, which drive motor is linked with a rack plate 141 fixed to the photographic lens 138 through a worm 140 fixedly provided on its output shaft 139a; 142 denotes a potentiometer mechanically linked with the abovementioned photographic lens 138 and is connected to one of the input terminal of a differential amplifier 143. Incidentally, the other input terminal of the differential amplifier 143 is connected to the output terminal 33a of the D/A converter 33 shown in Figure 2. 144 refers to a motor control circuit to control the abovementioned motor 139 based on the output from the amplifier 143; 145 denotes a power source; and a symbol F designates a film surface.

In the above-described construction, when the range detecting device shown in Figure 2 or 11 completes the range detection upto an object, and the output from the D/A converter 33 is applied to the differential amplifier 143 through the output terminal 33a thereof, the differential amplifier 143 assumes an output in accordance with a difference between a signal corresponding to the distance to the object from the D/A converter 33 and a signal from the potentiometer corresponding to the adjusting position of the photographic lens 138, whereby the motor control circuit 144 determines the rotational direction of the motor 139 in accordance with polarity of the output from the amplifier 143, and starts adjustment of the photographic lens 138 by the motor 139. In the course of adjustment of the photographic lens 138, when a signal from the potentiometer 142 becomes coincided with a signal from the D/A converter 33, the

output from the differential amplifier 143 becomes zero, and the motor control circuit 144 stops the motor 139. Accordingly, the photographic lens 138, at this time, is accurately focussed to the object, and the clearest image of the object can be formed on the film surface F.

Figure 24 shows one concrete example of the automatic focus adjusting system, particularly for a photographic camera, wherein the photographic lens is arranged to be automatically adjusted at a position according to the position of the deflectable indicator needle 34a of the meter 34. This needle constitutes the means providing the data output in the device described above as to object range.

In the drawing, 146 designates a photographic lens which is held in a lens holding barrel 147 which, in turn, is supported in a freely slidable manner within a fixed lens barrel 148. 149 indicates a lens driving ring which is mounted on the outer periphery of the fixed lens barrel 148 in a freely rotatable manner. This driving ring 149 is provided with a helical slot (or a cam slot) 149a for moving along the optical axis OA of the photographic lens 146, a cam piece 149b for indicating the adjusting position of the lens 146, and a gear section 149c, and is energized by a coil spring 150 to rotate in the clockwise direction about the optical OA. The slot 149a is engaged with a follower pin 147a embedded in the outer periphery of the lens holding barrel 147 after it has passed through an axial guide slot (not shown) formed in the fixed lens barrel 148. Accordingly, when the lens driving ring 149 rotates, the lens 146 is driven by the slot 149a together with the lens holding barrel 147 along the optical axis OA through the follower pin 147a. 151 designates a stop lever for stopping the lens driving ring 149 (hence the lens 146) at a position indicated by the indicator needle 34a of the meter 34. The stop lever 151 has a follower 151a which contacts the cam piece 149b of the lens driving ring 149 and a gear section 151b to be engaged with the indicator needle 34a of the meter 34, is axially supported by a shaft 152 in a freely rotatable manner, and is energized by a spring 153 to rotate in the clockwise direction with the shaft 152 as the center of its rotation, i.e., in the direction, in which the follower 151a contacts the cam piece 149b of the lens driving ring 149. 154 designates a U-shaped restricting member to restrict further rotation of the stop lever 151 in the anti-clockwise direction, when the gear section 151b of the stop lever 151 becomes engaged with the indicator needle 34a of the meter 34. This restricting member 154 is disposed as closely as possible to the indicator needle 34a of the meter 34 so that it may permit free swinging of the indicator needle 34*a* and stop rotation of the stop lever 151 at the time when the gear section 151b of the stop lever 151 is engaged with the needle 34a to push it toward the restricting member 154. 155 designates a shutter charging lever for the camera which is linked with a shutter charging mechanism (not shown) and a film winding-up mechanism through a gear 156 mounted on the shaft 15a, and is so energized by a coil spring 157 as to rotate in the clockwise direction, whereby, when an operator removes his hand from the lever after the shutter charging operation, it may automatically return to the illustrated position. 160 denotes a rotational lever for returning the lens to its original position, which lever 160 is linked with the gear 156 through a gear 159 integral with the lever and an intermediate gear 158. The rotational lever is so constructed that, when the shutter charging lever 155 is rotated in the arrow direction in the drawing, it may rotate in the arrow direction as shown in the drawing by the action of the gear train 156, 158 and 159, and, at this time, by rotating a sector gear 161 in the arrowed direction (i.e., clockwise direction) around a supporting shaft 162 through an arm portion 161b of the sector gear 161 meshed with the gear section 149c of the lens driving ring 149 at its gear section 161a, it may rotate the lens driving ring 149 in the anti-clockwise direction to a position shown in the drawing with the optical axis OA as the center of its rotation. Incidentally, by the anti-clockwise rotation of the lens driving ring 149, the spring 150 is charged. 163 refers to an engaging and stopping lever which receives a bent arm 161c at the tail end of the sector gear 161 at an engaging stage 163b thereof when the lens driving ring 149 is rotated by the sector gear 161 to a position shown in the drawing to thereby stop the driving ring 149 through the sector gear 161 at the position shown in the drawing. This engaging and stopping lever 163 is axially supported by a shaft 164 in a freely rotatable manner, and is rotationally biased by a spring 165 in the anti-clockwise direction with the shaft 164 as the center of its rotation, i.e., in the direction to receive the bent arm 161c of the sector gear 161.

The slot 149c in the lens driving ring 149 is so designed that, in a state wherein the driving ring 149 is returned to a position shown in the drawing by the sector gear 161, it may set the photographic lens 146 at a position focussing to infinity, and that, at the time of rotation of the lens driving ring 149 in the clockwise direction with the optical axis OA as the center of its rotation, it may move the lens 146 in the forward direction along the optical axis OA, i.e., to a

position where the lens focusses to a finite distance. 166 refers to a shutter release button for the camera, which is shown in the drawing to the supported by a fixed base plate 167 of the camera so as to be freely slidable up and down and also to be biased upwardly by a coil spring 169 arranged between the base plate 167 and a washer 168 on the button. 170 designates a click spring which becomes engaged with a click groove 166a formed in one part of the shutter release button 166 during the course of pushing the release button 166 downward to thereby click-stop the release button. It should be understood that the spring 169 has sufficient spring power to release the click-stop of the release button 166 by this click spring 170 in the absence of manual force applied downwardly to the button 166. 172 denotes a normally open power source switch, which is connected to a range detecting unit incorporated in the camera, to be described later. The switch is disposed at such a position that, at the time of depression of the release button 166, it may be closed by a switch closing member 171 carried on the shutter release button 166, at the time instant when the click spring 170 is just engaged with the click groove 166a. The abovementioned engagement lever 163 is so constructed that it has the bent portion 163b to be engaged by the tip end part 166b of the release button 166 at the time of further depression of the release button 166 from its position where the click spring 170 becomes engaged with the click groove 166a of the release button 166, that the bent portion 163b thereof is rotated in the clockwise direction against the action of the spring 165 with the shaft 164 as the center of its rotation by being pushed by the tip end part 166b of the release button 166 to release the engagement of the sector gear 161 with the engaging stage 163a, and that it may release the shutter (not shown) by pushing the tail end part 173a of the shutter release lever 173 by the tail end part 163c thereof in the vicinity of the final stage of depression of the release button 166, and rotating the shutter release lever 173 to rotate in the arrow direction shown in the drawing with the supporting shaft 174 as the center of its rotation. 175, 176, and 177 respectively refer to an objective lens, a semi-transparent mirror, and an eye-piece lens, together constituting the view finder optical system of the camera. 178 designates a mask plate provided with four openings 178a to indicate a photo-taking sight within the view finder of the camera and a single opening 178b for regulating the range detecting sight. Though not clearly shown in the drawing, the four openings 178a for indicating the photo-taking sight are covered with, for example, a yellow-colored light transmitting film. 179 denotes a mirror which is obliquely disposed behind the mask plate 178 to deflect light arriving through the four openings 178a for indicating the photo-taking sight of the mask plate 178 toward the semi-transparent mirror. This mirror has an opening 179a corresponding to the opening 178b for regulating the range detecting sight in the mask plate 178.

In such construction as described above, the range detecting device shown in Figure 2, for example, is arranged, in compact form, sealed in a package box 180, which is then incorporated in the camera as the range detecting unit U. In this case, openings are provided at both left and right sides of the box 180 (in the drawing, only the opening 180a at the right side of the box is shown, and the photo-sensor array 12 and 14 shown in Figure 2 are disposed within the box 180 facing the respective left and right openings. 181 and 182 refer to lenses corresponding to the lenses 11 and 13 shown in Figure 1 or 2, respectively. In particular, the lens 181 is disposed behind the mirror 179 in confrontation with the opening 179a thereof so that it may receive light from the object to be photographed coming through the opening 178b for regulating the range detecting sight of the mask plate 178 and the opening 179a of the mirror 179 to form a reference image of the object with the consequence that the sight thereof is restricted in comparison with that of the lens 182 to form a comparative image. 183 designates a mirror which is obliquely disposed behind the lens 181 for reflecting the light forming the reference image formed by the lens 181 in the sensor array 12 disposed in confrontation with the opening 180a at the right side of the box 180. 184 indicates a mirror which is obliquely disposed behind the lens 182 for reflecting the light forming the comparative image of the object formed by the lens 182 in the sensor array 14 disposed in confrontation with the opening (not shown) at the left side of the box 180. 185 designates a light emitting diode for indicating termination of the range detection in the above-mentioned range detecting unit *U*. The light emitting diode 185 is disposed in opposition to a small hole 178c formed in the upper center part of the mask plate 178 so that indicating light may be projected onto the semi-transparent mirror 176 through the mirror 179. For the light emitting diode 185, those emitting red or green light, for example, would be preferable for such light to be sufficiently distinguished from yellow light coming through from the photographic sight indicating opening in the mask plate 178. The control circuit of the light emitting diode 185 for indicating termination of the range detection may for

example, be of a construction as shown in Figure 25. In the drawing, 186 denotes a flip-flop which receives the output of the coincidence detecting circuit 27 in Figure 2, i.e., the coincided signal (Figure 3Q), at its set input terminal *S*, and the third reference clock pulse from the pulse generating circuit 16 shown in Figure 2 (output c shown in Figure 3C) at its reset input terminal through the inverter 187. Tr' designates a transistor, the base of which is connected to the Q output terminal of the flip-flop 186, and the emitter of which is grounded. The light emitting diode 185 is connected to the collector side of the transistor Tr' together with a protective resistor *r*.

According to such circuit construction, the flip-flop 186 is reset at the start of the range detection, and the output Q thereof is at the "low" level, with the result that the transistor Tr' is non-conductive and the light emitting diode 185 is turned off; however, in the course of the range detection, when the coincidence detecting circuit 27 detects coincidence of the contents in the shift registers 23 and 24 and produces a coincided signal output (Figure 3Q), the flip-flop 186 is set and the output Q thereof changes from the "low" level to the "high" level with the result that the transistor Tr' becomes conductive and the light emitting diode 185 is turned on at this time, whereby termination of the range detection is indicated. Thereafter, when the third reference clock pulse (output c shown in Figure 3C) is produced from the pulse generating circuit 16, the flip-flop 186 is reset and the output Q thereof changes from the "high" level to the "low" level, on account of which the transistor Tr' is turned off, and the light emitting diode 185 is extinguished.

In the above-described construction of the photographic camera shown in Figure 24, when the shutter charging lever 155 is manipulated in the arrow direction in the drawing to prepare for the photo-taking operation, the gear 156 rotates in the arrow direction to acutate the shutter charging mechanism and the film winding mechanism (not shown), whereby the shutter charging and the film winding are carried out, and the rotational lever 160 is rotated in the arrow direction in the drawing through the gears 158 and 159, whereby the sector gear 161 is rotated in the arrow direction in the drawing through the arm portion 161b, and the lens driving ring 149 is rotated in the anti-clockwise direction with the optical axis OA as the center of its rotation. Accordingly, when the lens driving ring 149 arrives at a position shown in the drawing the photographic lens 146 is set at a position which focusses to the infinite distance, and the spring 150 is sufficiently charged, the engaging and stopping lever 163 stops the bent arm 161c of the sector gear 161 at the engaging stage 163a by the action of the spring 165, whereby the lens driving ring 149 is stopped at a position shown in the drawing.

By the above-described process, preparation for the photographic operation has been completed. In this state, when the camera is collimated to a photographic object so as to place a desired photographic object appearing in the view finder within the photographic sight defined by the four openings 178a in the mask plate 178, while viewing through the view finder, the lens 181 at this time forms an image of the photographic object mainly at its center part on the sensor array 12 disposed in opposition to the opening 180a at the right side of the box 180, as a reference image, through the mirror 183 by means of light arriving through the opening 178b for regulating the range sight in the mask plate 178 and the opening 179a of the mirror 179, as is understood from the illustrated construction. On the other hand, the lens 182 forms through the mirror 184 an image of the photographic object as a comparative image on the sensor array 14 disposed in confrontation to the opening at the left side surface of the box 180 with a relative positional difference corresponding to the distance to the object from the camera through the mirror 184 with a range wider than the range the lens 181 possesses. In this state, when the shutter release button 166 is first pushed down to a position where the click spring 170 is engaged with the click groove 161a, the switch 172 is closed by the switch closing member 171, and electric power is fed from the power source (not shown) to the range detecting unit *U*, whereby the unit commences the range detecting operation as already explained in connection with the device shown in Figure 2. When the range detection in this range detecting unit *U* is completed, i.e., when the coincidence detection signal output (Figure 3Q) is produced from the coincidence detecting circuit 27 shown in Figure 2, the light emitting diode 185 is turned on as explained in connection with Figure 25, and indication is given within the view finder to the effect that the range detection is completed, and at this time the deflection of the indicator needle 34a of the meter 34 indicates the distance to the photographic object by the output from the D/A converter 33 shown in Figure 2. When the light emitting diode 185 is turned on, the shutter release button 166 is further depressed, and the engaging lever 163 is rotated in the clockwise direction in the drawing with the shaft 164 as the center of

its rotation against action of the spring 165 by means of the tip end part 166b of the shutter release button 166 to release engagement and stoppage of the sector gear 161, whereby the lens driving ring 149 rotates in the clockwise direction by the action of the spring 150 with the optical axis OA as the center of its rotation, and the lens 81 is pushed forward along the optical axis OA by the interengagement of the moving slot 149a and the pin 147a. On the other hand, when the lens driving ring 149 is rotated by the action of the spring 150, the stop lever 151 is rotated in the anti-clockwise direction by the cam member 149b provided on the outer periphery thereof against the spring 153 with the shaft 152 as the center of rotation. When the gear section 151b of the stop lever 151 is engaged with the indicator needle 34a of the meter 34 to cause it to collide against the restricting member 154, further rotation of the stop lever 151 is prevented, on account of which the driving ring 149 is stopped, and the photographic lens 146 is set at the forward position to be indicated by the indicator needle 34a, i.e., the forward position corresponding to the distance of the object. Accordingly, if the shutter release button 166 is further depressed, at the time of stoppage of the lens 146, the shutter release lever 173 is actuated by further rotation of the engaging and stopping lever 163 to release the shutter (not shown), whereby the clearest image of the object can be photographed on the film (not shown). Thereafter, when the photographer removes his hand from the shutter release button 166, it returns to the position shown in the drawing by the action of the spring 169, at which time the switch 172 is opened and the range detecting unit *U* is disconnected from the power source and accordingly ceases operation.

Thus, in the camera shown in Figure 24, very quick and accurate automatic focussing of the photographic lens 146 becomes possible with an extremely simple construction, and in utilization of the range detecting device shown in Figure 2, particularly, by utilizing the indicator needle 34a of the meter 34 for indicating the object distance as the final data output means of the detecting device. Also, according to this camera construction, when the release button 166 is depressed to a position where it is click-stopped by the click spring 170, the switch 172 is closed, but the lens 146 is not released. If, at this instant, the operator releases the pressure on the release button 166, the switch 172 is opened and the distance information from the detecting unit *U* is cancelled to permit reselection of the object to be photographed, and corresponding change of object distance provided such release occurs prior to release of the lens 146.

The above-described two embodiments of the automatic focus adjusting system are of such type that the photographic lens is adjusted according to the object distance as represented by the output from the range detecting device. However, it is also possible, with in the scope of this invention, to obtain from the range detecting device information permitting continuous retro active control of the in-focus position of the taking lens, at which the taking lens focusses the object image on the film plane, by interlocking the lens 13 shown in Figure 1 or 2 with the photographic lens, for example.

This will be explained in reference to Figure 26. In the drawing, the component elements corresponding to elements shown in Figures 1, 2 and 23 are designated by the same reference numerals. Also, those portions which overlap with the construction shown in Figure 2 are omitted from the illustration. First of all, as already explained in connection with Figure 1, the lens 13 is so arranged that it may cause the exact center part of the object image position at an infinite distance to coincide with the center part of the sensor region consisting of initial (or the rightmost) N sensors (N is an even number) in the sensor array 14, as shown in the drawing. Now, assume that an object distance, in which the center part of the image becomes just coincided by the lens 13 with the center *C* of the sensor array 14, as the reference, is d'. Any object, the center part of the image of which is positioned to the left of this center *C*, i.e., to the side indicated by arrow A, is closer to the camera than the point at distance D'. Conversely, any object, the center part of the image of which is positioned to the right of this center *C*, i.e., to the side indicated by arrow B, is further from the camera than the point at distance D'. The lens 13 is not fixed, but made movable in the arrow directions *a* and *b* as shown in the drawing, and is adjusted by a coupling 188 as shown generally by broken lines with respect to the photo-taking lens 138 in such a relationship that it may cause the center of the image of an object to coincide with the center *C* of the sensor array 14 when the photo-taking lens 138 is accurately focus-adjusted to that object. Thus, if the image center of the object to be formed on the sensor array 14 by the lens 13 is positioned to the side A of center C, the object is positioned closer than the point of focus of lens 138 with the consequence that the taking lens 138 is in the "back" focus state with respect to this object. Conversely, when the image center of the object is positioned within the region of the arrow-

indicated B side, in the drawing, the object is positioned further away than the point of focus of the taking lens 138 with the consequence that the taking lens 138 is in the "front" focus state. In this case, in the course of shifting the two-value image signals recorded in the shift register 24, just M-N/2 shifting operations are required counting from the instant when the two-value signals of the image element signals from the initial N numbers of the sensors of the sensor array 14 have been completed recorded in the shift register 24, as is understandable from the drawing, until the two-value signals of the image element signals from the N numbers of the sensors with the abovementioned center *C* of the sensor array 14 as the center will become recorded in the shift register 24. Therefore, if the M-N/2 is subtracted from the counted values of the counter 28 when the coincidence detection circuit 27 shown in Figure 2 detects the coincidence, in the course of carrying out such coincidence detection while causing the two-value signals of the image element signals from the sensor array 14 recorded in the shift register 24 to shift bit by bit with respect to the two-value signals of the image element signals from the sensor array 12 recorded in the shift register 23, the sign of the result (i.e. positive or negative) represents the direction of the abovementioned deviation, i.e., whether it is the "back" focus (positive) or the "front" focus (negative), and the absolute values thereof represent the quantity of this deviation (if the subtracted result is zero, this represents that the taking lens 138 is in the in-focus position).

From the above view point, the embodiment shown in Figure 26 is so constructed that it may produce the reference voltage V_{ref} corresponding to the value M-N/2 by the reference voltage setting circuit 189 in accordance with the equation D=d.f/x which has been explained in connection with Figure 1 and apply the output to the (+) input side of the differential amplifier 143, while applying the output voltage from the D/A converter 33 to its (–) input side. That is, according to such construction, the polarity of the output from this differential amplifier 143 represents the deviation, i.e., directivity of the focus deviation (the absolute value of the output, of course, represents the quantity of the deviation). Therefore, when the output from this differential amplifier 143 is applied to the motor control circuit 144, the control circuit 144 causes the motor 139 to drive either in the direction of arrow *a* or *b* to eliminate this deviation in accordance with the polarity of the output from the differential amplifier 143, thereby moving the taking lens 138 in the direction of the arrow *a* or *b* along the optical axis thereof. At this time, the lens 13 is shifted in the direction *a* or the direction *b* in correspondence with the moving direction of the taking lens 138 through the linking mechanism 188, and, when the image center of the object becomes coincided with the center *C* of the sensor array 14 in the course of shifting of the lens 13, the output of the differential amplifier 143 becomes zero, whereby the motor control circuit 144 stops the motor 139, and the taking lens 138 is accurately focussed to the abovementioned object. In the embodiment shown in Figure 26, the automatic focus adjustment of the taking lens 138 is thus achieved.

As has been stated in the foregoing, the devices described herein are so constructed that, by adoption of the range finding principle in the so-called double-image coincidence type range finder meter, apparent parallax in accordance with the distance, i.e., a relative displacement between two images to be formed, is detected by a purely electrical method such that digitallized image scanning signals of the two images are relatively shifted and compared. Accordingly, deterioration in the range finding precision or various inconveniences due to complicated device construction, etc., as has been experienced with previously proposed range detecting methods and apparatuses, can be alleviated to a marked extent and the highly precise range detection is made possible with a relatively simple circuit construction. Also, since the image scanning signals obtained in analog quantities are converted by a quantization into digital data, highly precise detection is possible, and, moreover, the construction of the processing circuit can be much simplified. In particular, since the coincidence detecting circuit utilizes digital data as its object of processing, its construction can be simple. Further, by utilizing IC components in the circuit construction, the device can be made very compact so that it can be applied highly advantageously to the automatic focus adjusting system in optical apparatus such as cameras, etc.

Incidentally, when a pair of the photo-sensor arrays are used as shown in Figure 2, the position of the image on the photosensor 14 changes in accordance with the object distance, so that the number of the sensors sufficient for covering the displacement of the image is determined by the base line length, focal distance, and range finding region, etc., between the lenses 11 and 13. On the contrary, as the image on the photo-sensor array 12 is the reference image, it can be focussed at a substantially constant position, so that the number of sensors can be less than the

number required in the photo-sensor array 14.

Also, when the coincidence of the recorded value in the shift registers 23 and 24 is to be detected, it is desirable that the data from the entire bits (i.e., N bits) in the shift registers 23 and 24 be appraised and detected, as shown in the illustrated embodiment, although, when the bit number becomes large, the construction of the coincidence detecting circuit 27 becomes complicated and the wiring becomes also complicated. In such case, it is practical to detect the coincidence in appropriate numbers of bits in the N numbers such as, for example, N/2 number at every one bit, or N/4 number at every three bits, or any arbitrary bit numbers.

For the photo-sensor array to be used in the above devices, CCD image sensor and self-scanning type photo-diode array are convenient and easy to use. Also, by introducing each output of the ordinary photo-diode array into the analog shift register as the input thereto, these signals can be used as the time-sequential signals.

The size of a single sensor in the commercially available CCD image sensor and self-scanning type photo-diode array, is ordinarily 10 to 50 microns, depending on the precision required in the range finding operation. More particularly the smaller the size of the sensor, the smaller is the smallest image movement which can be detected by the photo-sensor array, and the more accurate is the distance information which can be obtained. On the other hand, if the size of the sensor is large, the signal output becomes great, but very small variations in the distance cannot be detected. However, in utilization of the advantage of large signal output, such large-sized sensor can be used to advantage in the zone focus system in the camera, etc.

In the above-explained embodiments, the processing of the data is carried out in conformity to the sampling of the image data such that, after the quantized image data concerning the initial N−1 successive image elements of the second image, i.e., the quantized signals concerning the outputs of the sensors 14_1 to 14_{N-1} in the photo-sensor array 14, or the sensors 69_{N+1} to 69_{2N-1} in the second sensor region 69b of the photo-sensor array 69 are stored in the shift register 24 or 85, the data processing for the coincidence detection is repeated every time the quantized image data concerning the subsequent one image element of the second image becomes stored. It is, of course, possible that this data processing be carried out after the quantized data concerning the entire M image elements of the L-N image elements of the second image, i.e., the quantized signals concerning the outputs of the entire sensors 14_1 and 14_M in the sensor array 14, or the entire sensors 69_{N+1} to 69_L in the second sensor region 69b of the sensor array 69 are obtained by clearly separating the image data sampling and their processing as the sequence, and then stored in the shift registers. In this case, it may be feasible to arrange that, in the embodiment shown in Figure 2 or Figure 11, for example, the shift register is made the M-bit or L-N bit construction, or a serial-in-serial-out type third shift register of the M-N or L-2N bit construction is coupled to the input side of the shift register 24; and, in the embodiment shown in Figure 14, the serial-in-serial-out type third shift register of the M-N bit or L-2N bit construction is further provided to the input side of the shift register 85, thereby carrying out the sequence control of the data processing so that the quantized data for each of M or L-N sets of N successive image elements of the second image may be successively compared with the quantized data for N successive image elements of the 1st image. According to this construction, the timing of the data processing can be arbitrarily selected without being governed by the timing for the image data sampling.

WHAT WE CLAIM IS:—

1. A method of detecting the range of an object, comprising the steps of:—

deriving first and second mutually spaced images of the object from radiation passing from the object along different optical paths;

deriving quantized data concerning each of N successive elements of the first image and quantized data concerning each of M successive elements of the second image, wherein M is greater than N; and

detecting, on the basis of the quantized data concerning the N successive elements of the first image and the quantized data concerning the M successive elements of the second image, a location, within the M successive elements of the second image, of one set of N successive elements which is most similar to the N successive elements of the first image, the said location being indicative of the said range of the object, the quantized data deriving step comprising the steps of:—

electrically sensing the elements of the first and second images to produce an electrical representation of each of the elements;

setting the value of a variable quantization standard on the basis of at least a portion of the electrical representations produced by a previous said sensing step, and

quantizing, on the basis of the quantization standard so set, each of the

electrical representations produced by the sensing step to produce the said quantized data.

2. A method according to claim 1 wherein the said value of said variable quantization standard is derived from the electrical representations, produced by said previous sensing step, only of the N elements of the said first image.

3. A method according to claim 1 or claim 2 wherein said value of said variable quantization standard is derived from that electrical representation having the greatest magnitude out of said at least a portion of electrical representations.

4. A method according to claim 3 wherein said variable quantization standard comprises a threshold level determined by a preset proportion of said greatest magnitude.

5. A method according to claim 3 or claim 4 wherein the repetition rate of said sensing steps is determined by a timing pulse train, wherein the electrical representation having the maximum magnitude out of said at least a portion of said electrical representations is caused to be stored in a storage means and wherein in response to each timing pulse an output indicative of the stored electrical representation is taken from said store for the derivation of said quantization standard and, after a predetermined delay following the occurrence of said timing pulse, said storage means is cleared and thereby prepared for the reception and storage of the electrical representation of maximum magnitude in the electrical representations supplied subsequent to the clearance.

6. A method according to any preceding claim wherein said quantization step comprises the step of comparing each of the electrical representations with the quantization standard so as to produce, as the quantized data, binary data on each element of said first and second images.

7. A device for detecting the range of an object, comprising:—

optical means arranged to form first and second mutually spaced images of the object from radiation passing from the object along different optical paths;

image sensing means arranged for sensing the first and second images to produce an electrical representation of each of successive elements of the first and second images;

quantization standard setting means for setting the value of a variable quantization standard on the basis of at least a portion of the electrical representations produced by the sensing means;

quantization means for quantizing each of the electrical representations produced by the sensing means on the basis of the quantization standard previously set by the quantization standard determination means to produce quantized data concerning each of the elements of the first and second images; and

a detection system for receiving the quantized data from the quantization means and for detecting, on the basis of quantized data concerning N successive elements of the first image and quantized data concerning M successive elements of the second image, where M is greater than N, a location, within the M successive elements of the second image, of one set of N successive elements which is most similar to the N successive elements of the first image, the said location being indicative of the range of the object.

8. A device according to claim 7 wherein said quantization standard setting means is arranged to derive the value for said variable quantization standard from the electrical representations, produced by said image sensing means, only of the N elements of said first image.

9. A device according to claim 7 or claim 8 wherein said quantization standard setting means is arranged to derive the value for said variable quantization standard from that electrical representation having the greatest magnitude out of said at least a portion of electrical representations.

10. A device according to claim 9 wherein said quantization standard setting means includes means for setting a threshold to constitute said quantization standard in accordance with a preset proportion of said greatest magnitude.

11. A device according to claim 9 or claim 10 including means for producing a train of timing pulses which determine the repetition rate of the operation of the image sensing means to produce said electrical representations, and wherein the quantization standard setting means includes storage means which is arranged to store therein the electrical representaton having the maximum magnitude out of said at least a portion of said electrical representations and which is arranged to produce, in response to each said timing pulse an output indicative of the stored electrical representation for the derivation of said quantization standard, and to be cleared of its contents after a predetermined delay following the occurrence of said timing pulse, thereby to become prepared for the reception and storage of the electrical representation of maximum magnitude in the electrical representations supplied subsequent to the clearance.

12. A device according to any of claims 7 to 11 wherein said quantization means is arranged to compare each of the electrical

representations with the quantization standard so as to produce, as the quantized data, binary data in each element of said first and second images.

13. A method of detecting the range of an object, substantially as herein before described with reference to the accompanying drawings.

14. A device for detecting the range of an object, substantially as hereinbefore described with reference to any of the accompanying drawings.

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Sheet 1

FIG. 1

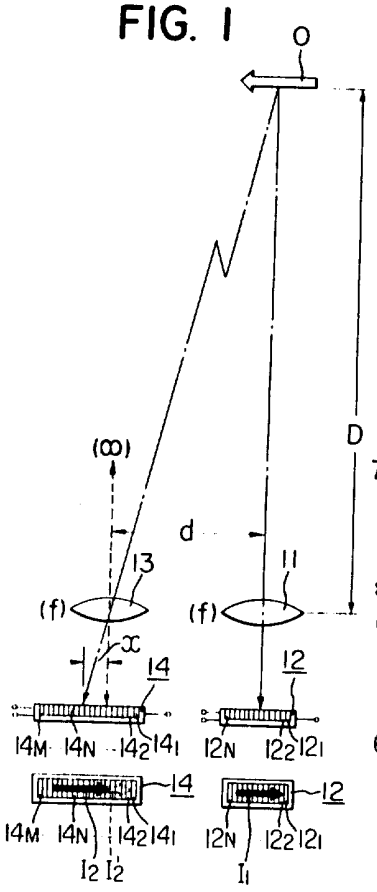


FIG. 10

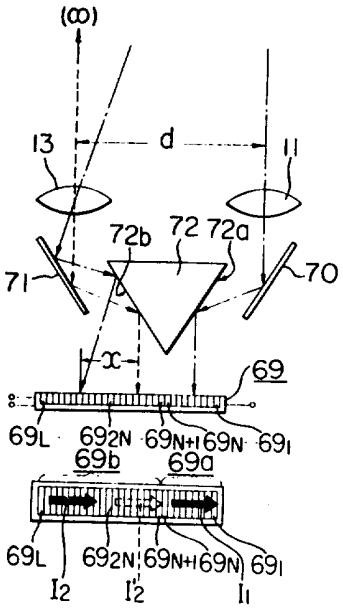


FIG. 2A

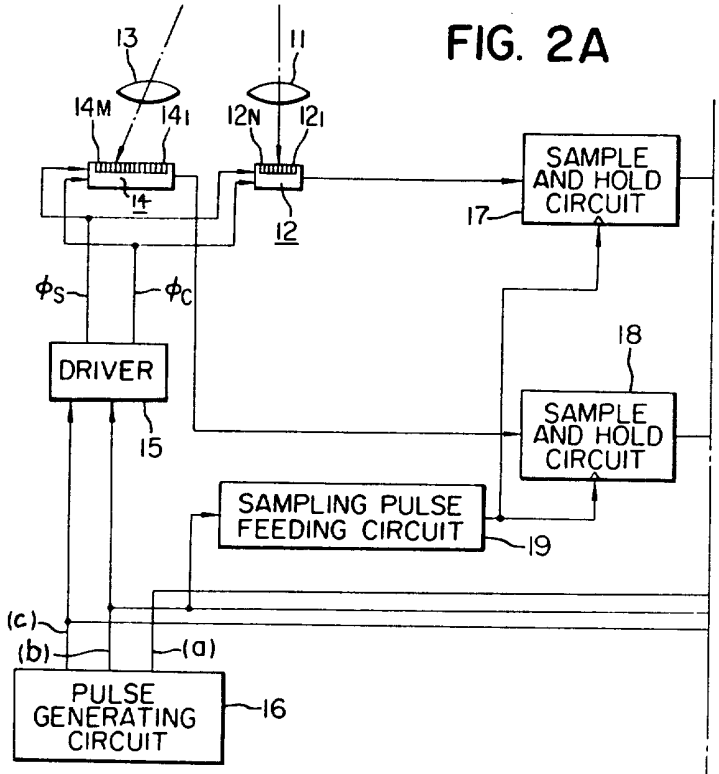
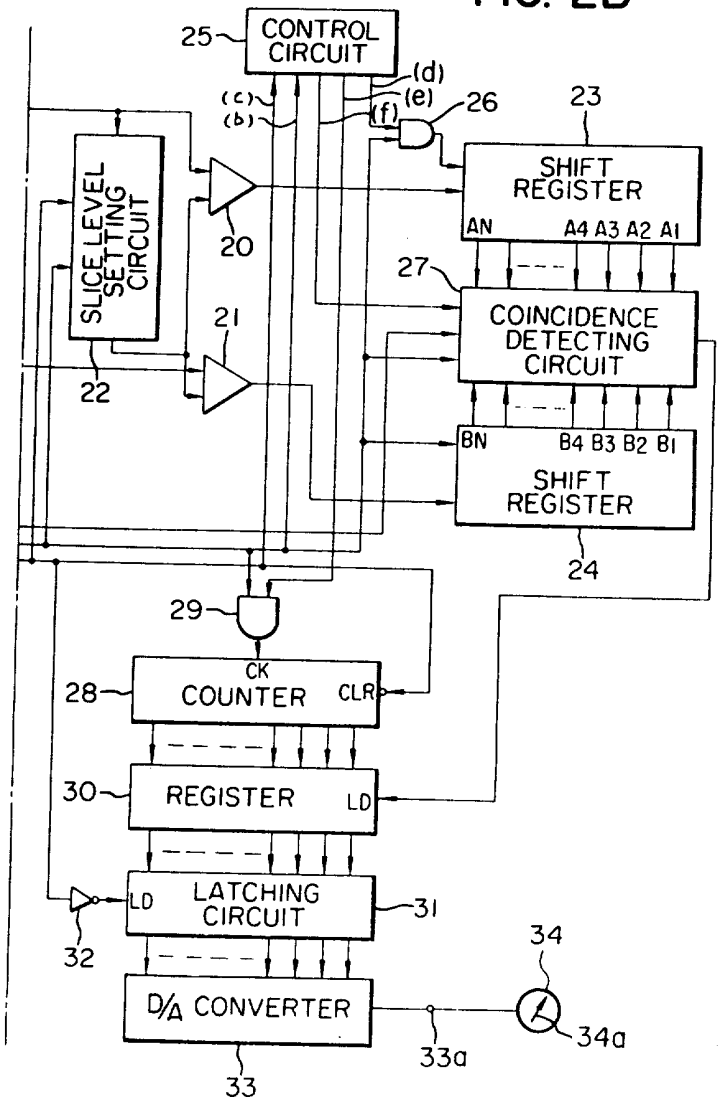


FIG. 2

FIG. 2A	FIG. 2B

FIG. 2B


25
CONTROL CIRCUIT
(d)
(c)
(e)
(b)
(f)
26
23
SHIFT REGISTER
AN
A4 A3 A2 A1
SLICE LEVEL SETTING CIRCUIT
20
21
22
27
COINCIDENCE DETECTING CIRCUIT
BN
B4 B3 B2 B1
SHIFT REGISTER
24
29
CK
28
COUNTER
CLR
30
REGISTER
LD
LD
LATCHING CIRCUIT
31
32
34
D/A CONVERTER
34a
33a
33

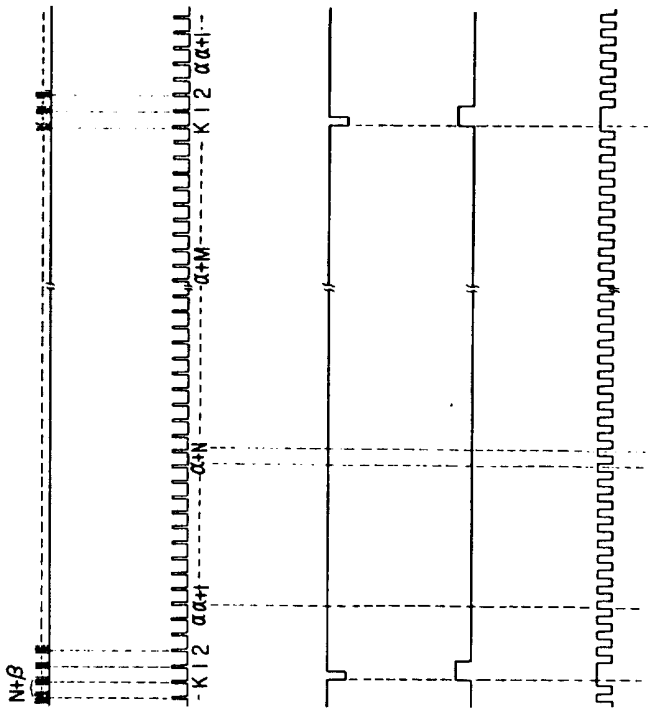


FIG. 3A
PULSE GENERATING CIRCUIT 16 OUTPUT (OUTPUT a)

FIG. 3B
PULSE GENERATING CIRCUIT 16 OUTPUT (OUTPUT b)

FIG. 3C
PULSE GENERATING CIRCUIT 16 OUTPUT (OUTPUT c)

FIG. 3D
DRIVER 15 OUTPUT (START PULSE ϕ_S)

FIG. 3E
DRIVER 15 OUTPUT (DRIVE CLOCK ϕ_C)

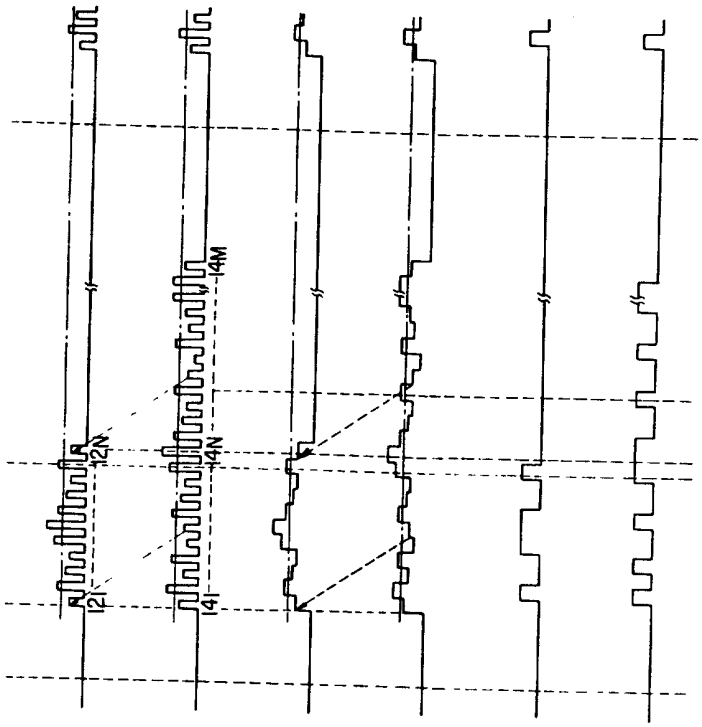


FIG. 3F
SENSOR ARRAY 12 OUTPUT

FIG. 3G
SENSOR ARRAY 14 OUTPUT

FIG. 3H
SAMPLE AND HOLD CIRCUIT 17 OUTPUT

FIG. 3I
SAMPLE AND HOLD CIRCUIT 18 OUTPUT

FIG. 3J
COMPARATOR 20 OUTPUT

FIG. 3K
COMPARATOR 21 OUTPUT

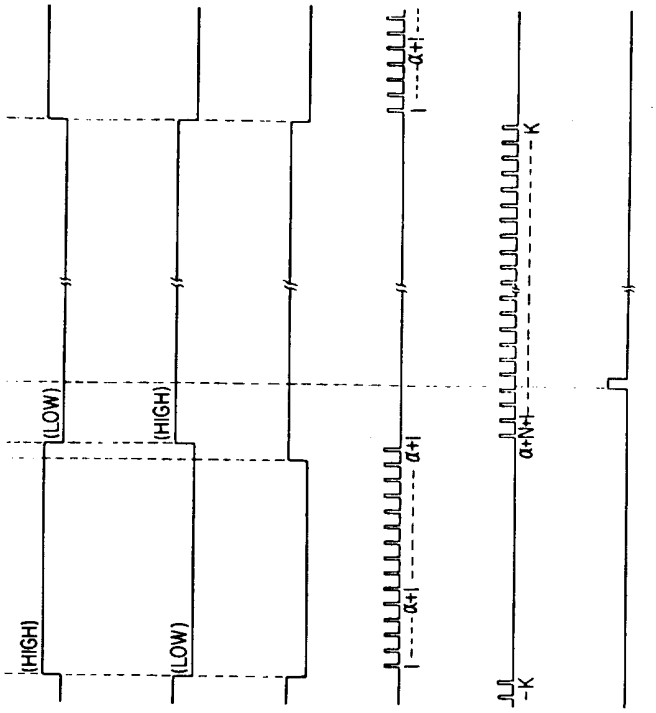


FIG. 3L
CONTROL CIRCUIT 25 OUTPUT (OUTPUT d)

FIG. 3M
CONTROL CIRCUIT 25 OUTPUT (OUTPUT e)

FIG. 3N
CONTROL CIRCUIT 25 OUTPUT (OUTPUT f)

FIG. 3O
"AND" GATE 26 OUTPUT

FIG. 3P
"AND" GATE 29 OUTPUT

FIG. 3Q
COINCIDENCE DETECTING CIRCUIT 27 OUTPUT (COINCIDENCE SIGNAL)

FIG. 4

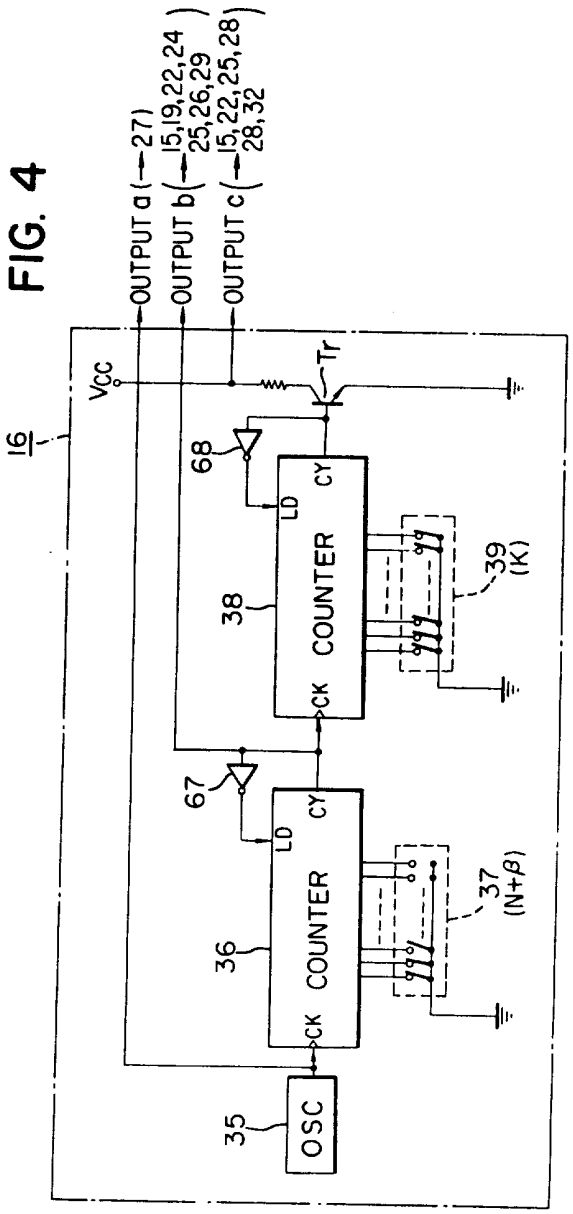

OUTPUT a (→27)
OUTPUT b (→15,19,22,24 25,26,29)
OUTPUT c (→15,22,25,28 28,32)
16
Vcc
Tr
68
LD
CY
38
COUNTER
CK
39
(K)
67
LD
CY
36
COUNTER
CK
37
(N+β)
35
OSC

FIG. 5

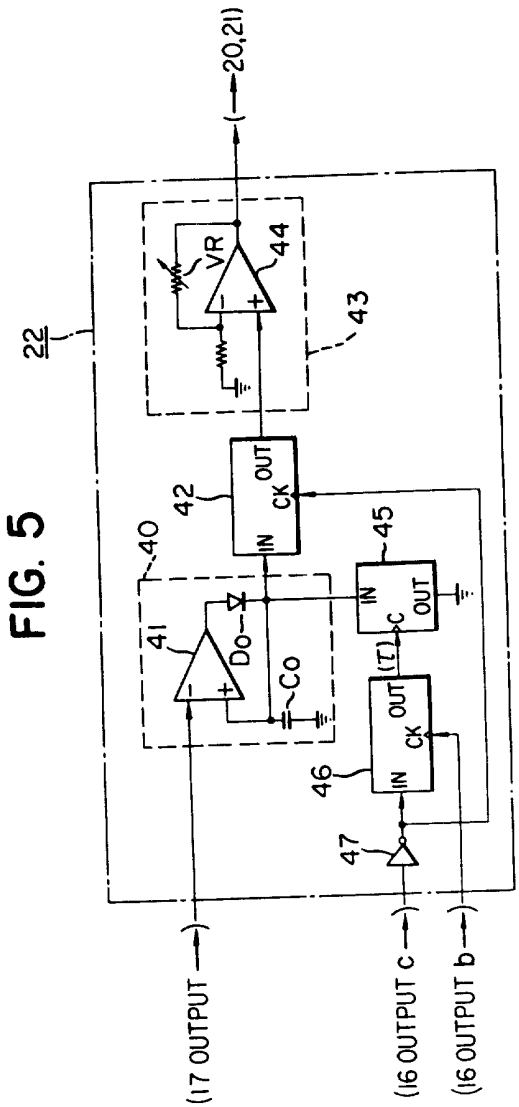

(20,21)
22
VR
44
43
42
OUT
CK
IN
40
45
IN
OUT
C
(T)
41
Do
Co
OUT
CK
IN
46
47
(17 OUTPUT
(16 OUTPUT c
(16 OUTPUT b

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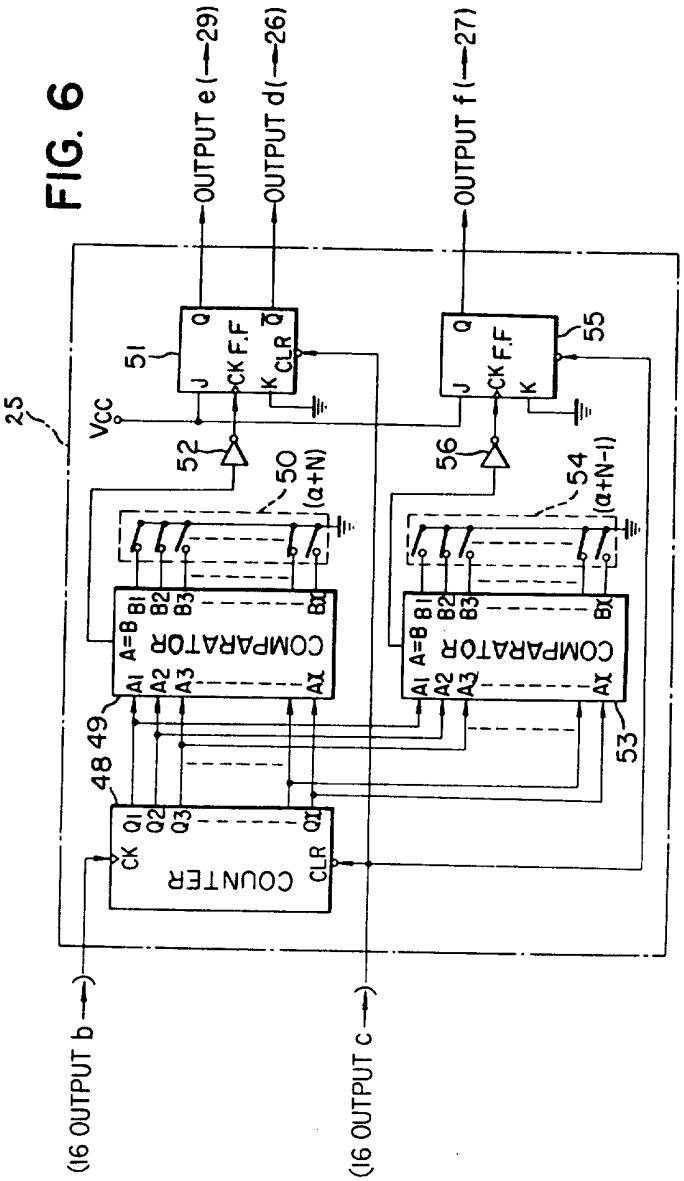
FIG. 6



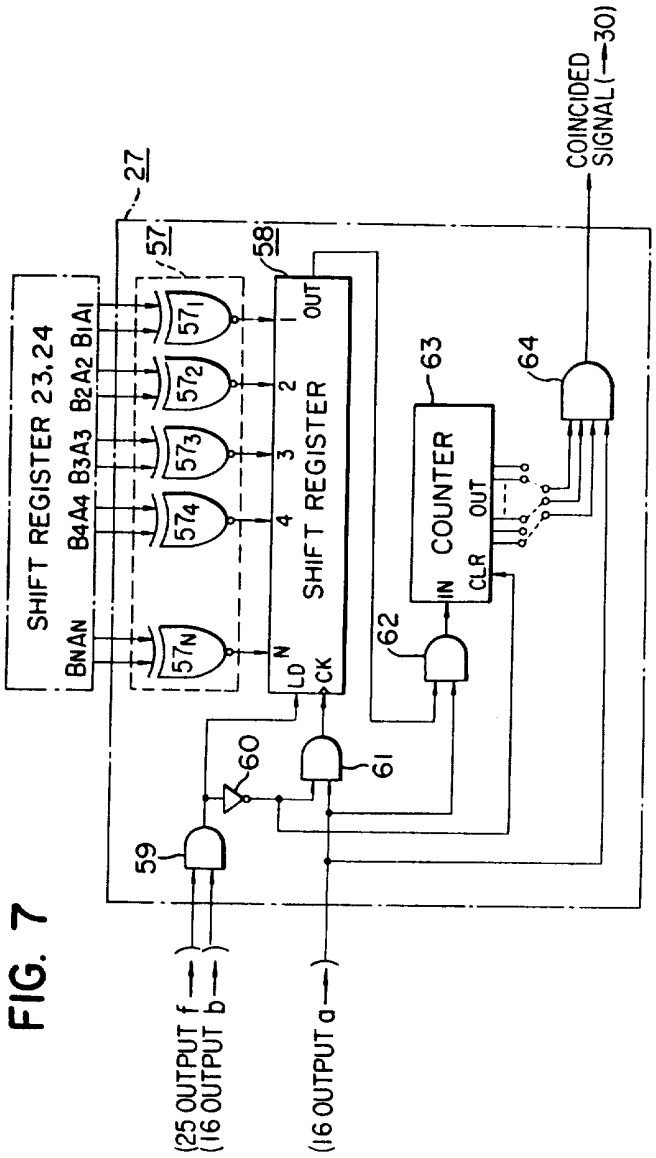

COINCIDED SIGNAL (—30)
27
57
58
SHIFT REGISTER 23,24
BNAN B4A4 B3A3 B2A2 B1A1
57N
57₄
57₃
57₂
57₁
SHIFT REGISTER
OUT
LD
CK
COUNTER
IN
CLR
OUT
63
64
62
60
61
59
(25 OUTPUT f —)
(16 OUTPUT b —)
(16 OUTPUT a —)

FIG. 7

FIG. 8A
PULSE GENERATING CIRCUIT 16 OUTPUT a
N+β1 2
N+β1 2
N+β1 2
FIG. 8B
PULSE GENERATING CIRCUIT OUTPUT b
α+N-1
α+N
α+N+1
α+N+1
FIG. 8C
CONTROL CIRCUIT 25 OUTPUT f
(LOW)
(HIGH)
FIG. 8D
"AND" GATE 59 OUTPUT
FIG. 8E
INVERTER 60 OUTPUT
(HIGH)
(LOW)
FIG. 8F
"AND" GATE 61 OUTPUT
N+β-1 1 2
N+β-1 1 2
N+β-1 1 2
FIG. 8G
"AND" GATE 64 OUTPUT
(COINCIDED SIGNAL)

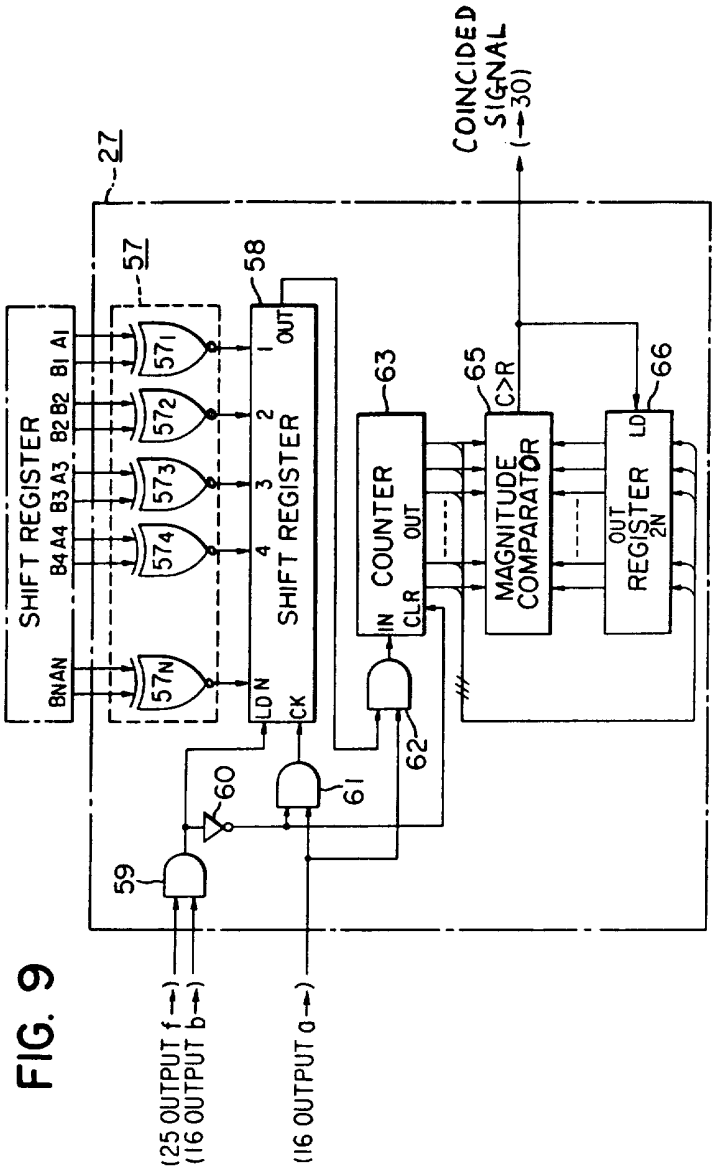

COINCIDED SIGNAL (→30)
27
57
58
63
65
66
SHIFT REGISTER
B1 A1
B2 B2
A3 B3
B4 A4
BN AN
571
572
573
574
57N
SHIFT REGISTER
OUT
LD N
CK
COUNTER
IN
CLR
OUT
MAGNITUDE COMPARATOR
C>R
REGISTER
LD
OUT
2N
59
60
61
62
(25 OUTPUT f→)
(16 OUTPUT b→)
(16 OUTPUT a→)

FIG. 9

FIG. 11

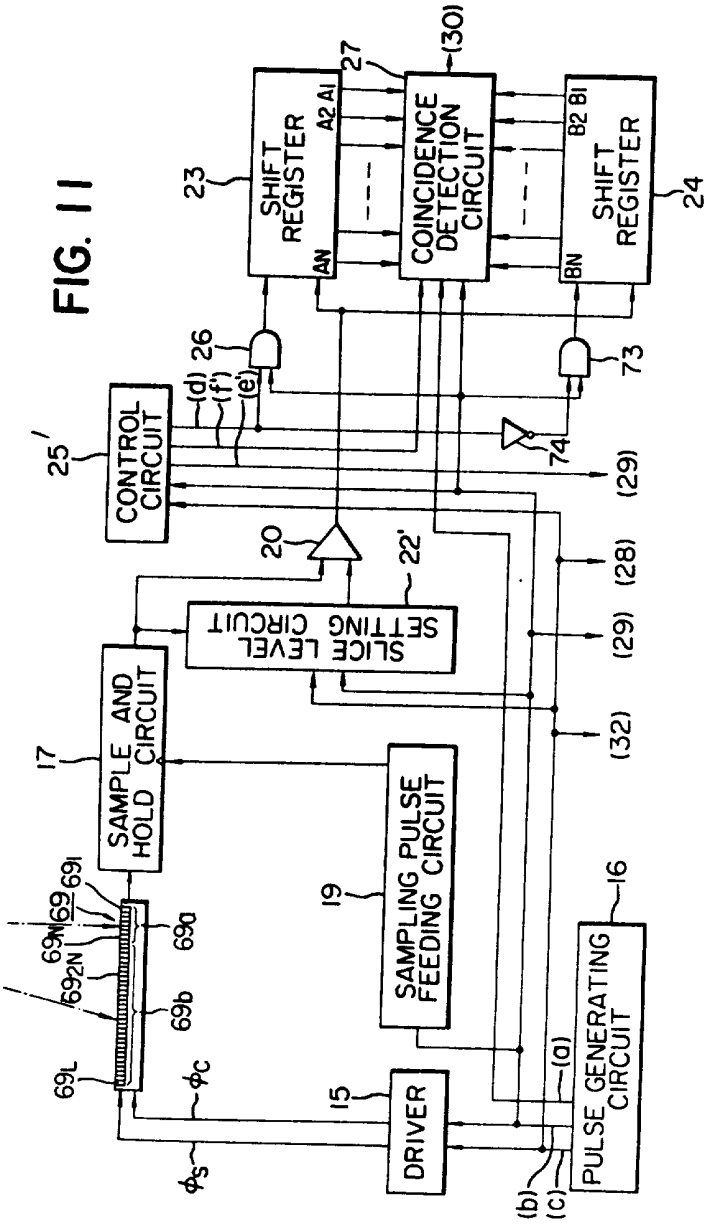

SHIFT REGISTER
A2 A1
AN
COINCIDENCE DETECTION CIRCUIT
B2 B1
BN
SHIFT REGISTER
CONTROL CIRCUIT
SLICE LEVEL SETTING CIRCUIT
SAMPLE AND HOLD CIRCUIT
SAMPLING PULSE FEEDING CIRCUIT
DRIVER
PULSE GENERATING CIRCUIT
23
24
25'
26
27
(30)
73
74
(29)
20
22'
(28)
17
19
16
15
(32)
(0)
(b)
(c)
(d)
(f')
(e)
69
69N
69N
69N
69a
69b
69L
φc
φs

FIG. 12

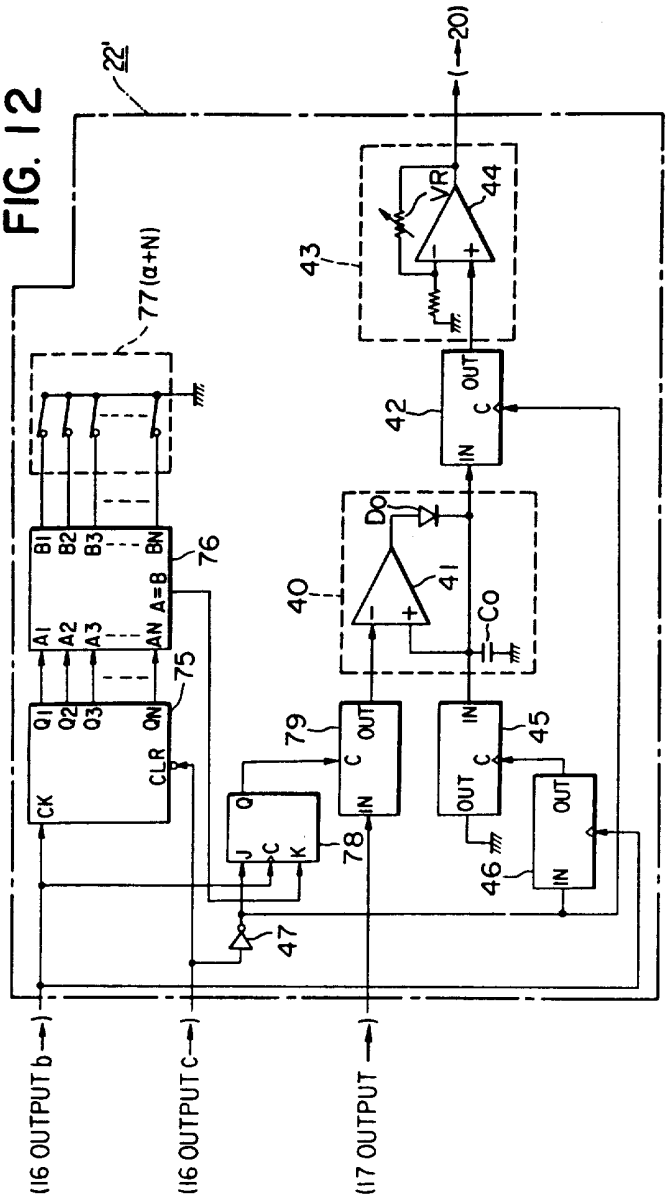

22'
(20)
VR
44
43
77(a+N)
42
OUT
C
IN
D0
41
40
C0
B1
B2
B3
BN
A=B
A1
A2
A3
AN
76
75
Q1
Q2
Q3
QN
CLR
CK
79
45
0
J
C
K
78
46
47
(16 OUTPUT b)
(16 OUTPUT C)
(17 OUTPUT)

FIG. 13

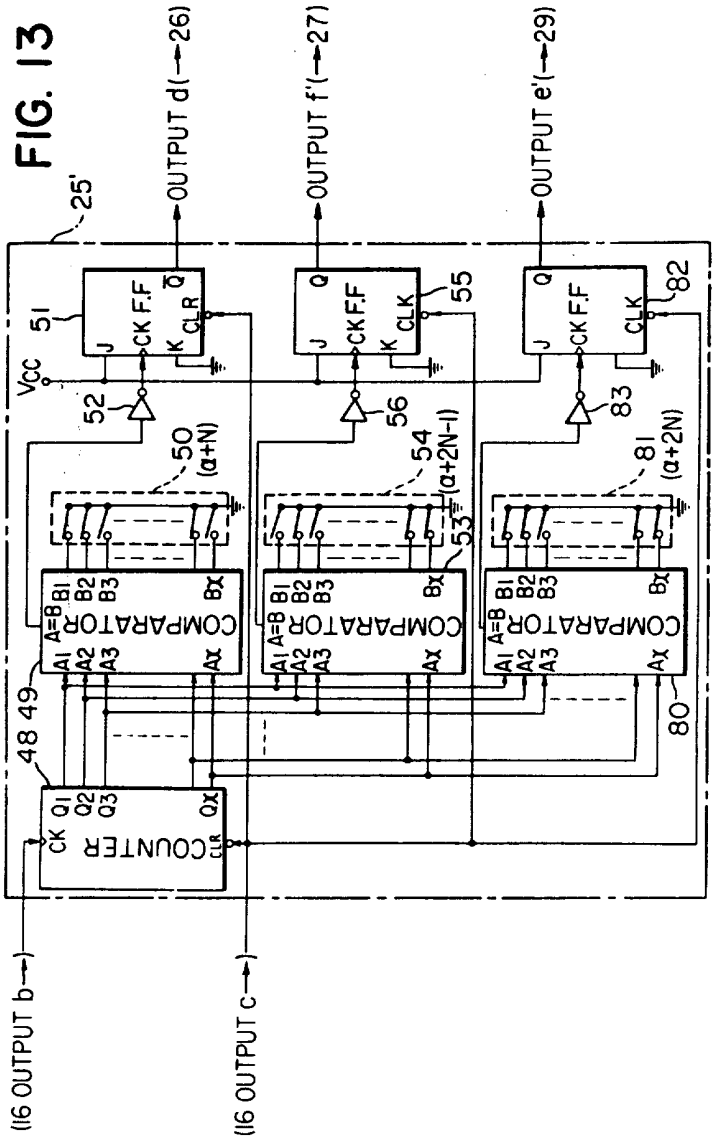
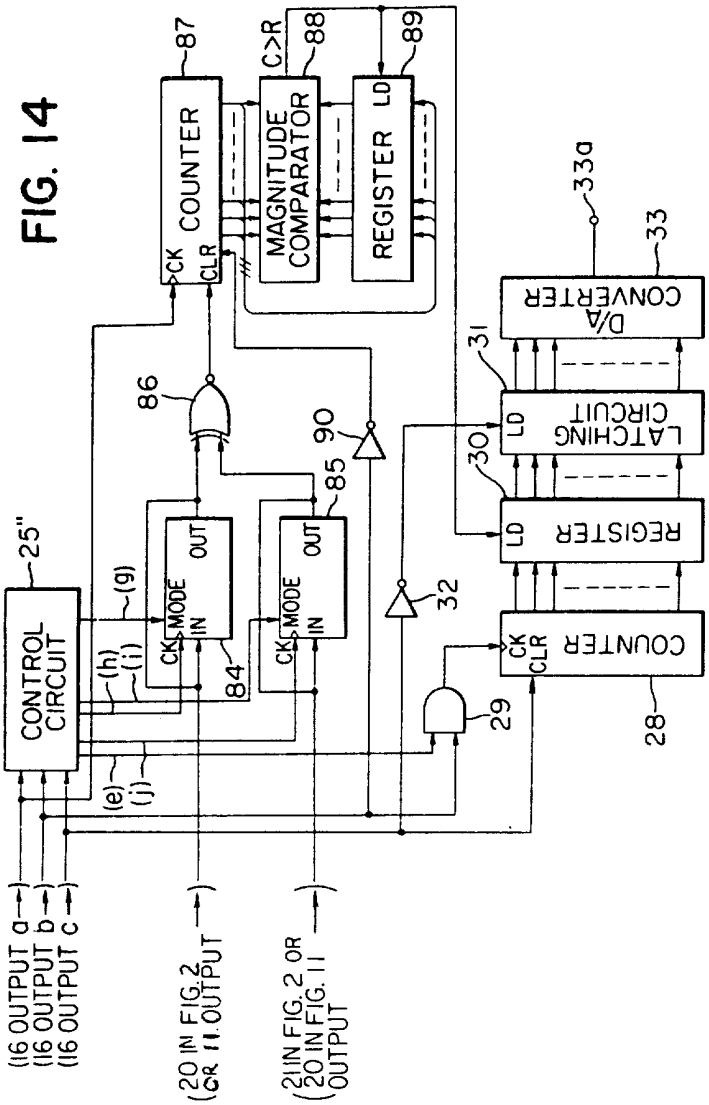

25'
OUTPUT d(→26)
OUTPUT f'(→27)
OUTPUT e'(→29)
51
55
82
Vcc
52
56
83
50 (a+N)
54 (a+2N-1)
81 (a+2N)
53
COMPARATOR
A=B
A1 A2 A3 Ax
B1 B2 B3 Bx
48 49
80
COUNTER
CK Q1 Q2 Q3 Qx CLR
(16 OUTPUT b→)
(16 OUTPUT c→)

FIG. 14


87
C>R
88
89
COUNTER
MAGNITUDE COMPARATOR
REGISTER
CK
CLR
LD
33a
33
D/A CONVERTER
31
LATCHING CIRCUIT
30
REGISTER
COUNTER
28
29
32
86
90
85
84
25"
CONTROL CIRCUIT
MODE IN
OUT
(g)
(h)
(i)
(e)
(j)
(16 OUTPUT a)
(16 OUTPUT b)
(16 OUTPUT c)
(20 IN FIG. 2 OR 11 OUTPUT)
(21 IN FIG. 2 OR 20 IN FIG. 11 OUTPUT)

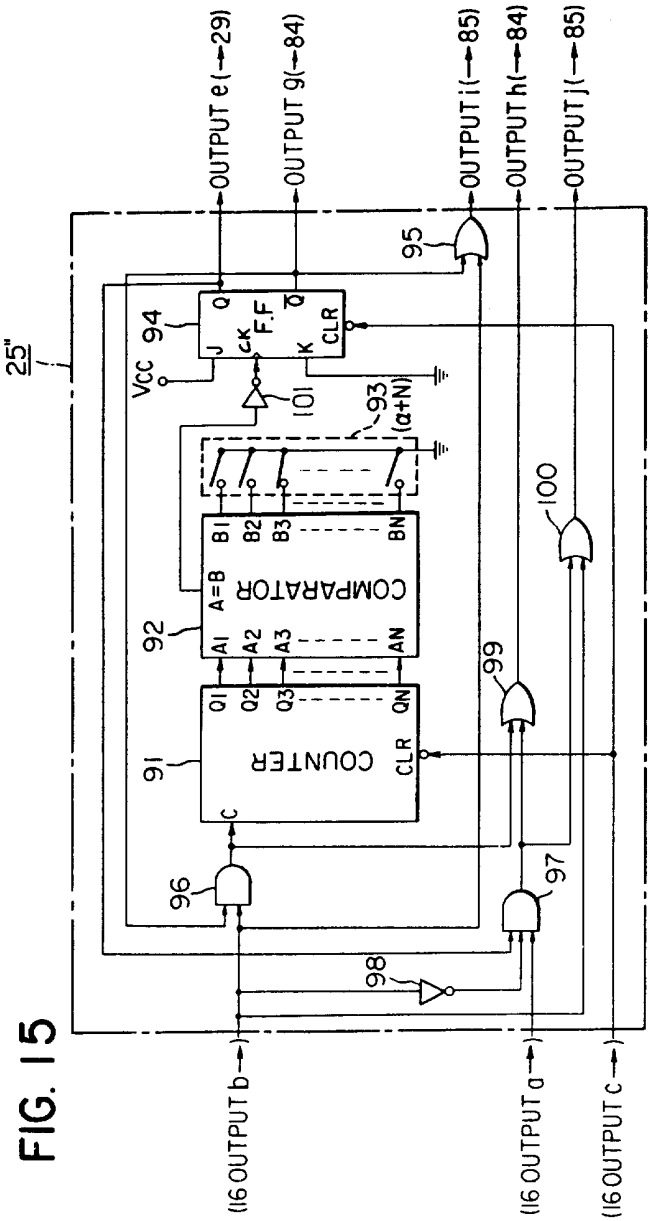

OUTPUT e(→29)
OUTPUT g(→84)
OUTPUT i(→85)
OUTPUT h(→84)
OUTPUT j(→85)
25"
95
94
Q
F.F
Q̄
J
CK
K
CLR
Vcc
101
93
(a+N)
100
B1
B2
B3
BN
A=B
COMPARATOR
92
A1
A2
A3
AN
99
Q1
Q2
Q3
QN
91
COUNTER
CLR
C
96
97
98
(16 OUTPUT b→)
(16 OUTPUT a→)
(16 OUTPUT c→)

FIG. 15

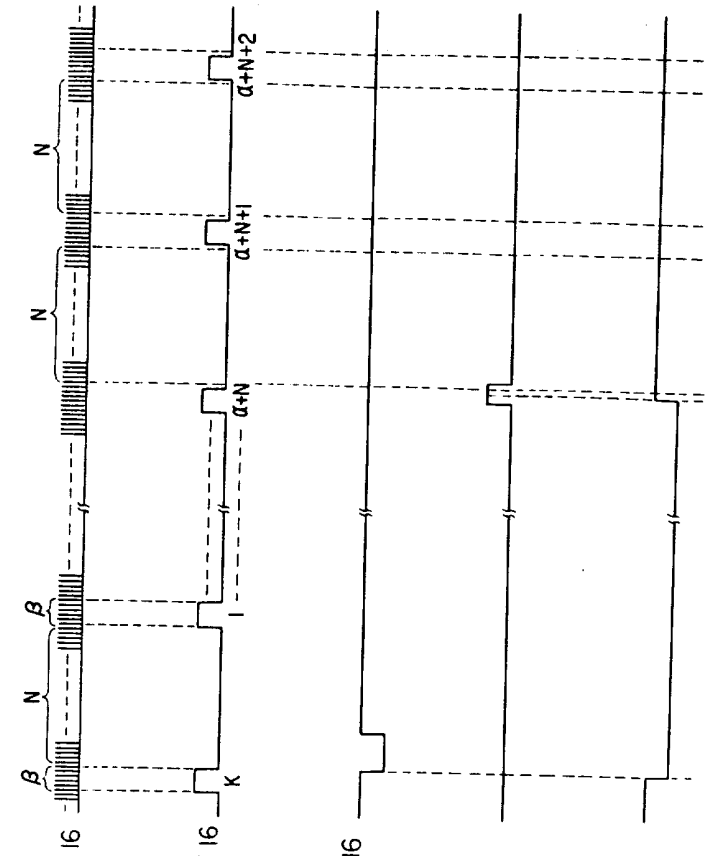


FIG. 16A
PULSE GENERATING CIRCUIT 16 OUTPUT a

FIG. 16B
PULSE GENERATING CIRCUIT 16 OUTPUT b

FIG. 16C
PULSE GENERATING CIRCUIT 16 OUTPUT c

FIG. 16D
COMPARATOR 92 OUTPUT

FIG. 16E
FLIP-FLOP 94 Q OUTPUT (OUTPUT e)

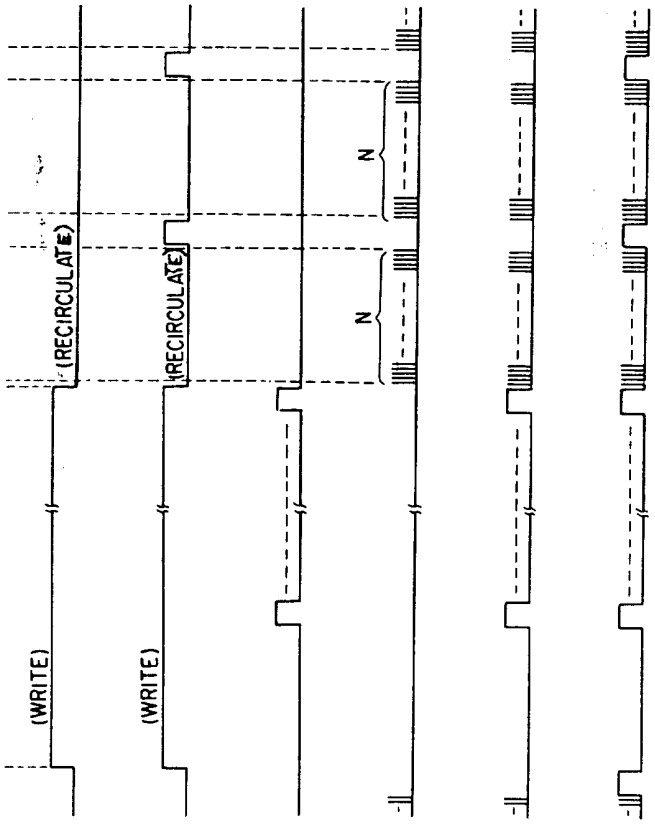


FIG. 16F
FLIP-FLOP 94 $\bar{Q}$ OUTPUT (OUTPUT g)

FIG. 16G
"OR" GATE 95 OUTPUT (OUTPUT i)

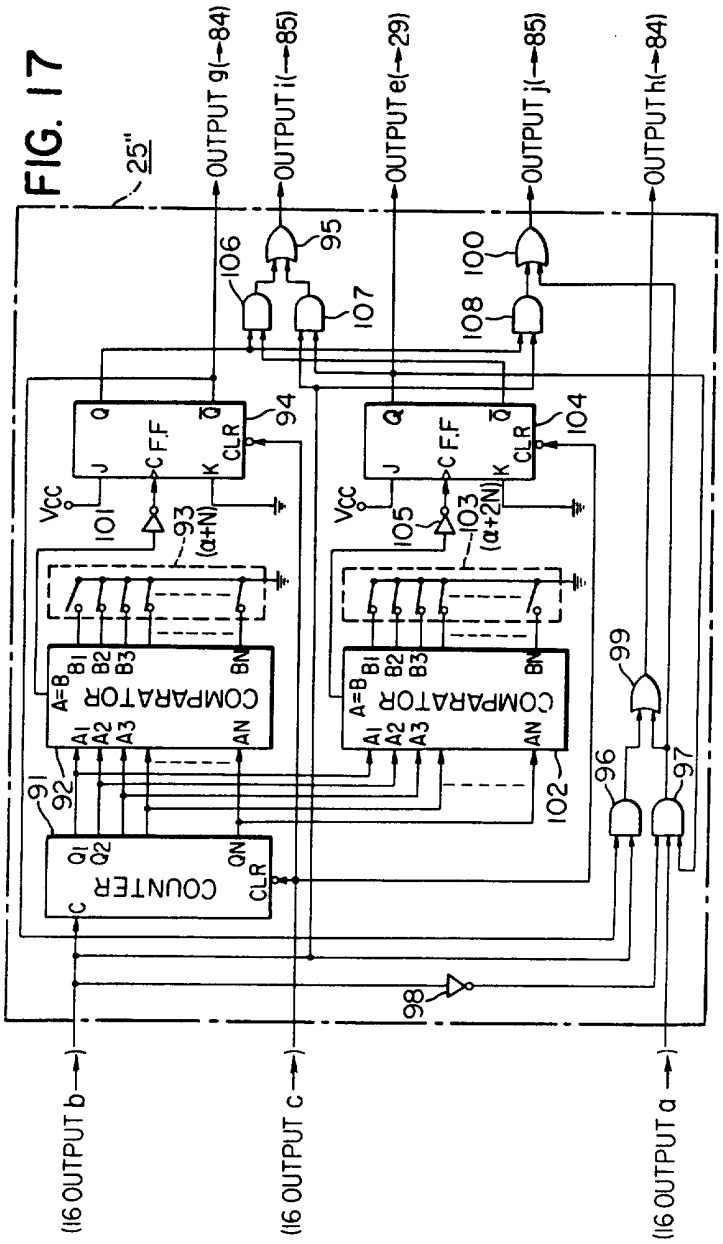
FIG. 16H
"AND" GATE 96 OUTPUT

FIG. 16I
"AND" GATE 97 OUTPUT

FIG. 16J
"OR" GATE 99 OUTPUT (OUTPUT h)

FIG. 16K
"OR" GATE 100 OUTPUT (OUTPUT j)

FIG. 17


25"
OUTPUT g(→84)
OUTPUT i(→85)
OUTPUT e(→29)
OUTPUT j(→85)
OUTPUT h(→84)
106
95
107
100
108
94
104
Vcc
101
93
(α+N)
105
103
(α+2N)
COMPARATOR
A=B
B1 B2 B3 BN
A1 A2 A3 AN
COUNTER
Q1 Q2 QN
CLR
C
J
K
C F.F
Q
99
96
97
91
92
102
98
(16 OUTPUT b)
(16 OUTPUT c)
(16 OUTPUT a)

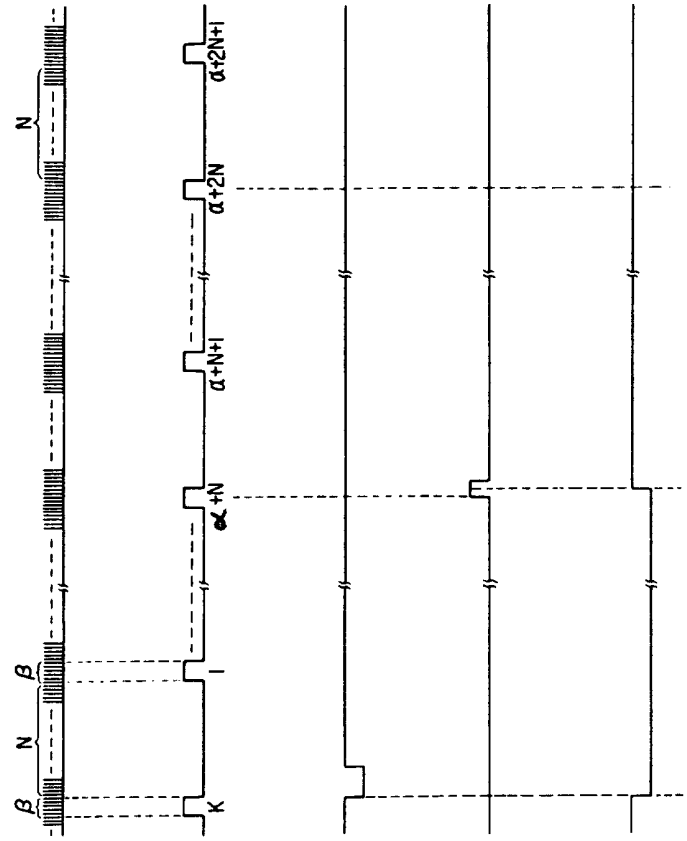


FIG. 18A
PULSE GENERATING CIRCUIT 16 OUTPUT

FIG. 18B
PULSE GENERATING CIRCUIT 16 OUTPUT

FIG. 18C
PULSE GENERATING CIRCUIT 16 OUTPUT

FIG. 18D
COMPARATOR 92 OUTPUT

FIG. 18E
FLIP-FLOP 94 Q OUTPUT

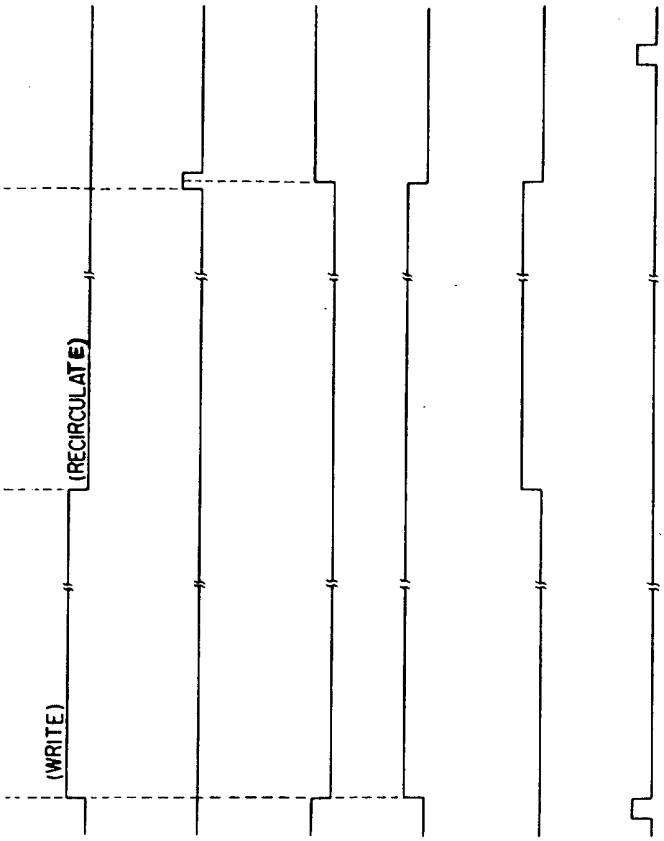


FIG. 18F FLIP-FLOP 94 $\bar{Q}$ OUTPUT (OUTPUT g)

FIG. 18G COMPARATOR 102 OUTPUT

FIG. 18H FLIP-FLOP 104 Q OUTPUT (OUTPUT e)

FIG. 18I FLIP-FLOP 104 $\bar{Q}$ OUTPUT

FIG. 18J "AND" GATE 106 OUTPUT

FIG. 18K "AND" GATE 107 OUTPUT

FIG. 18L
"OR" GATE 95 OUTPUT (OUTPUT i)

FIG. 18M
"AND" GATE 96 OUTPUT

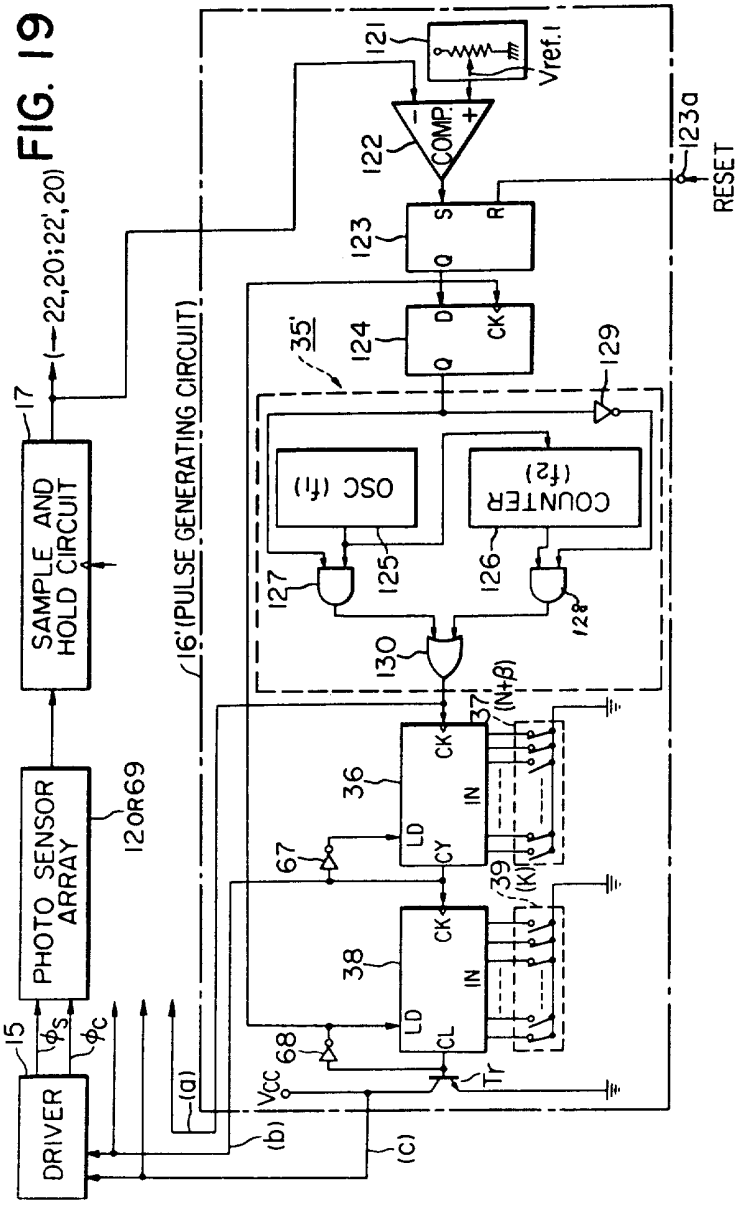
FIG. 18N
"AND" GATE 97 OUTPUT

FIG. 18O
"OR" GATE 99 OUTPUT (OUTPUT h)

FIG. 18P
"AND" GATE 108 OUTPUT

FIG. 18Q
"OR" GATE 100 OUTPUT (OUTPUT j)

FIG. 19


DRIVER
PHOTO SENSOR ARRAY
SAMPLE AND HOLD CIRCUIT
16'(PULSE GENERATING CIRCUIT)
OSC (f1)
COUNTER (f2)
COMP.
Vref.1
RESET
Vcc
Tr
CK
IN
LD
CY
CL
D
Q
S
R

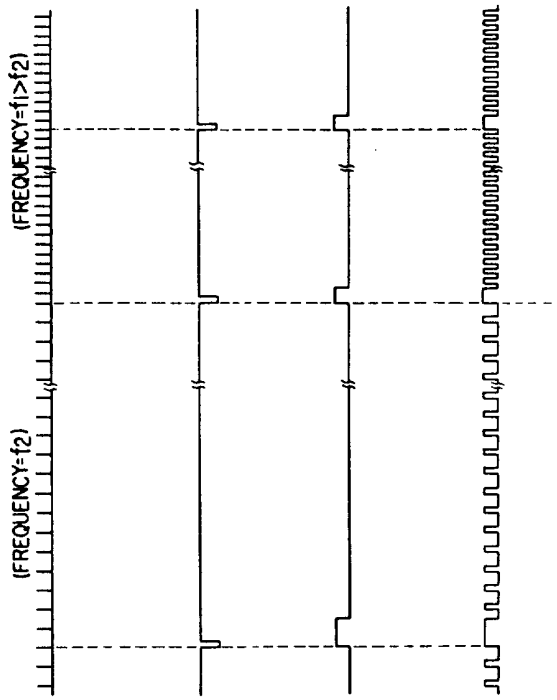


FIG. 20A
PULSE GENERATING CIRCUIT 16' OUTPUT (OUTPUT b)

FIG. 20B
PULSE GENERATING CIRCUIT 16' OUTPUT (OUTPUT c)

FIG. 20C
DRIVER 15 OUTPUT (START PULSE ϕs)

FIG. 20D
DRIVER 15 OUTPUT (DRIVE CLOCK ϕc)

FIG. 20E
SENSOR ARRAY 12 OR 69 OUTPUT

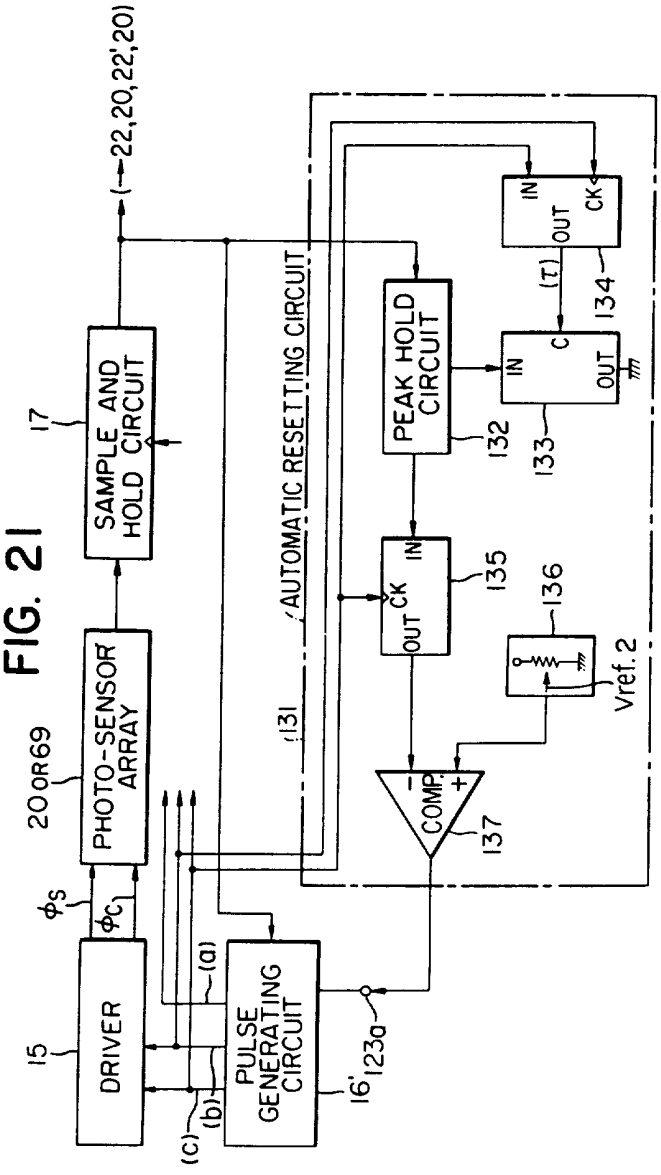
FIG. 20F
SAMPLE AND HOLD CIRCUIT 17 OUTPUT

FIG. 20G
COMPARATOR 122 OUTPUT

FIG. 20H
FLIP-FLOP 123 Q OUTPUT

FIG. 20I
FLIP-FLOP 124 Q OUTPUT

FIG. 21


(→22,20,22',20)
17
SAMPLE AND HOLD CIRCUIT
20 OR 69
PHOTO-SENSOR ARRAY
15
DRIVER
φS
φC1
(a)
(b)
(c)
PULSE GENERATING CIRCUIT
16'
123a
AUTOMATIC RESETTING CIRCUIT
131
PEAK HOLD CIRCUIT
132
133
134
(T)
IN
OUT
CK
C
135
136
Vref. 2
COMP.
137

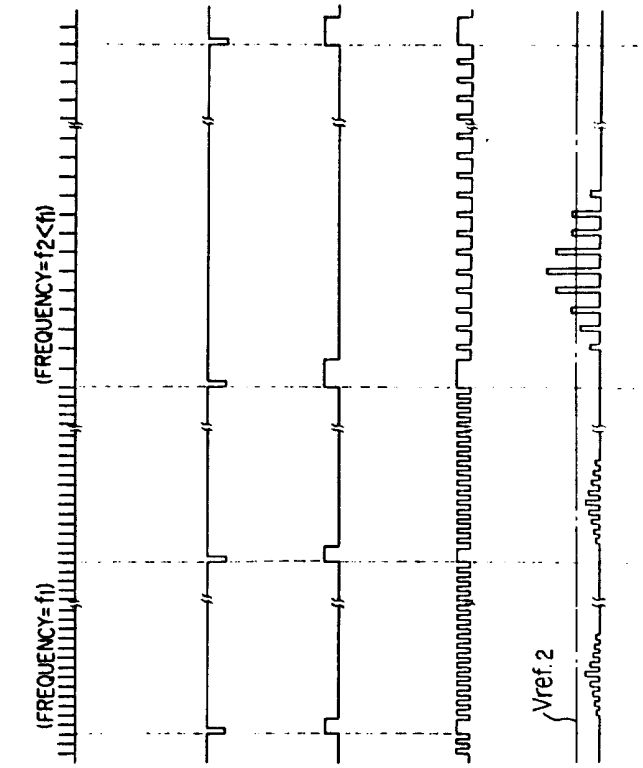


FIG. 22A
PULSE GENERATING CIRCUIT 16' OUTPUT (OUTPUT b)

FIG. 22B
PULSE GENERATING CIRCUIT 16' OUTPUT (OUTPUT c)

FIG. 22C
DRIVER 15 OUTPUT (START PULSE ϕ_S)

FIG. 22D
DRIVER 15 OUTPUT (DRIVE CLOCK ϕ_C)

FIG. 22E
SENSOR ARRAY 12 OR 69 OUTPUT

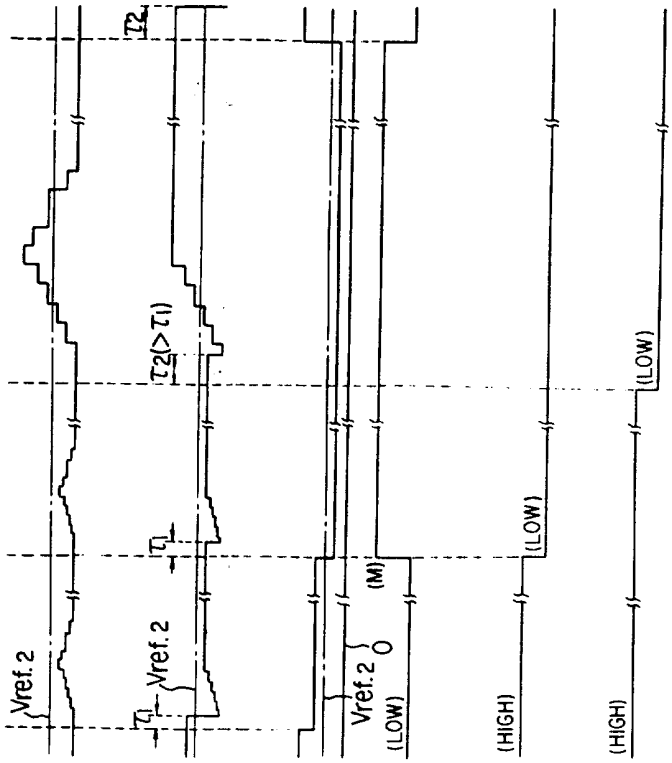


FIG. 22F
SAMPLE AND HOLD CIRCUIT 17 OUTPUT

FIG. 22G
PEAK HOLD CIRCUIT 132 OUTPUT

FIG. 22H
SAMPLE AND HOLD CIRCUIT 135 OUTPUT

FIG. 22I
COMPARATOR 137 OUTPUT (RESET SIGNAL)

FIG. 22J
FLIP-FLOP 123 (CIRCUIT 16') OUTPUT

FIG. 22K
FLIP-FLOP 124 (CIRCUIT 16') OUTPUT

FIG. 23

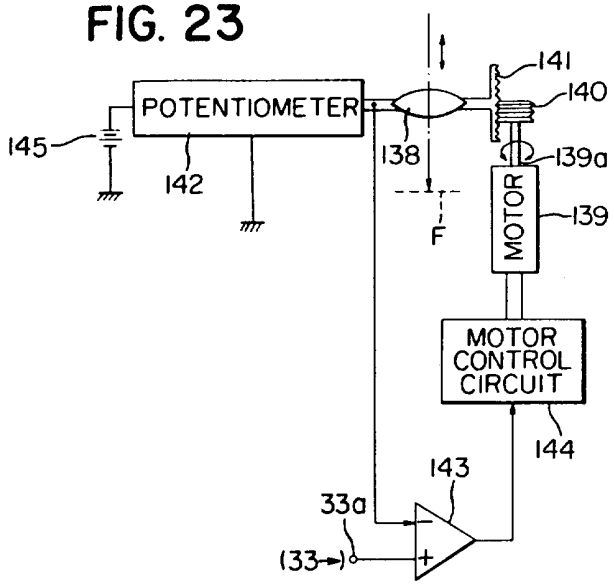
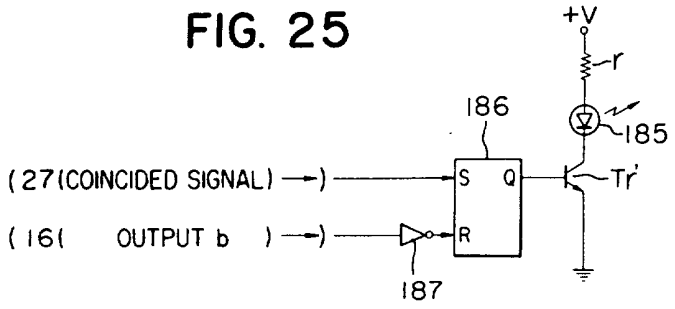

POTENTIOMETER
145
142
138
F
141
140
139a
MOTOR
139
MOTOR CONTROL CIRCUIT
144
143
33a
(33→)
+
-

FIG. 25

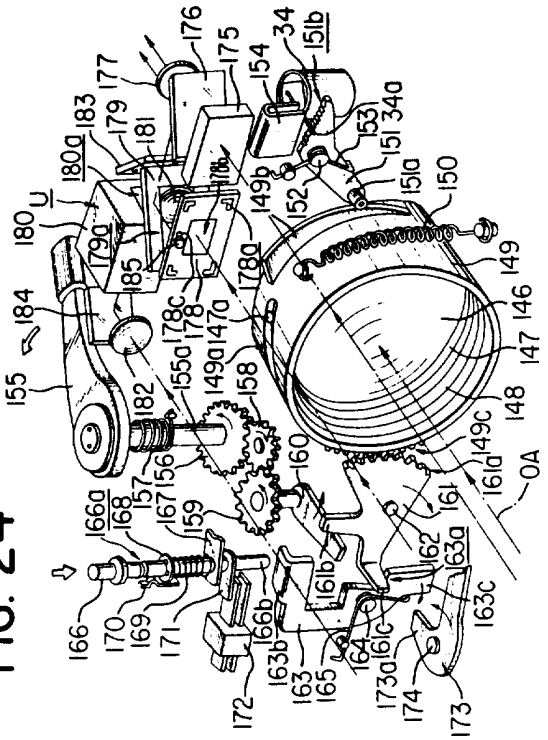

+V
r
186
185
(27(COINCIDED SIGNAL) →)
(16(OUTPUT b) →)
S
Q
R
Tr'
187

1599552 COMPLETE SPECIFICATION

32 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 31

FIG. 24



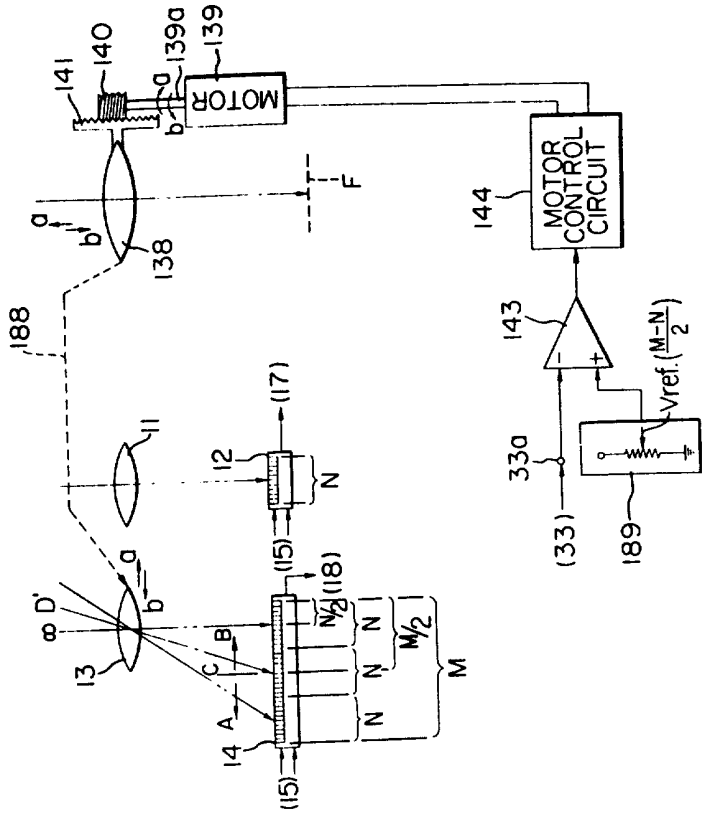

MOTOR
MOTOR CONTROL CIRCUIT
Vref.(M-N/2)
141
140
139a
139
144
143
138
188
11
12
17
N
15
18
M/2
M
13
14
33a
33
189
A
B
C
D'
F

FIG. 26