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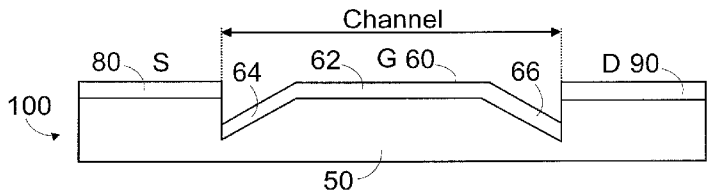



Fig. 2

(57) Abstract: According to an aspect of the invention, a method is provided for embossing electronic thin-film components. An input material comprising a compressible layer and a conductive layer on the compressible layer is provided. An embossing operation is performed on the conductive layer to galvanically separate portions of the conductive layer to form an electrode pattern, wherein the embossing operation is applied to form, by a single embossing operation, an electrode separated by at least two embossed lines.

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# Embossing of electronic thin-film components

## Field

The invention relates to embossing of electronic thin-film components.

## Background

Modern integrated circuits, typically silicon based structures, have very high integration density. As one descriptive parameter of this, the number of transistors per given surface area is growing steadily. However, integrated circuit based electronics are not optimal for all applications. For some applications the integration density and/or speed of the electronics is less crucial. Therefore, for certain applications different types of printable electronics are becoming more and more interesting. One approach to reducing transistor cost, while still maintaining acceptable performance, is to produce thin-film transistors on a suitable substrate by printing. Here printing means that at least some device layers have been manufactured by printing techniques. There are several known ways of manufacturing basic conductive patterns of printed circuit boards. As compared to traditional printing of electronics structures, embossing, which may also be referred to as imprinting, provides a simple and economic mass production with possibility to obtain smaller and better-controlled details in the electronic structures. Embossing is typically used to pattern a 3-dimensional structure on a layered substrate.

US 2008/0012151 discloses a method applying embossing to separate electrodes from each other. A source-drain or gate electrodē in a transistor device is embossed on a substrate of a transistor device to have transistor electrodes at least on two different vertical levels.

## Brief description

According to an aspect of the present invention, there is provided a method for embossing electronic thin-film components. An input material comprising a compressible layer and a conductive layer on the compressible layer is provided. An embossing operation is performed on the conductive

layer to galvanically separate portions of the conductive layer to form an electrode pattern, wherein the embossing operation is applied to form, by a single embossing operation, an electrode separated by at least two embossed lines.

According to another aspect, there is provided an apparatus for manufacturing electronic thin-film components by embossing, comprising: means for receiving an input material comprising a compressible layer and a conductive layer on the compressible layer; and means for performing an embossing operation on the conductive layer to galvanically separate portions of the conductive layer to form an electrode pattern, wherein the apparatus is configured to apply the embossing operation to form, by a single embossing operation, an electrode separated by at least two embossed lines.

According to a further aspect, there is provided an electronic thin-film component, comprising a compressible layer, and a conductive layer on the compressible layer, the conductive layer comprising an embossed electrode pattern, an electrode of the electrode pattern being separated by a single embossing operation by at least two embossed lines.

The invention and various embodiments of the invention provide several advantages, which will become apparent from the detailed description below. By the presently claimed arrangement it is, for example, easier to arrange further electrical contacts from the electrode separated by embossing, since the remaining non-embossed part of the electrode is better available for further electrical contacts. Another important feature is that the imprinted lines can be arranged to form a narrow electrical channel on the substrate. In other words using just two parallel imprinted lines, which can be produced in a single manufacturing step, it becomes possible to create an imprinted narrow gate structure with well-controlled dimensions.

**List of drawings**

Embodiments of the present invention are described below, by way of example only, with reference to the accompanying drawings, in which

Figure 1 illustrates a cross-sectional view of an electrode structure embossed according to an embodiment;

Figure 2 illustrates a cross-sectional view of a structure for a transistor device embossed according to an embodiment;

Figures 3a to 3c illustrate an embossing method according to an embodiment to separate transistor electrodes;

Figure 4 illustrates an example of imprinted transistor electrodes from a top-view;

Figure 5 illustrates manufacturing of electronic thin-film components applying embossing according to an embodiment;

Figure 6 illustrates a cross-sectional view of a structure for a transistor device embossed according to an embodiment;

Figure 7 illustrates a cross-sectional view of a structure for a transistor device embossed according to an embodiment;

Figure 8 illustrates a cross-sectional view of a transistor structure embossed according to an embodiment; and

Figure 9 illustrates a transistor component structure according to an embodiment.

**Description of embodiments**

Although the specification may refer to “an”, “one”, or “some” embodiment(s) in several locations, this does not necessarily mean that each such reference is to the same embodiment(s), or that the feature only applies to a single embodiment. Single features of different embodiments may also be combined to provide other embodiments.

Embossing of transistor electrodes is known from US 2008/0012151. According to this document, the embossed area defines a transistor gate. Thus, the embossed gate is formed into the bottom of a “dwell”. In this kind of configuration it is difficult to use the embossed gate for further connections as the embossed area is electrically separated from other neighboring metal layers. Connection to the gate requires arranging galvanic connection to the bottom of said "dwell". Therefore, there is a clear need to

further improve production efficiency of manufacturing of embossed electronics and connectability of embossed electrodes.

Figure 1 illustrates in a simplified form cross-sectional view of electrode structure embossed according to an embodiment. The electrodes 20 and 30 have been separated from an initial unitary conductive layer by an embossing operation forcing a compressible and substantially non-conductive layer 10 to compress and form a gap between the electrodes 20 and 30, in the present embodiment in a triangle form. Hence, embossing is applied only to a portion 22 of an electrode 20 to be separated. Thus, since the remaining part 24 of the electrode 20 is not embossed, the embossed portion 22 of the electrode and the remaining part 24 of the electrode are positioned on at least two different levels in transverse direction in relation to the plane of the compressible layer. Such embossing operation is obtained by an embossing tool comprising a non-embossing area and a protrusion producing the embossed portion 22 when pressed against the conductive layer. It will be appreciated that a tool suitable for the present purposes may instead or in addition to the non-embossing area comprise an area producing less compression than the protrusion. The electrode structure of Figure 1 enables easy use of the non-embossed part 24 of the electrode for further electrical connections.

Some further embodiments of such partially embossed electrodes are illustrated below in connection with transistor devices. However, it will be appreciated that an application of the present embossing features is not limited to manufacturing of transistor devices, but the present features may be applied for manufacturing of various other kinds of electrode structures.

Figure 2 illustrates a simplified cross-sectional view of a transistor device 100 structure embossed according to an embodiment. A source (S) 80, gate (G) 60, and drain (D) 90 are provided by a conductive layer on a compressible layer 50. The gate 60 is formed by an embossing operation applied only to edges 64, 66 of the gate area 60 of the conductive layer being separated. Thus, at least one portion 64, 66 of the gate 60 is positioned in a different level, in transverse direction in relation to the plane of the

compressible layer, than the source 80 and/or gate 90, whereas a remaining part 62 of the gate may remain substantially on the same level as the source 80 and/or the drain 90. The embossing operation produces two embossed lines 64 and 66 to separate the gate 60 from the source 80 and the drain 90. A transistor channel length is defined as the distance between the source and drain electrodes 80, 90. As illustrated in Figure 2, the distance between the terminating ends of the two embossed gate portions 64, 66 defines the transistor channel length.

The compressible layer 50 may form a substrate for the transistor device. In an alternative embodiment a further substrate layer is provided below the layer 50 in vertical direction (not shown in Figure 2). The compressible layer 50 may be any of a variety of suitable compressible plastics. Examples of suitable plastics for the compressible layer 50 include polyester (PET), polyamide (PI), polystyrene (PS), polycarbonate (PC), polymethayl methacrylatl (PMMA), polyether imide (PEI), polytetraflouroethylene (PTFE/Teflon) or polyetheretherketone (PEEK). Also other insulating materials may be used, to which materials it is possible to produce a permanent deformation by embossing in suitable conditions.

The conductive layer and the electrodes 60, 80, 90 may be any of a variety of suitable conductive materials for forming electrode patterns of thin-film transistor structures. For example, transparent semiconductor oxides, metals, or conducting polymers may be applied. In certain applications, the conductor material may be metal or carbon particle ink.

The embodiment of Figure 2 enables definition of a high performance three electrode transistor structure that can be manufactured using a single embossing step producing two imprinting lines 64, 66 at the same time. By the examples below various benefits of the invention become more clear for a person skilled in the art.

Figures 3a to 3c illustrate an embossing method according to an embodiment to separate electrodes of a thin-film device, such as electrodes for the transistor device 100 of Figure 2.

As illustrated in Figure 3a, input material comprising at least the conductive layer 55 and a compressible layer 50 is provided. A tool, which may be referred to as an embossing mold or a pressing plate 110, comprising at least two protrusions, which may be referred to as stamps 112, 114, is provided for driving a portion of the conductive layer material 55 into the compressible layer material 50. The pressing plate 110 may be an independent plate or part of an endless rotated metal belt, for instance.

The tool 110 may be manufactured by etching. However, also other manufacturing methods may be used. Electron beam lithography and/or optical patterning may be applied for forming the protrusion 112, 114 patterning. For instance, electron beam lithography may be used for features requiring highest resolution and optical patterning may be used for forming larger stamp features.

Figure 3b illustrates the embossing operation by the pressing plate 110 at suitable conditions, such as temperature. The pressing plate 110 is brought into contact with the input material. The pressing plate 110 drives the conductive material 55 to the compressible material 50. The compressible material is deformed and the stamps 112 and 114 break the conductive layer 55 to separate the electrodes, in the present embodiment the gate 60, the source 80 and the drain 90.

As illustrated in Figure 3c, the pressing plate 110 is then removed from the embossed transistor device 100. Suitable de-embossing technique(s) may be applied to ensure an effective and defect free separation of the pressing plate 110 from the embossed component. In one embodiment a suitable type of cooling is applied prior to the separation, in order to ensure that the deformed material 50 is sufficiently cooled to maintain the gap between the gate 60 and the source 80 and the gap between the gate 60 and the drain 90.

The thin-film transistor (TFT) channel is generally preferable to be made as narrow as possible, in order to improve electrical performance, i.e. switching speed of the device. According to the present embodiment this is now achieved with only one manufacturing step as both imprints 64, 66 in

Figures 2 or 3b, 3c are achieved using the same tool 110 that needs to be applied only once per transistor. Therefore, the channel length is defined by the tool 110 and this is the key to provide smaller channel length and/or better repeatable accuracy in the manufacturing method according to the present embodiment as compared to methods taught by prior art.

Because embossing of all electrodes 60, 80, 90 is done in a single embossing step, there is no need for alignment between successive steps, which increases manufacturing simplicity and and enables very high transistor-to-transistor repeatability. Further, it is possible to manufacture smaller transistor channels accurately with manufacturing tools that are suitable for large-scale manufacturing. It is expected that minimum channel lengths in the range of 0.1-50 μm can be readily achieved by the present method. Such narrow channel increases transistor performance and such transistors are well suitable for manufacturing of radio frequency identification RFID circuitry, for instance. Especially useful for very narrow transistor channel configurations is that it is easier to use all three electrodes 60, 80, 90 of the transistor for further contacts, and high resolution tools are not necessarily needed. A further advantage is that, since electrodes do not make overlap, it is possible to obtain small stray capacitances leading to higher speed.

It will be appreciated that the patterning of the conductive layer 55 may include patterning of multiple transistor devices that are part of a larger structure. That is, while electrodes of only one transistor are shown, there may be numerous transistors that are part of the device being manufactured. The embossing operation may also serve to separate different transistors on the same substrate.

The present features may be applied for various nanoimprint lithography methods. In one embodiment nanoprint lithography, which may also be referred to as hot embossing or thermoplastic embossing, is applied. In this embodiment the compressible layer 10, 50 is cured by heating during the embossing process.

In one embodiment the pressing plate 110 is, instead of or in addition to the heating of the compressible layer 10, 50, heated prior to being

brought into contact with the conductive layer 55 (Figure 3a). For example, at least protrusions 112, 114 of the plate 110 are heated above the softening temperature of material of the layer 50. Thus, it will be appreciated that the plate 110 may be made of a thermally-conductive material, such as a metal. The compressible layer 10, 50, such as substrate of a polymer layer on a substrate, is thus molded under pressure and heat. In one embodiment the temperature of inputted polymer film is raised just above the glass transition temperature before or while the stamp is being pressed against the polymer film. During the pressing, the temperature is lowered below the glass transition temperature to maintain the structure.

In another embodiment photo nanoprint lithography is applied, whereby the compressible layer 10, 50 is cured by heating or ultraviolet UV light during the embossing process.

A still further applicable method is electrochemical nanoimprinting using a stamp 112, 114 made from a superionic conductor, such as silver sulfide. However, the present embossing features may be applied also in various other current and future embossing or imprinting methods.

In one embodiment the embossing step produces a gate having at least two areas having different widths, which herein refers to the distance between the imprinted lines 72, 74. Figure 4 illustrates a top-view of a transistor according to an embodiment. The gate 60 separated by embossing has a channel portion 68 separating the transistor channel and a contact portion 70 for electrical contact to the gate 60. The contact portion 70 is, when viewing the transistor structure from top, wider than the channel portion 68. Thus, the single embossing operation is adapted to produce the two embossed lines 72, 74 having a first distance within the gate portion 62 and a second distance, greater than the first distance, within the contact portion 70.

Illustrative contacts 84, 94, and 76 for the source 80, the drain 90, and the gate 60, respectively, are depicted in Figure 4. The increased area of the contact portion 70 for the gate 60 further improves electrical contactibility of the gate 60, and the advantages of the present single-embossing step method are still achieved. Thus, by the present embossing arrangement producing

electrodes having variable width, it becomes easier to arrange further electrical contacts. Although the gate electrode may be large at a distance, a micrometer size channel may be imprinted by using the single embossing step.

In the embodiment of Figure 4 the first distance and the second distance are substantially invariable and there is also a third portion between the channel portion 68 and the contact portion 70 extending between the channel portion 68 and the contact portion 70, i.e. then forming a (upturned) Y-shape. It is evident that this third portion may be considered as belonging to the contact portion, and that various other shapes may be used to produce the contact portion having greater distance between the two embossed lines than that of the channel portion.

An electrode structure as illustrated in Figure 4 can be produced by a single imprinting step by applying a suitably formed protrusions or stamps 112, 114 within the embossing tool 110. In the embodiment of Figure 4, the distance between the stamps 112, 114 would be substantially invariable at the channel portion 68 to separate the gate 60 from the source 80 and the drain 90, but then the distance would increase to form the contact portion 70 having a greater width than the channel width. Thus, the tool 110 produces two unitary embossed lines together forming a (upturned) Y-shaped gate electrode.

In one embodiment the patterning is a part of a roll-to-roll process. Figure 5 illustrates an example of a manufacturing method and means for an apparatus for roll-to-roll electronic thin-film component manufacturing process system 150, such as manufacturing of transistors according Figures 2, 3, 4, or 6 to 9. A web of input film 170 is obtained from a first rotated roll 160 and the embossed film web is rolled on a second rotated roll 162. The input material for the embossing process from the first roll 160 comprises at least the compressible layer, but may also comprise further layers, such as a separate substrate and/or a conductive layer.

In the embodiment of Figure 5 the embossing operation is arranged by means of two rollers 180 and 182. A belt 190 including protrusions, such as stamps 112, 114 illustrated in Figures 3a to 3c, may move around the two rollers 180, 182 which advance the belt at a predetermined controlled speed or

rate. However, it will be appreciated that this is only one example of the various available pressing mechanisms. For instance one or more than two rollers may be applied, or the pressing operation may be applied by a non-rotatable plate.

A preparation station 200 prepares or cures the input film 170 prior to the embossing operation. In case thermoplastic nanoprint lithography is applied, the preparation station 200 may heat the input material from the first roll 160 to a suitable temperature for deformation of a thermo-compressible material layer 50 of the input material. In another embodiment the rollers 180, 182 and/or the belt 190 is heated.

In an embodiment, in which the input film from the first roll 160 does not comprise the conductive layer, the station 200, or a further station may also be provided to form the conductive layer 55 on top of the flexible layer 50 by a suitable coating process.

Embossing occurs on the web of input material 170 as it and the belt 190 pass around the roller 180 and while pressure is applied by one or more pressure rollers causing the input film 170 to be pressed onto the protrusions of the belt 190 and to partially deform. A backing support plate, belt or film may be pressed against the non-embossed surface of the film.

The source 80, gate 60 and drain 90 electrodes are separated by embossing at selected positions of the metal lines by means of the suitably patterned belt 190. The protrusions of the belt 190 are formed such that the embossing operation causes, for at least one of these electrodes being separated by embossing, that only portion of the conductive layer defining such at least one electrode being embossed.

A cooling station or other suitable detachment preparation station 210 may be provided between the two rollers 180, 182. The embossed film, which may have been laminated to other films during the embossing process, is thus cooled and then moved to the second rotated roll 162.

The apparatus 150 configured for at least the embossing operation is controlled by a computer-based control block, control unit, or controller. Such controller may be implemented by a suitably programmed computer

program and executed in a processor of the apparatus. The computer program may be stored on a computer program storage medium, such as an internal memory of the apparatus or an external memory connectable to the apparatus. A specific hardware unit, which may embody software-controlled features, in one embodiment controls at least some of the steps for manufacturing electronic thin-film components according to embodiments.

It is to be noted that the structures and steps illustrated in connection with Figure 5 represent only an example of a possible manufacturing method and apparatus, and various modifications, replacements and additions may be to these features. For instance, it is possible to arrange further steps and means for manufacturing additional transistor features illustrated below.

Figures 6 to 8 illustrate some further embodiments of transistor structures in which only a portion of a transistor electrode is embossed. Figure 6 illustrates that the embossing operation may be performed by rectangular stamps. Thus, two embossed lines 64, 66, substantially entirely on a same vertical level, may be produced.

In Figure 7 an embodiment is illustrated, where the embossing is applied to an edge 82 of a conductive layer portion forming a source 80 and to an edge 92 of a conductive layer portion forming a drain 80. Hence, the gate electrode 60 is separated by two embossed lines, but the entire gate electrode 60 is easily available for further contacts. The structure of Figure 7 is well suitable for narrow imprinted structures as the distance between the source and the drain defines the thin-film transistor (TFT) channel and the gap between the source and drain electrodes 80, 90 to the gate electrode 60 must be small.

Figure 8 illustrates a further embodiment of a transistor device. A dielectric layer 220 is formed on top of the embossed gate electrode 60 to form an insulator. The dielectric 220 on the gate electrode 60 may be fabricated in various ways. For instance, a masking process may be used where the preceding embossing step is used for defining the dielectric area. Depending

on the metal applied, anodisation may be used to grow an insulator on the gate electrode 60.

Electroplating may be used to grow a different metal onto the source electrode 80 and the drain electrode 90 (not shown in Figure 8). These electrodes 80, 90 may be treated for obtaining ohmic contact.

Semiconductive material is deposited on top of the dielectric layer 220, the source 80 and the drain 90 to form a semiconductor 230. Examples of suitable semiconductor materials are various polymeric semiconductor materials, such as polythiophene and polyacetylene. The semiconductor 230 may be printed or patterned. However, it will be appreciated that other suitable semiconductive materials and/or deposition methods may be applied.

With the illustrated embodiment in which the dielectric 220 covers only the gate electrode 60, the semiconductor 230 can be deposited over the channel area. As illustrated in Figure 9, the width of the semiconductor 230 defines the transistor channel width. In another embodiment the semiconductor 230 covers only part of the channel defined by embossing, whereby the transistor channel width is the same as the printed layer width, which means less need for high accuracy alignment. The dielectric layer 220 or the dielectric layer 220 and the semiconductor may be added during the embossing process, for instance as part of the system and method illustrated in Figure 5.

It will be appreciated that the configuration of Figure 8 is only one example of further material layers. For instance, the semiconductor 230 may be also extend over the drain and source electrodes 80, 90.

Further, Figure 8 illustrates the possibility to use a separate substrate layer 240 underneath the compressible layer 50. This substrate may be part of the originally inputted material, such as the material from the first roll 160. The additional substrate layer 240 may have a higher glass transition temperature than the flexible layer 50. For example, plastics, such as polyester (PET), polyamide (PI), polystyrene (PS), or polycarbonate (PC), may be used as the substrate material.

Figure 9 further illustrates a top-view of a transistor device with a semiconductor 230 placed on top of the electrodes 60, 80, 90 embossed according to an embodiment.

It is to be noted that above illustrated Figures illustrate only some examples of possible forms of the stamps 112, 114 and the cavities formed by the stamps. It is possible to provide various other shapes, such as U-shaped stamps or stamps having curved edges. Further, it is possible to combine these embodiments in various ways. The present embossing features may be applied also for other transistor electrode configurations. For instance, a gate may be added at a separate step after only the source and drain electrodes have been embossed by a single embossing operation.

Structures and features illustrated above may be applied for various applications of electronic devices. As already indicated, various radio frequency identification tags, for instance, are devices for which at least some of the above-illustrated features may be applied and particular advantages may be achieved. However, the present features may be applied in a wide variety of devices in which it is feasible to use transistors or other electrode structures manufactured by imprinting. Some further examples include active matrix displays and organic light-emitting diode (OLED) drivers, for instance.

It will be obvious to a person skilled in the art that, as technology advances, the inventive concept can be implemented in various ways. The invention and its embodiments are not limited to the examples described above but may vary within the scope of the claims. The features of the embodiments described herein may be combined in all possible combinations of methods, apparatuses, and products. The combinations of claim elements as stated in the claims can be changed in a number of different ways and still be within the scope of various embodiments of the invention.

## Claims

1. A method for embossing electronic thin-film components, comprising:

providing an input material comprising a compressible layer and a conductive layer on the compressible layer,

performing an embossing operation on the conductive layer to galvanically separate portions of the conductive layer to form an electrode pattern, wherein the embossing operation is applied to form, by a single embossing operation, an electrode separated by at least two embossed lines.

2. The method of claim 1, wherein the single embossing operation is applied to separate a source, a gate and a drain of a transistor structure.

3. The method of claim 2, wherein the single embossing operation is applied to edges of an electode area to form the gate, separating the gate from the source and the drain.

4. The method of claim 2 or 3, wherein an insulator covering all portions of the gate is added after the embossing operation, and semiconducting material is deposited on the insulator.

5. The method of any preceding claim 2 to 4, wherein the single embossing operation produces the two embossed lines having a first distance within a first gate portion to separate a transistor channel portion and a second distance within a second gate portion to separate a gate contact portion, the second distance being greater than the first distance.

6. The method of any preceding claim 5, wherein the first distance and the second distance are substantially invariable and there is a third gate portion between the first gate portion and the second gate portion, a distance

between the two embossed lines at the third gate portion gradually increasing from the first distance to the second distance.

7. The method of any preceding claim, wherein the compressible layer is a thermoplastic substrate layer or a thermoplastic coating layer formed on top of a substrate layer, and

the flexible material and/or at least protrusions of an embossing tool driving a portion of the of the electrode to be separated to the compressible layer material is/are heated prior to the embossing operation.

8. The method of any preceding claim, wherein the compressible layer is selected from a group comprising polyester, polyamide, polystyrene, polycarbonate, polymethayl methacrylatl, polyether imide, polytetraflouroethylene or polyetheretherketone.

9. The method of any preceding claim, wherein the input material or part thereof is obtained from a web, and the embossing operation is performed by a rotating pressing plate with a plurality of stamps.

10. An apparatus for manufacturing electronic thin-film components by embossing comprising:

means for receiving an input material comprising a compressible layer and a conductive layer on the compressible layer; and

means for performing an embossing operation on the conductive layer to galvanically separate portions of the conductive layer to form an electrode pattern, wherein the apparatus is configured to apply the embossing operation to form, by a single embossing operation, an electrode separated by at least two embossed lines.

11. The apparatus of claim 10, wherein the apparatus is configured to apply the single embossing operation to separate a source, a gate and a drain of a transistor structure.

12. The apparatus of claim 11, wherein the apparatus is configured to apply the single embossing operation to edges of an electode area to form the gate, separating the gate from the source and the drain.

13. The apparatus of claim 11 or 12, wherein the apparatus comprises at least two protrusions to produce the two embossed lines, the protrusions being adapted to produce a first distance between the two embossed lines within a first gate portion to separate a transistor channel portion and a second distance within a second gate portion to separate a gate contact portion, the second distance being greater than the first distance.

14. The apparatus of claim 13, wherein the first distance and the second distance are substantially invariable and there is a third gate portion between the first gate portion and the second gate portion, a distance between the two embossed lines at the third gate portion gradually increasing from the first distance to the second distance.

15. The apparatus of any preceding claim 10 to 14, wherein the compressible layer is a thermoplastic substrate layer or a thermoplastic coating layer formed on top of a substrate layer, and

the apparatus is configured to heat the flexible material and/or at least protrusions of an embossing tool driving a portion of the of the electrode to be separated to the compressible layer material prior to the embossing operation.

16. The apparatus of any preceding claim 10 to 14, wherein the input material or part thereof is obtained from a web, and the embossing operation is performed by a rotating pressing plate with a plurality of stamps.

17. An electronic thin-film component, comprising

a compressible layer, and

a conductive layer on the compressible layer,

the conductive layer comprising an embossed electrode pattern, an electrode of the electrode pattern being separated by a single embossing operation by at least two embossed lines.

18. The component of claim 17, wherein the at least two embossed lines separates a source, a gate and a drain of a transistor structure.

19. The component of claim 18, wherein the at least two embossed lines are positioned to edges of an electode area to form the gate, separating the gate from the source and the drain.

20. The component of claim 18 or 19, further comprising an insulator covering all portions of the gate and semiconducting material on the insulator.

21. The component of claim 18, 19, or 20, wherein the two embossed lines have a first distance within a first gate portion to separate a transistor channel portion and a second distance within a second gate portion to separate a gate contact portion, the second distance being greater than the first distance.

22. The component of claim 21, wherein the first distance and the second distance are substantially invariable and there is a third gate portion between the first gate portion and the second gate portion, a distance between the two embossed lines within the third gate portion gradually increasing from the first distance to the second distance.

23. The component of any preceding claim 17 to 22, wherein the compressible layer is a thermoplastic substrate layer or a thermoplastic coating layer formed on top of a substrate layer.

24. The component of any preceding claim 17 to 23, wherein the compressible layer is selected from a group comprising polyester, polyamide, polystyrene, polycarbonate, polymethayl methacrylatl, polyether imide, polytetraflouroethylene or polyetheretherketone.

5

25. A radio frequency identification tag, comprising an electronic thin-film component according to any one of claims 17 to 24.

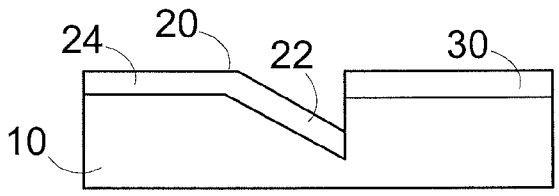



Fig. 1

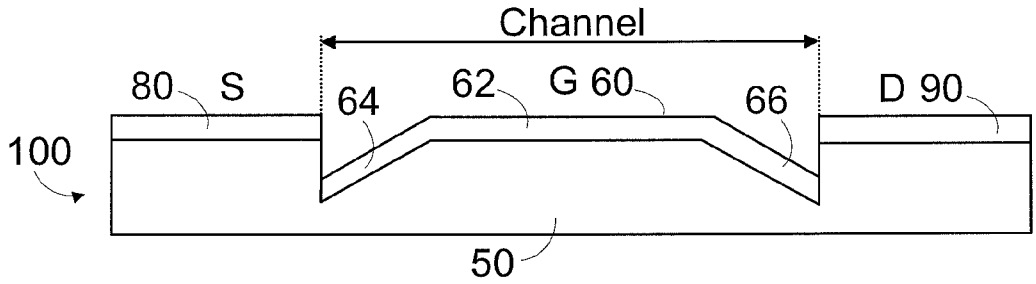



Fig. 2

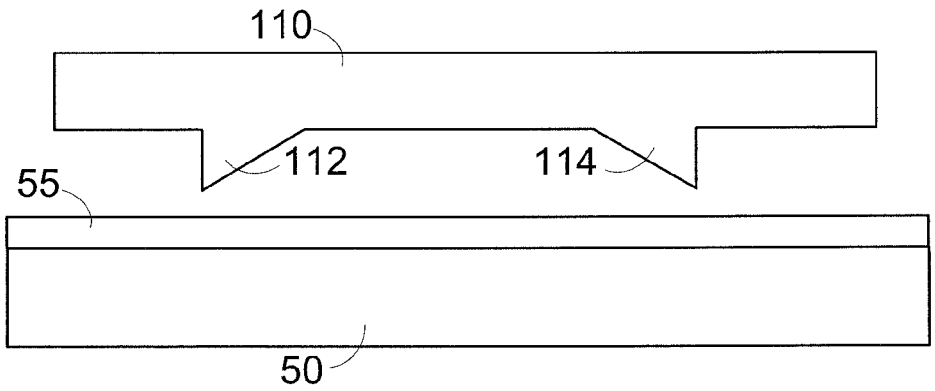



Fig. 3a

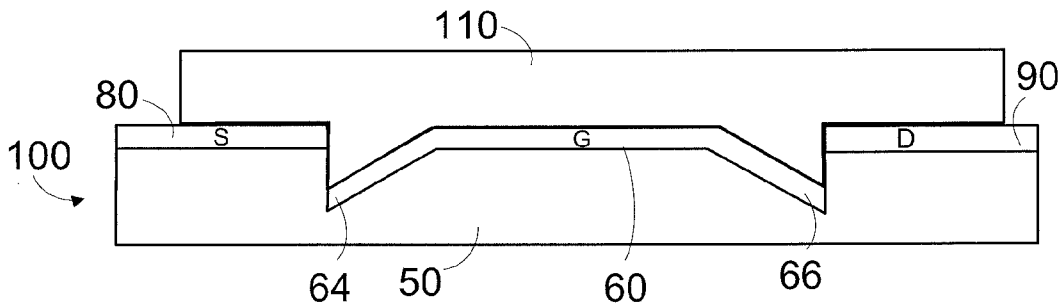



Fig. 3b

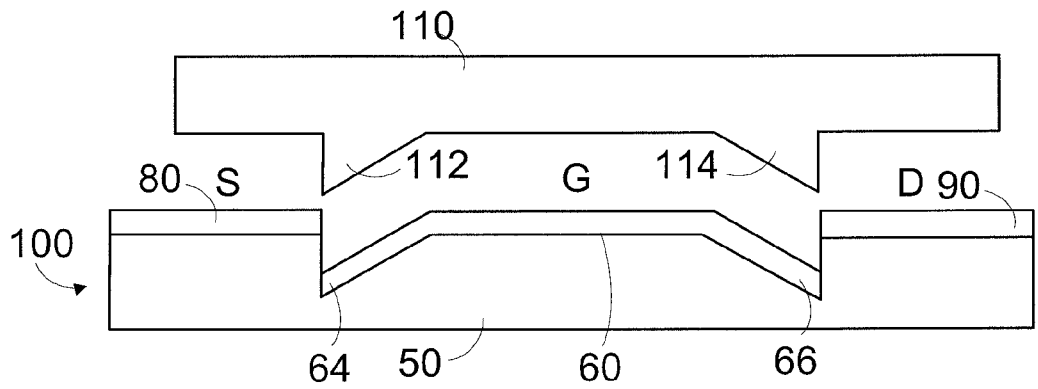



Fig. 3c

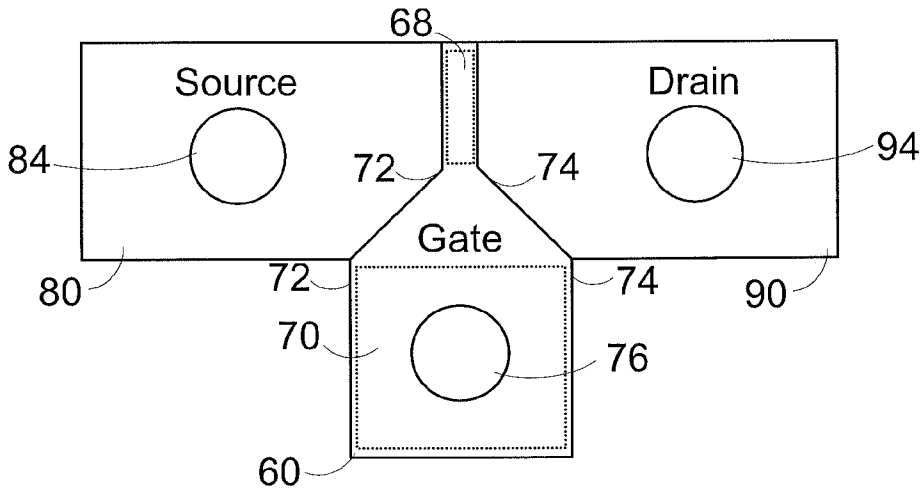



Fig. 4

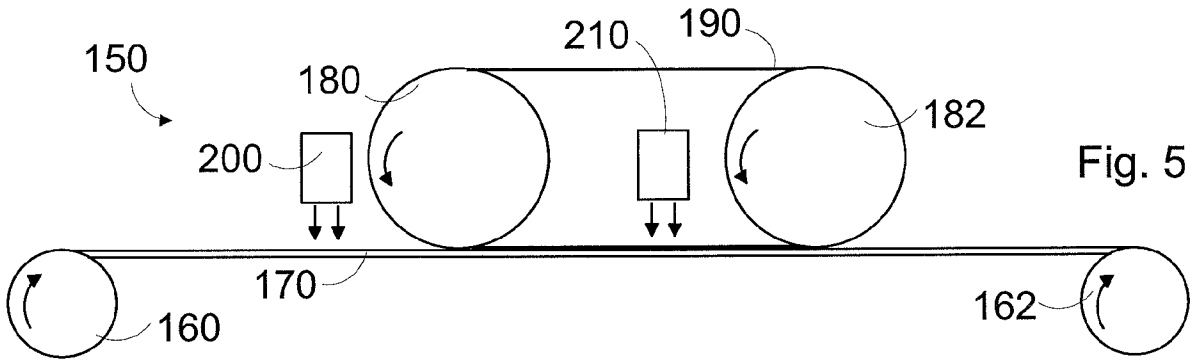



Fig. 5

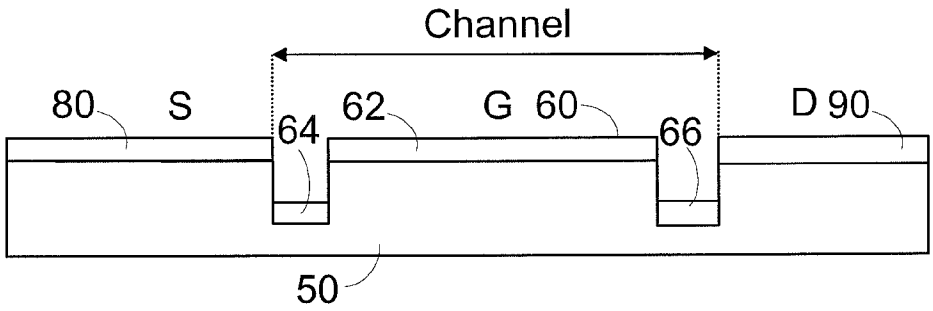



Fig. 6

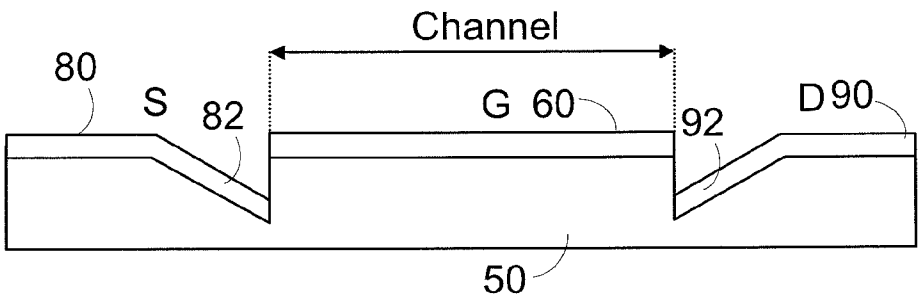



Fig. 7

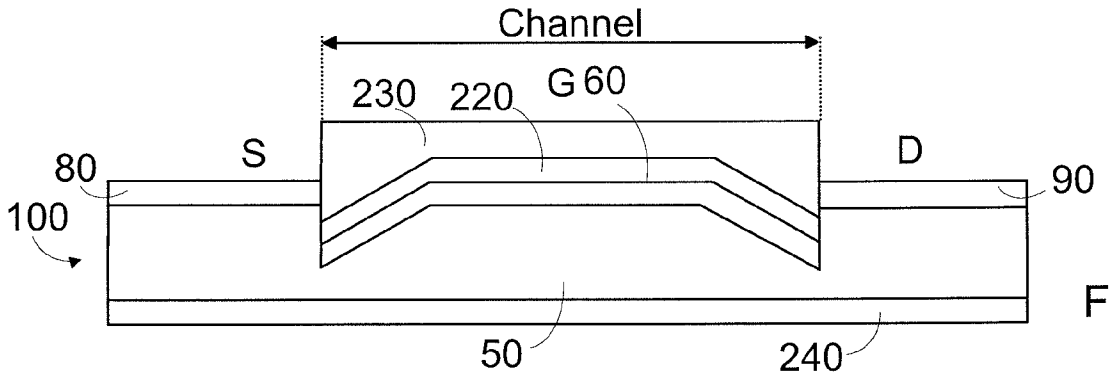

Channel
230
220
G 60
S
D
80
90
100
50
240

Fig. 8

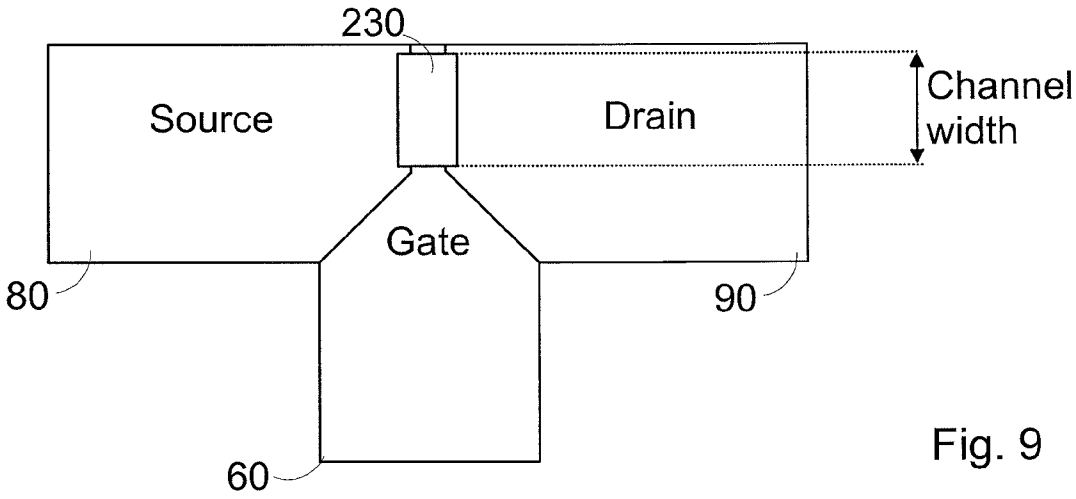

230
Source
Drain
Channel
width
Gate
80
90
60

Fig. 9

**INTERNATIONAL SEARCH REPORT**

International application No.
PCT/FI2008/050695

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

FI, SE, NO, DK

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPODOC,WPI,NPL

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 6911385 B1 (HAUBRICH SCOTT et al.) 28 June 2005 (28.06.2005), column 1 line 58 - column 2 line 39, column 6 lines 33-35 and 50-65, column 7 lines 9-40, figure 3 | 1, 7-10, 15-17, 23-25 |
| X | WO 2007074404 A2 (SUISSE ELECTRONIQUE MICROTECH et al.) 05 July 2007 (05.07.2007), page 7 lines 16-19, page 8 lines 15-25, page 15 lines 12-19, page 18 lines 11-21, figure 1a | 1, 7-10, 15-17, 23-25 |
| A | EP 1748502 A1 (SONY CORP) 31 January 2007 (31.01.2007) | |
| A | US 2006157443 A1 (MEI PING) 20 July 2006 (20.07.2006) | |
| A | US 2004075155 A1 (HUANG ZHISONG et al.) 22 April 2004 (22.04.2004) | |
| A | US 6517995 B1 (JACOBSON JOSEPH M et al.) 11 February 2003 (11.02.2003) | |

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

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"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 18 June 2009 (18.06.2009) | 02 July 2009 (02.07.2009) |


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**INTERNATIONAL SEARCH REPORT**
**Information on patent family members**

International application No.
PCT/FI2008/050695

| Patent document cited in search report | Publication date | Patent family members(s) | Publication date |
|---|---|---|---|
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| WO 2007074404 A2 | 05/07/2007 | JP 2009516382T T | 16/04/2009 |
| | | US 2009038683 A1 | 12/02/2009 |
| | | CN 101331624 A | 24/12/2008 |
| | | KR 20080073331 A | 08/08/2008 |
| | | EP 1949469 A2 | 30/07/2008 |
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| | | CN 1905131 A | 31/01/2007 |
| US 2006157443 A1 | 20/07/2006 | None | |
| US 2004075155 A1 | 22/04/2004 | None | |
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| | | AU 7372800 A | 17/04/2001 |

**INTERNATIONAL SEARCH REPORT**

International application No.
PCT/FI2008/050695

CLASSIFICATION OF SUBJECT MATTER

Int.Cl.
***H01L 21/48*** (2006.01)
***H01L 29/41*** (2006.01)