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S. G. SEM-SANDBERG ETAL

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CIRCUIT ARRANGEMENT FOR PRODUCING POTENTIALS HAVING EQUAL
ABSOLUTE VALUES BUT OPPOSITE SIGN DEPENDING
ON RECEIVED SIGNAL COMBINATIONS

Filed Aug. 22, 1961

2 Sheets-Sheet 1

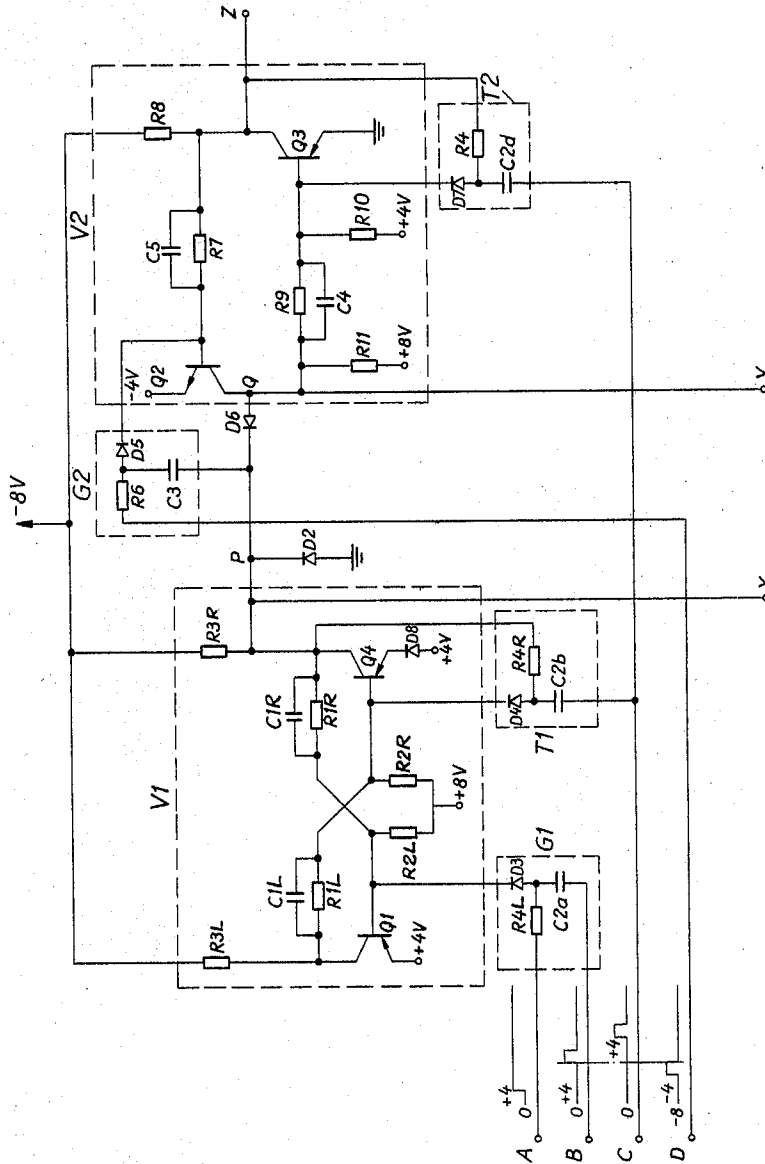


Fig. 1

INVENTORS
SVERRE GEORGE SEM-SANDBERG
PER-ARNE MANNBY

BY Hane and Nydink

ATTORNEYS

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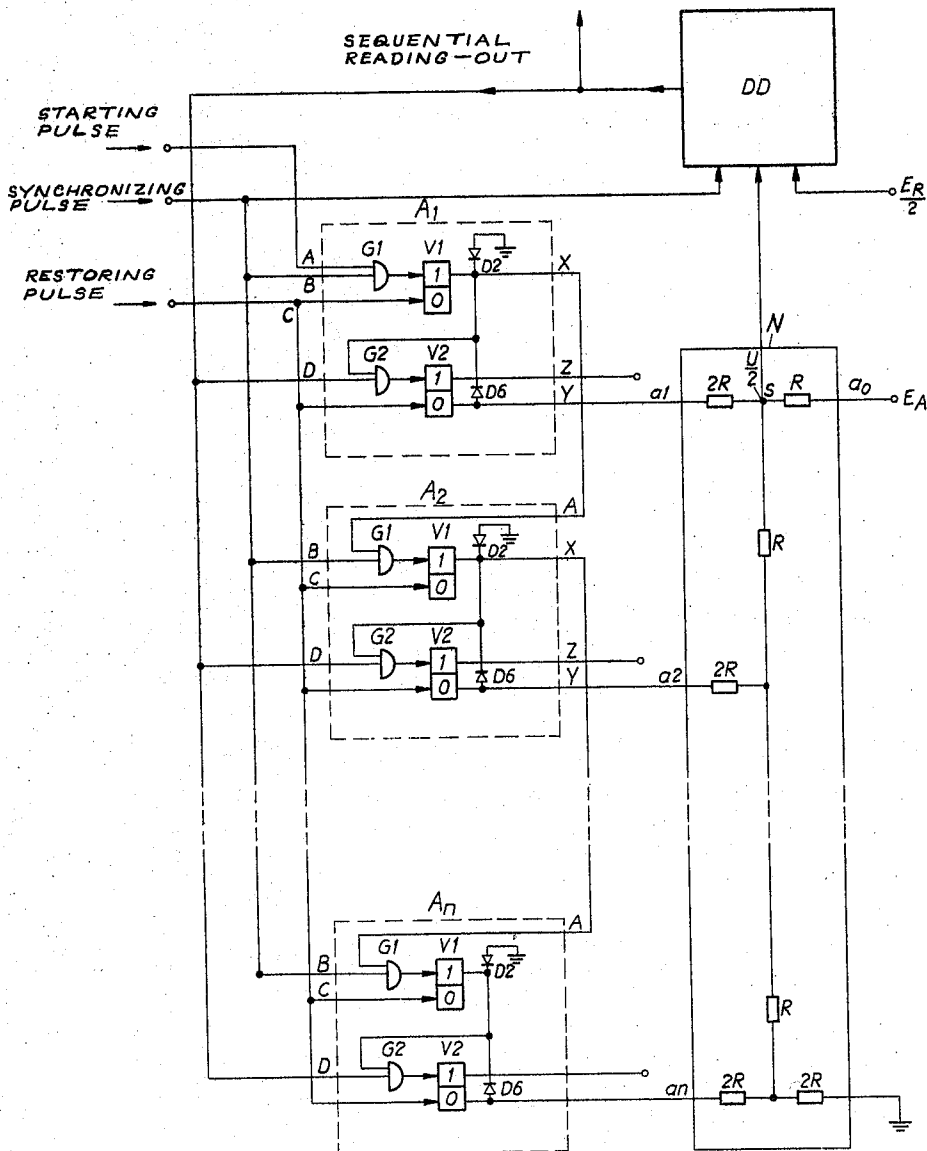


Fig. 2

INVENTORS
SVERRE GEORGE SEM-SANDBERG
PER-ARNE MANNBY

By *Hane and Nydick*
ATTORNEYS

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CIRCUIT ARRANGEMENT FOR PRODUCING POTENTIALS HAVING EQUAL ABSOLUTE VALUES BUT OPPOSITE SIGN DEPENDING ON RECEIVED SIGNAL COMBINATIONS

Sverre George Sem-Sandberg, Vendelso, and Per-Arne Mannby, Hagersten, Sweden, assignors to Telefonaktiebolaget L M Ericsson, Stockholm, Sweden, a corporation of Sweden

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5 Claims. (Cl. 307—88.5)

The present invention refers to a circuit arrangement adapted particularly for use in analog-digital converters. A purpose of the arrangement is to produce potential at an output which potentials have the same absolute value but an opposite sign when a first input signal is received alone or simultaneously with another input signal respectively and to produce a 0-potential on the same output when both signals are absent.

There are known analog-digital converters in which a reference potential in a discriminator is compared in turn at first with an analog potential, which has to be expressed as an n -digit binary number, and after this with modified potential values which are obtained by adding to said analog potential successively decreasing $\frac{1}{2}n$ portions of the reference potential with plus sign if the result of the comparison in the discriminator shows that said reference value is greater, and with minus sign if the result of the comparison in the discriminator shows that said reference value is less than said addition result.

This principle of comparison is indicated by way of example in FIG. 1a, which shows the timing sequence of a system which has a maximum deviation of $2^5-1=31$, and in which the value of an analog signal is expressed as a 5-digit binary number. Assuming that the analog value is to be 7, said value is at first compared with a reference value $2^5-1=16$. Such comparison shows that the analog value is less than 16. A 0 appears, and the reference value 2^5-2 is added to the analog value with a plus sign, making the total $7+8=15$. Since a second comparison shows that the modified analog value 15 is still less than 16, a new reference value $2^5-3=4$ is added with a plus sign to the first modified value 15, producing a second modified value 19. In the third stage the value $2^5-4=2$ is added with a negative sign, since the second modified value was greater than 16, and a third modified analog value 17 results. Finally, in the last stage, the value $2^5-5=1$ is added, also with a negative sign, producing the final modified value 16, which corresponds to the original reference level. If the modified value is less than the reference value, a 0 appears. If it is greater than or equal to the reference value, a 1 appears. The advantage with such a system is that the sum of the different operation times will be less than in analog-digital conversions systems as heretofore known.

The successively decreasing portions of the reference potential (2^{n-1} , 2^{n-2} . . .) are generally obtained on the output of a resistance network or another known potential converting network by connecting the reference potential to two successive inputs of said network. It is important in such a system not only that the reference potential is connected to said inputs in turn with plus or minus signs respectively, depending on the indication of the discriminator, but also that the respective input is maintained on zero potential before a comparison is carried out, to allow a reliable function of the device. This is due to the fact that upon deviation from zero potential on one of the non-working inputs said value would be

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added to or subtracted respectively from the potential on the output of the discriminator.

The object of the present invention is to obtain a circuit arrangement which fulfills said conditions, that is, which, depending on the signal combination obtained, produces three alternative potentials, (+E, 0, -E) on its output. Another object of the invention is to obtain a circuit arrangement or a circuit which, when connected to other identical circuits, in coaction with them forms a shift register in which upon feeding periodical pulses (said first input signal) to inputs of all the circuits, only one circuit is activated so that said potential having a plus sign, a minus sign, or being 0, depending on the indication of the discriminator, appears on successive outputs.

The circuit arrangement according to the invention comprises two bistable flip-flops of transistor type, the first of which is operable by said first signal so as to be brought to working condition and the second of which is operable by said second signal so as to be brought to working condition. Said second flip-flop has a transistor electrode which conducts only in the active condition of the flip-flop and is connected to the output of the circuit arrangement and also through a non-linear element, for example a diode, to a transistor electrode in said first flip-flop, which electrode conducts only in the working condition of said first flip-flop. The non-linear element is connected to such potential in a manner such that it connects the output to said electrode in said first flip-flop when said electrode has 0-potential defined by the blocked condition due to the fact that said electrode is connected to ground through another non-linear element, and also when the electrode has a potential defined by the conducting condition of the transistor and different from 0-value. A gate circuit is furthermore connected to said first-mentioned non-linear connecting element which gate circuit upon receiving said second signal deblocks the transistor connected to the output and simultaneously blocks said first-mentioned non-linear element so that the output is disconnected from the potential of said electrode in the first flip-flop and obtains the potential of said electrode of the second flip-flop, said potentials being equal but having opposite signs.

The invention will be explained more in detail with reference to the enclosed drawing. FIG. 1 shows a circuit arrangement according to the invention and FIG. 2 shows the use of the circuit arrangement in a shift register for analog-digital converters.

FIG. 1 shows a circuit arrangement according to the invention comprising two bistable flip-flops V1 and V2. The device has four inputs A, B, C and D, each arranged for an incoming signal, and three outputs Y, X and Z. The Y output has a potential depending on the combination of received input signals. The X output delivers a signal whenever the circuit has operated and is used when the circuit is included in a plurality of similar circuits to form a shift register. The Z output is used when parallel read out of a plurality of similar circuits is required. Both shift register operation and parallel read out will hereinafter be more fully described with respect to FIG. 2.

In the embodiment shown in FIG. 1, flip flop V1 is a conventional transistor flip-flop comprising two pnp-transistors Q1 and Q4. The transistors are interconnected to form a conventional bistable circuit wherein, at any one time, one of the transistors is conducting and the other cut off. The conducting states of the transistors can only be changed by external triggers. In particular, the 0-condition of flip-flop V1 is when transistor Q1 conducts and transistor Q4 is cut off. The 1-condition of the flip-flop is when transistor Q1 is cut off and transistor Q4 conducts. The second flip-flop V2 is also a bistable circuit and is according to a preferred embodiment a so-called

"Hook" type flip-flop. In such a flip-flop two complementary transistors are employed. In one stable state, both transistors are conducting (the 1-condition) while in the other stable state (the 0-condition) both transistors are cut-off. Flip-flop V2 comprises npn-transistor Q2 and pnp-transistor Q3 suitably interconnected. The flip-flop V2 does not need to be a flip-flop of the Hook type, but the advantage of a flip-flop of the Hook type will be that it does not conduct current at all in rest position (the 0-condition when both transistors are cut-off), and that the collector potential of the one transistor will be more negative and the collector potential of the other transistor will become more positive upon activation. This can be used for obtaining suitable potential levels on the outputs, as will appear from the description.

The flip-flops are brought to working condition in response to certain conditions on the inputs of the circuit arrangement. When both flip-flops are in inactive or 0 condition, only the transistor Q1 is conducting. Assume transistor Q1 is conducting. Therefore, its collector is substantially at +4 volts. By virtue of the potential divider action of resistors R1L and R2R with resistor R2R connected to +8 volts, the base of transistor Q4 is at a higher potential than its emitter. Accordingly, transistor Q4 is cut off. With transistor Q4 cut off its collector is substantially at ground potential. The clamping action of diode D2 having its anode connected to ground and its cathode connected to the collector prevents the point P from going below ground potential. By virtue of the potential divider action of resistors R1R and R2L with resistor R2L connected to +8 volts the voltage of the base of transistor Q1 is considerably less than +4 volts (the emitter voltage). Accordingly, transistor Q1 remains conducting. It should be noted that capacitors C1L and C1R are merely conventional "speed-up" capacitors. Flip-flop V1 remains in the 0-condition until a sufficiently positive pulse is transmitted from gate G1 via diode D3 to the base of transistor Q1.

Now, consider flip-flop V2. The initial or 0-condition of flip-flop V2 is when both transistors Q2 and Q3 are cut off. Assume transistor Q2 is cut off. The emitter of transistor Q2 is at ground potential. Note transistor Q4 is cut off and returned via resistor R3R to -8 volts, but diode D2 clamps the voltage at point P to ground. The potential divider action of resistors R9 and R10 connected between point Q and +4 volts maintains the base of transistor Q3 above ground (the emitter voltage). Transistor Q3 is cut off and its collector is connected via resistor R8 to a -8 volt potential. Therefore, the base of transistor Q2 is below -4 volts (the emitter voltage) and transistor Q2 is cut off. Capacitors C4 and C5 are merely "speed-up" capacitors.

It has been shown that the initial condition of the flip-flops is such that only transistor Q1 conducts. How the initial condition is obtained by external triggers from circuits T1 and T2 connected respectively to the bases of transistors Q4 and Q3 will hereinafter be described. The subsequent operation of the circuit, once initiated in response to triggers from circuits T1 and T2 will now be described.

The circuit yields a first indication (a positive polarity signal on output Y) if it is triggered by only one signal, and a second indication (a negative polarity signal on output Y) if it is triggered by the first signal while also being triggered by a second signal (a signal on input D). The circuit also yields a zero signal on output Y if it has received no input signals.

The signal on input B passes through gate G1 to the base of transistor Q1. It is possible that if the amplitude of a positive going pulse at input B is sufficiently high, the output of gate G1 is sufficiently positive to raise the voltage of the base of transistor Q1 to higher than +4 volts cutting off transistor Q1. However, because the circuit is one stage of the shift register shown in FIG. 2, wherein each stage has an input B to receive synchronizing pulses,

gate G1 has a control input connected to input A. Input A is connected to the preceding stage of the shift register. In this way, sequential operation of the stages is insured. With this in mind, when input A is at +4 volts indicating the preceding stage has registered, the voltage at the junction of diode D3 and resistor R4L is raised and when a four volt positive synchronizing pulse is received at input D, diode D3 transmits a positive pulse which back biases the emitter-base junction of transistor Q1. Transistor Q1 cuts off. Its emitter goes to about -8 volts. The voltage at the base of transistor Q4 drops below +4 volts. Transistor starts conducting and its collector goes to about +4 volts. The voltage on output X rises from ground potential to +4 volts indicating the circuit has registered.

It should be noted that diode D6 connects the collector of transistor Q4 to point Q which is connected to output Y with the cathode of diode D6 connected to the collector of transistor Q4. While flip-flop V1 is in the 0-condition, point Q and output Y are at zero potential. At that time transistor Q4 is cut off. Therefore, current flows from +8 volts via resistor R11, diode D6 and resistor R3R to -8 volts. Diode D2 clamped point P to ground and therefore point Q is effectively at ground potential. When flip-flop V1 is in the 1-condition, the collector of transistor Q4 and point P are at about +4 volts. Hence, point Q is also at +4 volts. It is, therefore, seen that with the flip-flops in the 0-condition and no input signal is received the output Y is at zero potential and when a signal is received at input B the output Y is at a +4 volt potential. The third state is when signals are substantially simultaneously received at inputs B and D and is indicated by a -4 volt potential on output Y. This state will now be discussed.

Assume flip-flops V1 and V2 are in the 0-condition and pulses substantially simultaneously occur on inputs B and D. The pulse at input B triggers flip-flop V1 to the 1-condition as previously described. The pulse on input D passes via resistor R6 to the anode of diode D5. At the same time, point P (connected to the collector of transistor Q4) shifts to a +4 volt potential by virtue of flip-flop V1 being triggered to the 1-condition. The positive going transient at the point P passes through capacitor C3 to the anode of diode D5 where it cooperates with the signal from input D to pass a positive going pulse to the base of transistor Q2. Transistor Q2 starts conducting and its collector drops to -4 volts (the emitter voltage). The drop in the collector voltage is transferred via resistor R9 and capacitor C4 to the base of transistor Q3 turning this transistor on. The collector of transistor Q3 goes to ground potential. The collector voltage is fed via resistor R7 and capacitor C5 to the base of transistor Q2 locking the latter in the on condition. Accordingly, flip-flop V2 is set to the 1-condition with output Y at -4 volts. Diode D6 is back biased and flip-flop V2 is isolated from flip-flop V1. Hence, when two input pulses or signals are simultaneously received the circuit gives a third indication represented by a negative voltage at output Y.

The flip-flops V1 and V2 are restored, or set to the 0-condition by a pulse on input C fed to circuits T1 and T2. When the flip-flop V1 is in the 1-condition, its collector voltage is at about +4 volts. This potential is connected via resistor R4R to the anode of diode D4. When a +4 volt pulse is present on input C it passes via capacitor C2b to the anode of diode D4. The anode voltage is then sufficiently high to pass a positive pulse of sufficient amplitude to back bias the base-emitter junction of transistor Q4. Transistor Q4 cuts off and its emitter voltage drops to substantially ground potential causing the turning on of transistor Q1. Similarly, when flip-flop V2 is in the 1-condition, ground potential is fed from the collector of transistor Q3 via resistor R4 to the anode of diode D7. The pulse on input C passes through capacitor C2d and cooperates with the voltage from the collector

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to pass a sufficiently positive pulse to cut off transistor Q3. The collector of transistor Q3 goes to -8 volts and this voltage is fed to the base of transistor Q2 which cuts off. Flip-flop V2 is thus restored to the 0-condition.

It should thus be noted that the potential on output X indicates whether the circuit has been triggered and the output Z transmits a voltage which is utilizable in parallel readout when the circuit is included in a chain of similar circuits to provide a shift register.

FIG. 2 shows the use of a circuit arrangement according to the invention in an analog-digital converter which has the purpose of expressing by comparison with a reference value, an analog potential as an n -digit binary number, as is explained hereinbefore in connection with FIG. 1a. In a discriminator DD at first the analog potential $E_A = 7V$ according to the example is compared with a reference potential, the value of which is 2^{n-1} , that is approximately half the whole possible indication and ($E_p = 16V$ according to the example). If the comparison shows that the analog potential was greater (for instance, if the discriminator produces a signal), "1" is recorded for the first position, and if it was less (if the discriminator does not generate a signal), "0" is recorded. After this a comparison is carried out between said reference value and the sum U of the analog potential and the $\frac{1}{2}$ reference potential, which latter has been added to the analog potential with a sign depending on the preceding comparison, that is with plus in the present case, as the preceding comparison $7 < 16$ has resulted in 0. The sign would be minus if the preceding comparison had resulted in 1. Corresponding to the comparison result ($15 < 16$) in the second digit position 0 is recorded, after which the comparison continues between the reference potential and the sum of the analog potential and the $\frac{1}{4}$ portion ($4V$) of the reference potential, the sign of the latter being dependent again on the preceding comparison result, and the comparison continues until the last digit has been defined.

In order to carry out such a conversion it is necessary to provide in addition to a discriminator a device which depending on each indication of the discriminator (signal or no signal respectively) produces a $\frac{1}{2} n-2$ portion of the reference potential (the value of the reference potential is 2^{n-1} and the $\frac{1}{2}$, $\frac{1}{4}$, $\frac{1}{8}$ a.s.o. portion should be produced) with a sign (plus or minus) defined by the said indication to be used when adding said portion to the analog potential so that the next comparison is carried out in the discriminator between said sum and the reference potential. Generally the conversion is carried out by means of a number of separate converting stages, corresponding to the number of comparisons which have to be carried out. Said stages each produce a value of the reference potential corresponding to the position of the stage. The circuit arrangement according to the invention when used as a converting stage renders an analog-digital converter more simple. Furthermore it will allow obtaining an n -digit binary number by means of only $n-1$ comparison stages.

For producing the $\frac{1}{2} n-1$ portions of the reference potential, a resistance network N known per se and formed by links comprising resistances of the values R and $2R$ is used. It is easy to show that when connecting the reference potential to one of the inputs a_1-a_n and connecting the analog potential to the input a_0 in the point S, the sum of the analog potential E_A and of the portion of the reference potential E_R corresponding to the respective input (upon connection to the input a_1 $\frac{1}{2} E_R$, upon connection to the input a_2 $\frac{1}{4} E_R$, and so on) is obtained. To said inputs has to be fed the reference potential with a sign defined by the preceding comparison in the discriminator. As mentioned before, it is important not only that the reference potential is connected to the inputs, but also that said inputs have exactly 0-potential before they obtain $+E_R$ or $-E_R$ respectively. This is necessary to prevent the potential of non-working inputs

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being added to the potential of the working input. The circuit according to the invention is particularly suitable for the purpose.

As shown in FIG. 2, to each input of the converting network N belongs a converting stage A_1, A_2 and so on, each consisting of a circuit according to the invention, said stages together forming a shift register. This circuit gives different indications, depending upon whether one or two signals are coming in at the same time. All the stages are fed by synchronizing pulses, while a pulse from the discriminator is obtained only when a comparison between the reference potential E_R and the sum of the analog potential E_A and the $\frac{1}{2} n-2$ portions of the reference potential shows that the reference potential has been less in value. If the reference potential has greater value, then there will be no sign.

The circuits A_1 and A_2 correspond to the circuit arrangement according to FIG. 1 in which the respective parts are replaced by logical symbols having the same reference numerals. The input A in the first stage is connected to a starting pulse source, while the inputs A in the other stages are connected to the output X in the preceding stage, the inputs B are connected to a source of synchronizing pulses, the inputs C are connected to a source of restoring pulses, and the inputs B are connected to the output of the discriminator.

When the analog-digital converter receives a synchronizing pulse, this pulse is fed simultaneously to all the stages in the shift register and to the discriminator, as the presence of the synchronizing pulse is the condition that the discriminator and the converting stages should begin to function. When the discriminator gives an indication depending upon whether the analog voltage respectively its altered value U is greater than the reference potential, a pulse will occur on the input D of the first stage at the same time as a pulse occurs on the input B. As mentioned before, the starting of the flip-flop V1 depends on a further condition, that is, that a signal occurs on the input A. Said condition is used in the device according to FIG. 2 in order to make the first stage ready by means of a starting signal respectively for rendering the function of the subsequent stages dependent upon the fact that the preceding stage has carried out its function. When a pulse has been obtained on the input D, both the flip-flops V1 and V2 in the first stage are operated so that on the output a_1 the reference potential is obtained with a negative sign. If the discriminator does not produce any signal due to the fact that the analog potential respectively its altered value was less than the reference potential, only the flip-flop V1 will be operated so that on the output the reference potential is obtained with plus sign.

As mentioned before, the output X obtains a definite potential as soon as the stage has been operated. This can be used also for operating the stages as a shift register in which always the next stage only is operated when a synchronizing pulse is fed to the inputs of all the stages. As according to the embodiment the function of the flip-flop V1 depends on the fact that a signal is present on the input A, it will be possible to cause a starting condition in the next stage only in turn.

The reading out of the comparison result in the form of an n -digit binary number can be carried out on the output of the discriminator sequentially in step with the synchronizing pulses. The invention allows also parallel reading out through the outputs Z which have zero potential if the comparison has resulted in a "1" (the output Y is negative) in the respective stage, whereas they have negative potential if the comparison has resulted in a "0" (the output Y is positive). One of the reasons that the flip-flop V2 is a flip-flop of the Hook type is that the "1"-signal obtained from the transistor Q3 to be more positive than the "0"-signal at the same time as the signal obtained from the transistor Q2 has to be more negative when "1" is indicated as should be clear from the description. The reading out of the condition of the flip-flops

V2 in all the stages is carried out by means of a synchronizing pulse after the stages have been operated by the preceding synchronizing pulses in a manner known per se, after which all the stages are restored to non-working condition by means of a restoring pulse which is fed to the inputs C.

We claim:

1. A circuit adapted to receive first and second signals for producing a ground potential signal when no signals are received, a signal having a first potential of given polarity and amplitude when only said first signal is received, and a signal having a second potential of said given amplitude and an opposite polarity when said first and second signals are substantially simultaneously received, said circuit comprising: a source of voltage having a first voltage output terminal for transmitting said ground potential, a second voltage output terminal for transmitting said first potential, a third voltage output terminal for transmitting said second potential, a fourth voltage output terminal for transmitting a potential of the same polarity and greater amplitude than said first potential, and a fifth voltage output terminal for transmitting a potential of the same polarity and greater amplitude than said second potential; a first bistable circuit including first and second transistors each having emitter, collector and base electrodes, means for regeneratively interconnecting said first and second transistors, means for connecting electrodes of said first transistor to voltage output terminals of said source of voltage for energizing said first transistor, resistor means for connecting the collector electrode of said second transistor to said fifth voltage output terminal, means for connecting the emitter electrode of said second transistor to said second voltage output terminal; means adapted to receive said first signal for triggering said first bistable circuit to a first stable state wherein at least said second transistor is conducting; a second bistable circuit including third and fourth transistors each having emitter, collector and base electrodes, means for regeneratively interconnecting said third and fourth transistors, means for connecting electrodes of said fourth transistor to voltage output terminals of said source of voltage for energizing said fourth transistor, resistor means for connecting the collector electrode of said third transistor to said fourth voltage output terminal, means for connecting the emitter electrode of said third transistor to said third voltage output terminal; gating means including a first input adapted to receive said second signal and a second input connected to the collector electrode of said second transistor for triggering said second bistable circuit to a first stable state wherein at least said third transistor is conducting when said second signal is received substantially simultaneously with the triggering of said first bistable circuit to said first stable state; a first unilateral conducting device connecting the collector electrodes of said second and third transistors; a second unilateral conducting device connecting the collector electrode of said second transistor to said first voltage output terminal for clamping the potential of the emitter electrode of said second transistor to ground potential; and a signal output terminal connected to the collector electrode of said third transistor for transmitting the ground potential signal when neither of said bistable circuits is in a first stable state, the first potential signal when only said first bistable circuit is in a first stable state, and the second potential signal when both of said bistable circuits are in the first stable state.

2. The circuit of claim 1 further comprising a further output terminal connected to the collector electrode of said second transistor for transmitting said first potential signal when said first bistable circuit is in said first stable state and for transmitting a ground potential signal when said first bistable circuit is in the other stable state.

3. The circuit of claim 1 further comprising means including an input adapted to receive a restoring signal and

an output connected to the base electrodes of said second and fourth transistors for triggering said first and second bistable circuits to a second stable state.

4. The circuit of claim 1, wherein said third and fourth transistors are complementary so that in the first stable state of said second bistable circuit both of said transistors conduct and in the other stable state of said second bistable circuit both of said transistors are cut off.

5. A two stage sequentially operable circuit for storing two bits of information represented by signals comprising:

a source of periodically occurring synchronizing pulses, a source of pulses representing the information to be stored,

first and second storage circuits, each of said storage circuits receiving first and second signals for producing a ground potential signal when no signals are received, a signal having a first potential of given polarity and amplitude when only said first signal is received, and a signal having a second potential of said given amplitude and an opposite polarity when said first and second signals are substantially simultaneously received, each of said storage circuits comprising: a source of voltage having a first voltage output terminal for transmitting ground potential, a second voltage output terminal for transmitting said first potential, a third voltage output terminal for transmitting said second potential, a fourth voltage output terminal for transmitting a potential of the same polarity and greater amplitude than said first potential, and a fifth voltage output terminal for transmitting a potential of the same polarity and greater amplitude than said second potential; a first bistable circuit including first and second transistors each having emitter, collector and base electrodes, means for regeneratively interconnecting said first and second transistors, means for connecting electrodes of said first transistor to voltage output terminals of said source of voltage for energizing said first transistor, resistor means for connecting the collector electrode of said second transistor to said fifth voltage output terminal, means for connecting the emitter electrode of said second transistor to said second voltage output terminal; first gating means including a first input adapted to receive a D.C. signal, a second input for receiving said synchronizing pulses and an output for transmitting a signal when said D.C. signal and a synchronizing pulse are simultaneously present at said inputs for triggering said first bistable circuit to a first stable state wherein at least said second transistor is conducting; a second bistable circuit including third and fourth transistors each having emitter, collector and base electrodes, means for regeneratively interconnecting said third and fourth transistors, means for connecting electrodes of said fourth transistor to voltage output terminals of said source of voltage for energizing said fourth transistor, resistor means for connecting the collector electrode of said third transistors to said fourth voltage output terminal, means for connecting the emitter electrode of said third transistor to said third voltage output terminal; second gating means including a first input adapted to receive said pulses representing the information to be stored and a second input connected to the collector electrode of said second transistor for triggering said second bistable circuit to a first stable state wherein at least said third transistor is conducting when a pulse representing the information to be stored is received substantially simultaneously with the triggering of said first bistable circuit to said first stable state; a first unilateral conducting device connecting the collector electrodes of said second and third transistors; a second unilateral conducting device

connecting the collector electrode of said second transistor to said first voltage output terminal for clamping the potential of the emitter electrode of said second transistor to ground potential; a signal output terminal connected to the collector electrode of said third transistor for transmitting the ground potential signal when neither of said bistable circuits is in a first stable state, the first potential signal when only said first bistable circuit is in a first stable state, and the second potential signal when both of said bistable circuits are in the first stable state; and a D.C. signal output terminal connected to the collector electrode of said second transistor for transmitting a D.C. signal when said first bistable circuit is in said first stable state,

means for connecting the D.C. signal output terminal of said first storage circuit to the first input of the first gating means of said second storage circuit,

and means for transmitting a D.C. signal to the first input of the first gating means of said first storage circuit.

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ARTHUR GAUSS, *Primary Examiner*.

JOHN W. HUCKERT, *Examiner*.