Oct. 18, 1960 E. W. MANTEUFFEL 2,957,122

TEMPERATURE COMPENSATED VOLTAGE STABILIZER

Filed June 30, 1955

FIG.1.

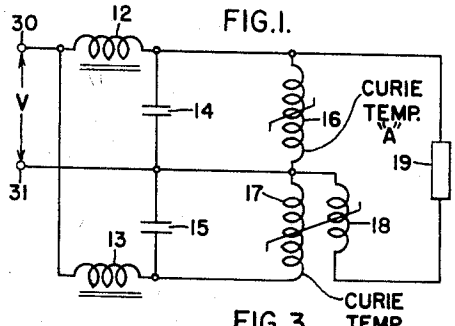


FIG.2.

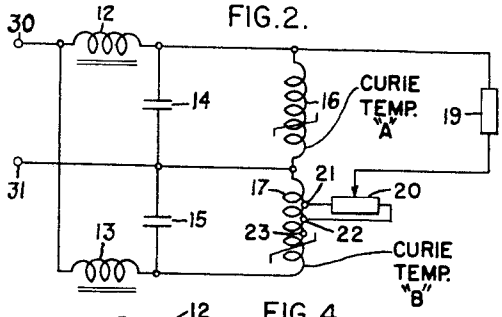


FIG.3.

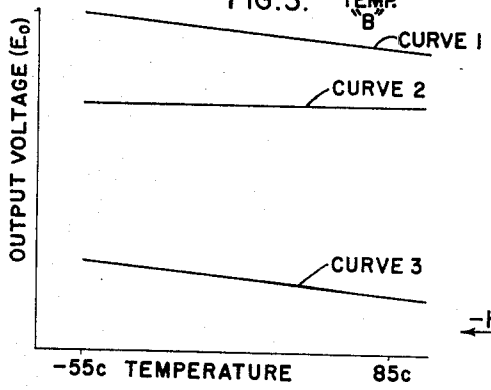


FIG.4.

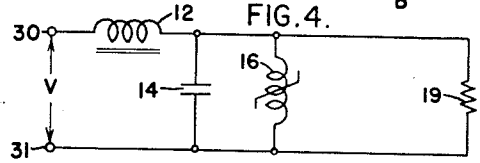


FIG.5.

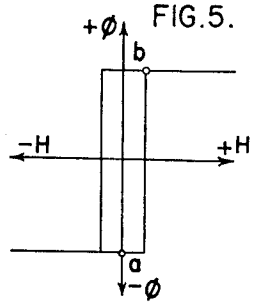


FIG.11.

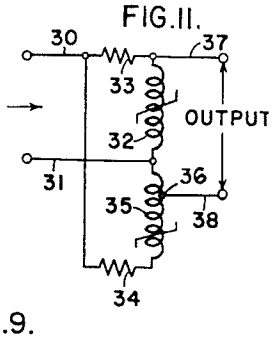


FIG.6.

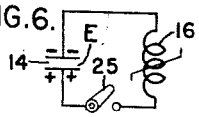


FIG.7.

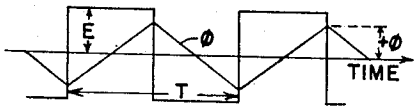


FIG.8.

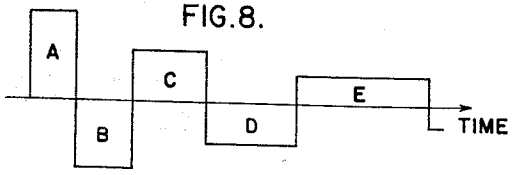


FIG.9.

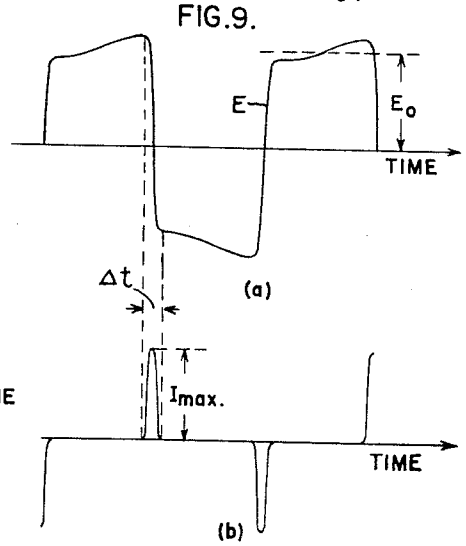
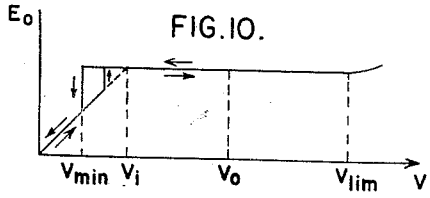


FIG.10.



INVENTOR:
ERICH W. MANTEUFFEL,
BY George Wiltgrath
HIS ATTORNEY.

United States Patent Office 2,957,122
Patented Oct. 18, 1960

2,957,122

TEMPERATURE COMPENSATED VOLTAGE STABILIZER

Erich W. Manteuffel, Ithaca, N.Y., assignor to General Electric Company, a corporation of New York

Filed June 30, 1955, Ser. No. 519,180

16 Claims. (Cl. 323—70)

This invention relates to magnetic voltage stabilizer circuits and more particularly to temperature compensating circuits of this character.

Magnetic materials have been developed which have a substantially rectangular magnetization curve making them suitable for use in voltage or current stabilization. In many cases, the effectiveness of magnetic materials used in stabilizer circuits will depend largely upon their ability to maintain a constant saturation flux density. Since all magnetic materials exhibit the property of a decreasing saturation flux density with increasing temperature until their Curie point is reached, i.e. they become non-magnetic, temperature compensation must be provided for the stabilizer to operate properly. Prior art disclosures have provided this compensation by means of series or parallel combinations of resistors with either negative or positive coefficients of temperature. Compensation achieved by these methods is limited to a relatively narrow range of temperature variations because of the non-linearities inherent in the temperature responsive elements used and their adverse effects upon load circuits.

It is an object of this invention to provide a new and improved magnetic voltage stabilizer circuit.

A further object of this invention is to provide a new and improved magnetic temperature compensation means for magnetic voltage stabilizer circuits.

Another object of this invention is to provide magnetic temperature compensation for voltage stabilizer circuits which gives excellent results over wide temperature ranges.

A further object of this invention is to provide a temperature compensated magnetic voltage stabilizer which is small, compact and durable.

Another object of the present invention is to provide a new and improved temperature compensated magnetic voltage stabilizer which combines simple and rugged construction with efficient operation.

This invention provides a new type of temperature compensation for magnetic voltage stabilizers which employs two saturable reactors having different Curie temperatures. This method of compensation gives excellent results over wide temperature ranges and eliminates the disadvantages associated with prior art disclosures.

These and other advantages of the invention will be more clearly understood from the following description taken in connection with the accompanying drawings, and its scope will be apparent from the appended claims.

In the drawings:

Fig. 1 is a diagrammatic illustration of one embodiment of the invention;

Fig. 2 is a diagrammatic illustration of another embodiment of the invention;

Fig. 3 shows curves which are representative of the output voltage vs. temperature characteristics of the saturable reactors used in the invention;

Fig. 4 is a diagrammatic illustration of the basic stabilizer circuit used in the invention;

Fig. 5 is an idealized hysteresis loop curve of saturable core material of the type used in this invention;

Fig. 6 is a diagrammatic non-linear oscillating circuit incorporating a saturable reactor;

Fig. 7 shows the voltage-time and flux-time relationships for the circuit of Fig. 6 (no loss condition);

Fig. 8 shows a curve representing the voltage-time relationship for the circuit of Fig. 6 considering losses;

Fig. 9 shows curves for the voltage across the capacitor and the current through the saturable reactor of the basic stabilizer shown in Fig. 4;

Fig. 10 shows the output voltage vs. input voltage for the basic stabilizer circuit of Fig. 6;

Fig. 11 shows a schematic diagram of another embodiment of the invention.

In the specification, for purposes of simplicity, like elements are designated with like reference characters.

Fig. 1 illustrates one embodiment of the new type of temperature compensation employed by this invention. It consists of a non-linear oscillating circuit having a capacitance **14** and a saturable reactor **16** and a serially connected choke coil **12**. These elements are connected to input terminals **30** and **31**. A second non-linear oscillating circuit having a capacitance **15** and a saturable reactor **17** with a secondary winding **18** and a serially connected choke coil **13** are also connected across input terminals **30** and **31**. An alternating current supply voltage V is fed to this circuit across input terminals **30** and **31**. A load circuit **19** is connected across saturable reactor **16** and the secondary winding **18** of saturable reactor **17**.

Fig. 2 shows another embodiment of the invention in which the secondary winding **18** of saturable reactor **17** is replaced by a series of taps **21**, **22** and **23** on saturable reactor **17**. A variable resistance **20** is also shown which is connected to the variable taps.

In order to better comprehend the invention as embodied in Figs. 1 and 2, reference will be made to the operation of the basic stabilizer circuit shown in Fig. 4 and used in the invention. The basic stabilizer circuit shown in Fig. 4 consists of a choke coil **12** serially connected to a non-linear oscillating circuit having a capacitance **14** and a saturable reactor **16**. A varying input voltage V is applied to this circuit at input terminals **30** and **31**, and a load **19** which may comprise a resistance is connected across saturable reactor **16**. The core material of saturable reactor **16** has a substantially rectangular hysteresis loop such as shown in Fig. 5.

For a better understanding of the basic stabilizer circuit shown in Fig. 4, the operation of the non-linear oscillating circuit shown in Fig. 6 should be considered. Fig. 6 shows the non-linear oscillating circuit comprising capacitor **14** and saturable reactor **16**, and includes a switch **25**. It will now be assumed that the capacitor **14** has been charged to a voltage E as indicated in Fig. 6 and that this charge has built up previously the negative saturation flux, minus ϕ in the coil with an instantaneous working point of the coil being assumed to be at point *a* (see Fig. 5). If switch **25** is then closed with these conditions, the voltage E is applied to the saturable reactor **16**. A small magnetizing current is drawn from the capacitor which is given by the coercive force of core material, and the voltage E changes the flux of saturable reactor **16** from $-\phi$ to $+\phi$. Assuming that the magnetizing current furnished by capacitor **14** is negligibly small, the voltage E will remain substantially constant

during the flux change in saturable reactor 16. When the flux ϕ of saturable reactor 16 reaches point b on the magnetization curve shown in Fig. 5, the magnetization curve of saturable reactor 16 abruptly flattens out. A short, peaked pulse of current occurs during the discharge of capacitor 14. Assuming that the time of discharge of capacitor 14 is infinitely small and that no losses occur within the circuit during the transient, the voltage and flux oscillate as shown in Fig. 7. Since internal losses occur within practically realizable networks, the voltage E on capacitor 14 in Fig. 6 decreases with each reversal in charge, as shown in Fig. 8. However, the areas A, B, C, D and E as shown in Fig. 8 must remain equal since the total amount of flux change must be constant. Therefore, the frequency of oscillation decreases with each change in polarity of the voltage on capacitor 14.

To obtain continuous operation, the basic stabilizer circuit shown in Fig. 4 is utilized. An alternating current voltage V is applied through an inductance 12 to the non-linear oscillatory circuit in which the loss occuring during an operating half-cycle of the non-linear oscillating circuit is furnished by the supply source during the following half cycle. Fig. 9 shows the voltage E across capacitor 14 and the current through saturable reactor 16 of the basic stabilizer when operated from an alternating current source. The voltage curve E deviates slightly from the ideal rectangular shape due to the fact that the loss in voltage during transients has to be regained in periods between succeeding transients, and that the time Δt of the transients is of finite duration. As previously explained, the current which flows through saturable reactor 16 comprises a series of peaked pulses which occur almost simultaneously with the change in polarity of the charge on capacitor 14.

The basic stabilizer shown in Fig. 4 offers excellent voltage stabilization for large excursions of input voltage as is evidenced by the output voltage vs. input voltage curve shown in Fig. 10. As the input voltage V is increased to the ignition point V_1, the output voltage E_0 also increases until it levels off at the ignition point. Due to a slight decrease in series inductance 12 with rising input voltage, the circuit actually jumps into ignition slightly before point V_1 is reached. The output voltage then remains substantially constant until point V_{lim} is reached which indicates that thereafter the limiting action begins failing. As the input voltage V is decreased, the output voltage remains substantially constant until point V_{min} is reached, at which instant the circuit ceases oscillating and E_0 jumps down. Point V_0 represents the ideal operating point on the curve for the basic stabilizer.

The inductance 12 of the basic stabilizer might be replaced by a resistance. However, the performance and efficiency of the circuit would be less satisfactory because of the lack of inductive reactance furnished by the choke 12 and the losses in such resistance.

As will be apparent from the foregoing explanation, the constant output voltage of the basic stabilizer depends largely on maintaining a constant saturation flux density in the core materials used for the saturable reactor of the stabilizer. Since all magnetic materials have the property of decreasing saturation flux density with increasing temperature, some type of compensation must be provided in order that the basic stabilizer will provide the desired constant output voltage. For example, the output of a stabilizer having a saturable reactor using an Orthonal or Deltamax core decreases .07 percent per degree centigrade over the range −55° C. to +100° C. in nearly a linear fashion. This may be compensated for by providing a fixed load with a serially connected temperature-responsive device such that as the core temperature increases, the resistance of the temperature responsive device decreases. However, good compensation is difficult to achieve over a wide temperature range due to the non-linear characteristics associated with temperature-responsive devices and is limited in any event to the fixed load condition.

In order to obtain a wide range of temperature compensation for stabilizers using saturable reactors, a new method has been developed which is shown in Fig. 1. By this method, two basic stabilizer circuits are connected to the same alternating current source input. The first stabilizer comprises an inductance 12, capacitance 14 and saturable reactor 16. Curve 1 in Fig. 3 represents the output voltage E_0 vs. temperature curve for this stabilizer. The average slope of curve 1 may be .07 percent per degree centigrade, if an Orthonal or Deltamax core is used in saturable reactor 16. The second voltage stabilizer consists of an inductance 13, a capacitance 15, and saturable reactor 17. Saturable reactor 17 has a magnetic core, such as ferrite, with a considerably lower Curie point than that of saturable reactor 16. Curve 3 on Fig. 3 represents the output voltage vs. temperature characteristic of the second stabilizer. Using a ferrite core material for saturable reactor 17 provides curve 3 with a slope, for example, of .25 percent per degree centigrade. Consequently, the percentage slope of curve 3 is obviously considerably higher than the slope of curve 1 and has the same absolute slope, so that the ordinal separation between the curves is constant. If, therefore, the outputs represented by curves 1 and 3 are subtracted, the resultant curve 2 provides the desired compensation. It will appear obvious that the lower Curie point provides a steeper relative slope and lessens the amount of subtraction necessary for good compensation. In Figure 1 saturable reactor 17 is provided with a secondary winding 18 which is connected to the winding on saturable reactor 16 such that the voltage across its terminals is subtracted from the voltage across the terminals of saturable reactor 16. The number of turns on winding 18 is chosen so that the actual decrease in output voltage across saturable reactor 17 due to temperature change equals the actual decrease in output voltage across saturable reactor 16 due to the same temperature change. The resultant voltage exhibits excellent compensation over a wide range of temperature variations. This voltage is applied to load 19. This compensation has the added advantage of being load-sensitive only to a minor degree.

A modified version of the basic circuitry shown in Fig. 1 is illustrated in Fig. 2. In this embodiment saturable reactor 17 is provided with a series of taps, 21, 22 and 23, and has no special secondary winding. In this case, the desired compensating voltage is tapped off saturable reactor 17 in opposition to the voltage appearing across saturable reactor 16 to provide the desired compensation. A potentiometer 20 may be connected to these taps to allow for a fine adjustment in temperature compensation.

Experimental results using the new method of magnetic temperature compensation show that in percent deviation from the value of output voltage at room temperature of 25° C., a variation of +.24 percent at −50° C. to −.13 percent at 85° C. was attained. These results show the new method of magnetic temperature compensation to be effective over a wide temperature range.

With the principles of the invention as applied to resonant saturating regulators in mind, it now becomes possible to extend the reasoning basic to the phenomena discussed, whence it becomes clear that a pair of saturating reactors whose magnetic circuits have different temperature coefficients of variations in saturation flux offers a basis, when properly connected and proportioned, for developing a wave having a temperature independent stabilized volt-time area for each operating cycle.

Consider now the network of Fig. 11, in which a resistance 33 is connected in series with a saturating inductance 32 between the input lines 30, 31 and resistance 34 is connected in series with a saturating inductor 35 between

the said input lines **30, 31**. The core of inductance **32** has a saturating flux of

$$\phi_{s1}=\phi_1(1-\alpha_1 T) \quad (1)$$

while the core of inductance **35** has a saturating flux of

$$\phi_{s2}=\phi_2(1-\alpha_2 T) \quad (2)$$

Where

V=Amplitude of input rectangular wave
ϕ_{s1}=Saturation flux in inductor **32**
ϕ_{s2}=Saturation flux in inductor **35**
ϕ_1=Saturation flux in inductor **32** at reference temperature
ϕ_2=Saturation flux in inductor **35** at reference temperature
α_1=Temperature coefficient of variation in ϕ_1
α_2=Temperature coefficient of variation in ϕ_2
T=Temperature rise above reference temperature
N=Number of turns in inductor.

Resistance **33** is chosen to have an impedance large with respect to the saturated impedance of inductor **32**, and small with respect to the unsaturated impedance of said inductor **32**. Resistance **34** is selected to have an impedance large with respect to the saturated impedance of inductor **35** and small with respect to the unsaturated impedance of said inductor **35**. The inductor **35** may be tapped at **36**. Output conductors **37** and **38** may be respectively connected with the junction between resistance **33** and inductor **32**, and with the tap **36**. In a proper case, depending upon the proportioning of the relative electrical and magnetic characteristics of inductors **32** and **35**, the output conductors may be connected with the respective opposing ends of the inductors **32, 35**.

Assuming, for simplicity of explanation, that a source of rectangular voltage waves is connected between the input lines **30, 31**; that such waves have a volt-time area greater than that required to saturate both inductors by traversing them from one end of the saturation loop to the other; and that the conditions of operation are such (as for example, by use of a symmetrical input wave) that the cores are always driven from one limit of saturation flux to the opposite limit of saturation flux.

Under these conditions, the volt-time areas are

$$Vt_1=2N_1\phi_{s1}=2N_1\phi_1(1-\alpha_1 T) \quad (3)$$

and

$$Vt_2=2N_1\phi_{s2}=2N_2\phi_2(1-\alpha_2 T) \quad (4)$$

It will be noted that both of these volt-time areas of the voltage waves appearing across the inductors **32, 35** respectively, are temperature dependent. Such temperature dependence of volt-time wave areas is extremely undesirable in regulators, as shown and discussed above, and in magnetic counters of the type where the counting core is traversed incrementally over its B—H loop. Temperature dependence of the volt-time wave area seriously limits the performance which can be obtained from the last named counter.

Connecting the output lines **37, 38** to the opposing ends of inductors **32, 35** combines the volt-time areas of (3) and (4) subtractively, whereby

$$\text{volt-time area}=Vt_1-Vt_2=2(N_1\phi_1-N_2\phi_2)-2T(N_1\phi_1\alpha_1-N_2\phi_2\alpha_2) \quad (5)$$

This can be resolved into the constant term:

$$2(N_1\phi_1-N_2\phi_2) \quad (6)$$

and the temperature dependent term:

$$2T(N_1\phi_1\alpha_1-N_2\phi_2\alpha_2) \quad (7)$$

The temperature dependent component can be eliminated by selecting the parameters such that:

$$N_1\phi_1\alpha_1-N_2\phi_2\alpha_2=0 \quad (8)$$

from which we must exclude the trivial solutions satisfying the relationship:

$$N_1\phi_1-N_2\phi_2=0 \quad (9)$$

else the output wave vanishes entirely.

Thus, excluding only the condition of (9), a useful, temperature independent volt-time area is obtained in the output wave on the lines **37, 38** when

$$\alpha_2=\frac{N_1\phi_1\alpha_1}{N_2\phi_2} \quad (10)$$

If it is desired to operate in the range prescribed by (9), then one or both of the output lines **37, 38** may be connected with a tap on its associated inductor. Treating now the case of the tap **36** on inductor **35**, and considering it to be so located that 1/k of the voltage across that inductor is connected in opposition with the voltage from inductor **32**, the volt-time area of the output wave is given by:

$$2\left(N_1\phi_1\frac{-N_2\phi_2}{K}\right)-2T\left(N_1\phi_1\alpha_1\frac{-N_2\phi_2\alpha_2}{K}\right) \quad (11)$$

This is independent of temperature when

$$N_1\varphi_1\alpha_1\frac{-N_2\phi_2\alpha_2}{K}=0 \quad (12)$$

excluding now the trivial solutions satisfying the relationship

$$N_1\varphi_1\frac{-N_2\phi_2}{K}=0 \quad (13)$$

Subject to the restriction of (13), therefore, the volt-time area of the output wave is finite and independent of temperature when

$$\alpha_2=K\alpha_1\frac{N_1\phi_1}{N_2\phi_2} \quad (14)$$

Since other modifications varied to fit particular operating requirements and environments will be apparent to those skilled in the art, the invention is not considered limited to the examples chosen for purposes of disclosures and covers all changes and modifications which do not constitute departures from the true spirit and scope of this invention.

What I claim as new and desire to secure by Letters Patent of the United States:

1. A circuit including two saturable reactors connected in parallel, each having different Curie temperatures, means for applying a voltage to said saturable reactors, means for obtaining a temperature compensated output voltage by subtracting a portion of the voltage appearing across one of said saturable reactors from the voltage appearing across the other of said saturable reactors.

2. In combination, a first voltage stabilizing means for providing a substantially constant output voltage from a varying input voltage source, said voltage stabilizing means including a saturable reactor having a substantially rectangular magnetization characteristic, a second voltage stabilizing means including a saturable reactor having a substantially rectangular magnetization characteristic and a lower Curie temperature than said first named saturable reactor, and means for parallel interconnecting said first and second voltage stabilizing means for obtaining an output voltage in which variations due to temperature changes are compensated for, said voltage output thereby being substantially constant over wide temperature ranges.

3. In combination, a circuit having first and second input points, first and second impedances each having one terminal connected to said first input point, a first capacitor connected between the other terminal of said first impedance and said second input point, a second capacitor connected between the other terminal of said second impedance and said second terminal point, a first saturable reactor connected across said first capacitance, a second

saturable reactor connected across said second capacitance, and load means connected across said saturable reactors.

4. A temperature compensated voltage stabilizer circuit having first and second saturable reactors each having rectangular hysteresis loops, said second saturable reactor having a lower Curie temperature than said first saturable reactor, means for applying a voltage to said reactors, means interconnecting said saturable reactors for obtaining a temperature stabilized output voltage, said last-named means including a circuit in which a portion of the voltage across said second saturable reactor decreases the voltage across said first saturable reactor an amount depending in magnitude upon the effects which changes in temperature have on the saturation flux density of said saturable reactors, and load means associated with said reactors for utilizing the temperature stabilized voltage derived from the said saturable reactors.

5. In combination, an inductance, a non-linear oscillatory circuit having a capacitance and a saturable reactor, means serially connecting said inductance to said oscillating circuit, a second inductance, a second non-linear oscillatory circuit, means serially connecting said second inductance to said second oscillatory circuit, means for applying a varying voltage source through said inductances to said non-linear oscillatory circuits, means for subtracting a portion of the voltage across one of said oscillatory circuits from the voltage across the other of said oscillatory circuits, and load means associated with said circuits for utilizing the compensated output voltage derived from said circuits.

6. The circuit defined in claim 5 wherein the means for subtracting a portion of the voltage of one oscillatory circuit from the voltage of the other oscillatory circuit includes a secondary winding on one of said saturable reactors.

7. The circuit defined in claim 5 wherein the means for subtracting a portion of the voltage of one oscillatory circuit from the voltage of the other oscillatory circuit includes a variable tap means connected to one of said saturable reactors for tapping off a portion of the voltage across said reactor.

8. The circuit defined in claim 5 wherein the means for subtracting a portion of the voltage of one oscillatory circuit from the voltage of the other oscillatory circuit includes a variable tap means connected to one of said saturable reactors for tapping off a portion of the voltage across said reactor and a potentiometer means connected to said variable tap means.

9. A magnetic temperature-compensated voltage stabilizer circuit for providing a constant voltage output over a wide temperature range, input terminals for applying a voltage source to said circuit, first and second inductances connected to one of said input terminals, first and second capacitances, means connecting said first and second capacitances to said first and second inductances respectively, and to the other of said input terminals, first and second saturable reactors each having a rectangular magnetization curve and said second saturable reactor having a lower Curie temperature than said first saturable reactor, means connecting said first and second saturable reactors across said first and second capacitances respectively, whereby the voltage across the said second saturable reactor opposes the voltage across said first saturable reactor with the magnitude of said voltages being dependent on temperature, and load means associated with said reactors for deriving a temperature compensated constant voltage output.

10. A magnetic temperature-compensated voltage stabilizer circuit for providing a constant voltage output over a wide temperature range, input terminals for applying a voltage source to said circuit, first and second inductances connected to one of said input terminals, first and second capacitances, means connecting said first and second capacitances to said first and second inductances respectively, and to the other of said input terminals, first and second saturable reactors each having a rectangular magnetization curve and said second saturable reactor having a lower Curie temperature than said first saturable reactor, means connecting said first and second saturable reactors across said first and second capacitances respectively, whereby the voltage across said second saturable reactor opposes the voltage across said first saturable reactor with the magnitude of said voltages being dependent on temperature, a secondary winding on said second saturable reactor for coupling a portion of the opposing voltage of said second saturable reactor to said first saturable reactor, and load means associated with said reactors for deriving a magnetic temperature compensated constant voltage output.

11. A magnetic temperature-compensated voltage stabilizer circuit for providing a constant voltage output over a wide temperature range, input terminals for applying a voltage source to said circuit, first and second inductances connected to one of said input terminals, first and second capacitances, means connecting said first and second capacitances to said first and second inductances respectively, and to the other of said input teminals, first and second saturable reactors each having a rectangular magnetization curve and said second saturable reactor having a lower Curie temperature than said first saturable reactor, means connecting said first and second saturable reactors across said first and second capacitances respectively, whereby the voltage across said second saturable reactor opposes the voltage across said first saturable reactor with the magnitude of said voltages being dependent on temperature, variable tap means connected to said second saturable reactor for coupling a portion of the opposing voltage of said second saturable reactor to said first saturable reactor, and load means associated with said reactors for deriving a magnetic temperature compensated constant voltage output.

12. In an electric network, a first reactor comprising a magnetic core characterized by a first Curie temperature, a first capacitor coupled with at least a portion of said first reactor, a second reactor comprising a magnetic core characterized by a second different Curie temperature, a second capacitor coupled with at least a portion of said second reactor, means including an impedance for impressing electric energy on the said first reactor, means including an impedance for impressing electric energy on said second reactor, and circuit means for delivering an output voltage representing the resultant of opposing voltages derived from said first and second reactors to a utilization circuit.

13. The electric network according to claim 12 in which said impedances are reactors.

14. In an electric network, a first reactor comprising a magnetic core characterized by a first temperature coefficient of variation of saturation flux, a first capacitor coupled with at least a portion of said first reactor, a second reactor comprising a magnetic core characterized by a second different temperature coefficient of variation of saturation flux, a second capacitor coupled with at least a portion of said second reactor, means including an impedance for impressing electric energy on said first reactor, means including an impedance for impressing electric energy on said second reactor, and circuit means for delivering an output voltage representing the results of opposing voltages derived from said first and second reactors to a utilization circuit.

15. In an electric network, a first reactor characterized by a first temperature coefficient of variation of saturation flux, a second reactor connected in parallel with said first reactor characterized by a second different temperature coefficient of variation of saturation flux, means including an impedance for impressing electric energy on said first reactor, means including an impedance for impressing electric energy on said second reactor, and circuit means for delivering an output voltage represent-

ing the resultant of opposing voltages derived from said first and second reactors to a utilization circuit.

16. In an electric network, a first reactor characterized by a first temperature coefficient of variation of saturation flux, a second reactor connected in parallel with said first reactor characterized by a second different temperature coefficient of variation of saturation flux, means including an impedance larger than the saturation impedance of said first reactor and smaller than the unsaturated impedance of said first reactor for impressing electric energy on said first reactor, means including an impedance larger than the saturated impedance of said second reactor and smaller than the unsaturated impedance of said second reactor for impressing electric energy on said first reactor, and circuit means for delivering an output voltage representing the resultant of opposing voltages derived from said first and second reactors to a utilization circuit.

References Cited in the file of this patent

UNITED STATES PATENTS

1,697,148	Spooner	Jan. 1, 1929
2,040,763	Summers	May 12, 1936
2,082,121	Rypinski	June 1, 1937
2,439,809	Hunter	Apr. 20, 1948

FOREIGN PATENTS

115,758	Australia	Aug. 19, 1942