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(54) Title: METHOD FOR FORMING METAL INTERCONNECTION

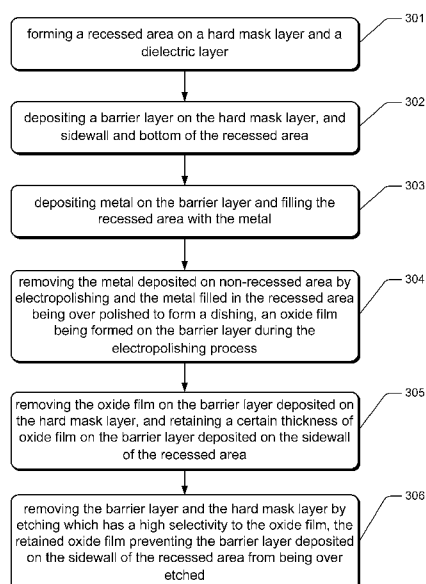


FIG 5

(57) Abstract: A method for forming metal interconnection, which can avoid a barrier layer (204) deposited on the sidewall of recessed area (207) being over etched. The method includes the following steps: forming a recessed area (207) on a hard mask layer (203) and a dielectric layer (202); depositing a barrier layer (204) on the hard mask layer (203), sidewall of the recessed area (207) and bottom of the recessed area (207); depositing metal (205) on the barrier layer (204) and filling the recessed area (207) with the metal (205); removing the metal (205) deposited on non-recessed area by electropolishing and the metal (205) filled in the recessed area (207) being over polished to form a dishing, an oxide film (206) being formed on the barrier layer (204) during the electropolishing process; removing the oxide film (206) on the barrier layer (204) deposited on the hard mask layer (203), and retaining a certain thickness of oxide film (206) on the barrier layer (204) deposited on the sidewall of the recessed area (207); removing the barrier layer (204) and the hard mask layer (203) by etching which has a high selectivity to the oxide film (206), the retained oxide film (206) preventing the barrier layer (204) deposited on the sidewall of the recessed area (207) from being over etched.



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GW, KM, ML, MR, NE, SN, TD, TG).

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## METHOD FOR FORMING METAL INTERCONNECTION

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

[0001] The present invention generally relates to a field of fabricating semiconductor devices, and more particularly relates to a method for forming metal interconnection, which can avoid over etching of a barrier layer deposited on sidewalls of trenches.

#### 2. The Related Art

[0002] With the development of semiconductor devices fabrication technology, the integration of the semiconductor devices has become higher and higher. Two layers or more than two layers of metal interconnection structures are widely used. The traditional metal interconnection structures are made of aluminum. However, as the feature size of the semiconductor devices continues to decrease, RC delay effect on the properties of the semiconductor devices is more and more obvious. For reducing the RC delay effect, copper, instead of aluminum is used for making the interconnection structures because the resistance of copper is lower than aluminum. Besides, low-k material, instead of traditional dielectric material is used as the dielectric layer of the interconnection structures for reducing the stray capacitance.

[0003] Referring to FIG. 1(a) to FIG. 1(c), a method for forming copper interconnection generally includes the following steps: providing a substrate 101, such as a wafer; depositing a dielectric layer 102 on the substrate 101; depositing a hard mask layer 103 on the dielectric layer 102; forming trenches on the hard mask layer 103 and the dielectric layer 102, a trench 106 is shown as an example in FIG. 1(a) to FIG. 1(c); depositing a barrier layer 104 on the hard mask layer 103 and on sidewalls and bottoms of the trenches; depositing a copper seed layer on the barrier layer 104

and on sidewalls and bottoms of the trenches, the copper seed layer is deposited above the barrier layer 104; depositing copper 105 on the copper seed layer and into the trenches to fill the trenches with the copper 105; removing the copper 105 deposited on non-recessed area and the copper 105 remained in recessed area (such as trenches) forming copper interconnection; removing the barrier layer 104 on the non-recessed area and the hard mask layer 103 on the dielectric layer 102.

**[0004]** A traditional method for removing the copper 105, the barrier layer 104 and the hard mask layer 103 is CMP (chemical mechanical polishing). In a CMP process, the substrate 101 is positioned on a CMP pad located on a platen. A force is applied to press the substrate 101 against the CMP pad. The CMP pad and the substrate 101 are moved relatively to each other while applying the force to polish and planarize the copper 105, the barrier layer 104 and the hard mask layer 103. A polishing solution, often known as polishing slurry, is dispensed on the CMP pad to facilitate the polishing. Although a perfect barrier layer removing result can be obtained by using the CMP method, however, the CMP method has several deleterious effects on the semiconductor structure because of the relatively strong mechanical force involved. The mechanical force can cause permanent damage to the low-k dielectric. Moreover, the polishing slurry can reduce the property of the low-k dielectric. The aforesaid perfect barrier layer removing result means the barrier layer 104 deposited on the non-recessed area is absolutely removed and the barrier layer 104 deposited on the sidewalls of the trenches are not destroyed and etched, as shown in FIG. 1(c).

**[0005]** Due to the disadvantages of the CMP method, a dry etch method is used for removing the barrier layer 104 and the hard mask layer 103.  $\text{XeF}_2$  gas phase etching with a high temperature and low pressure environment is utilized to remove the barrier layer 104 and the hard mask layer 103 after removing copper 105 by CMP, where the material of the barrier layer 104 is Tantalum, Tantalum nitride, Titanium, or Titanium nitride and the material of the hard mask layer 103 is Titanium nitride. The  $\text{XeF}_2$  gas phase etching has no damage to the copper 105 and the dielectric layer 102.

However, the  $\text{XeF}_2$  gas phase etching can easily cause under etching or over etching of the barrier layer 104. As shown in FIG. 2, FIG. 2 shows an under etching of the barrier layer 104. It can be seen from FIG. 2 that the barrier layer 104 on the non-recessed area is not completely removed and a part of barrier layer 104 is remained on the non-recessed area. As shown in FIG. 3, FIG. 3 shows an over etching of the barrier layer 104. It can be seen from FIG. 3 that although the barrier layer 104 on the non-recessed area is completely removed, but a part of the barrier layer 104 deposited on the sidewall of the trench 106 is also removed. The top surface of the barrier layer 104 in the trench 106 is lower than the top surface of the copper 105 in the trench 106. Whatever the under etching or over etching of the barrier layer 104 will reduce the quality of the semiconductor devices.

## SUMMARY

**[0006]** Accordingly, the present invention provides a method for forming metal interconnection, which avoids a barrier layer deposited on sidewalls of recessed areas being over etched.

**[0007]** A method for forming metal interconnection according to an exemplary embodiment of the present invention includes the following steps: forming a recessed area on a hard mask layer and a dielectric layer; depositing a barrier layer on the hard mask layer, sidewall of the recessed area and bottom of the recessed area; depositing metal on the barrier layer and filling the recessed area with the metal; removing the metal deposited on non-recessed area by electropolishing and the metal filled in the recessed area being over polished to form a dishing, an oxide film being formed on the barrier layer during the electropolishing process, the thickness of the oxide film on the barrier layer deposited on the sidewall of the recessed area being thicker than the oxide film on the barrier layer deposited on the hard mask layer; removing the oxide film on the barrier layer deposited on the hard mask layer, and retaining a certain thickness of oxide film on the barrier layer deposited on the sidewall of the recessed

area; removing the barrier layer and the hard mask layer by etching which has a high selectivity to the oxide film, the retained oxide film preventing the barrier layer deposited on the sidewall of the recessed area from being over etched.

[0008] As described above, when the metal is removed and over polished by electropolishing, because of the anodic oxidation effect, the exposed barrier layer is passivated by forming the oxide film on the barrier layer. The dielectric layer is under the barrier layer and the hard mask layer, hence, charges are uniformly distributed in the conductive layer (composed of the barrier layer and the hard mask layer), and the charges will accumulate on the surface of the dielectric layer. Based on the non-conductive material surface potential equilibrium theory, the charges distribution on the non-conductive material surface is inversely proportional to radius of curvature, therefore, more charges are accumulated on the shoulder of the barrier layer than the flat surface, so this area's oxide film is thicker than the other area's. That is why the thickness of the oxide film on the barrier layer deposited on the sidewall of the recessed area is thicker than the oxide film on the barrier layer deposited on the hard mask layer. After the oxide film on the barrier layer deposited on the hard mask layer is removed, the retained oxide film on the barrier layer deposited on the sidewall of the recessed area forms a continue film on the barrier layer for preventing the barrier layer deposited on the sidewall of the recessed area from being over etched during removing the barrier layer and the hard mask layer, which improves the quality of semiconductor devices.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The present invention will be apparent to those skilled in the art by reading the following description of embodiments thereof, with reference to the attached drawings, in which:

[0010] FIGS. 1(a) to 1(c) are sectional views illustrating a process of forming metal interconnection;

- [0011] FIG. 2 is a sectional view illustrating under etching of a barrier layer;
- [0012] FIG. 3 is a sectional view illustrating over etching of the barrier layer;
- [0013] FIGS. 4(a) to 4(d) are sectional views illustrating a method for forming metal interconnection of the present invention;
- [0014] FIG. 5 is a flow chart illustrating the method for forming metal interconnection of the present invention;
- [0015] FIG. 6 illustrates a measuring result of weight percentage content of oxygen element after electropolishing process;
- [0016] FIG. 7 illustrates STEM cross section of POST-TFE sample, showing a perfect barrier layer removing result; and
- [0017] FIG. 8 illustrates FIB/SEM cross section of POST-TFE sample, showing over etching of a barrier layer.

## DETAILED DESCRIPTION OF EMBODIMENTS

[0018] Referring to FIGS. 4(a) to 4(d) and FIG. 5, a method for forming metal interconnection according to an exemplary embodiment of the present invention is illustrated and the method comprises the following steps which will be described in detail hereinafter.

[0019] Step 301, forming a recessed area on a hard mask layer and a dielectric layer. As shown in FIG. 4(a), a substrate 201, such as a wafer, is provided. A dielectric layer 202 is deposited on the substrate 201. The dielectric layer 202 may include materials such as SiO<sub>2</sub>, SiOC, SiOF, SiLK, BD, BDII, BDIII, etc. Preferably, the dielectric layer 202 selects low-k dielectric for reducing capacitance between the interconnection structures in a semiconductor device. According to different structure requirement, the dielectric layer 202 can be composed of two layers or more than two layers. If the dielectric layer 202 is composed of two layers, the dielectric constant of the upper layer is higher than the dielectric constant of the lower layer. A hard mask

layer 203 is deposited on the dielectric layer 202. The material of the hard mask layer 203 may include tantalum nitride or titanium nitride. Recessed areas, for example, trenches, vias, etc., are formed on the hard mask layer 203 and the dielectric layer 202 by using existing methods in prior art. A recessed area 207 is shown in the figures as an example.

[0020] Step 302, depositing a barrier layer 204 on the hard mask layer 203, sidewall of the recessed area 207 and bottom of the recessed area 207. Still refer to FIG. 4(a), the barrier layer 204 is deposited on the hard mask layer 203 and on the sidewall and the bottom of the recessed areas by any appropriate deposition method, such as chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), and the like. The barrier layer 204 may be formed from a conductive material, for instance, the barrier layer 204 may include materials such as tantalum, tantalum nitride, titanium, titanium nitride, ruthenium, cobalt, etc.

[0021] Step 303, depositing metal 205 on the barrier layer 204 and filling the recessed area 207 with metal 205. As shown in FIG. 4(a), metal 205 is deposited on the barrier layer 204 and filling the recessed area 207 by any appropriate method, such as PVD, CVD, ALD, electroplating and the like. Furthermore, in some applications, such as a plating process is used to deposit metal 205, a metal seed layer can be deposited onto the barrier layer 204 before depositing the metal 205. The metal seed layer may include the same material as metal 205 in order to facilitate the deposition and bonding of metal 205 onto the barrier layer 204. Metal 205 fills the recessed area 207 and covers non-recessed areas, as shown in FIG. 4(a). Preferably, the metal 205 is copper.

[0022] Step 304, removing the metal 205 deposited on non-recessed area by electropolishing, the metal 205 filled in the recessed area 207 is over polished to form a dishing. During the electropolishing process, an oxide film 206 is formed on the barrier layer 204, and the thickness of the oxide film 206 on the barrier layer 204 deposited on the sidewall of the recessed area is thicker than the oxide film 206 on the

barrier layer 204 deposited on the hard mask layer 203. As shown in FIG. 4(b), when the metal 205 is removed and over polished by electropolishing, because of the anodic oxidation effect, the exposed barrier layer 204 is passivated by forming the oxide film 206 on the barrier layer 204. The dielectric layer 202 is under the barrier layer 204 and the hard mask layer 203, hence, charges are uniformly distributed in the conductive layer (composed of the barrier layer 204 and the hard mask layer 203), and the charges will accumulate on the surface of the dielectric layer 202. Based on the non-conductive material surface potential equilibrium theory, the charges distribution on the non-conductive material surface is inversely proportional to radius of curvature, therefore, more charges are accumulated on the shoulder of the barrier layer 204 than the flat surface, so the oxide film 206 on the shoulders of the barrier layer 204 is thicker than the other area's oxide film 206. That is why the thickness of the oxide film 206 on the barrier layer 204 deposited on the sidewall (corresponding to the shoulder) of the recessed area is thicker than the oxide film 206 on the barrier layer 204 deposited on the hard mask layer 203 (corresponding to the flat surface). Referring to FIG. 6, it is proved that the thickness of the oxide film 206 on the barrier layer 204 deposited on the sidewall of the recessed area is thicker than the oxide film 206 on the barrier layer 204 deposited on the hard mask layer 203 by experiment. After the metal 205 on the non-recessed areas is removed and the metal 205 filled in the recessed areas is over polished by electropolishing, cutting a part of the substrate 201 as a sample. Then, using an electron microscope of which model is HELIOS 660 and an energy disperse spectroscopy of which model is X-Max<sup>N</sup> SDD to line scan the surface of the sample. The energy of the electron beam is 3kv. The scan length is about 2 $\mu$ m and the number of scan points is 400 points. The scan length of the barrier layer 204 is 1 $\mu$ m and the scan length of the metal structures on either side of the barrier layer 204 is 1 $\mu$ m. It can be seen from the measuring result that the weight percentage content of oxygen element in the barrier layer 204 close to the metal structure is higher than the other area, which proves that the thickness of the oxide film 206 on the barrier layer 204 deposited on the sidewall of the recessed area is

thicker than the oxide film 206 on the barrier layer 204 deposited on the hard mask layer 203.

**[0023]** Still in the step 304, for forming the oxide film 206 on the shoulders of the barrier layer 204, the metal 205 filled in the recessed areas is over polished to form a dishing, as shown in FIG. 4(b). The thickness of the oxide film 206 formed on the barrier layer 204 is proportional to the over polished amount of the metal 205 filled in the recessed area. The over polished amount of the metal 205 is equal to or larger than the thickness of the barrier layer 204 and the hard mask layer 203. In an embodiment, the over polished amount of the metal 205 is 300-500 angstrom.

**[0024]** Step 305, removing the oxide film 206 on the barrier layer 204 deposited on the hard mask layer 203, and retaining a certain thickness of oxide film 206 on the barrier layer 204 deposited on the sidewall of the recessed area, as shown in FIG. 4(c). The oxide film 206 on the barrier layer 204 is removed by wet etching, such as BHF solution. Alternatively, the oxide film 206 on the barrier layer 204 is removed by dry etching, such as HF vapor or the mixture of HF vapor and one of the following, ethyl alcohol, methyl alcohol or IPA. The retained oxide film 206 on the barrier layer 204 deposited on the sidewall of the recessed area 207 forms a continuous film on the barrier layer 204 and the thickness of the retained oxide film 206 is larger than 5 angstrom. If the oxide film 206 on the barrier layer 204 deposited on the sidewall of the recessed area 207 is etched and cannot form a continuous film on the barrier layer 204, the barrier layer 204 sandwiched between the metal 205 and the dielectric layer 202 will be over etched, as shown in FIG. 8 which illustrates FIB/SEM cross section of POST-TFE sample, showing over etching of the barrier layer.

**[0025]** Step 306, removing the barrier layer 204 and the hard mask layer 203 by etching which has a high selectivity to the oxide film 206, the retained oxide film 206 preventing the barrier layer 204 deposited on the sidewall of the recessed area from being over etched, as shown in FIG. 4(d). The high selectivity means the etch

rate of the barrier layer 204 and the hard mask layer 203 is much higher than the etch rate of the oxide film 206. The barrier layer 204 and the hard mask layer 203 are removed by gas phase etching, and the gas selects from the following:  $\text{XeF}_2$ ,  $\text{XeF}_4$ ,  $\text{XeF}_6$ ,  $\text{KrF}_2$ ,  $\text{BrF}_3$ . Taking  $\text{XeF}_2$  for example, the  $\text{XeF}_2$  reacts spontaneously with the barrier layer Ta/TaN at certain temperature and pressure.  $\text{XeF}_2$  is an isotropic selective etching of Ta/TaN. The  $\text{XeF}_2$  gas has a good selectivity to both copper and dielectric materials. The pressure of  $\text{XeF}_2$  gas during the etch process is between 0.1 Torr and 100 Torr, however 0.5 Torr~20 Torr is preferred. The  $\text{XeF}_2$  has a high selectivity to the oxide film 206, so during the etching process of the barrier layer 204 and the hard mask layer 203, the oxide film 206 can prevent the barrier layer 204 deposited on the sidewall of the recessed area from being over etched. As shown in FIG. 7, FIG. 7 illustrates STEM cross section of POST-TFE sample, showing a perfect barrier layer removing result which means the barrier layer 204 deposited on the non-recessed areas is absolutely removed but the barrier layer 204 sandwiched between the metal 205 and the dielectric layer 202 are not destroyed and etched. When the barrier layer 204 and the hard mask layer 203 on the non-recessed areas are completely removed, the adjacent metal interconnections are separated by the dielectric layer 202.

**[0026]** As described above, when the metal 205 is removed and over polished by electropolishing, the exposed barrier layer 204 is passivated by forming the oxide film 206 on the barrier layer 204 and the thickness of the oxide film 206 on the barrier layer 204 deposited on the sidewall of the recessed area is thicker than the oxide film 206 on the barrier layer 204 deposited on the hard mask layer 203. After the oxide film 206 on the barrier layer 204 deposited on the hard mask layer 203 is removed, the retained oxide film 206 on the barrier layer 204 deposited on the sidewall of the recessed area forms a continuous film on the barrier layer 204 for preventing the barrier layer 204 deposited on the sidewall of the recessed area from being over etched during removing the barrier layer 204 and the hard mask layer 203, which improves the quality of semiconductor devices.

[0027] The foregoing description of the present invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously many modifications and variations are possible in light of the above teaching. Such modifications and variations that may be apparent to those skilled in the art are intended to be included within the scope of this invention as defined by the accompanying claims.

## CLAIMS

1. A method for forming metal interconnection, comprising:  
forming a recessed area on a hard mask layer and a dielectric layer;  
depositing a barrier layer on the hard mask layer, sidewall of the recessed area and bottom of the recessed area;  
depositing metal on the barrier layer and filling the recessed area with the metal;  
removing the metal deposited on non-recessed area by electropolishing, the metal filled in the recessed area being over polished to form a dishing, an oxide film being formed on the barrier layer during the electropolishing process, the thickness of the oxide film on the barrier layer deposited on the sidewall of the recessed area being thicker than the oxide film on the barrier layer deposited on the hard mask layer;  
removing the oxide film on the barrier layer deposited on the hard mask layer, and retaining a certain thickness of oxide film on the barrier layer deposited on the sidewall of the recessed area;  
removing the barrier layer and the hard mask layer by etching which has a high selectivity to the oxide film, the retained oxide film preventing the barrier layer deposited on the sidewall of the recessed area from being over etched.
2. The method as claimed in claim 1, wherein the metal is copper.
3. The method as claimed in claim 1, wherein the barrier layer is selected from the following: tantalum, tantalum nitride, titanium, titanium nitride, ruthenium, cobalt.
4. The method as claimed in claim 1, wherein the thickness of the oxide film formed on the barrier layer is proportional to the over polished amount of the metal filled in the recessed area.

5. The method as claimed in claim 4, wherein the over polished amount of the metal is equal to or larger than the thickness of the barrier layer and the hard mask layer.

6. The method as claimed in claim 4, wherein the over polished amount of the metal is 300-500 angstrom.

7. The method as claimed in claim 1, wherein the oxide film formed on the barrier layer is removed by wet etching.

8. The method as claimed in claim 7, wherein the oxide film formed on the barrier layer is removed by BHF solution.

9. The method as claimed in claim 1, wherein the oxide film formed on the barrier layer is removed by dry etching.

10. The method as claimed in claim 9, wherein the oxide film formed on the barrier layer is removed by HF vapor or the mixture of HF vapor and one of the following, ethyl alcohol, methyl alcohol or IPA.

11. The method as claimed in claim 1, wherein the retained oxide film forms a continuous film on the barrier layer.

12. The method as claimed in claim 11, wherein the thickness of the retained oxide film is larger than 5 angstrom.

13. The method as claimed in claim 1, wherein the barrier layer and the hard mask layer are removed by gas phase etching.

14. The method as claimed in claim 13, wherein the gas selects from the following:  $\text{XeF}_2$ ,  $\text{XeF}_4$ ,  $\text{XeF}_6$ ,  $\text{KrF}_2$ ,  $\text{BrF}_3$ .

15. The method as claimed in claim 1, wherein the material of the dielectric layer is low-k dielectric.

16. The method as claimed in claim 1, wherein the dielectric layer is composed of two layers or more than two layers.

17. The method as claimed in claim 16, wherein the dielectric layer is composed of two layers and the dielectric constant of the upper layer is higher than the dielectric constant of the lower layer.

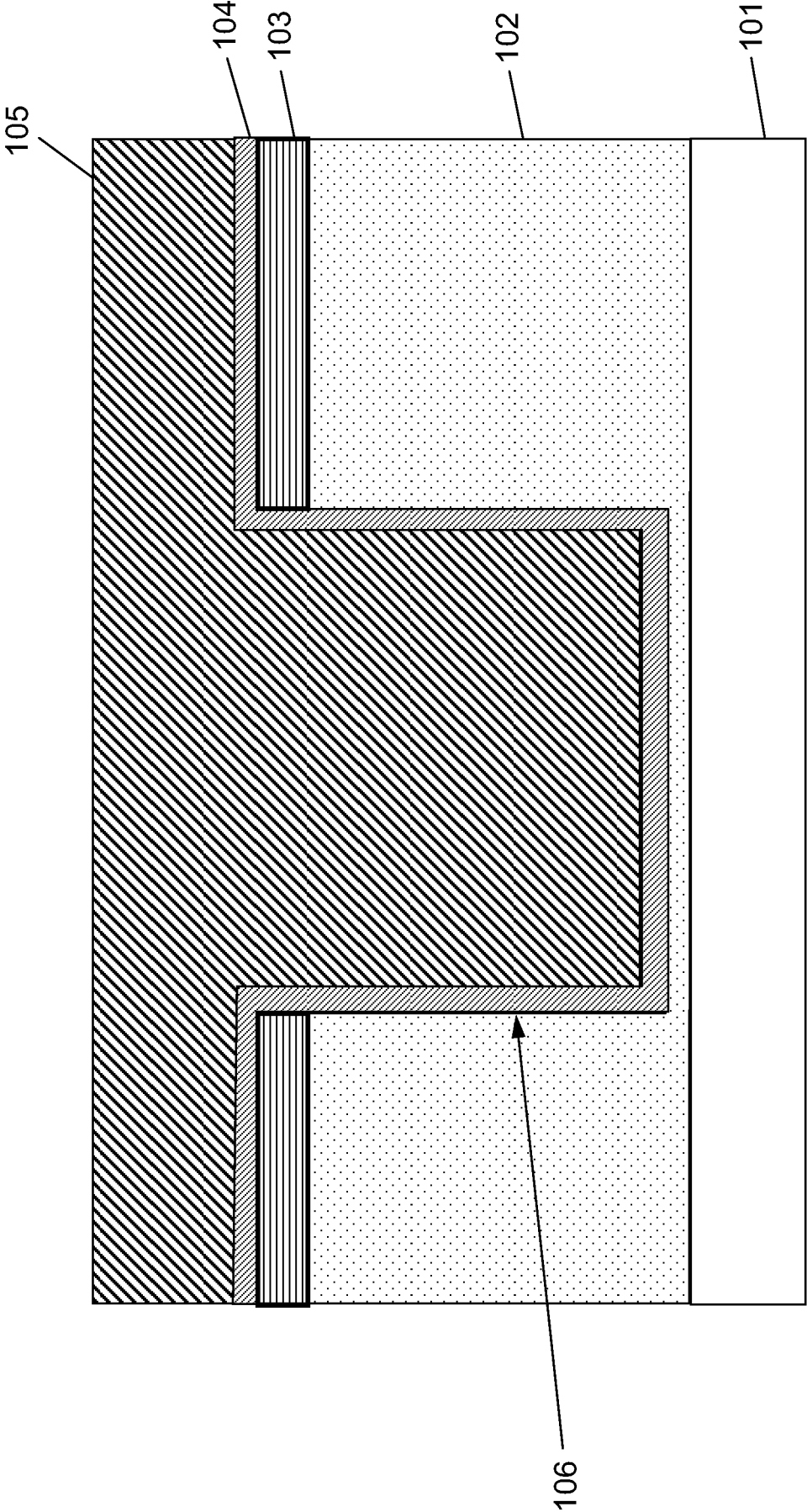


FIG 1(a)

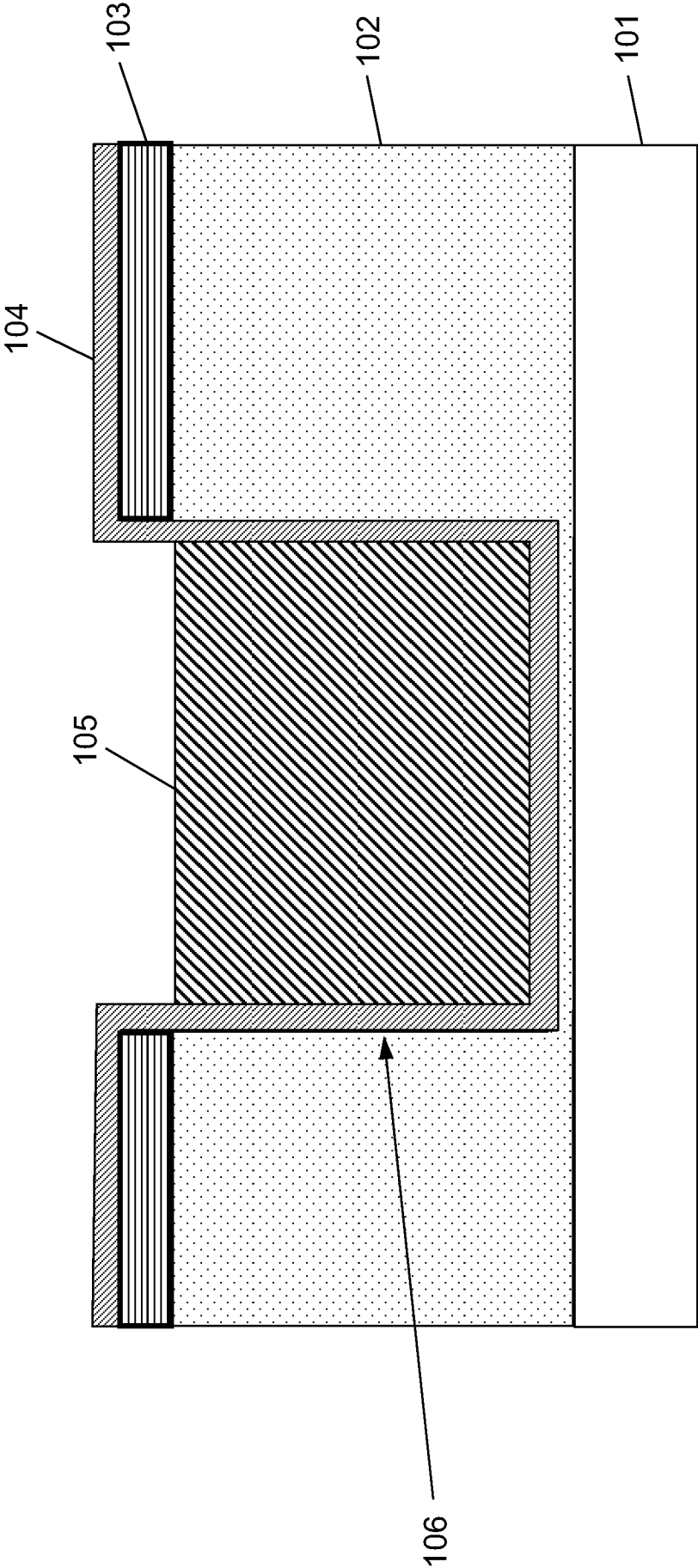


FIG 1(b)

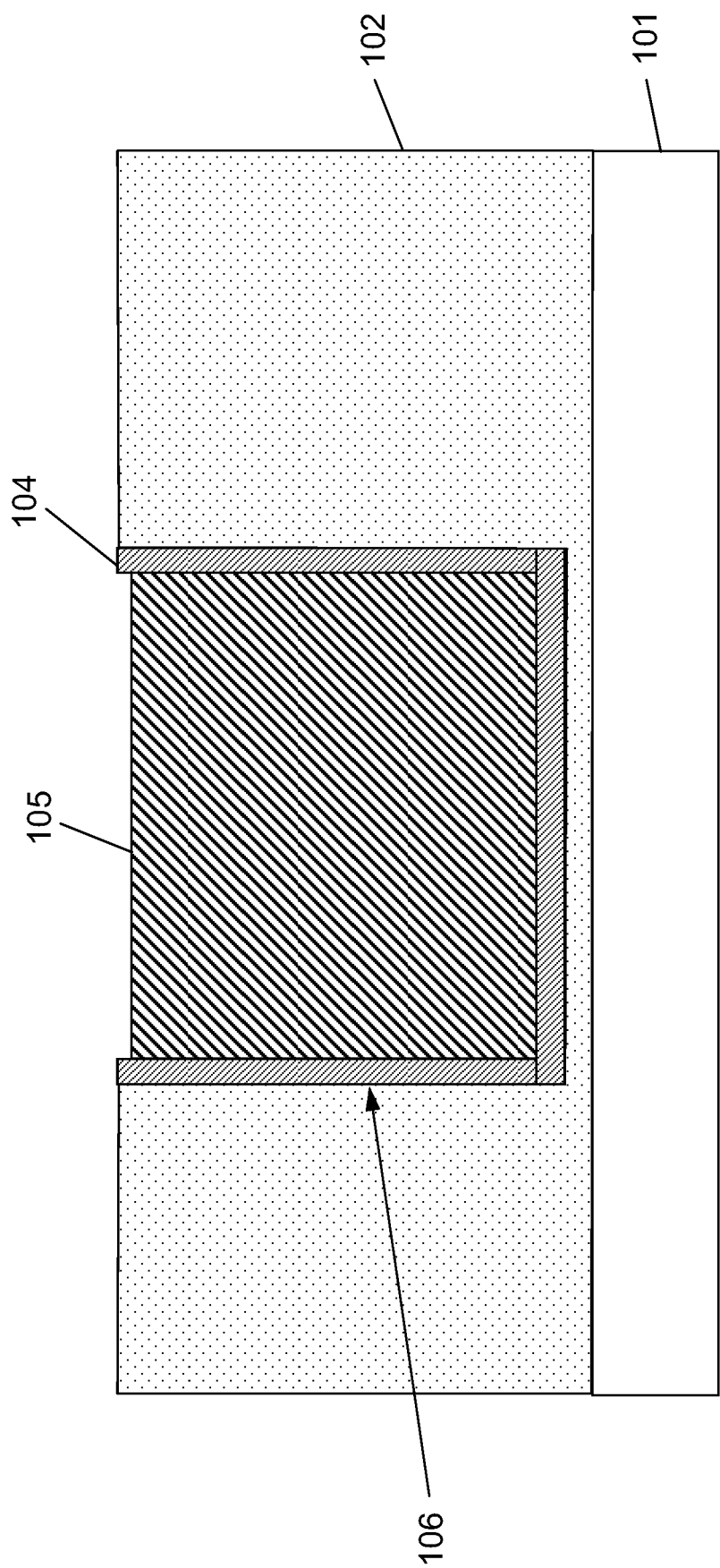


FIG 1(c)

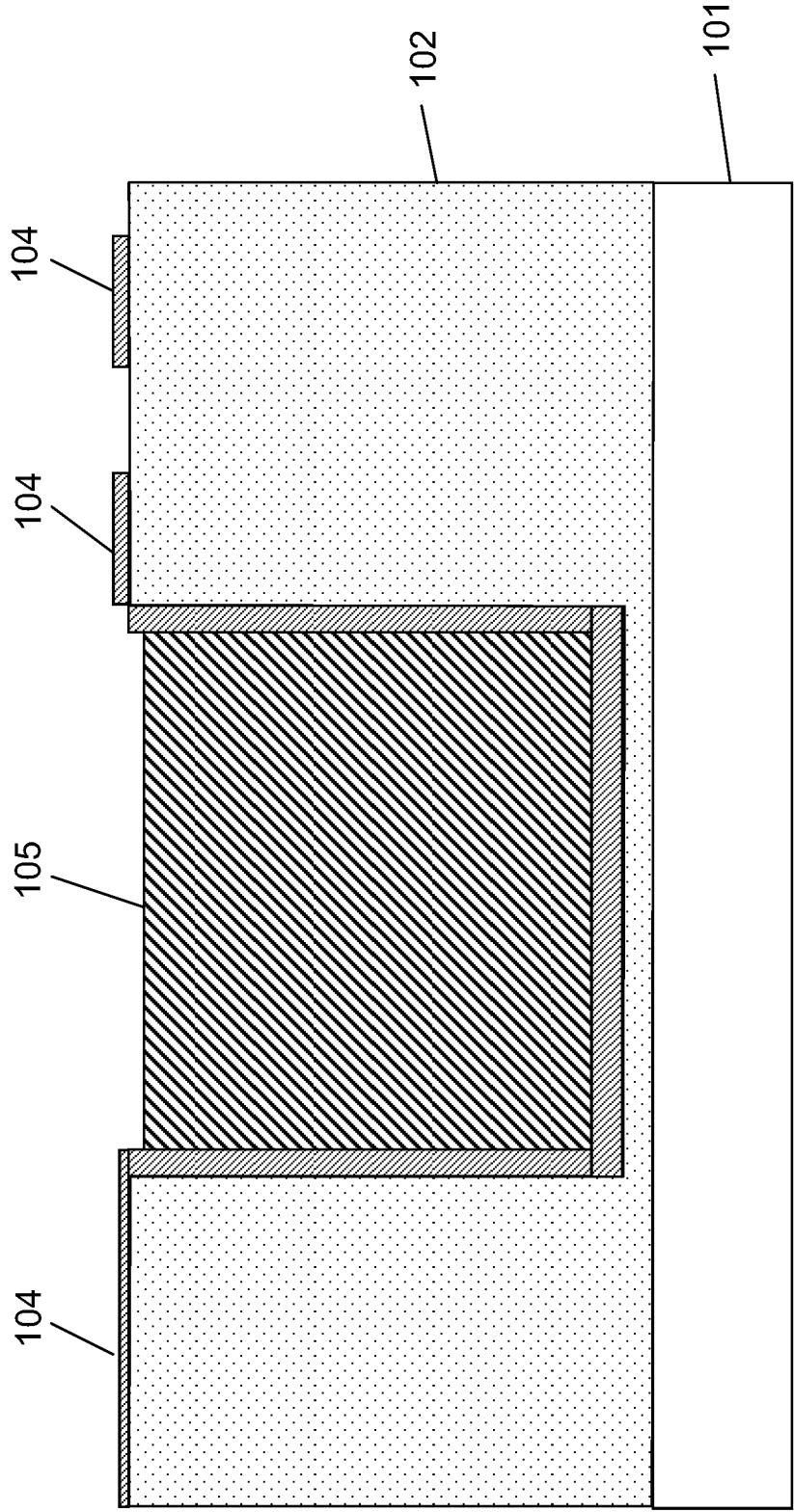


FIG 2

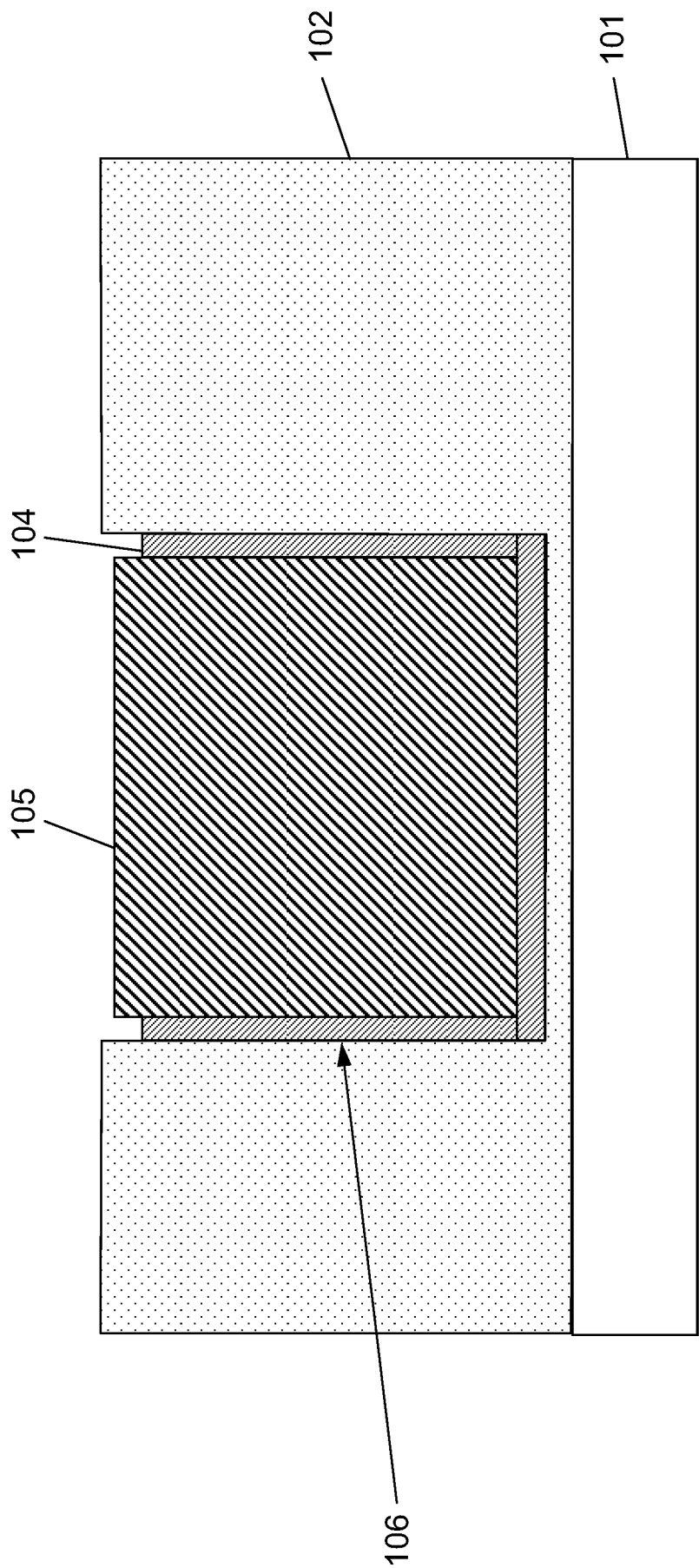


FIG 3

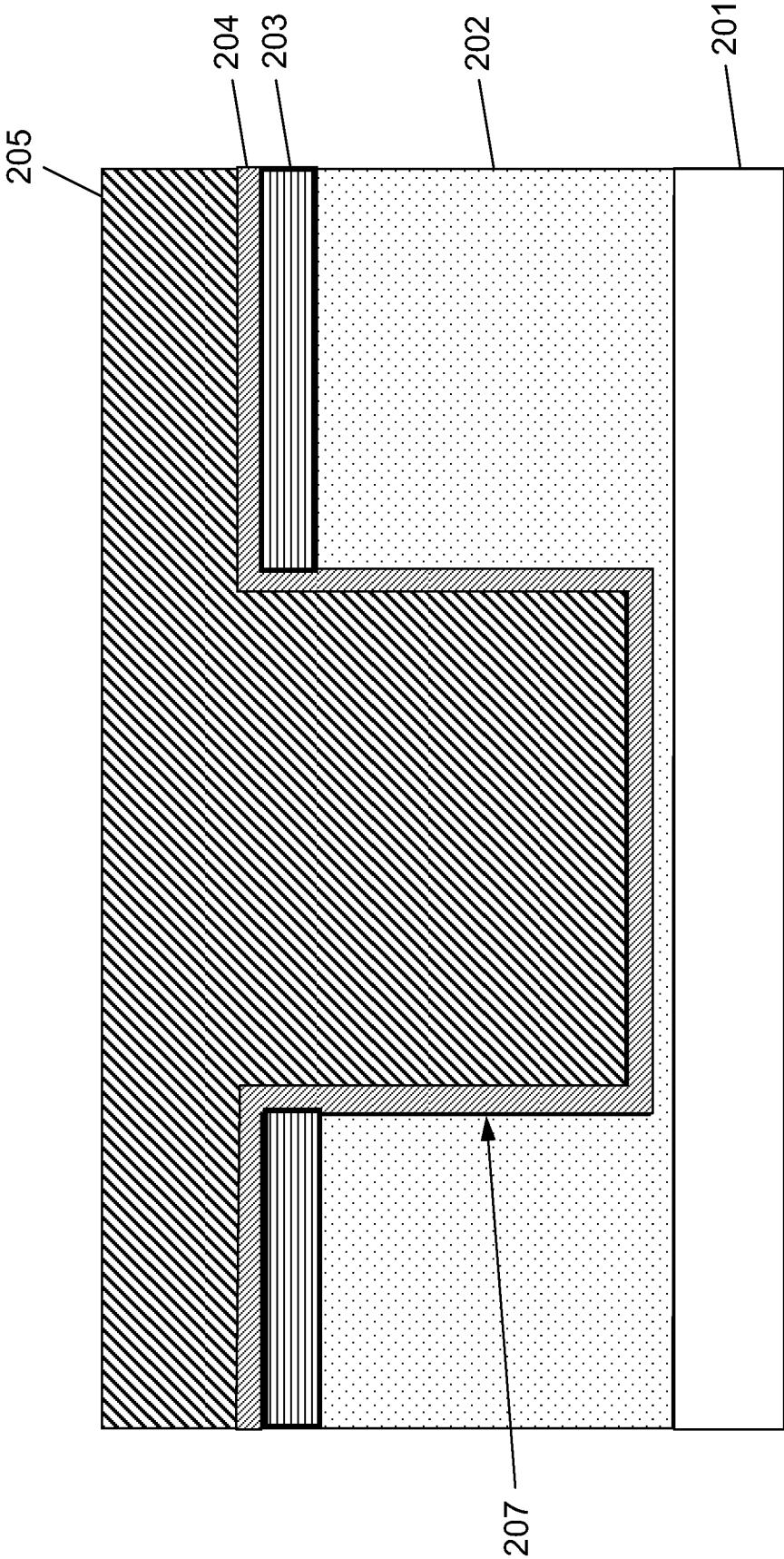


FIG 4(a)

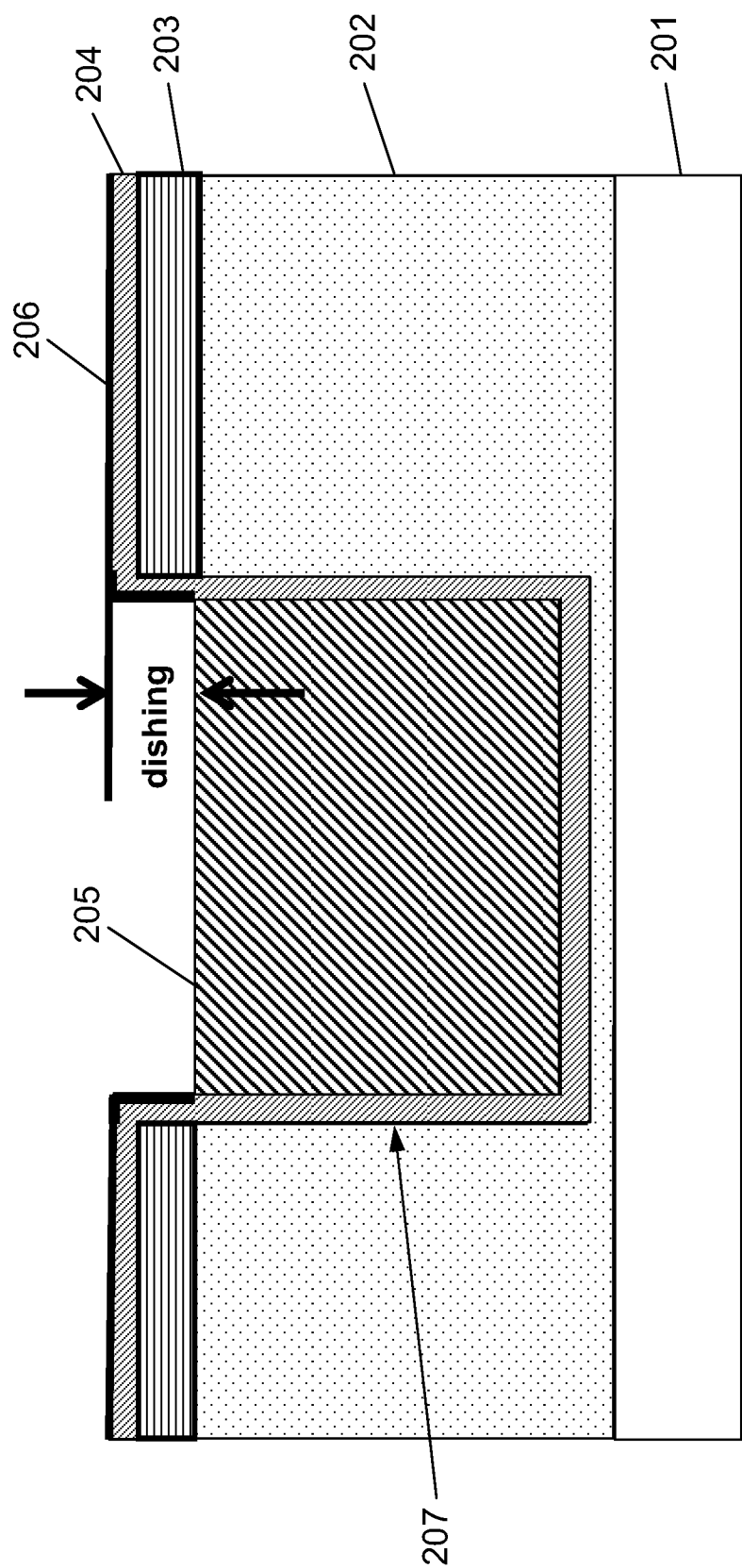


FIG 4(b)

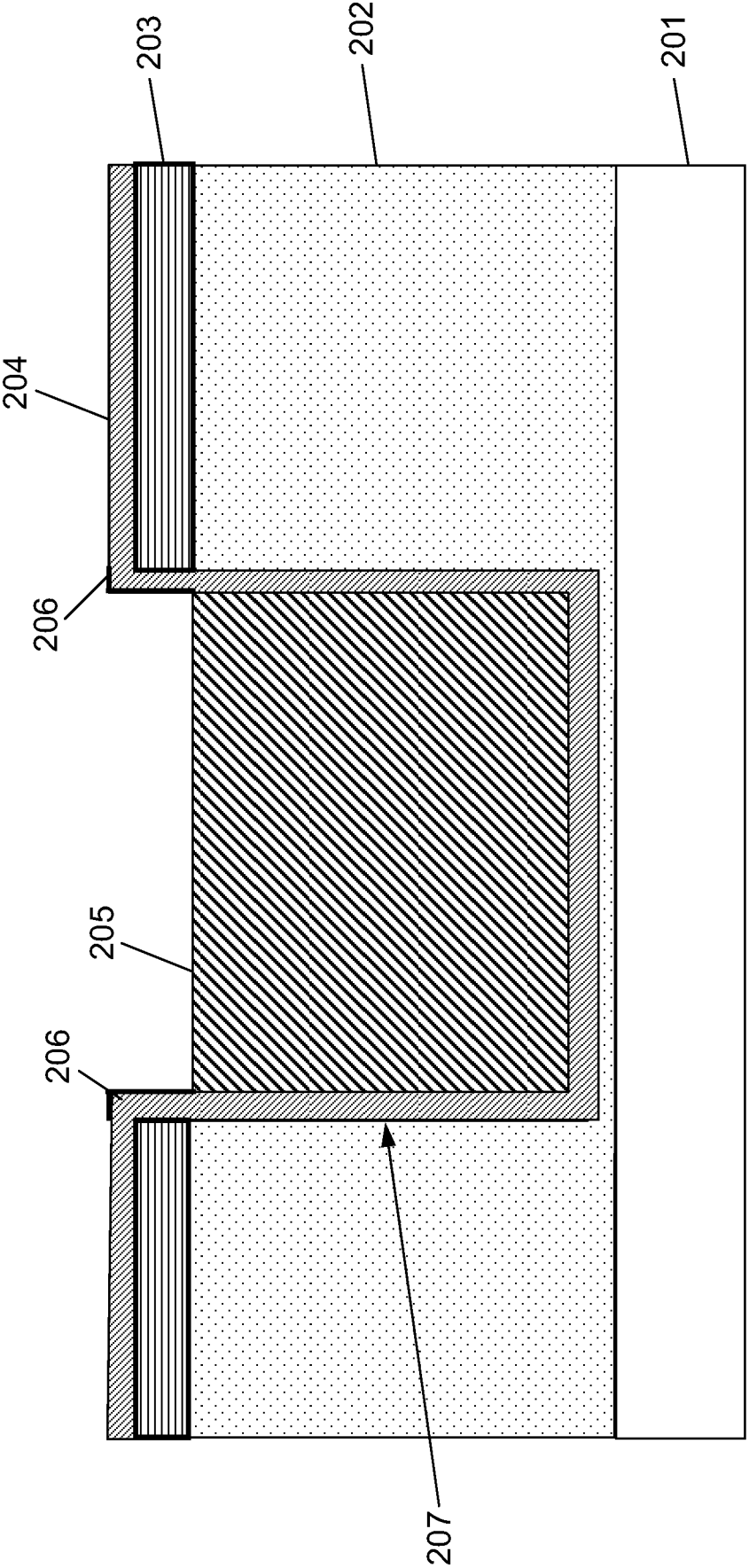


FIG 4(c)

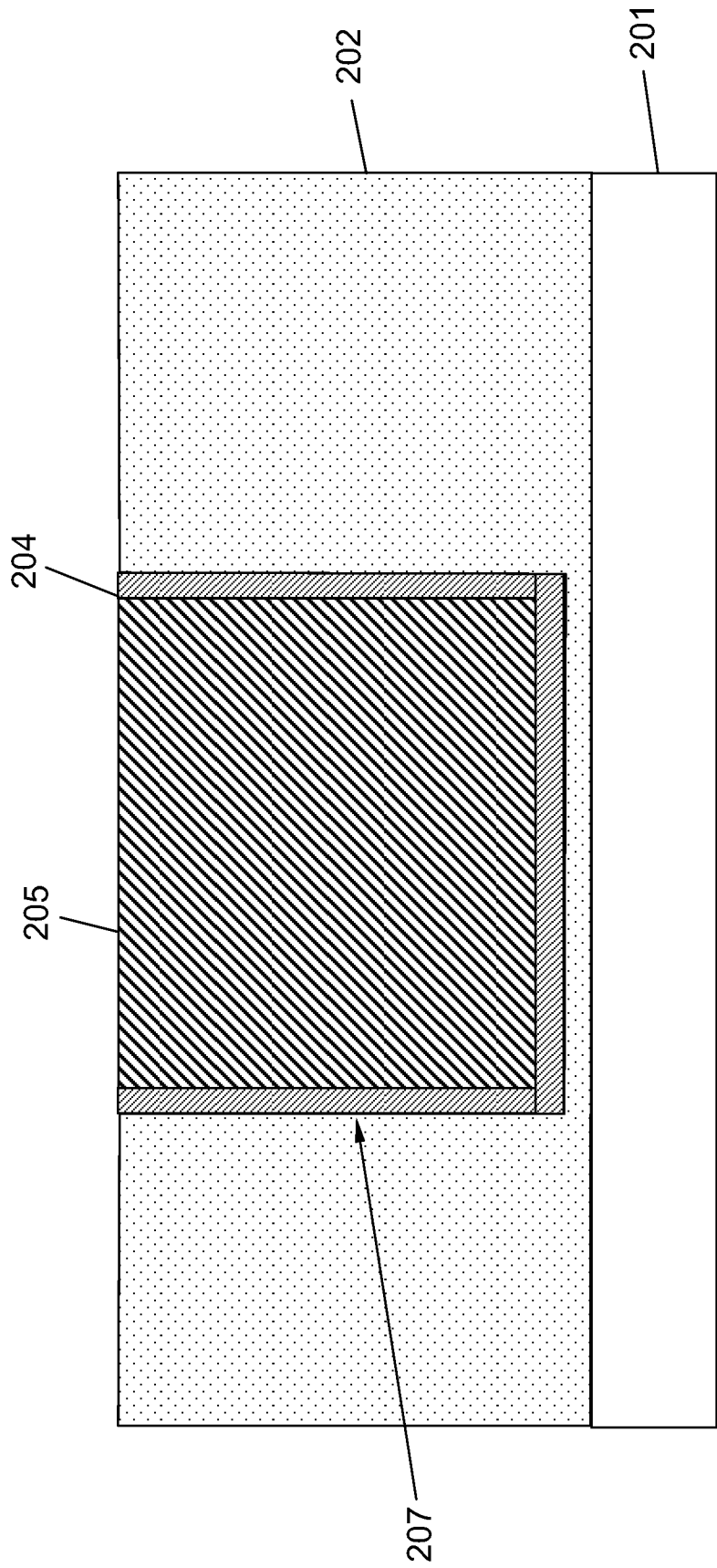
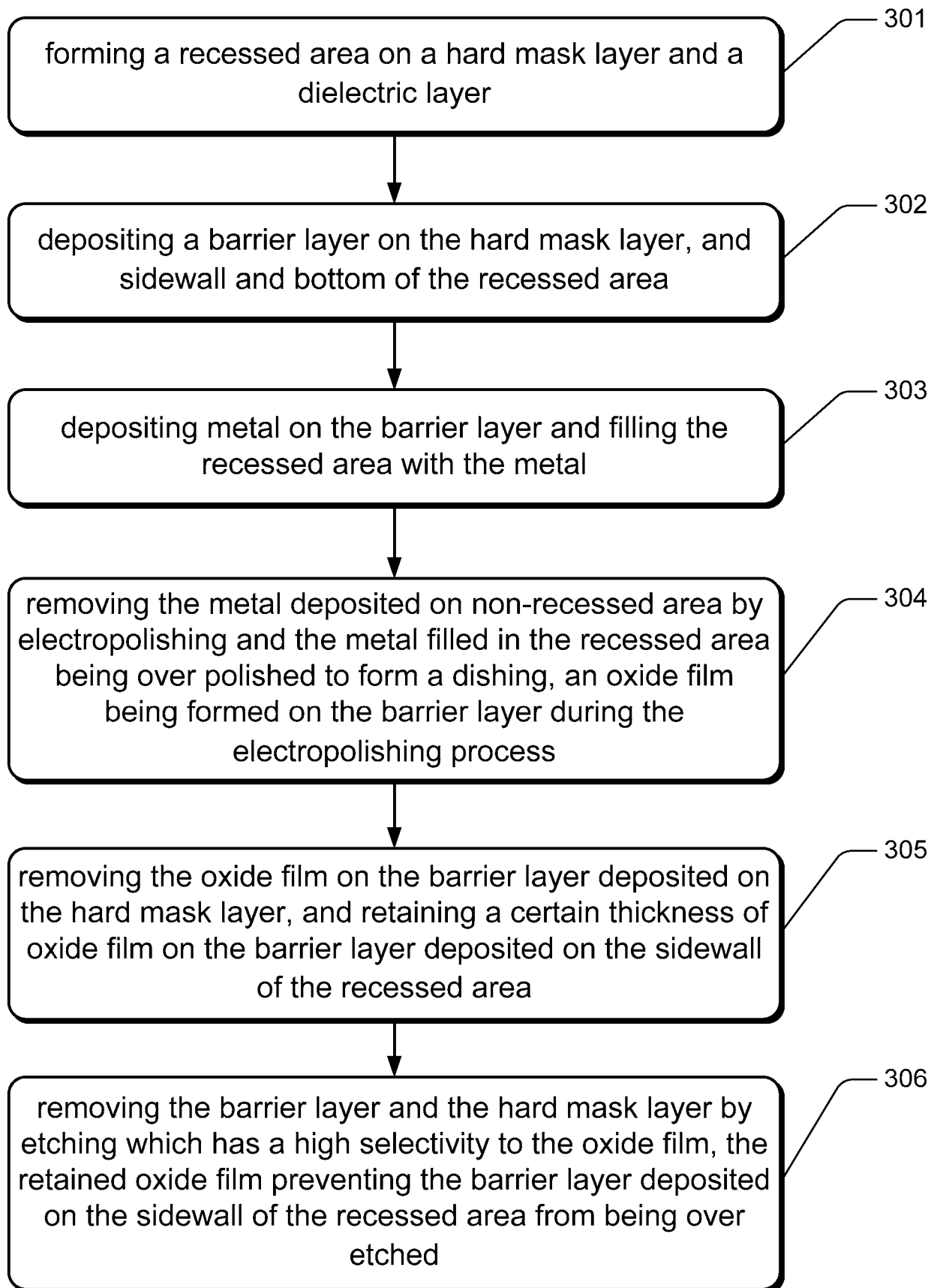


FIG 4(d)

**FIG 5**

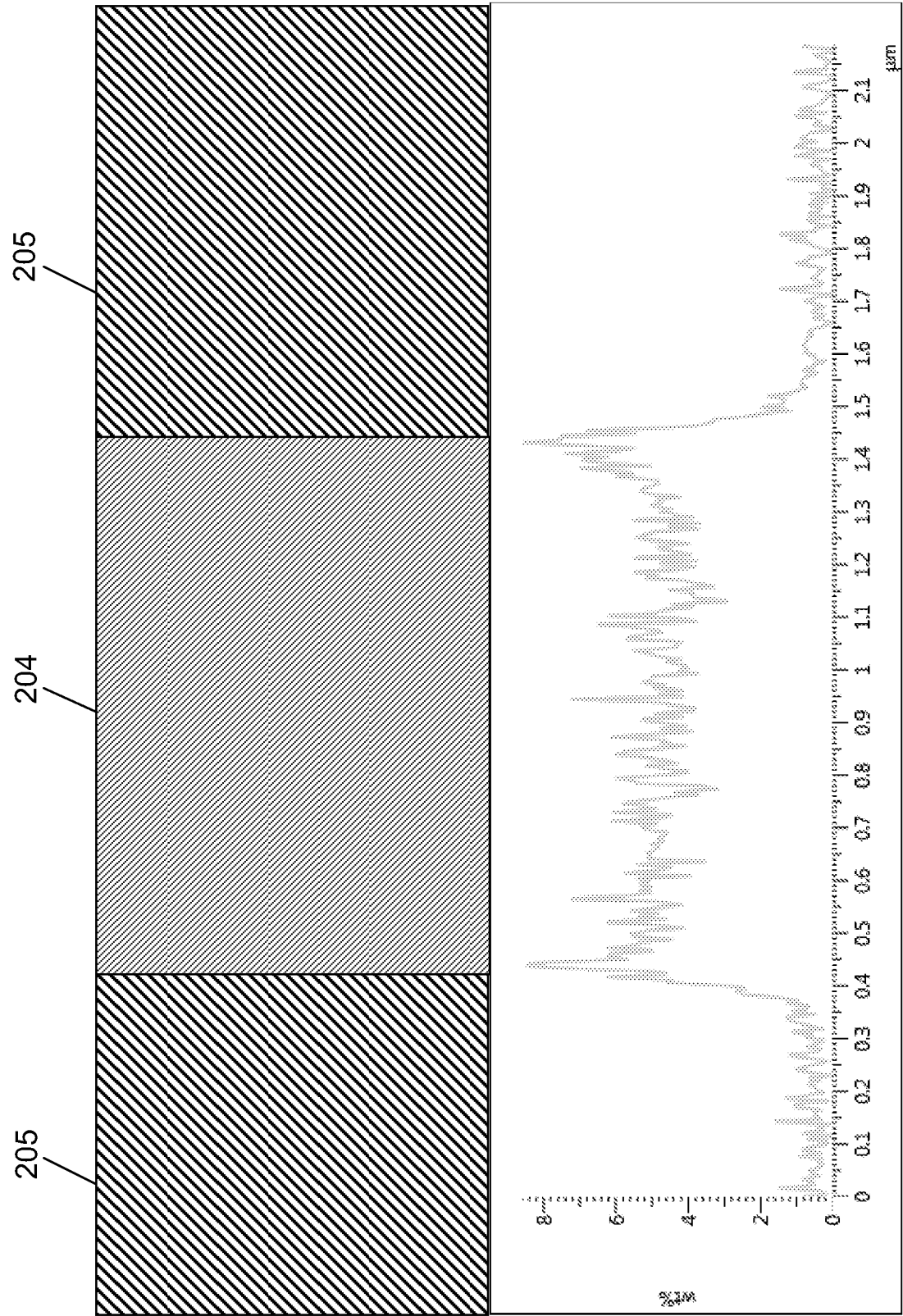
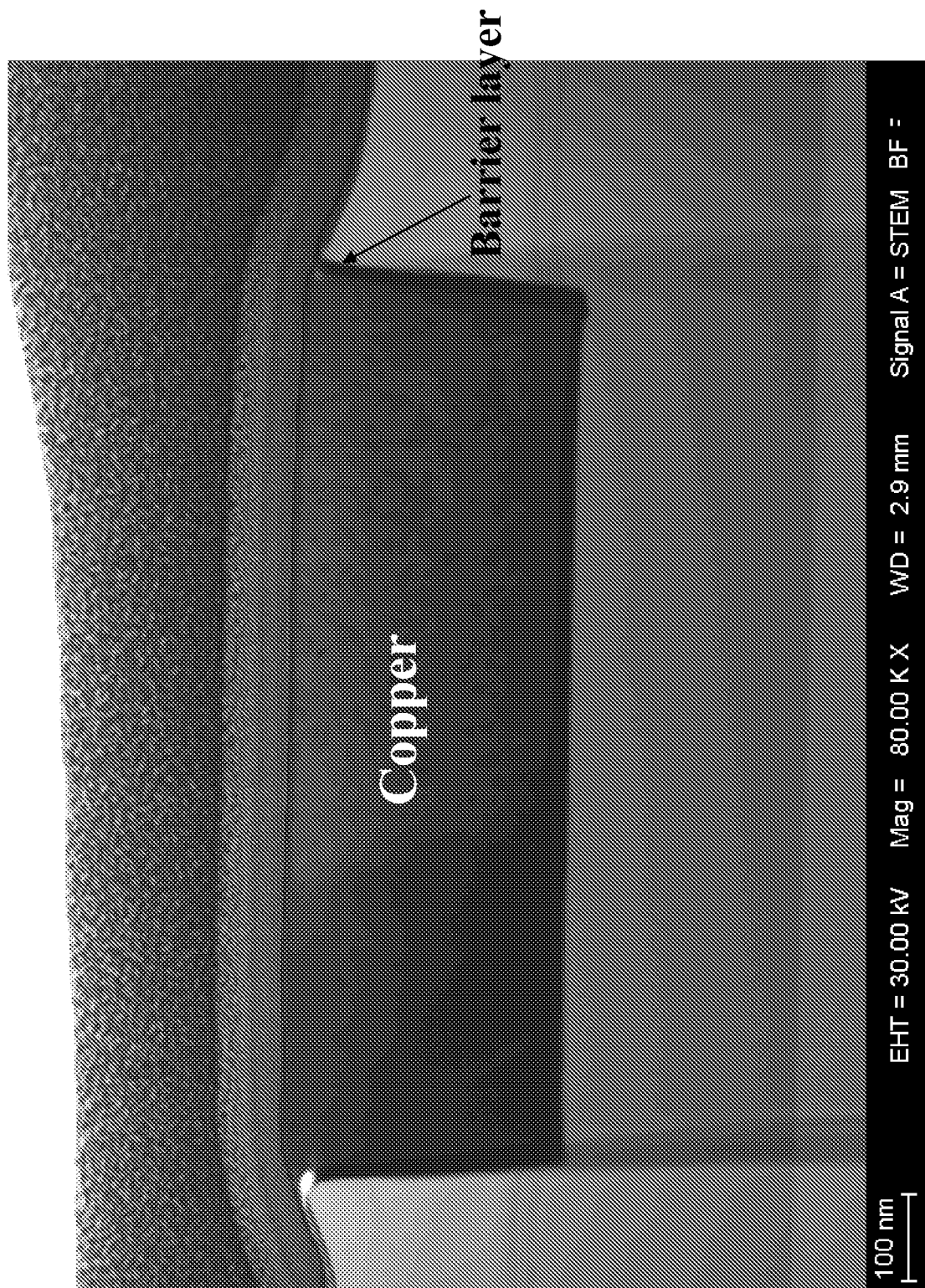


FIG 6

**FIG 7**

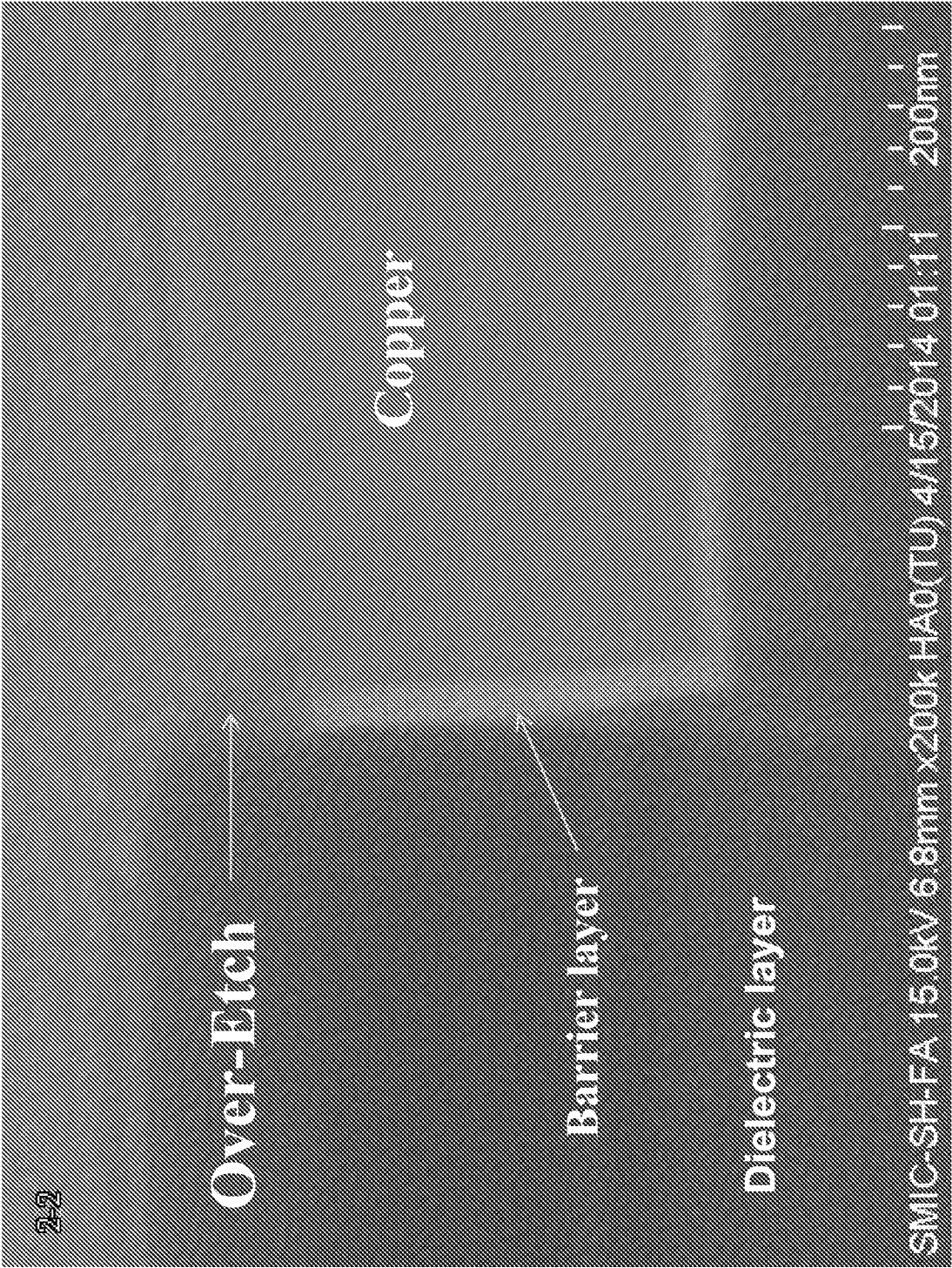


FIG 8

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2014/081790

**A. CLASSIFICATION OF SUBJECT MATTER**

H01L 21/768 (2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H01L21/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPODOC, WPI, CNPAT, CNKI, CA: over etched,oxide film,barrier layer,tantalic oxide, tantalum oxide,titanium oxide,hard mask layer,dielectric layer

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                                                                                          | Relevant to claim No. |
|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
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Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

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Date of mailing of the international search report

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**Information on patent family members**

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