United States Patent

Reiss et al.

[15] **3,641,547**

[45] **Feb. 8, 1972**

[54] LINE SECURITY SYSTEM

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[22] Filed: **May 25, 1970**

[21] Appl. No.: **40,285**

[52] U.S. Cl. .....**340/253 R**, 340/256, 340/276, 340/409

[51] **Int. Cl.**.....**G08b 13/22**

[58] **Field of Search**.....340/409, 416, 276, 227.1, 253, 340/253 B, 253 Q, 253 S, 256, 253 R, 253 A

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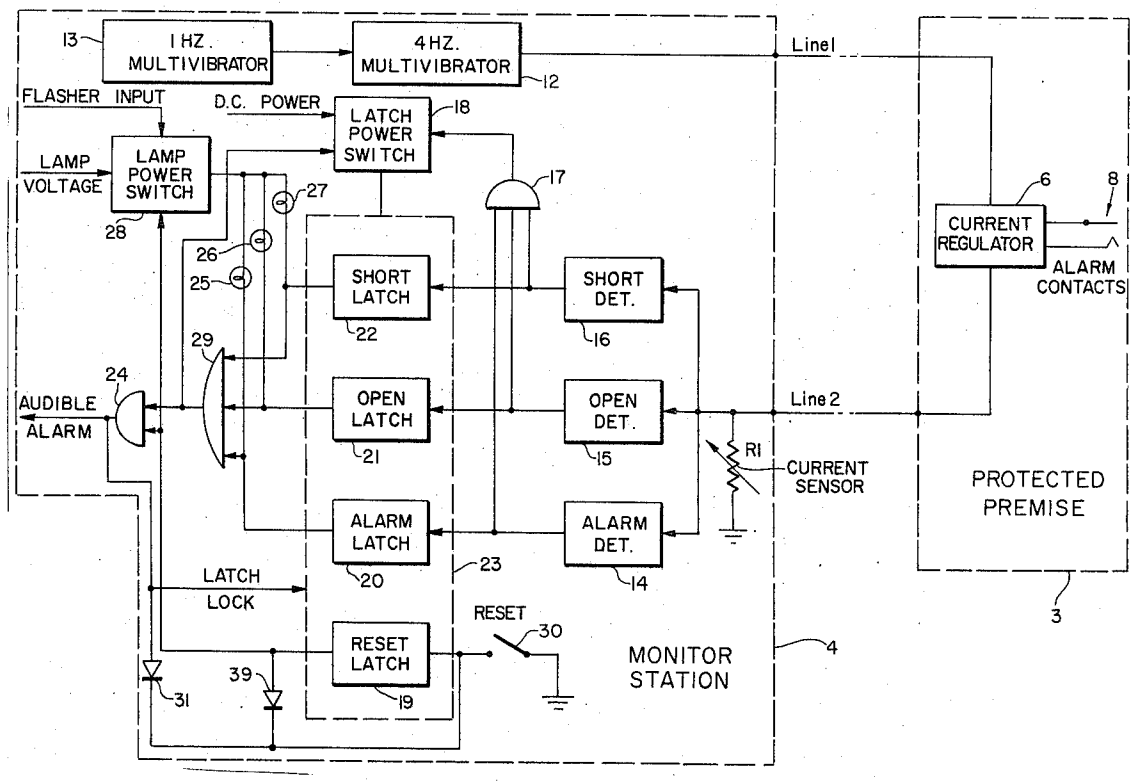
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[57] **ABSTRACT**

A system for insuring the security of electrical transmission lines extending between a monitor station and a remote station utilizes a voltage source at the monitor station which impresses an AC voltage signal on the transmission lines. At the remote station, the AC voltage signal is rectified and the rectified signal is applied to a current regulator which provides a quiescent pulsed direct current of constant level to the transmission lines. The current regulator is arranged to provide a higher alarm current when an intruder is detected at the remote station. At the monitoring station, a shorted line fault detector provides a signal when a reversal in the direction of normal current flow occurs in the transmission lines, an open line fault detector provides a signal when a drop in current below the quiescent current level is detected, and an alarm current fault detector provides a signal when a rise in current above the quiescent current level is detected. The impressed voltage is periodically reduced in amplitude to a level which barely sustains the minimum quiescent current level to test line impedance.

3 Claims, 8 Drawing Figures



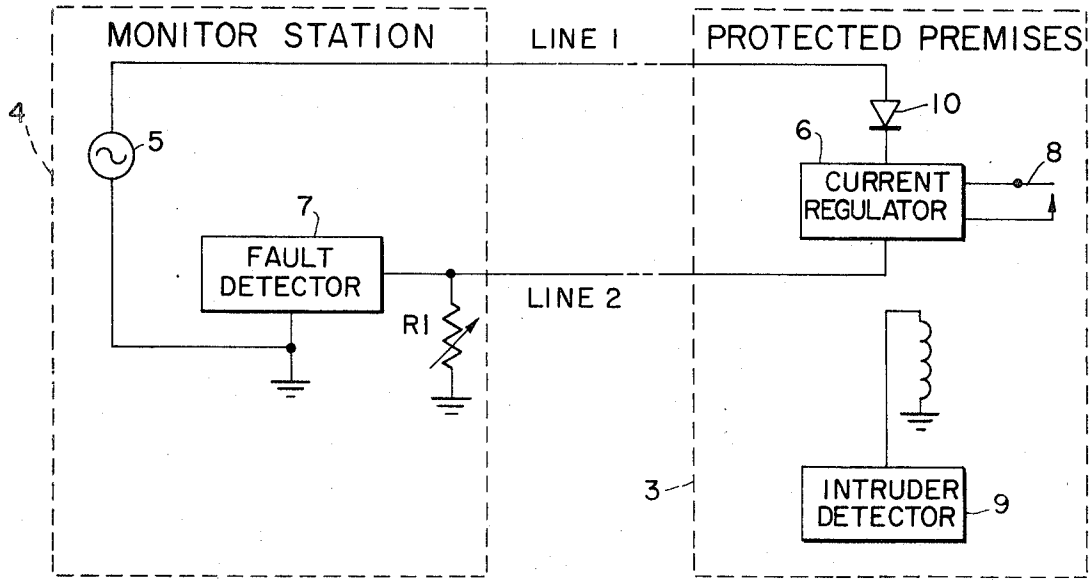


FIG. 1

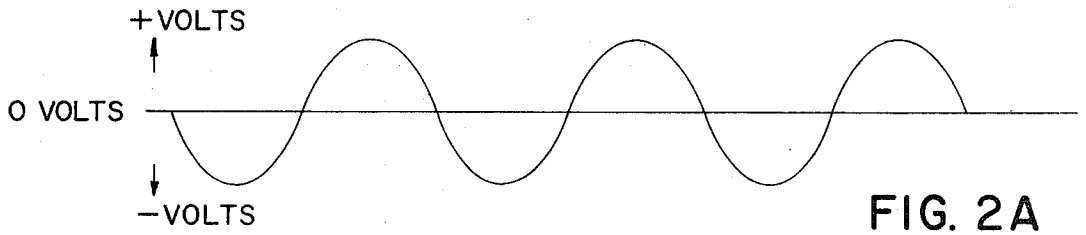


FIG. 2A

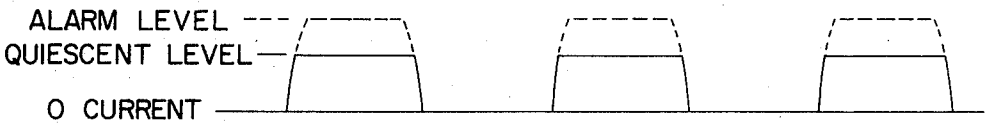


FIG. 2B

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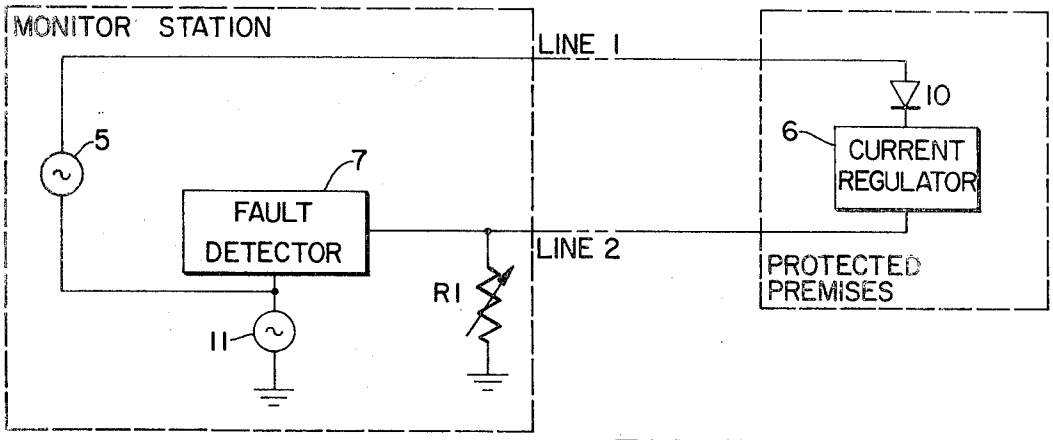
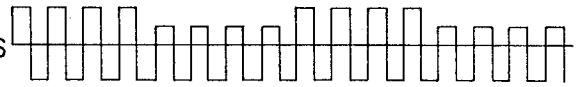


FIG. 3

FIG. 4A



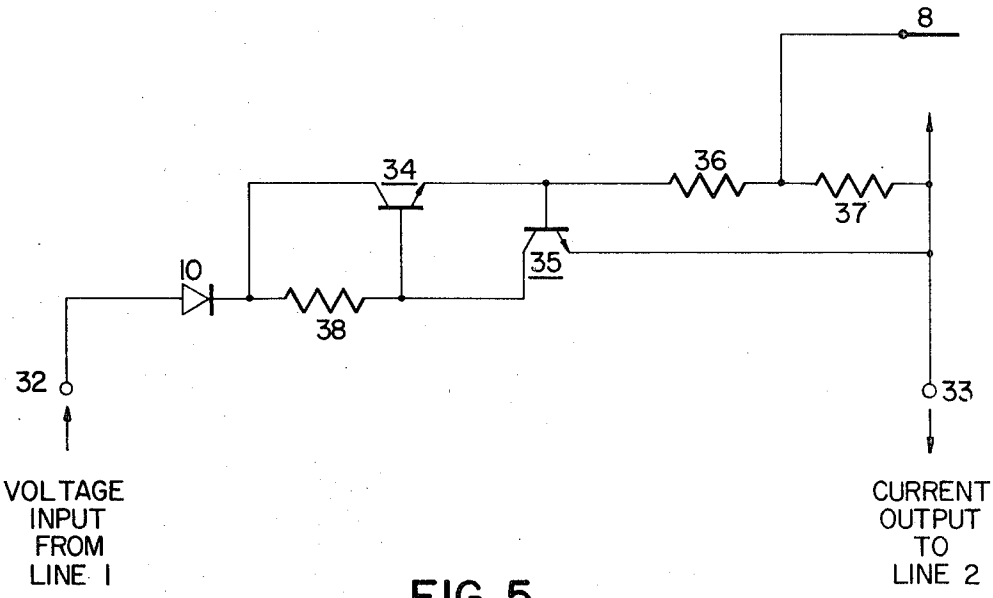


FIG. 5

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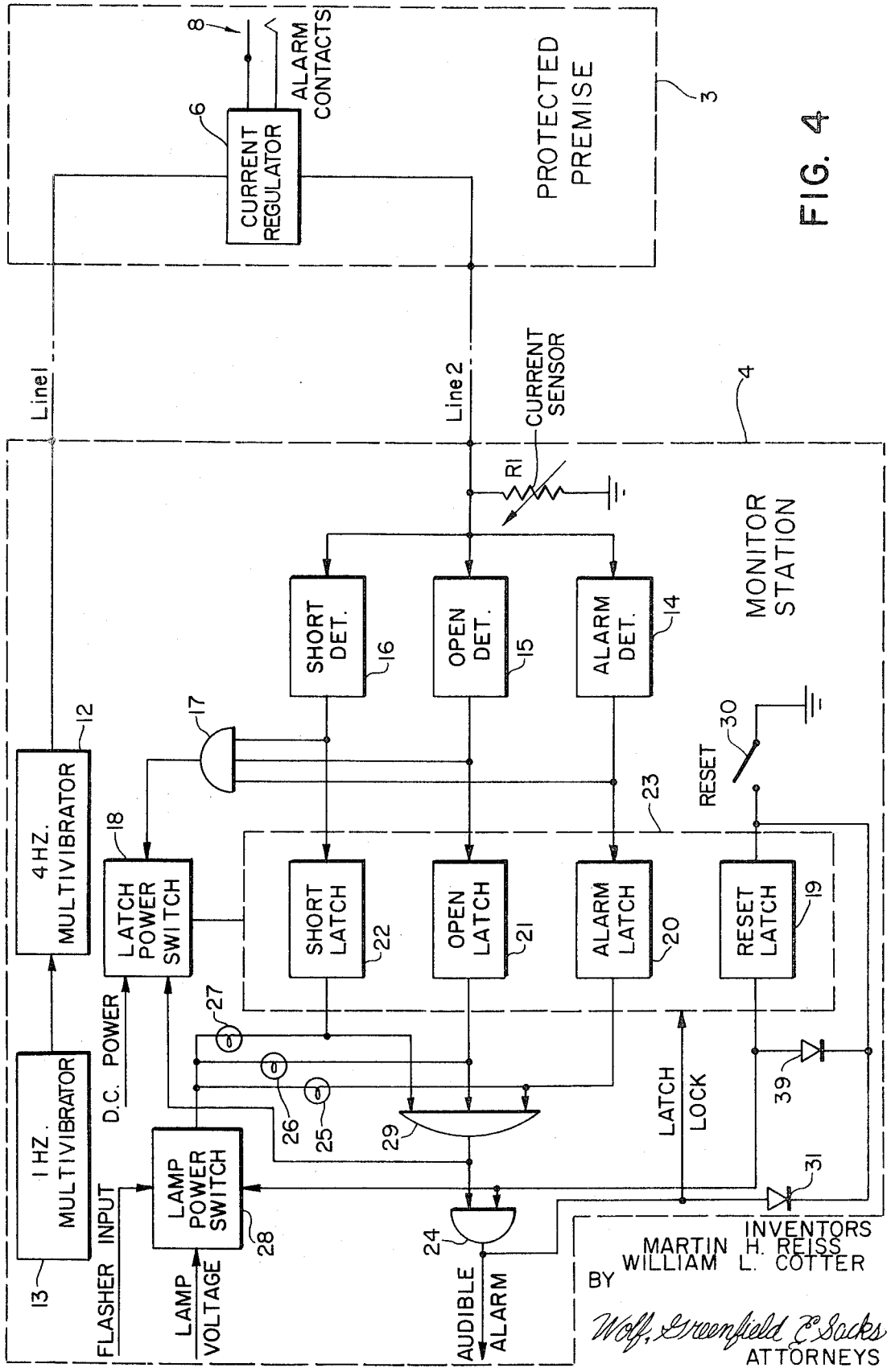


FIG. 4

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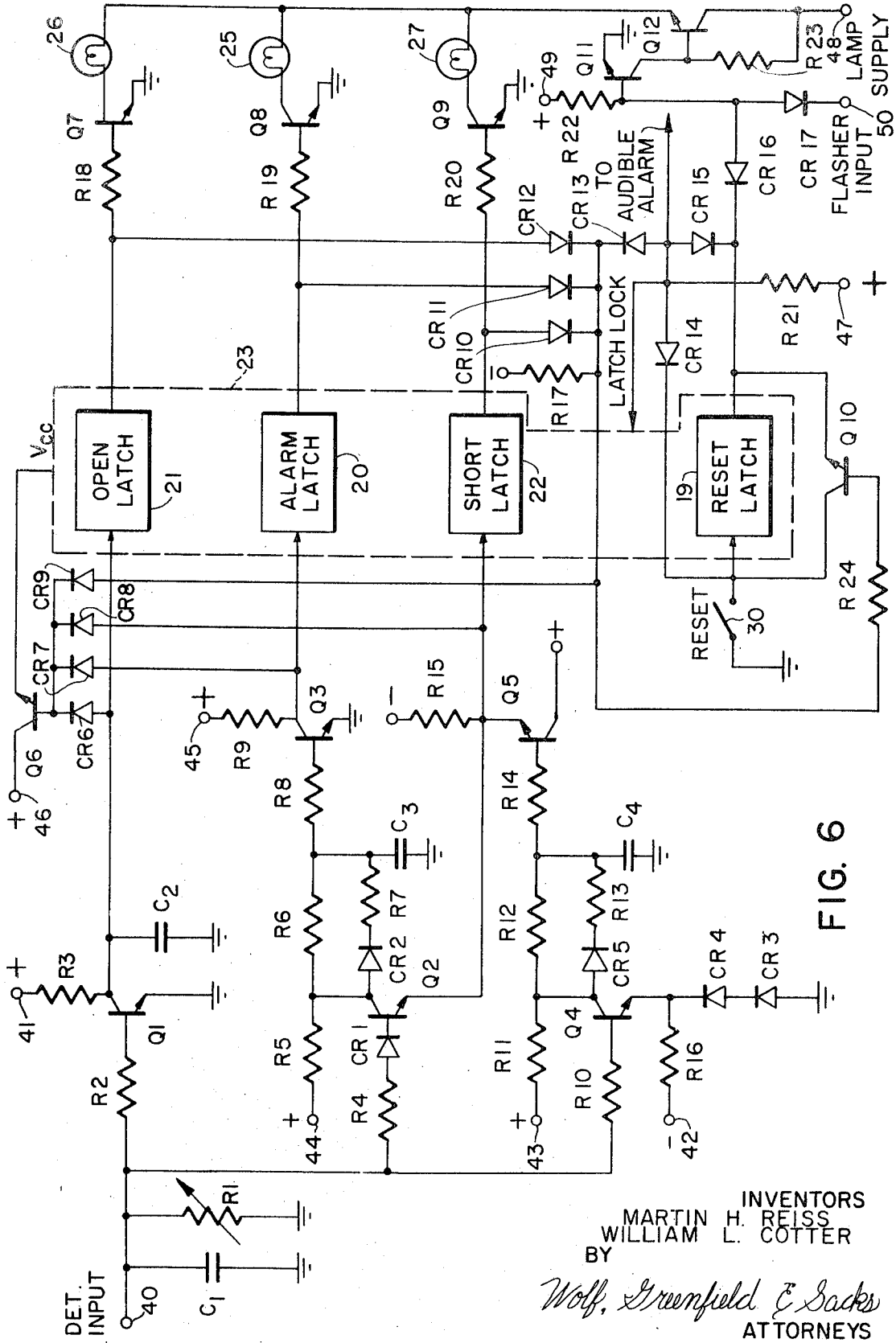


FIG. 6

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LINE SECURITY SYSTEM

FIELD OF THE INVENTION

This invention relates in general to systems for insuring the security of transmission lines. More particularly, the invention relates to apparatus for detecting tampering with a pair of electrical signal transmission lines extending between two separated locations.

BACKGROUND OF THE INVENTION

Where a monitoring station has been connected by electrical transmission lines to intrusion detectors situated at locations remote from the monitoring station, attempts have been made to defeat the intruder detection system by disabling the transmission lines or by placing a false signal on the transmission lines to deceive the monitoring station with indications that conditions are normal at the remote locations. To detect tampering with the transmission lines, devices have been proposed for monitoring some parameter of the transmission lines such as its impedance or an impressed voltage having a designated polarity and amplitude level. However, such devices have not provided the desired security because they are either (1) too sensitive to normal line impedance variations and normal line noise and result in an inordinate number of false line fault indications or (2) the devices are insensitive to some line faults that can disable or deceive the system.

OBJECTS OF THE INVENTION

The principal objective of the invention is to provide a line security system that reliably detects tampering with a pair of electrical transmission lines connecting two remote stations. It is a further object of the invention to provide a line security system having the ability to differentiate between different line fault conditions and to provide an indication which identifies the fault condition that has occurred.

THE DRAWINGS

The invention, both as to its arrangement and its modes of operation, can be better understood from the following exposition when it is considered in conjunction with the accompanying drawings in which:

FIG. **1** depicts the scheme of a rudimentary line security system;

FIGS. **2A** and **2B** depict waveforms occurring in the operation of the rudimentary line security system;

FIG. **3** depicts a modification of the rudimentary system in which the potential of the system relative to ground is altered.

FIG. **4** depicts the preferred embodiment of the invention in block diagrammatic form;

FIG. **4A** illustrates the pulse train voltage signals employed in the preferred embodiment;

FIG. **5** is a schematic drawing showing the details of a current regulator suitable for the preferred embodiment; and

FIG. **6** is a schematic diagram showing, in detail, circuits utilized in the preferred embodiment.

THE EXPOSITION

The block diagram of FIG. **1** depicts the scheme of a rudimentary line security system. A pair of transmission lines **1** and **2** connect the protected premises **3** to the monitor station **4**. At the monitor station is located a voltage source **5** having its output applied by line **1** to a current regulator **6** at the protected premises. The current regulator **6** is a device which converts the applied voltage to a constant current which flows through line **2** to a detector **7** at the monitor station. The current regulator **6** supplies a constant current to the line despite load variations. Thus variations in line conditions have no appreciable affect upon the current supplied by regulator **6**. The magnitude of the current supplied by regulator **6**, however, can be increased by causing contacts **8** to close. At the protected premises are located one or more intruder detection devices **9**, which, when activated cause contacts **8** to close.

The current regulator **6**, therefore, supplies a quiescent current when conditions at the protected premises are normal and emits a higher current if the intrusion detectors are activated at the protected premises. Where line **1** or **2** is cut to create an open circuit, no current will flow in the lines. By using the higher current output of regulator **6** to denote an "alarm" (i.e., the detection of an intruder) at the protected premises, the normal condition (viz the presence of a quiescent current) is bracketed on either side by a fault condition.

It is desirable for maximum security, to be able to detect three abnormal line conditions, i.e., an open line, a shorted line, and the transmission of an "alarm" signal by an increase in the current. The terms "shorted line" and "open line" employed in this exposition signify conditions where either a series or shunt impedance of a value adequate to adversely effect the ability of the intrusion detector to signal the monitor has appeared on the line. The rudimentary system thus far described detects only abnormal line conditions caused by an alarm signal (viz high current) or caused by an open line (viz low current). The third abnormal condition, where the line is shorted, can be detected by employing an alternating current (AC) source to furnish the voltage that is applied to line **1**. At the protected premises, a rectifier **10** is placed in series with current regulator **6**, as indicated in FIG. **1**. Regulator **6** then furnishes current only during alternate half cycles of the input voltage signal when the rectifier permits current to flow. Thus, if the rectifier is arranged to permit current to flow on the "positive" swing of the signal voltage, the regulator **6** emits current, as indicated in FIG. **2B**, only when the signal voltage indicated in FIG. **2A** swings "positive" above the zero voltage level. In FIG. **2B**, the quiescent current level is indicated in full lines whereas the "alarm" current level is indicated by broken lines. Where an attempt is made to bridge or shunt the transmission lines, then reverse current will flow in the lines if the bridge or shunt does not include a properly poled rectifier. This reverse current flows through the detector **7** in the monitor station and causes the detector to indicate a "shorted line" fault in the transmission lines. In the FIG. **1** system, the presence of an intrusion alarm at the protected premises is signified by a high current in the transmission line, an open line is signified by low or no current, and a shunted line is signified by reverse current. The employment of an AC voltage source has the additional advantage of reducing the probability of a potential tamperer measuring the normal line conditions with the intent of introducing a false signal into the line. A frequency of about 4 Hz. is sufficient to prevent measurement of the line conditions with an ordinary voltmeter or ammeter since the meter movements cannot follow the signal variations.

A second technique that can be used to make the measurement of the normal line conditions by a potential intruder more difficult, is to insert, as shown in FIG. **3**, an AC signal source **11** between the line security system and ground. The AC signal has no effect on normal operation of the security system while eliminating a fixed ground reference by which the line impedance can be determined. By inserting the AC signal source **11**, the possibility of measuring the line impedance and inserting an impedance in the line which provides the same quiescent current as the current regulator **6** provides is made more remote.

A mode exists which could be employed to defeat the rudimentary security system, thus far described. This mode assumes prior knowledge of the system and careful measurement of line conditions by a trained person. Any current source has a limiting drive condition which is reached when the series impedance becomes so large that the voltage source is no longer adequate to drive the current furnished by the source. In the line security system of FIG. **1**, current regulator **6** provides a higher current when an intrusion detector is activated (viz, a higher current for the "alarm" condition). It is impossible to insert in the transmission line a series impedance of a value that permits the voltage source **5** to drive the quiescent current of regulator **6** but does not permit the volt-

age regulator to drive the full alarm current. This possibility can be obviated by making the ratio of quiescent current to alarm current small so as to make it difficult to realize the correct impedance to defeat the security system. A small difference in magnitude between the quiescent current and alarm current, however, requires more stability by the current regulator and more sensitivity for the detector. An alternative to utilizing an alarm current that is but slightly higher than the quiescent current is to effectively test the condition of the line intermittently to insure that the line impedance is not excessive. The test is performed by reducing the voltage of source **5** (FIG. 1) occasionally to a value that will drive the quiescent current through the line if the line impedance is not excessive, but the reduced voltage will cause a sufficient reduction in quiescent current to indicate a "line open" condition if the line impedance is great enough to prevent the normal voltage from driving the alarm current through the line.

FIG. **4** is a block diagram depicting the scheme of the preferred embodiment of the invention. The voltage source at the monitor station is a free running multivibrator **12** having a frequency of 4 Hz. The output of multivibrator **12** is a train of square waves, as shown in FIG. 4A, having equal amplitude above and below the zero volt axis. To recurrently test the condition of lines **1** and **2** to insure that the line impedance is not so excessive as to prevent the full alarm current from being driven by the voltage source, multivibrator **13** which has a 1 Hz. frequency, causes the amplitude of the pulses emitted by multivibrator **12** to be reduced in amplitude, as indicated in FIG. 4A. The reduced amplitude pulses are sufficient to drive the quiescent current of current regulator **6** through the line if the line impedance is not excessive. In the pulse train depicted in FIG. 4A half the pulses are of full amplitude while the other half are of reduced amplitude. The ratio of full amplitude pulses to reduced amplitude pulses is purely arbitrary, as are the frequencies of multivibrators **12** and **13**. The voltage pulse train is transmitted over line **1** where only the positive going portions of the pulses are permitted by rectifier **10** to pass to current regulator **6**. The positive pulses are converted by regulator **6** to current pulses of uniform amplitude (i.e., a "-pulsing" constant current). Upon closure of alarm contacts **8**, the magnitude of the constant current increases to furnish an "alarm" current. The current output of regulator **6** flows through line **2** to a current sensing resistor R1. Resistor R1 converts the current to a voltage by the voltage drop which occurs across the resistor when the current flows through the resistor to ground. The voltage developed across resistor R1 is monitored by three detectors **14**, **15**, and **16** to insure that a significant change in the quiescent current does not pass unperceived. Alarm detector **14** is sensitive to a significant increase in voltage across resistor R1, open line detector **15** is sensitive to a significant decrease in voltage across resistor R1, and shorted line detector **16** is sensitive to "reverse" current flow. Each of the detectors **14**, **15**, **16** has its output applied to an OR-gate **17** which, in turn, has its output impressed on a latch power switch **18**. The latch power switch controls the application of DC power to the four latches **19**, **20**, **21**, **22** shown within the block **23**. Short latch **22** has its input derived from the output of shorted line detector **16**; open latch **21** has its input signal derived from the output of open line detector **15**; and alarm latch **20** has its input derived from the output of alarm detector **14**. The outputs of detectors **14**, **15** and **16** is a DC signal. Each latch has the characteristic that the output of the latch follows its input unless the latch lock line is activated by a signal from AND-gate **24**. Where the latch lock line is activated, the latches all remain locked in the states they were in when the signal from AND-gate **24** was first applied to the latch lock line. When so locked, the latches do not respond to the input signals from the detectors and the latches remain unresponsive until the lock signal from AND-gate **24** is removed. DC power is not normally applied by switch **18** to the latches in order to conserve power. This is done to prevent a drain on the emergency power system in the event the normal power system is disabled. The detection of a fault condition by any one of detectors **14**, **15** or **16** causes one of the inputs to OR-gate **19** to be activated. The output signal from the OR-gate causes switch **18** to apply DC power to the latches. The latch **20**, **21** or **22**, then permits the signal from detector **14**, **15** or **16** to be transmitted to the output of the latch. The output of latches **20**, **21**, and **22** are connected respectively to lamps **25**, **26**, **27** which are mounted on a panel at the monitor station. The lighting of lamp **25** indicates that an intruder has been detected as the protected premises. The lighting of lamp **26** indicates an open condition in the transmission line whereas the lighting of lamp **27** indicates a shorted condition of the transmission line. The lighted lamp is made to flash by applying a "-flasher" modulating signal to the lamp power switch **28** which is connected to each of the lamps.

The latches **20**, **21**, and **22** have their outputs coupled to an OR-gate **29** whose output provides one of the inputs to AND-gate **24**. Where the other input to AND-gate **24** is enabled, an enabling signal from OR-gate **29** causes the AND gate to activate the latch lock line. Activation of the latch lock line prevents the latches from changing states so that if any of lamps **25**, **26**, or **27** is lit, it remains lit even though the fault is removed. The output of OR-gate **29** is coupled to latch power switch **18** to insure that power is maintained although there is no further output signal from detector **14**, **15** or **16**. The output of AND-gate **24** also actuates an audible alarm (not shown) to alert the personnel at the monitor station that a fault has occurred. Upon noting that a fault has occurred, the operator at the monitor station can close the reset switch **30**. Upon closure of switch **30**, the output of AND-gate **24** is connected to ground through diode **31** thereby removing the signal from the latch lock line. The reset latch **19**, which had been providing an enabling signal to AND-gate **24**, has its input grounded by closure of reset switch **30**. The reset latch thereupon causes its output to inhibit AND-gate **24** whereupon that gate ceased to activate the latch lock line. The reset latch remains latched in this state through diode **39**. If the fault had been removed from the system, the fault indicator lamp would go out and the system would return to normal quiescent operation. However, where the fault is still present when the reset switch is actuated, the fault lamp would remain lit but the audible alarm would be discontinued by the inhibiting of AND-gate **24**. The output of reset latch **19** is connected to lamp power switch **28**. The lamp power switch, in response to a signal from reset latch **19**, overrides the flasher input and causes the indicator lamp to become steady. When the fault condition is removed from the system, the steady indicator lamp goes out and the system returns to normal operation without requiring any further action by the operator at the monitor station after closure of the reset switch.

FIG. **5** schematically depicts a circuit which is suitable for employment as the current regulator **6** in the preferred embodiment of the invention. Line **1** is connected to input terminal **32** of the current regulator and line **2** is connected to the regulator's output terminal **33**. Rectifier **10** is in series with the current regulator and rectifies the input voltage signal applied at terminal **32**. NPN-transistor **34** is the series current regulator and NPN-transistor **35** is the reference amplifier. Resistors **36** and **37** are current sensing resistors, with resistor **37** being shunted by switch **8** when its contacts are closed. The contacts of switch **8** are normally open and are closed by the intruder detector **9** (FIG. 1) at the protected premises upon detection of an intruder. As the input voltage signal at terminal **32** goes positive with respect to terminal **33**, transistor **34** commences to conduct current by virtue of the base current flowing in resistor **38** which is connected between the collector and base of transistor **34**. Initially, transistor **35** is cut off inasmuch as the current through resistors **36** and **37** is insufficient to generate a forward bias at the base of the reference amplifier transistor. However, as the input voltage increases, all the current in resistor **38** comes from the base of transistor **34** and that transistor continues to conduct an increasingly greater current until the voltage drop across resistors **36** and **37** is adequate to forwardly bias the base of reference amplifier transistor **35**.

When transistor 35 conducts, it obtains its collector current from resistor 38 and thereby diverts the base current of transistor 34. As the input signal voltage increases in amplitude, a stable condition is reached where the current through the regulator resistor 34 reaches a steady state value. Where the current tends to increase beyond the steady state value, the base current of transistor 35 increases, causing the collector current of that transistor to also increase and draw current away from the base of regulator transistor 34. Thus, the current available to the base of the regulator transistor is reduced and returns the current through the regulator transistor to the steady state value. The opposite effect occurs where the current through the regulator transistor tends to drop below the steady state value. The output current of the regulator changes to a higher level when the contacts of switch 8 are closed. Upon closure of that switch, resistor 37 is shunted, reducing the forward bias on transistor 35 and causing that transistor to draw less collector current. Where the forward bias is reduced sufficiently, transistor 35 may even reach cutoff. The base current available to regulator transistor 34 is sharply increased causing a larger current to flow from collector to emitter through the regulator transistor. The current through the regulator transistor increases until a new stable state is reached at a higher current level (viz, the alarm current level).

FIG. 6 schematically depicts the detector circuits employed in the apparatus at the monitor station. The current flowing through line 2 appears at the detector input terminal 40 and causes a voltage drop to appear across current sensing resistor R1. The capacitor C1, which shunts the R1 resistor, permits the higher frequency noise on the line to be bypassed to ground. Resistor R1 is variable to accommodate different values of quiescent currents. Transistor Q1 and its associated circuitry comprise the open line detector 15 (FIG. 4). Transistor Q4 and its associated circuitry comprise the shorted line detector 16. Transistor Q2 and its associated circuitry comprise the alarm detector 14. Where the condition of the lines 1 and 2 are normal and the current regulator 6 supplies the quiescent current to the detector input 40, transistors Q1 and Q4 are in their conductive states and transistor Q1 is cut off. The quiescent current, however, flows only during positive cycles of the input voltage and during the half cycle of the input voltage that the quiescent current does not flow, Q1 cuts off and its collector starts to rise toward the positive voltage at terminal 41 as current flows through resistor R3 into capacitor C2. Before the collector can rise to the level necessary to trigger latch 21, the quiescent current reappears and causes transistor Q1 to be biased into conduction. While transistor Q1 is in its conductive state, capacitor C2 discharges through that resistor. To prevent false indications, the time constant of R3–C2 is arranged so that the collector voltage rises to the level adequate to trigger latch 21 only when the quiescent current is missing over several half cycles.

The base of NPN-transistor Q4 is connected by resistor R10 to current sensing resistor R1. The emitter of transistor Q4 is biased slightly negative with respect to ground by applying a negative potential at terminal 42 to cause current to flow through diodes CR3, CR4 and resistor R16. The voltage drops occurring in diodes CR3 and CR4 cause the emitter of Q4 to be held slightly negative with respect to ground. Where lines 1 or 2 are open circuited, no quiescent current flows to terminal 40. However, transistor Q4 can still derive its base current through resistor R1. Where sufficient reverse current is drawn through resistor R1, due to tampering with the transmission lines, Q4 will be biased to cutoff. Reverse current flows through R1 when an attempt is made to shunt the transmission lines without having a properly poled rectifier in the shunt. Thus when a shunt is placed across the transmission lines, transistor Q4 cuts off every half cycle. When cut off, the collector of Q4 commences to rise to the positive voltage impressed at terminal 43 because of the current flowing through resistor R11, diode CR5, and resistor R13 into capacitor C4. The time constant of that charging path is selected to provide integration of successive current charges in order to reduce false alarms due to reverse current flow which does not persist for a sufficient time to constitute a "fault." Diode CR5 prevents capacitor C4 from discharging through resistor R13. Resistor R12, provides a discharge path for capacitor C4 when Q4 is conducting, but the value of resistor R12 is such as to prevent excessive discharge of the capacitor during conductive half cycles of Q4. The voltage across capacitor C4 is coupled through resistor R14 to the base of transistor Q5 which is arranged to function as an emitter follower. The emitter of transistor Q5 provides the drive current required for the input of latch 22.

Transistor Q2 in the alarm detector, unlike transistors Q1 and Q4, is normally cutoff when the quiescent current flows. The base of transistor Q2 is coupled to voltage sensing resistor R1 by resistor R4 and diode CR1. The emitter of Q2 is connected to the emitter of Q5. The collector of Q5 is connected by resistor R5 to the positive voltage impressed at terminal 44. The collector of Q5 is also connected through diode CR2 and resistor R7 to capacitor C3. The voltage across capacitor C3 is coupled through resistor R8 to the base of NPN-transistor Q3 which has its emitter grounded and its collector connected by resistor R9 to the positive voltage at terminal 45. The input signal to alarm latch 20 is obtained from the collector of transistor Q3. When the quiescent current flows to detector input terminal 40, transistor Q2 is biased off by the normal base to emitter voltage drop plus the voltage drop occurring across diode CR1. Where the current to terminal 40 increases (as where an "alarm" current is emitted by the current regulator 6) and that increase is sufficient to exceed the forward drop of the base and the diode CR1, Q2 is biased into conduction on the half cycles when the increased current flows. In the normal condition of the system with Q2 cut off, C3 charges to a positive voltage of sufficient magnitude to drive the base of transistor Q3 and cause that transistor to conduct so that its collector potential is only slightly above ground potential. Upon the occurrence of an "alarm" current at terminal 40, transistor Q2 conducts and permits capacitor C3 to discharge through resistor R6 and the transistor. If transistor Q2 conducts on a series of successive half cycles, capacitor C3 discharges sufficiently to cause Q3 to cut off. The circuit is arranged to prevent a single half cycle of Q2 conduction from causing Q3 to cut off. When transistor Q3 cuts off, the voltage at its collector rises to the level required to trigger alarm latch 20. Resistor R5, diode CR2, and resistor R7 constitute a charging path for capacitor C3 when Q2 is cut off. Resistor R6 shunts diode CR2 and resistor R7 and also provides a charging path for capacitor C3. To permit diode CR2 and resistor R7 to govern the charging time in conjunction with resistor R5, resistor R6 must be fairly large relative to resistor R7.

A "fault" condition of the system causes one of the detectors to emit a positive voltage signal to the input of its associated latch. The positive signal is applied through diode CR6, CR7, or CR8 to the base of transistor Q6. The collector of Q6 is tied to terminal 46 at which a positive supply voltage is applied. The emitter of Q6 is connected to the power (V_{cc}) input terminal of the latch module 23. The module 23 is a "Quad Latch" integrated circuit, such for example as the N-8275-B quad latch manufactured by Signetics Inc. The application of a positive signal to the base of transistor Q6 causes that transistor to conduct and apply power to the power input of the quad latch module. Upon the application of power to quad latch module 23, the latches 19, 20, 21, and 22 can respond to the signals applied to their inputs. Where a positive input signal is applied to one of the latches, the output of that latch furnishes a positive signal since the output of the latch follows its input. Where for example, a positive signal is applied by transistor Q3 to the input of alarm latch 20, the output of the alarm latch biases transistor Q8 into conduction, thereby causing indicator lamp 25 to be lit. Similarly, a signal from the output of latch 21 causes transistor Q7 to conduct and light lamp 26. A signal from the output of latch 22, similarly, biases transistor Q9 into conduction and cause the lighting of lamp 27.

The output of each of latches **20**, **21**, and **22** is coupled to a logical OR gate **29** (FIG. 4) consisting of diodes CR10, CR11, and CR12 and the resistor R17 which has one end tied to a negative voltage source. The output of the logical OR gate is connected to diode CR9 to assure that power (*Vcc*) is maintained at the power input of module **23** even where the detected fault is a transient condition. The output of the logical OR gate is also connected by resistor R24 to the base of transistor Q10 to insure that reset latch **19** will reset when the reset switch **30** is closed and the fault is removed from the system. The output of the logical OR-gate **29**, as indicated in FIG. **4**, is tied to one input of AND-gate **24**. In FIG. **6**, that AND gate is formed by diodes CR13, CR14, and CR15 in conjunction with resistor R21 which is tied to terminal **47** at which a positive voltage is impressed. When enabled, the output of the AND gate activates an audible alarm and locks the latches so that the latches cannot change states. In the reset condition of latch **19**, the output of the latch is a positive voltage so that diode CR15 is normally reversely biased. An output signal from any one of latches **20**, **21**, or **22** causes diode CR13 to be reversely biased, whereupon the output of the AND gate rises toward the voltage at terminal **47**, causing the latch lock and the audible alarm to be activated. Upon closing reset switch **30**, the output of the AND gate is shunted to ground through diode **14**.

The lamp supply is a DC voltage impressed at terminal **48** and is coupled through transistor Q12 to the lamps **25**, **26**, and **27**. Transistor Q12 functions as a power switch in series with the lamp supply. Transistor Q11 has its collector coupled to the base of Q12 and through resistor R23 to the DC voltage at terminal **48**. The emitter of Q11 is grounded and its base is connected to a logical OR circuit constituted by diodes CR16 and CR17 in conjunction with the resistor R22 which has one end connected to the positive voltage at terminal **49**. The input applied to flasher terminal **50** can be the same square wave train (FIG. 4A) impressed upon line **1** of the system. The input to reset latch **19** is normally positive inasmuch as reset switch **30** is normally open. Therefore, the series switch Q12 is alternately turned on and off at the line rate, thereby causing the DC lamp supply voltage to be intermittently applied to the indicator lamps **25**, **26**, and **27**. If a lamp is lit, flashing of the lamp results from the intermittent application of the DC power.

When reset switch **30** is closed, the input to latch **19** is grounded. Simultaneously, the latch lock line is deactivated by being grounded through diode CR14, permitting the output of latch **19** to fall toward ground. With the fall of the output of latch **19**, diode CR15 becomes forwardly biased and disables the AND gate. The output of reset latch **19** is now coupled to its input through transistor Q10. Where the fault condition still exists, Q10 is biased into conduction by the positive voltage on its base, and therefore, the output of latch **19** will drop essentially to ground when the latch is reset. Resetting latch **19** has three effects. First, the fault condition is no longer stored and the system indicates a fault condition only as long as the fault remains. Secondly, the audible alarm is deactivated. Thirdly, the diode CR16 becomes forwardly biased and overrides the flasher so that the indicator lamp changes from a flashing condition to a steady light condition. When the fault is removed, the indicator lamp is extinguished.

Although only the preferred embodiment of the invention has been illustrated and described, it is apparent that the invention can take different forms. For example, the multivibrator for providing the varying voltage signals to the transmission lines can be replaced by other devices for producing AC voltage signals. As another example, the fault detectors need not employ the precise circuitry set out in FIG. **6**. It is obvious to those skilled in the art of electrical security systems that modifications of the preferred embodiment may be made without departing from the underlying inventive concept. It is intended therefore that the invention not be restricted to the precise arrangement and circuits here illustrated, but rather that the invention be delimited by the appended claims and include only those systems that do not fairly depart from the essence of the invention.

We claim:

1. A system for insuring the security of electrical transmission lines extending between a monitor station and a remote station, the system comprising

a current regulator at the remote station, the current regulator being connected to the transmission lines and providing a quiescent pulsed direct current of constant level in response to an impressed periodic AC voltage, the current regulator having actuable means for causing the pulsed direct current to increase to a higher alarm current level upon the occurrence of an event at the remote station,

monitoring apparatus at the monitor station, the monitor apparatus being connected to the transmission lines and comprising

means for applying a periodic AC voltage to the transmission lines,

an open line detector having its input signal obtained from the current flowing in the transmission lines, the open line detector providing an output signal in response to a drop in current below the quiescent current level,

means for intermittently reducing the AC voltage applied to the transmission lines to a level barely sufficient to maintain the current at the quiescent current level when the impedance of the transmission lines is within the impedance range that is normal for such lines,

a shorted line detector having its input obtained from the current flowing in the transmission lines, the shorted line detector providing an output signal in response to a reversal in the direction of normal current flow in the transmission lines,

and an alarm current detector having its input obtained from the current flowing in the transmission lines, the alarm current detector providing an output signal in response to a rise in current to the alarm current level.

2. The system according to claim **1**, further including

rectifier means at the remote station, the rectifier means causing the current regulator to provide direct current in the transmission lines in response to the impressed AC voltage.

3. The system according to claim **2**, wherein the monitoring apparatus further includes

latch means connected to the output of each of the detectors, the latch means responding to an output signal from a detector by storing the output signal,

and latch reset means for removing the stored signal.

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