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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :	A1	(11) International Publication Number: WO 96/10840
H01L 21/8246, 21/8247		(43) International Publication Date: 11 April 1996 (11.04.96)

(21) International Application Number: PCT/US95/11563

(22) International Filing Date: 13 September 1995 (13.09.95)

(30) Priority Data:
08/315,876 30 September 1994 (30.09.94) US

(71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

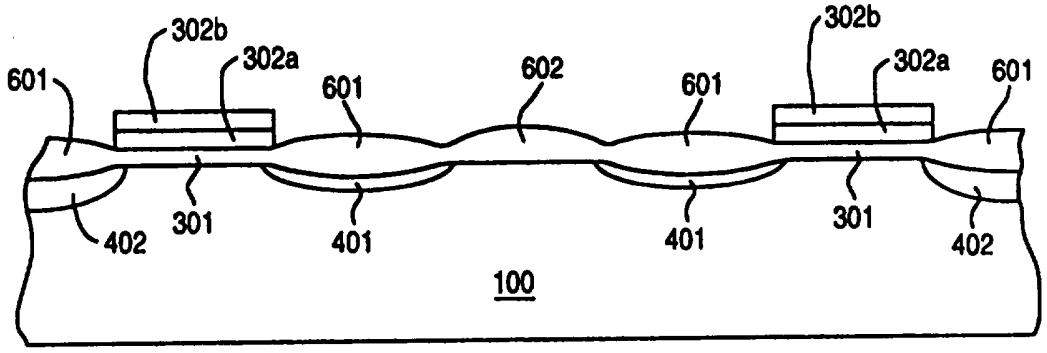
(72) Inventors: ONG, Tong-Chern; 1820 Mayall Court, San Jose, CA 95132 (US). TANG, Daniel, N.; 1692 Baclen Court, San Jose, CA 95132 (US).

(74) Agent: VINCENT, Lester, J.; Blakely, Sokoloff, Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025-1026 (US).

(81) Designated States: AM, AT, AT (Utility model), AU, BB, BG, BR, BY, CA, CH, CN, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TT, UA, UG, UZ, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG), ARIPO patent (KE, MW, SD, SZ, UG).

Published
With international search report.

(54) Title: IMPROVED ISOLATION BETWEEN DIFFUSION LINES IN A MEMORY ARRAY



(57) Abstract

A method of forming a memory device with improved isolation between diffusion lines. Parallel, spaced apart thick oxide strips (201) are grown on a substrate. Next, spaced apart, parallel strips (302) having a polysilicon (302a) and nitride (302b) layer, oriented perpendicular to the first strips (201), are formed. The oxide (201) between the second strips is removed, followed by an implantation to form source (402) and drain (401) regions. The nitride layer (302b) on the second strips is removed on those strips between two drain diffusions (401) and an oxidation is performed to form self-aligned thick oxide (602) over the source and drain regions. The strips from which the nitride has been removed are also oxidized, thus providing isolation between adjacent drain lines.

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IMPROVED ISOLATION BETWEEN DIFFUSION LINES IN A MEMORY ARRAY

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to memory devices, and more particularly to a method and apparatus for improved isolation between diffusion lines of the memory device.

2. Background Information

Numerous memory devices, including read only memory (ROM), programmable read only memory (PROM), electrically programmable read only memory (EPROM), electrically erasable programmable read only memory (EEPROM), etc., are well known and commercially available. In these devices, the memory can be arranged in an array comprising parallel, elongated, spaced-apart diffusion regions which function as the source and drain of the array. In this type of layout, the individual memory cells are arranged in rows and columns, with all cells in a column sharing a single drain diffusion and sharing a single source diffusion. Additionally, the source and drain regions typically alternate, such that adjacent columns of cells share each source and drain region. Strips of polysilicon run perpendicular to the diffusion regions to form the control gates.

Although sharing the same drain region with an adjacent column of cells results in a smaller cell size, this scheme complicates the decoder since, to access a cell, in addition to addressing the drain and word line of the cell, it is necessary to address one of the two source regions on each side of the drain. Additionally, a problem which may occur in such cells is parasitic program disturb, wherein an erased cell may get programmed during the programming of another cell on the same word line. This occurs because programming is typically accomplished by applying a voltage of, e.g. 12V, on the word line, a voltage of, e.g. 6V, on the drain line, and grounding the source of the cell to be programmed. In this

situation, if the source of another cell on the same word line is allowed to float, it may be turned on temporarily as its capacitance is charged, and hence may be programmed. Therefore, to overcome this problem, most devices require complicated disturb prevention circuitry which, for example, holds the source of the cell that is not being programmed at some voltage during programming.

What is needed is a method for forming a non-volatile memory array with improved isolation between diffusion lines. The method should be compatible with conventional processing and allow for forming a variety of memory devices which do not require complicated decoders or disturb prevention circuitry.

SUMMARY OF THE INVENTION

A method of forming an array of memory devices is disclosed. First, parallel, spaced-apart strips comprising, e.g., nitride, are formed on a semiconductor substrate. Field oxide regions are then formed between the strips. The first strips are removed, a gate or tunnel oxide is grown, and second strips comprising, e.g., a first layer of polysilicon and a layer of, e.g., nitride are formed in a direction perpendicular to the first strips. The field oxide between the second strips is etched, followed by an ion implantation. The nitride layer is removed on some of the second strips. An oxide is grown over the source and drain regions, to form buried source and drain regions. Additionally, in this step, the polysilicon of the second strips which have had the nitride layer removed are oxidized as well. In this way, improved isolation between the diffusion lines is obtained. Next, a second layer of polysilicon is deposited. The second layer may, together with the polysilicon of the second strip, comprise the gate for a single polysilicon memory array. Alternatively, these layers may form the floating gate of a floating gate memory device. Next, an intergate dielectric, followed by a third polysilicon layer is deposited. The third polysilicon is defined and an etch is performed to etch the third polysilicon, the intergate dielectric, the second polysilicon layer, and the first polysilicon layer between the third polysilicon lines.

Additional features and benefits of the present invention will become apparent from the detailed description, figures, and claims set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the accompanying figures in which:

Figure 1A shows a top view of a semiconductor substrate after formation of first strips.

Figure 1B shows a cross-sectional view of the structure of Figure 1A.

Figure 2A shows the structure of Figure 1A after an oxidation step.

Figure 2B shows a cross-sectional view of the structure of Figure 2A.

Figure 3A shows the structure of Figures 2A and 2B after formation of second strips.

Figure 3B shows a cross-sectional view of the structure of Figure 3A.

Figure 4A shows the structure of Figure 3A and 3B after an oxide etch.

Figure 4B shows a cross-sectional view of the structure of Figure 4A.

Figure 5A shows the structure of Figures 4A and 4B after the nitride layer has been removed from some of the second strips.

Figure 5B shows a cross-sectional view of the structure of Figure 5A.

Figure 6 shows a cross-sectional view of the structure of Figures 5A and 5B after an oxidation has been performed.

Figure 7A shows the structure of Figure 6 after formation of polysilicon strips over the second strips in the fabrication of a floating gate memory device.

Figure 7B shows a cross-sectional view of the structure of Figure 7A.

Figure 8 shows a cross-sectional view of the structure of Figures 7A and 7B after deposition of an insulator, third polysilicon layer, and masking layer.

Figure 9 shows a top view of the structure of Figure 8.

Figure 10 show the structure of Figure 9 after an etch step.

Figure 11A shows the structure of Figure 6 after deposition of a polysilicon layer and formation of a patterning layer in the fabrication of a ROM device.

Figure 11B shows a cross-sectional view of the structure of Figure 11A.

DETAILED DESCRIPTION

A method of forming a memory array with improved isolation between diffusion lines is disclosed. In the following description, numerous specific details are set forth such as specific materials, device layers, fabrication steps and sequences, dimensions, etc. in order to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art that these specific details need not be employed to practice the present invention. In other instances, well known materials or methods have not been described in detail in order to avoid unnecessarily obscuring the present invention.

Referring now to **Figure 1A** a top view of a semiconductor substrate 100 is shown. Prior to the point in processing in **Figure 1A**, in a currently preferred embodiment, substrate 100 has had pad oxide 101 grown thereon. In a currently preferred embodiment, pad oxide has a thickness of approximately 100Å-200Å. Next, an oxidation mask is formed by depositing a blanket layer of, for example, nitride, approximately 1000Å-2000Å thick. This blanket layer is then patterned using standard lithographic techniques, and etched to form the strips 102 shown in **Figure 1A**. **Figure 1B** shows a cross-sectional view of the structure of **Figure 1A**, along a portion of the section indicated in **Figure 1A**. Following the stage of processing shown in **Figures 1A** and **1B**, a recess etch is performed to remove a thickness of approximately 1000Å-2000Å of substrate 100 from the regions between strips 102. In one embodiment, this is followed by an ion implantation to increase the threshold voltage of the field oxide strips to be formed between the strips 102, as described below in conjunction with **Figures 2A** and **2B**.

Referring to **Figure 2A** a field oxide 201 is next grown between the strips 102. In a currently preferred embodiment, the field oxide is grown using a conventional local oxidation of silicon (LOCOS) process, to a thickness of approximately 2000Å-3000Å. **Figure 2B** shows a cross-sectional view of the structure **Figure 2A** through a portion of the cross-section indicated in **Figure 2A**. Following the point of processing shown in **Figures 2A** and **2B**, nitride strips 102, along with pad oxide layer 101 are etched away.

Next, a thin oxide, which may be a gate oxide or tunnel oxide, depending upon the device to be formed, is grown in the active areas, i.e. the areas previously covered by strips 102. Typically, the gate or tunnel oxide has a thickness of approximately 100 angstroms or less. Referring to **Figure 3A**, thin oxide 301 is disposed between the field oxide 201, in the regions previously occupied by strips 102. Next, substantially parallel, spaced apart strips 302 are formed above and in a direction substantially perpendicular to the direction of the field oxide 201 and thin oxide 301. Strips 302 are formed by depositing a first layer 302a of, for example, polysilicon, of approximately 500-700 angstroms thickness, followed by a thin layer 302b of, for example, nitride having a thickness of approximately 200 angstroms in a currently preferred embodiment. Next, a patterning layer 302c is deposited and patterned using standard lithographic techniques to define the strips 302. Then, an etch of the polysilicon and nitride layers is performed to form the strips 302. **Figure 3B** shows a cross-sectional view of the structure of **Figure 3A** through a portion of the section indicated in **Figure 3A**. As shown, each of the strips 302 comprise the polysilicon layer 302a, nitride layer 302b, and patterning layer 302c, as described above.

Following the stage of processing shown in **Figures 3A** and **3B**, an etch of field oxide 201, and thin oxide 301, in the regions between the strips 302 is performed. In this step, it is preferable to use an etch having a high selectivity of oxide to silicon. For example, it is desirable that the etch have an oxide silicon selectivity of 10:1 or greater. Etch processes to achieve this are known to one of skill in the art.

Figure 4A shows a top view of the substrate after the etch has been completed. **Figure 4B** shows a cross-sectional view through a portion of the cross-section indicated in **Figure 4A**. As shown in **Figure 4B**, thin oxide 301 remains underneath strips 302, but not between the strips 302. In a similar way, field oxide 201 remains underneath the strips 302 along the cross-section not shown in **Figure 4B**. As can be seen in **Figures 4A** and **4B**, one of regions 401 (which will become drain regions), or regions 402 (which will become source regions), is present between each of the strips 302.

Referring to **Figure 4B**, subsequent to the above-described oxide etch, an ion implantation, as shown by arrows 405 is performed on the substrate to form self-aligned source region 402 and drain regions 401. In a currently preferred embodiment, ion implantation 405 comprises arsenic and/or phosphorous. For example, in one embodiment, both regions 401 and 402 may be implanted with, for example, arsenic to a level in the range of approximately $1x10^{15}$ / cm^2 to $5x10^{15}$ / cm^2. Following this implantation, the patterning layer 302c may be removed, followed by a patterning layer which masks the drain regions 401 while exposing the source regions 402. Then, the source regions 402 may be implanted with phosphorus to a level of approximately $0.2x10^{15}$ / cm^2 to $0.8x10^{15}$ / cm^2 . In this way, during a diffusion step, the source regions will diffuse deeper, with a more gradual dopant ingredient than the drain regions. It will be understood that following implantation, the dopant ions are present near the surface of substrate 100 in the implanted regions. For purposes of illustration, the implanted ions are not shown prior to diffusion in Figures 4A-5B.

Following the stage of processing shown in **Figures 4A** and **4B**, patterning layer 302c, if it has not been removed during the source/drain implants, is removed. Next, an additional patterning layer is used to expose the strips 302 which lie between drain regions 401. For example, in a currently preferred embodiment, every third one of the strips 302 is exposed, which will provide for a shared source region between two drain regions 401, with the drain regions separated from other drain regions by isolation regions. After the patterning layer has been formed, exposing the above-described ones of strips 302, an etch of the nitride layer 302b from the exposed strips 302 is performed. Referring now to **Figure 5A**, as shown, two of the strips 302, identified by cross-hatching and reference numeral 302a, have had nitride layer 302b removed. The remaining strips 302 continue to have both polysilicon layer 302a and nitride layer 302b. In **Figure 5A** the oxide regions 201 and 301 beneath the strips 302 are not shown for clarity. **Figure 5B** shows a cross-section of the structure of **Figure 5A**, through a portion of the section indicated in **Figure 5A**.

Next, a low temperature (for example, approximately 850°C) oxidation is performed in steam to form a self aligned thick oxide on top of the source and drain regions, thus forming buried source and drain regions. Referring to **Figure 6**, a cross-sectional view through the same portion as shown in **Figure 5B**, after the oxidation, is shown. During this oxidation, the regions of the substrate not masked by the strips 302 now have self aligned thick oxide 601 therein, disposed directly above either a source 402 or drain 401. Additionally, the polysilicon layer 302a of the strips 302 between drain regions 401, which have had nitride layer 302b removed, is oxidized to form oxide region 602.

As shown in **Figure 6**, the oxidized polysilicon 602 now serves to isolate the two adjacent bit lines 401, such that each device in a column has its own drain 401 without sharing the drain 401 with adjacent cells. In this way, the decoder design is made less complicated since there is no need to address the source region 402. Additionally, because the drain is common to the cells in a single column, and is not adjacent to two sources, there is no need to apply a disturb prevention voltage to other sources along the same word line. Thus, the problem of program disturb is prevented, thereby eliminating the need for disturb prevention circuitry. Following the oxidation, the nitride layer 302b is removed from the remaining strips 302, to expose the polysilicon layer 302a.

The array of the present invention may be used, for example, for single polysilicon memories such as read only memories (ROM) and may also be used for various floating gate type memories. In an embodiment where a floating gate device is formed, in a preferred embodiment a layer of, for example, polysilicon is deposited and patterned as shown by polysilicon lines 702 of **Figure 7A**. As shown, each of the polysilicon strips 702 overlaps each of the first strips 302a which were not oxidized, on both sides. This overlap provides full coverage of the first polysilicon strip 302a, which provides for good control of the polysilicon etch in forming the strips 702, since no etch of the first polysilicon strip 302a can occur during the etch to form the strips 702. Also shown in **Figure 7A** is the oxide layer 602 formed from the first polysilicon layer 302a in the strips 302 between diffusion regions 401. Although thick oxide regions

601 are not shown in **Figure 7A**, they are understood to be present alongside the oxide regions 602 and generally continuous therewith as shown in **Figure 6**.

Referring now to **Figure 7B**, a cross-sectional view of the structure of **Figure 7A**, along a portion of the section indicated in **Figure 7A**, is shown. As can be seen in **Figure 7B**, since the source regions 402 and drain regions 401 are buried beneath the thick oxide region 601, the second polysilicon layer 702 may have the overlap described above without contact to the source regions 402 or drain regions 401. Additionally, as shown, second polysilicon layer 702 overlaps on the side of the drain 401 to a greater extent than on the side of the source 402. As will be seen, the polysilicon layers 302a and 702 together comprise the floating gate of the device. By overlapping the drain 401 to the extent shown, good floating gate to drain capacitive coupling is achieved, which is helpful in the programming and reading of many types of devices. Additionally, with only a minimal floating gate to source overlap, high fields may be established allowing for faster erase from the source 402.

It will be appreciated that the second polysilicon layer 702 may overlap either the source 402 or the drain 401 to a greater or lesser extent than that shown depending upon desired device characteristics. It will also be appreciated that in some devices, the polysilicon layer 702 may not be needed, and the floating gate may be made from polysilicon layer 302a alone.

Following the stage of processing shown in **Figure 7A** and **Figure 7B**, one or more dielectric layers is deposited on the substrate. For example, in a currently preferred embodiment a three layer composite dielectric comprising a first oxide layer having a thickness in the range of approximately 50Å, a layer of nitride having a thickness of approximately 100Å, and a second oxide layer having a thickness of approximately 50Å is deposited. Referring briefly to **Figure 8**, which is along the same cross-section as **Figure 7B**, this composite dielectric layer is shown as intergate dielectric 801. Following deposition of the composite intergate dielectric 801, a conductive layer comprising, in a currently preferred embodiment polysilicon having a thickness in the

range of approximately 1500Å, and a metal or silicide layer such as tungsten or tungsten silicide having a thickness in the range of approximately 1500Å is deposited, as shown by layer 802 of **Figure 8**. Next, a patterning layer 805 is formed by standard lithographic techniques.

Referring now to **Figure 9**, a top view of the structure of **Figure 8** is shown. The location of the cross-sectional view of **Figure 8** is indicated in **Figure 9**. As can be seen, patterning layer 805 is patterned into strips which run substantially perpendicular to the polysilicon strips 702 and disposed substantially above the active area of the device, including above the region having tunnel oxide 301.

After formation of the patterning layer 805, an etch through the polysilicon layer 802, intergate dielectric layer 801, polysilicon layer 702, and polysilicon layer 302a, in the regions not covered by the patterning layer 805 is performed. Following the etch, and removal of patterning layer 805, the substrate appears as shown in **Figure 10**. In each cell, the floating gate comprises polysilicon layer 302a, and polysilicon 702 which overlaps and is in contact with layer 302a as discussed previously. Further, the strips 802 form the control gate of the device. In **Figure 10**, four columns of devices, 1010, 1011, 1012, 1013, are shown. As described previously, while adjacent columns such as column 1011 and 1012 share a single source 402, each of the columns has its own drain 401. It will be understood that a device may comprise any number of columns. Additionally, although four rows are shown in **Figure 10**, the device may comprise any number of such rows. In a preferred embodiment, a contactless array is fabricated, i.e., each source 402 and drain 401 does not have a contact at each cell. Since the drain regions 401 and source regions 402 are continuous and common to each cell in a column, contact need not necessarily be made at each cell, but rather can be made at a common point along the diffusion lines. In a preferred embodiment, contact is made to each drain 401, and source 402 at approximately every sixteen cells or so along a column. It will be appreciated that this may be varied, depending upon the acceptable voltage drop (due to resistance along the diffusion lines) at cells distant from the contacts.

As described earlier, the array of the present invention may be used to fabricate the floating gate device described above, as well as single polysilicon memories such as ROMs. In the fabrication of a ROM, after the stage of processing shown in **Figure 6**, and deposition of a second conductive layer, for example, polysilicon layer 1102, which is substantially similar to layer 702, a patterning layer 1105 is formed as shown in **Figure 11A**. For clarity, the field oxide and thin oxide regions are not shown in **Figure 11A**. As shown, the patterning layer 1105 forms parallel strips covering the active area of the devices and extending substantially perpendicular to the source/drain strips. A multi-step etch process is then performed to remove those portions of layer 1102 not masked by the patterning layer strips 1105. Additionally in this process, the exposed portions of the intergate dielectric 801 and first polysilicon layer 302a between the patterning layer strips 1105 is also removed. Layer 1102, together with polysilicon layer 302a, makes up the gate of the device. **Figure 11B** shows a cross-sectional view of the structure of **Figure 11A** through a portion of the section indicated in **Figure 11A**. In the case of a ROM, thin oxide 301 comprises a gate oxide.

It will be appreciated that many modifications to the above described embodiments may be made by one of skill in the art. For example, different materials may be used in place of the various layers such as the polysilicon layers, nitride layers and dielectric layers, depending upon device and process requirements. Further, the polysilicon layer 702 may not be required in all cases, depending upon device requirements. As described above, use of the second polysilicon layer 702, patterned to have the asymmetrical overlap described above, results in improved device performance for many types of devices. In addition, the sequence of processing steps, including implantations, and depositions may be varied, and it is understood that the present invention is not limited to the processing sequence as described above. Finally, numerous other steps may be carried out either before, during, or after the processing described above to form the completed device. For example, in forming a ROM memory, a masked implant is typically carried out to program the device. As another example, although the

fabrication of a buried bit line device has been described, the present invention may be used in the fabrication of devices wherein diffusion lines are not buried under the thick oxide regions 601.

Thus, a method for forming improved isolation between diffusion lines in a memory array has been described. Although specific embodiments, including specific equipment, parameters, methods, and materials have been described, various modifications to the disclosed embodiments will be apparent to one of ordinary skill in the art upon reading this disclosure. Therefore, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention and that this invention is not limited to the specific embodiments shown and described.

CLAIMS

What is claimed is:

1. A method of forming a memory device comprising the steps of:

forming substantially parallel spaced apart first strips on a semiconductor substrate;

forming first oxide regions between said first strips;

forming substantially parallel spaced apart second strips on said substrate, said second strips oriented substantially perpendicular to said first strips, said second strips comprising a first conductive layer and a first masking layer; and,

oxidizing said conductive layer of a first set of said second strips comprising at least two of said second strips, said first set separated by a second set of said second strips comprising at least two of said second strips.

2. The method as described in claim 1 wherein said oxidizing step additionally oxidizes said substrate between said second strips.

3. The method as described in claim 1 further comprising doping said substrate in regions between said second strips prior to oxidizing said first conductive layer of said first set of said second strips.

4. The method as described in claim 3 wherein said doped regions between said second strips comprise source and drain regions, wherein adjacent ones of said drain regions are separated by at least one of said oxidized second strips.

5. The method as described in claim 1 further comprising forming third strips comprising a second conductive layer over and in electrical contact with said first conductive layer of said second strips.

6. The method as described in claim 4 further comprising forming third strips comprising a second conductive layer over and in electrical contact with said first conductive layer of said second strips.

7. The method as described in claim 5 wherein said third strips are formed by depositing said second conductive layer, forming a patterning layer on said second conductive layer having patterning layer strips corresponding to said third strips, said patterning layer strips being substantially perpendicular to said second strips, and removing said second conductive layer from regions not masked by said patterning layer strips, wherein portions of said first conductive layer between said patterning layer strips are also removed, wherein said first conductive layer and said second conductive layer form a gate of a ROM device.

8. The method as described in claim 6 wherein said third strips are formed by depositing said second conductive layer, forming a patterning layer on said second conductive layer having patterning layer strips corresponding to said third strips, said patterning layer strips being substantially perpendicular to said second strips, and removing said second conductive layer from regions not masked by said patterning layer strips, wherein portions of said first conductive layer between said patterning layer strips are also removed, wherein said first conductive layer and said second conductive layer form a gate of a ROM device.

9. The method as described in claim 5 wherein said third strips are formed by depositing said second conductive layer, forming a patterning layer on said second conductive layer having patterning layer strips corresponding to said third strips, said patterning layer strips being substantially parallel to said second strips and overlapping said second strips, and removing said second layer from regions not masked by said patterning layer strips, wherein said first conductive layer and said conductive layer form a floating gate of a floating gate memory device.

10. The method as described in claim 6 wherein said third strips are formed by depositing said second conductive layer, forming a patterning layer on said second conductive layer having patterning layer strips corresponding to said third strips, said patterning layer strips being substantially parallel to said second strips and overlapping said second strips, and removing said second layer from regions not masked by said patterning layer strips, wherein said first conductive layer and said conductive layer form a floating gate of a floating gate memory device.

11. The method as described in claim 9 further comprising forming fourth strips comprising a third conductive layer over said second conductive layer, said third conductive layer insulated from said second conductive layer by an insulative layer, said fourth strips formed by depositing said third conductive layer, forming a second patterning layer on said third conductive layer having second patterning layer strips corresponding to said fourth strips, said second patterning layer strips being substantially perpendicular to said third strips, and removing said third conductive layers from regions not masked by said second patterning layer strips, wherein portions of said first conductive layer, said insulative layer, and said second conductive layer between said second patterning layer strips are removed, wherein said third conductive layer comprises a control gate.

12. The method as described in claim 10 further comprising forming fourth strips comprising a third conductive layer over said second conductive layer, said third conductive layer insulated from said second conductive layer by an insulative layer, said fourth strips formed by depositing said third conductive layer, forming a second patterning layer on said third conductive layer having second patterning layer strips corresponding to said fourth strips, said second patterning layer strips being substantially perpendicular to said third strips, and removing said third conductive layers from regions not masked by said second patterning layer strips, wherein portions of said first conductive layer, said insulative layer, and said second conductive layer between said

second patterning layer strips are removed, wherein said third conductive layer comprises a control gate.

13. The method as described in claim 10 wherein said third strips overlap said drain region to a greater extent than said source region.

14. The method as described in claim 12 wherein said third strips overlap said drain region to a greater extent than said source region.

15. A method of forming a memory device comprising the steps of:

forming substantially parallel spaced apart first strips on a semiconductor substrate;

forming first oxide regions between said first strips;

forming substantially parallel spaced apart second strips on said substrate, said second strips oriented substantially perpendicular to said first strips, said second strips comprising a first conductive layer and a first masking layer;

forming doped regions between said second strips, said doped regions comprising source regions and drain regions; and,

oxidizing said conductive layer of those second strips between two of said drain regions.

16. The method as described in claim 15 wherein said oxidizing step additionally oxidizes said substrate between said second strips.

17. The method as described in claim 15 further comprising forming third strips comprising a second conductive layer over and in electrical contact with said first conductive layer of said second strips.

18. The method as described in claim 17 wherein said third strips are formed by depositing said second conductive layer, forming a

patterning layer on said second conductive layer having patterning layer strips corresponding to said third strips, said patterning layer strips being substantially perpendicular to said second strips, and removing said second conductive layer from regions not masked by said patterning layer strips, wherein portions of said first conductive layer between said patterning layer strips are also removed, wherein said first conductive layer and said second conductive layer form a gate of a ROM device.

19. The method as described in claim 17 wherein said third strips are formed by depositing said second conductive layer, forming a patterning layer on said second conductive layer having patterning layer strips corresponding to said third strips, said patterning layer strips being substantially parallel to said second strips and overlapping said second strips, and removing said second layer from regions not masked by said patterning layer strips, wherein said first conductive layer and said conductive layer form a floating gate of a floating gate memory device.

20. The method as described in claim 19 further comprising forming fourth strips comprising a third conductive layer over said second conductive layer, said third conductive layer insulated from said second conductive layer by an insulative layer, said fourth strips formed by depositing said third conductive layer, forming a second patterning layer on said third conductive layer having second patterning layer strips corresponding to said fourth strips, said second patterning layer strips being substantially perpendicular to said third strips, and removing said third conductive layers from regions not masked by said second patterning layer strips, wherein portions of said first conductive layer, said insulative layer, and said second conductive layer between said second patterning layer strips are removed, wherein said third conductive layer comprises a control gate.

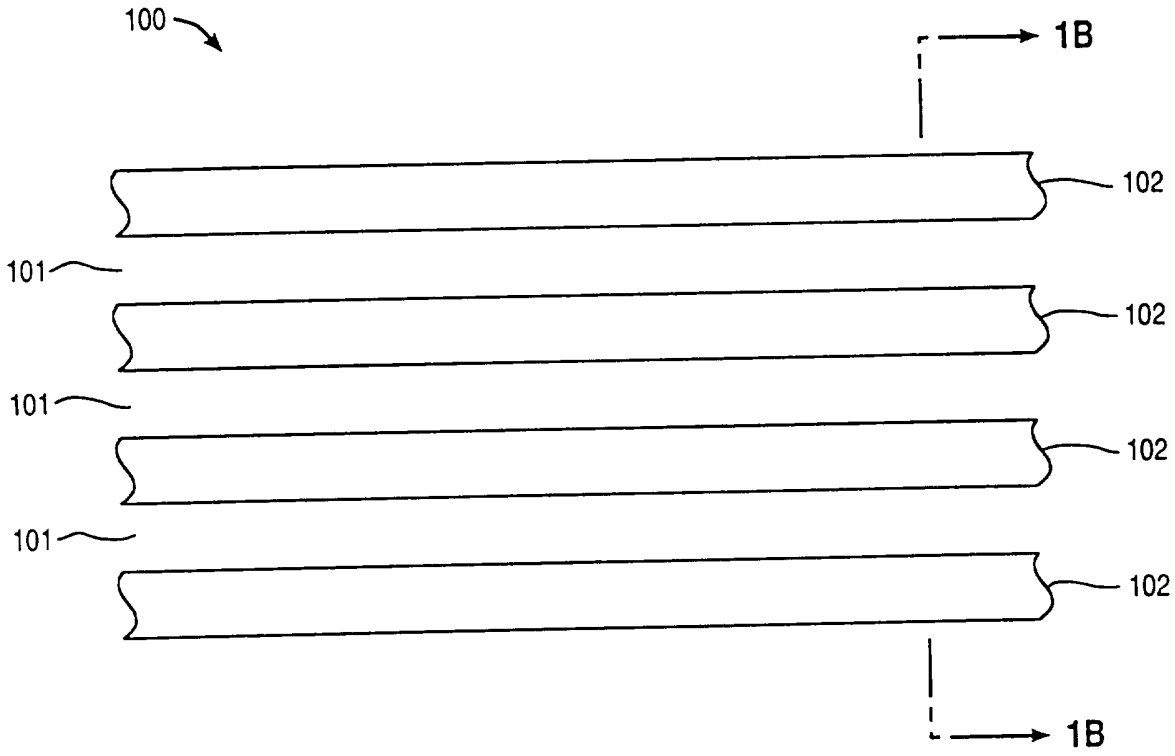


FIG_1A

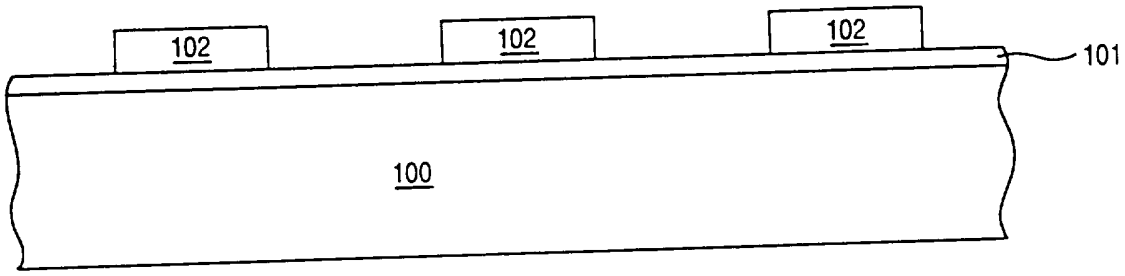


FIG_1B

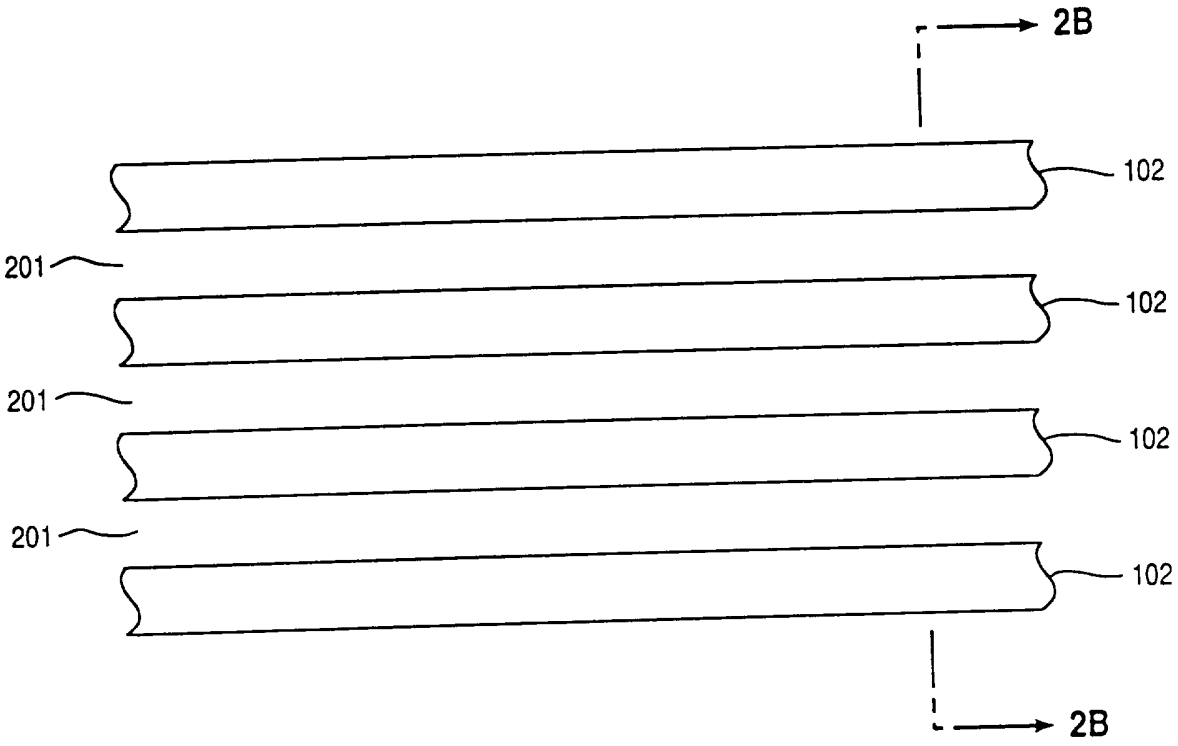


FIG_2A

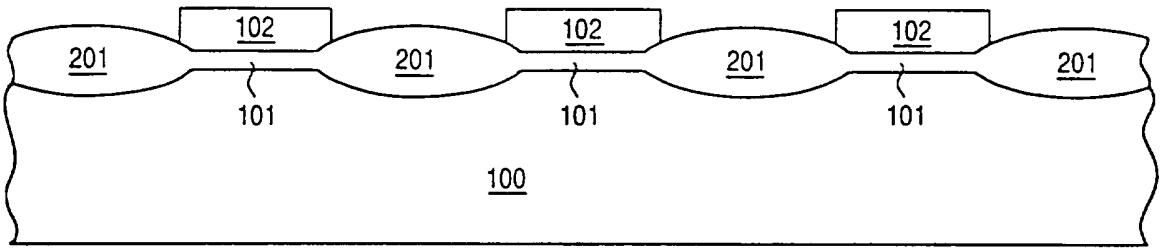


FIG_2B

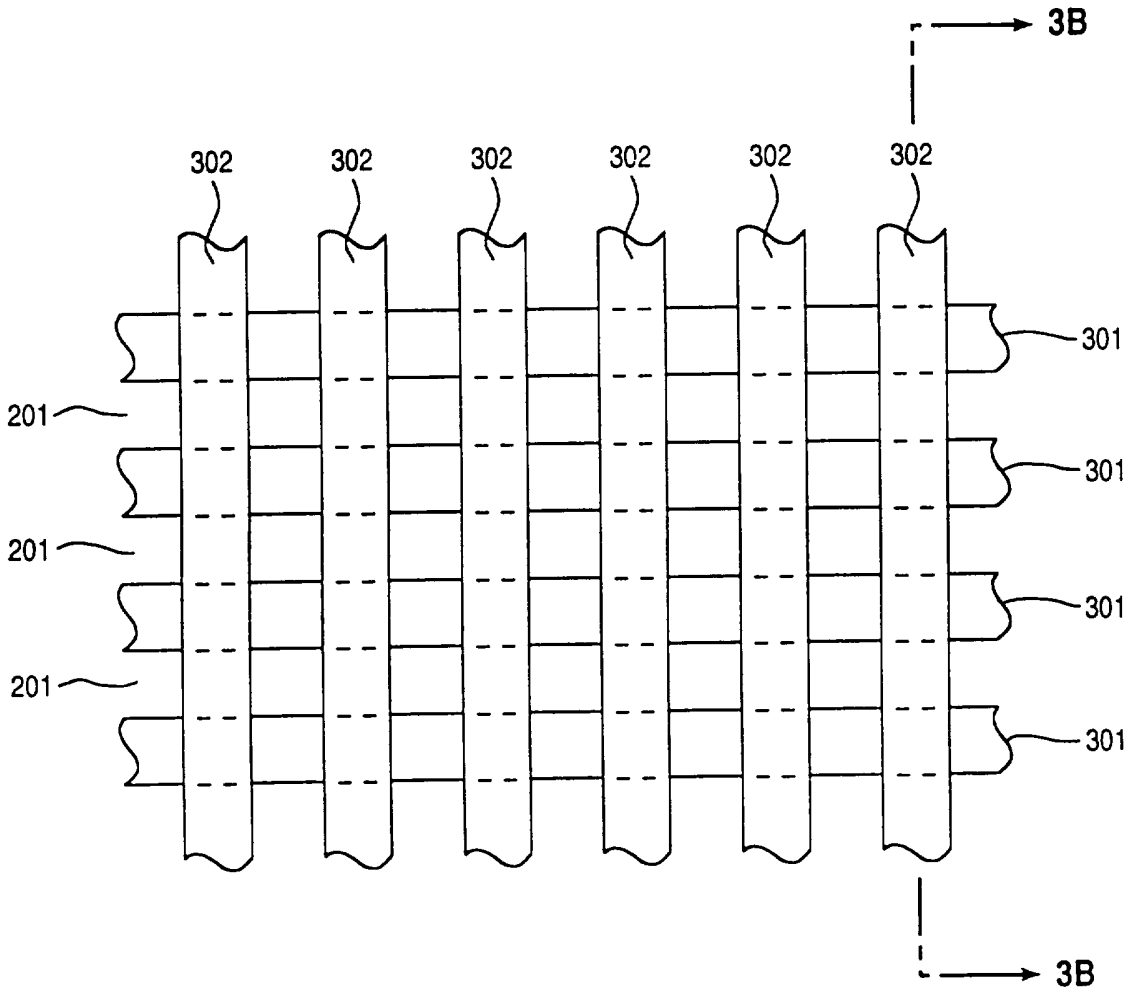


FIG_3A

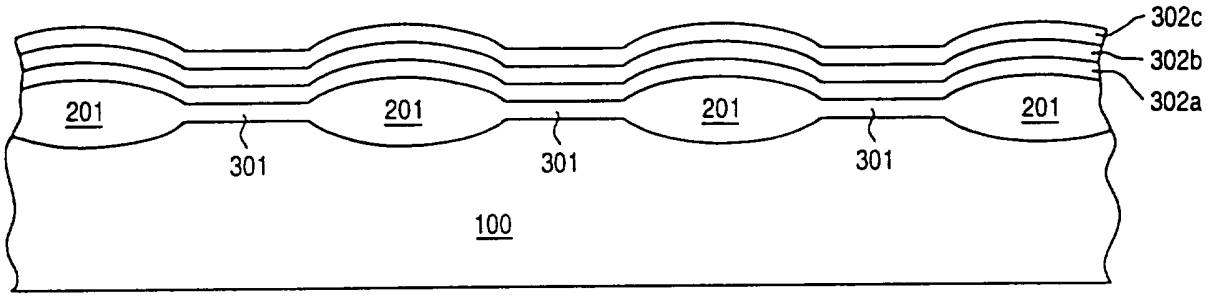


FIG_3B

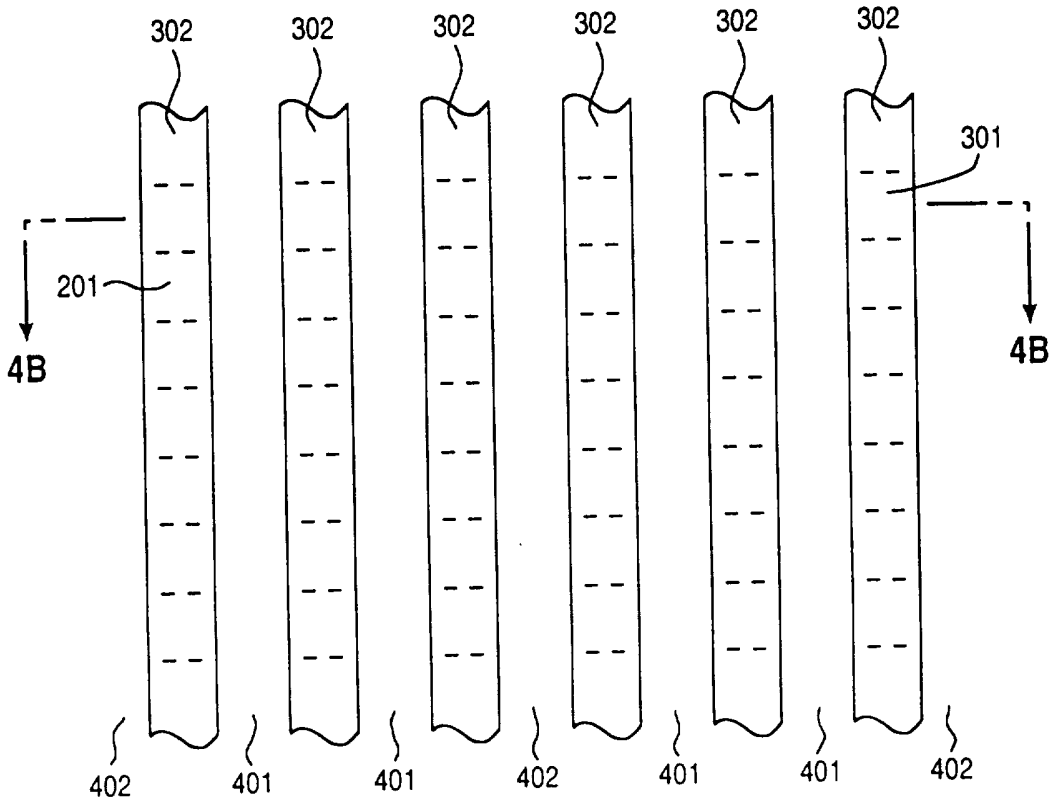


FIG_4A

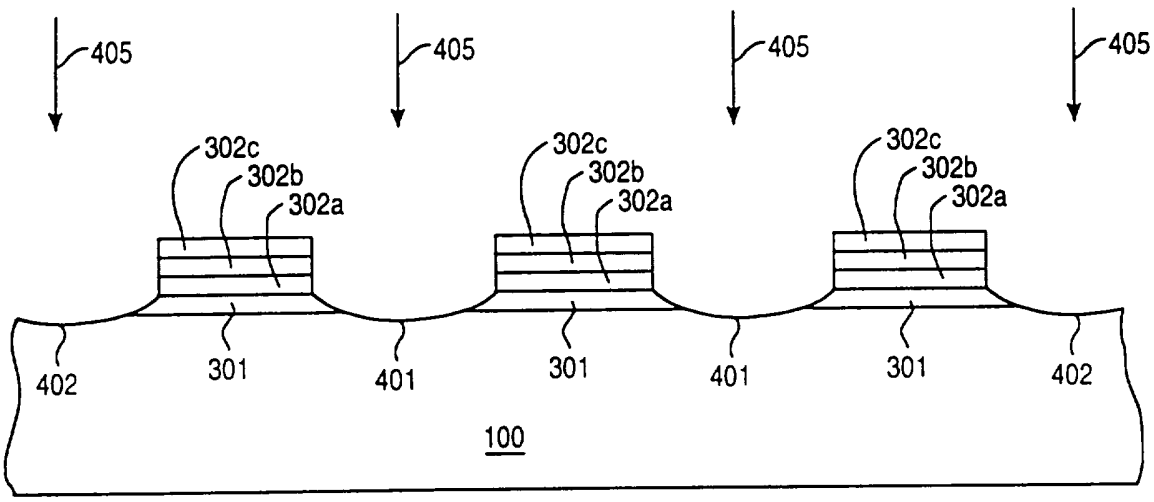

405
405
405
405
302c
302b
302a
302c
302b
302a
302c
302b
302a
402
301
401
301
401
301
402
100

FIG_4B

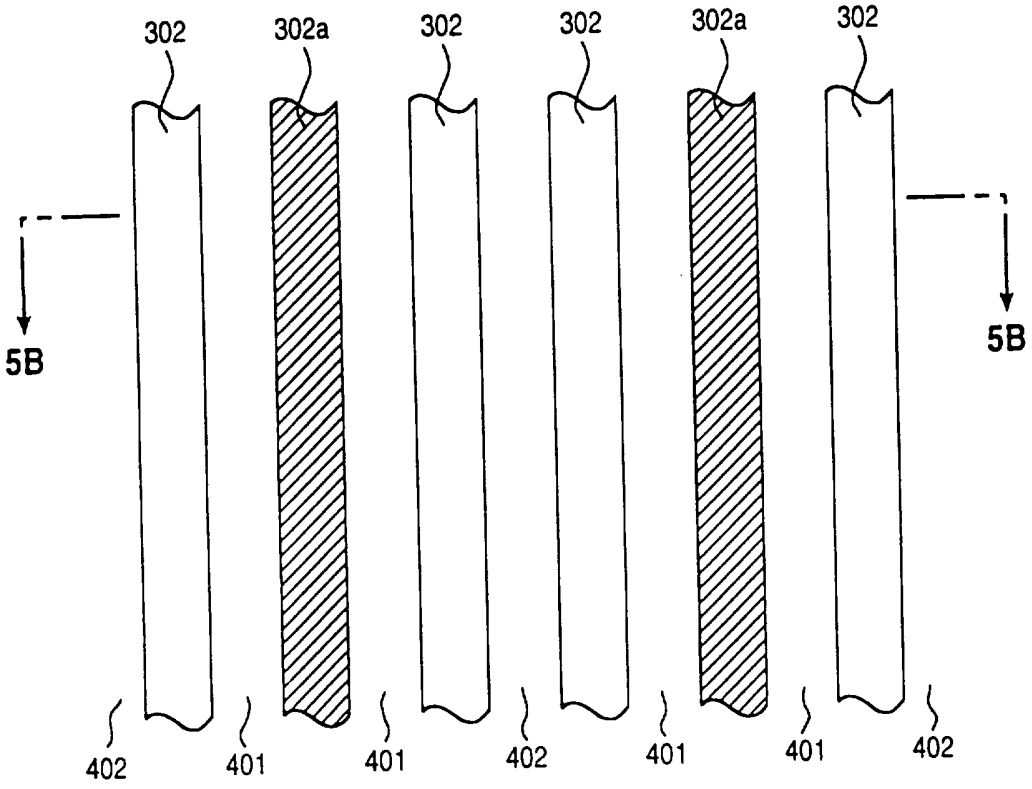


FIG_5A

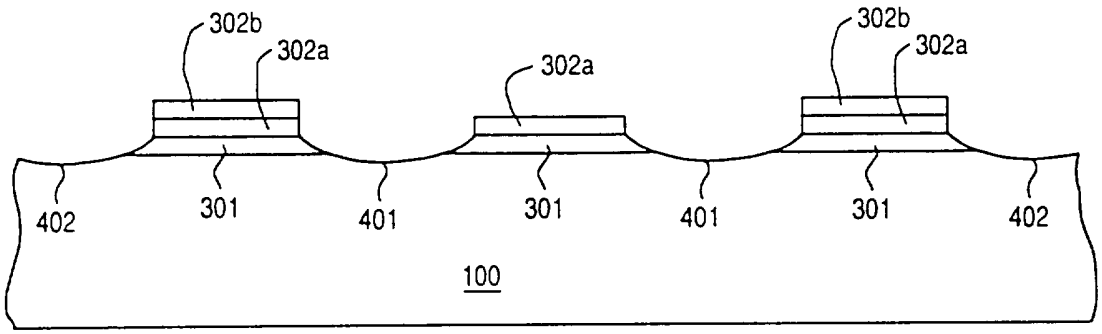


FIG_5B

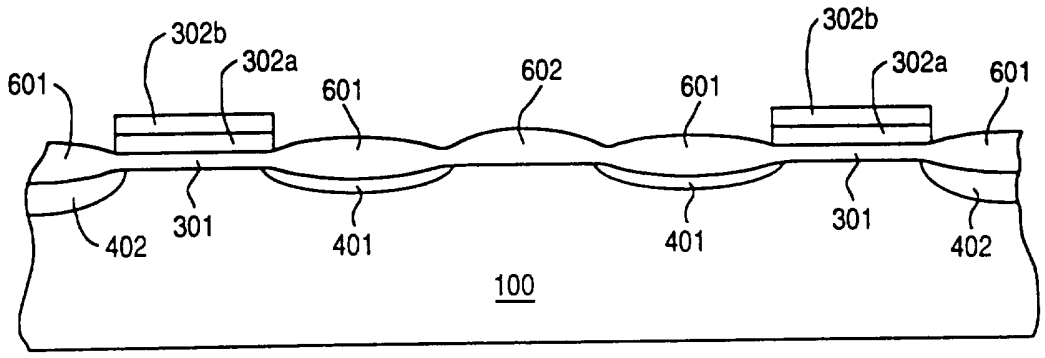

302b
302a
601
601
602
601
302b
302a
601
402
301
401
401
301
402
100

FIG_6

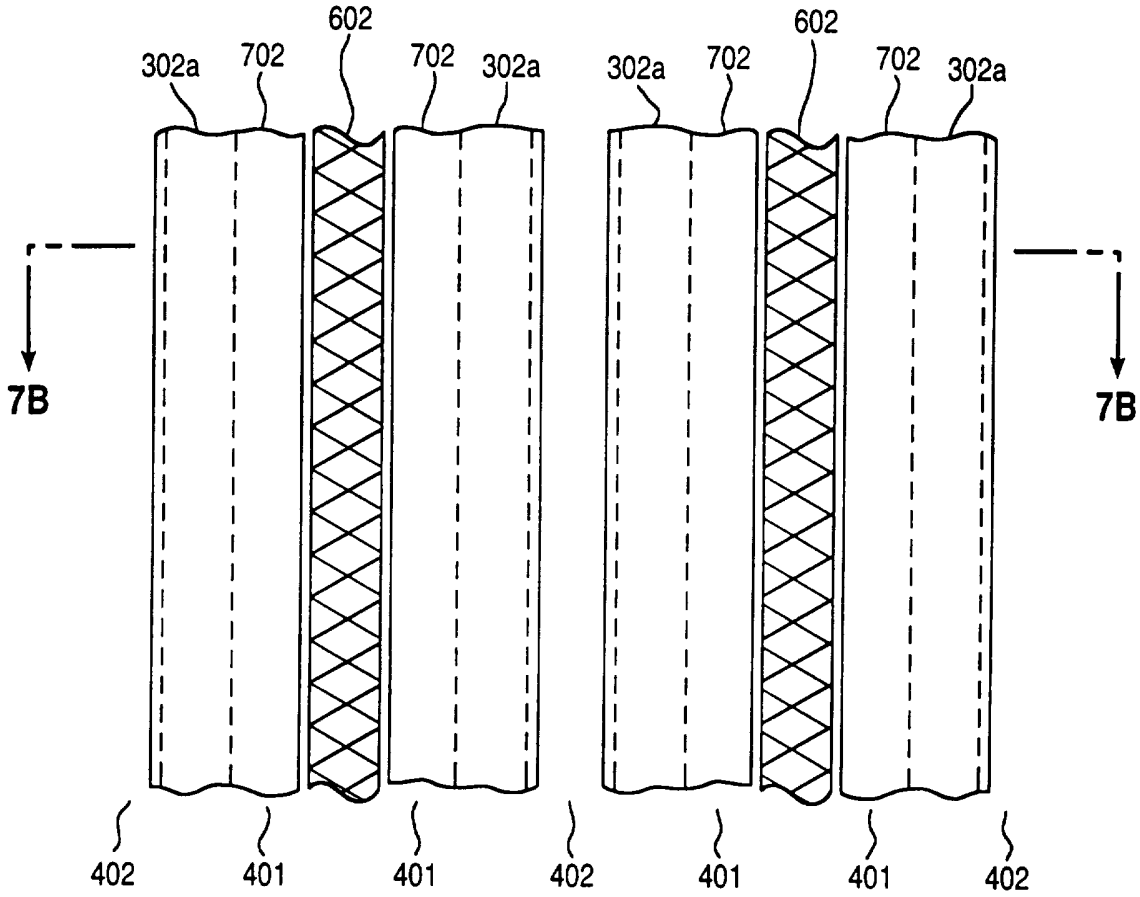

602
302a
702
702
302a
302a
702
602
702
302a
7B
7B
402
401
401
402
401
401
402

FIG_7A

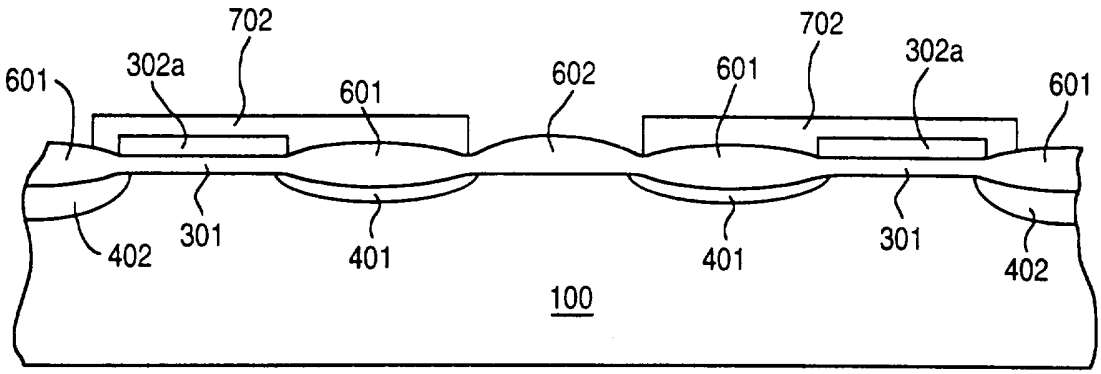

702
601
302a
601
602
601
702
302a
601
402
301
401
401
301
402
100

FIG_7B

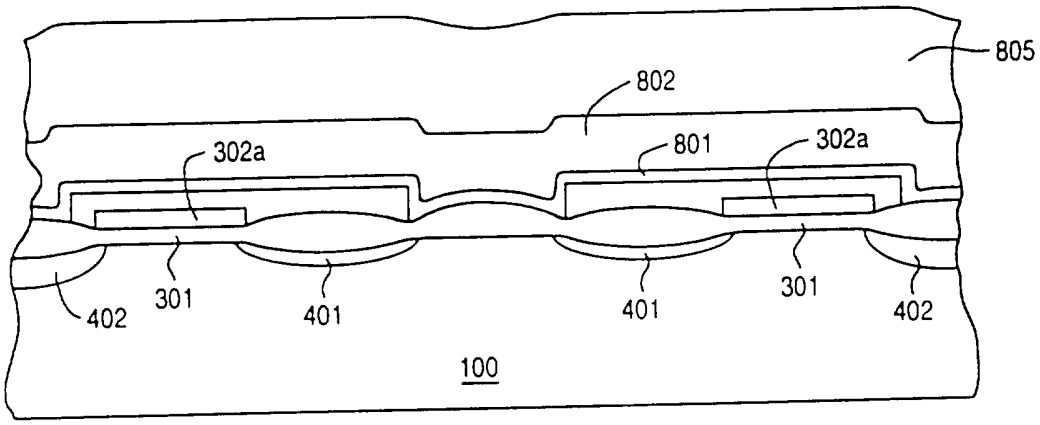
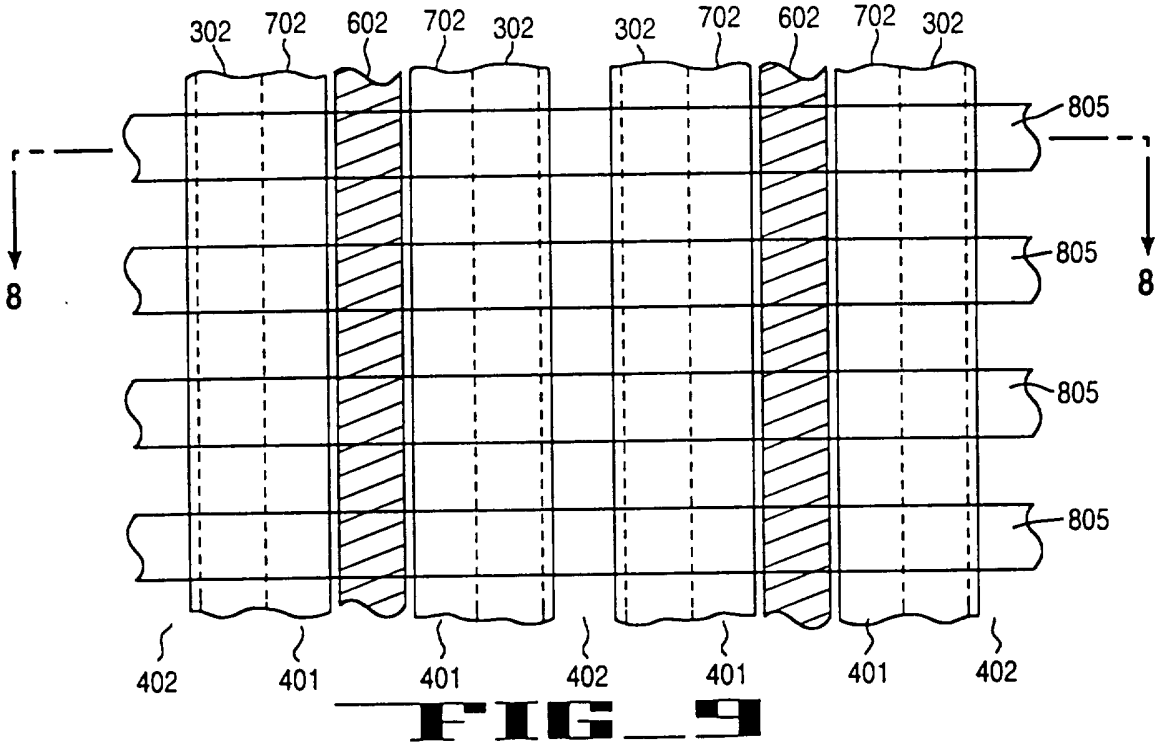


FIG_8


302
702
602
702
302
302
702
602
702
302
805
805
805
805
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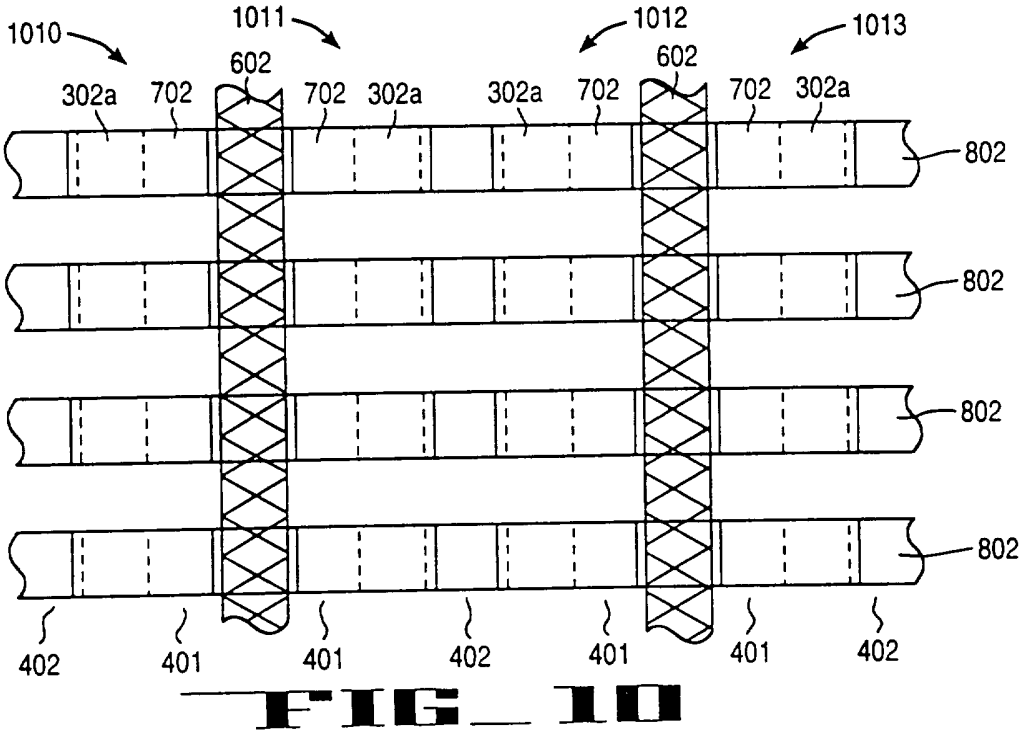
402

FIG_9


1010
1011
1012
1013
602
602
302a
702
702
302a
302a
702
702
302a
802
802
802
802
402
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402

FIG_10

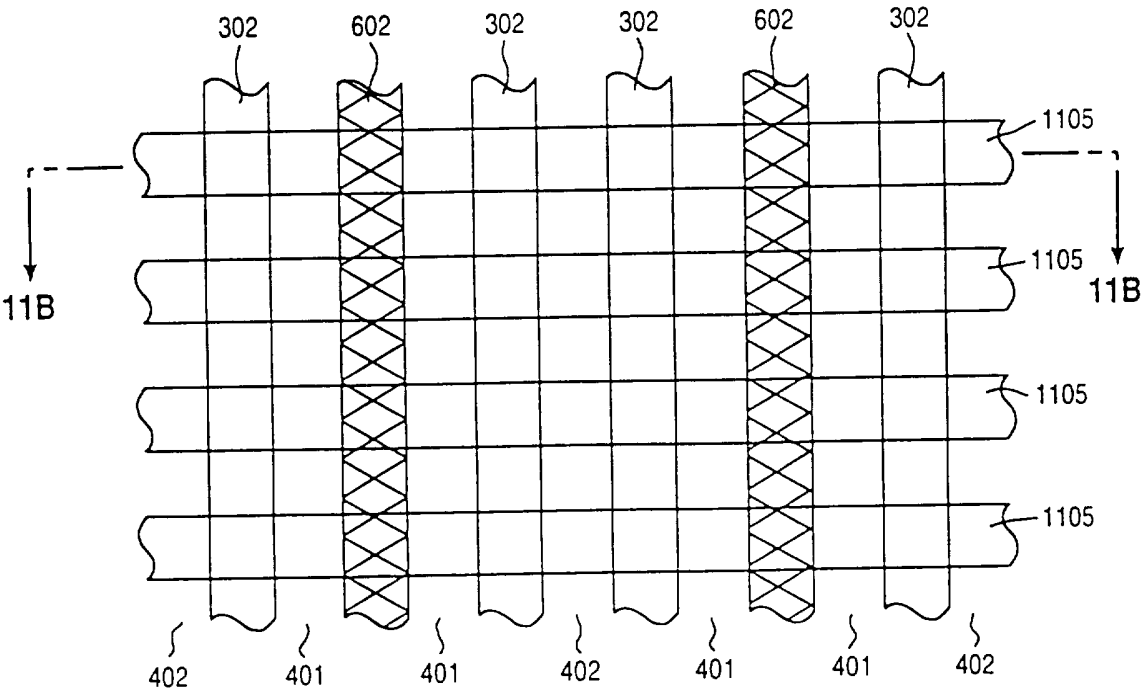

FIG_11A

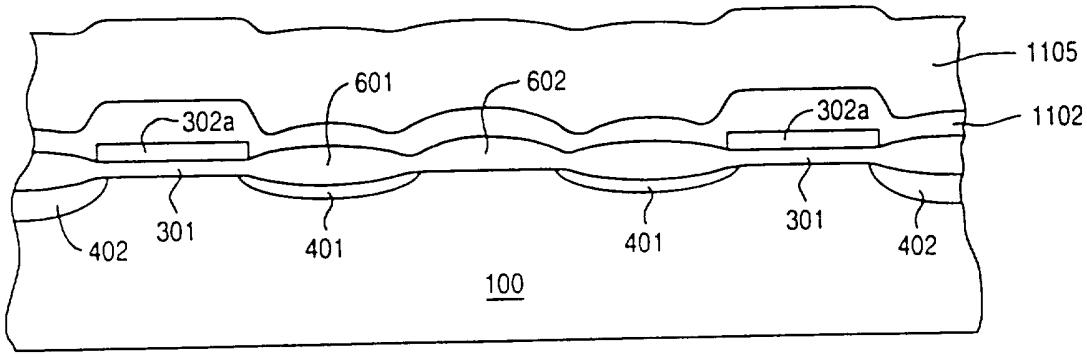

FIG_11B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/11563

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 21/8246, 8247
US CL : 437/43, 52, 61
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 437/43, 48, 52, 61, 69 257/315, 374

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A, 4,151,021 (McElroy) 24 April 1979. See Figures 3-6, and accompanying text.	1-6, 9-17, 19, 20
A	US,A, 5,075,245 (Woo et al.) 24 December 1991 See the entire document.	1-6, 9-17, 19, 20
A	US,A, 5,330,938 (Camerlenghi) 19 July 1994 See the entire document.	1-6, 9-17, 19, 20
A	US,A, 5,102,814 (Woo) 07 April 1992. See Figures 1-8, and Col. 5, line 7 to col. 9, line 64.	1-6, 9-17, 19, 20

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search
27 NOVEMBER 1995

Date of mailing of the international search report
04 JAN 1996

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231
Facsimile No. (703) 305-3230

Authorized officer
TOM THOMAS
Telephone No. (703) 308-2772

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/11563

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A, 4,818,716 (Okuyama et al) 04 April 1989. See Figures 4-7 and accompanying text.	1, 5-8, 15-18