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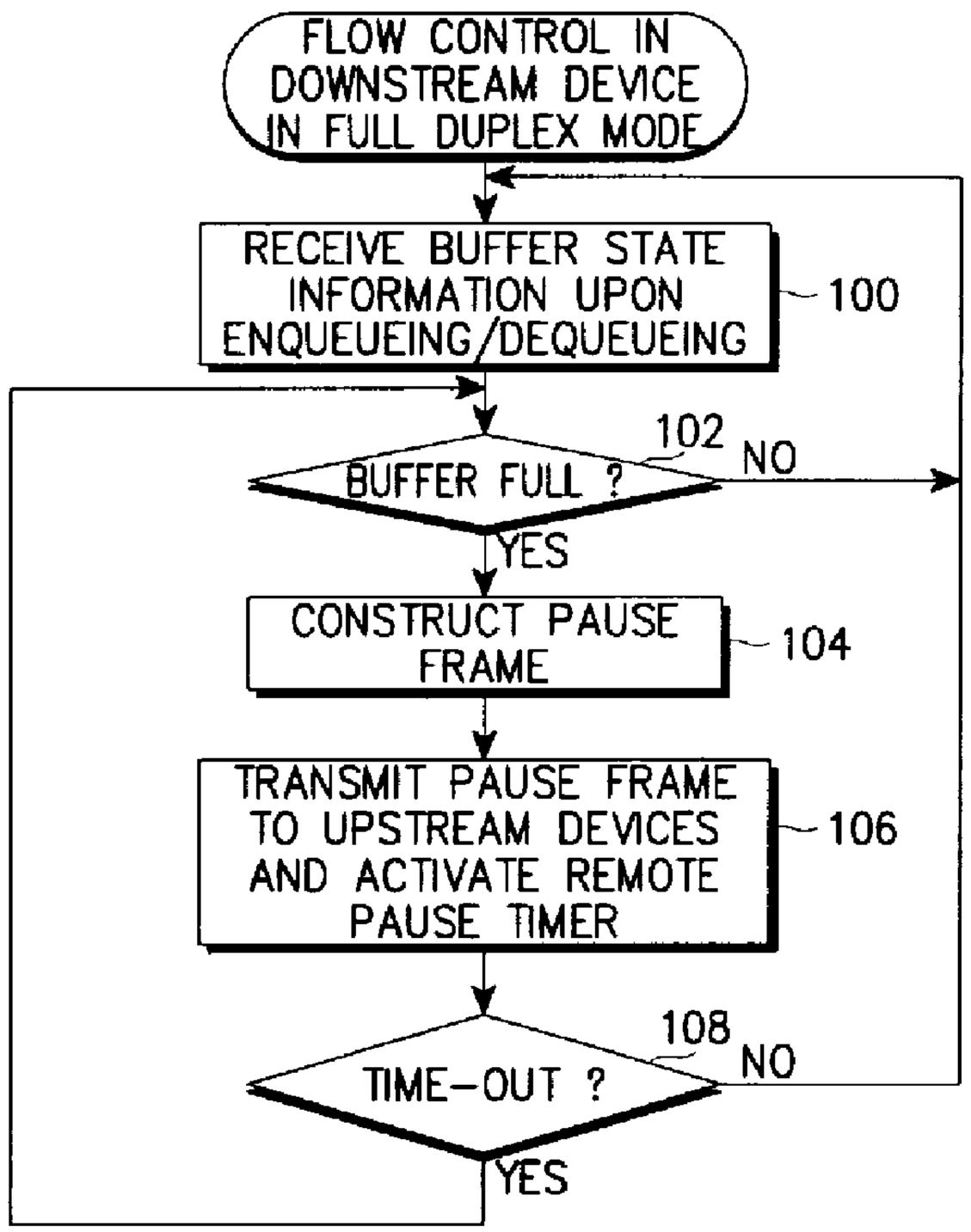

(57) Abrégé/Abstract:
A flow control method in an Ethernet switch being a downstream device using a full duplex mode in a packet switched network. The Ethernet switch has a plurality of input ports connected to a plurality of Ethernet switches being upstream devices and a common memory for storing packet data received from each input port, for transmitting packet data read from the common

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(57) Abrégé(suite)/Abstract(continued):
memory to a destination upstream device. In the flow control method, the buffer state of the common memory is first determined. If the buffer state is buffer-full, a pause frame including a predetermined pause time is transmitted to the plurality of Ethernet switches being upstream devices and an expected pause time of the upstream devices is counted. The buffer state of the common memory is determined again if the expected pause time is out. If the buffer state is buffer-full, the pause frame including the predetermined pause time is re-transmitted to the plurality of Ethernet switches being upstream devices and the expected pause time of the upstream devices is counted.

ABSTRACT OF THE DISCLOSURE

A flow control method in an Ethernet switch being a downstream device using a full duplex mode in a packet switched network. The Ethernet switch has a plurality of input ports connected to a plurality of Ethernet switches being upstream devices and a common memory for storing packet data received from each input port, for transmitting packet data read from the common memory to a destination upstream device. In the flow control method, the buffer state of the common memory is first determined. If the buffer state is buffer-full, a pause frame including a predetermined pause time is transmitted to the plurality of Ethernet switches being upstream devices and an expected pause time of the upstream devices is counted. The buffer state of the common memory is determined again if the expected pause time is out. If the buffer state is buffer-full, the pause frame including the predetermined pause time is re-transmitted to the plurality of Ethernet switches being upstream devices and the expected pause time of the upstream devices is counted.

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FLOW CONTROL METHOD

IN PACKET SWITCHED NETWORK

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to a packet switched network, and in particular, to a flow control method in a LAN (Local Area Network) device, which can minimize loss of packets over a LAN such as Ethernet and allow a bandwidth to be equally shared among input ports of the LAN device.

2. Description of the Related Art

Congestion is generally overcome by applying back pressure or transferring a pause frame in an Ethernet. The back-pressure is applied when an Ethernet switch is in a half duplex mode. A pause frame is one of MAC (Media Access Control) control frames and defined under the IEEE 802.3x standard. The pause frame transfer scheme is implemented in a full duplex mode. These two schemes control a flow to temporarily prevent Ethernet switches from sending packets to a specific Ethernet switch when the buffer capacity of the specific Ethernet switch reaches its limit and a congestion occurs.

The back-pressure application and the pause frame transfer will be described in detail.

The back-pressure scheme uses a jamming signal in a CSMA/CD (Carrier Sense Multiple Access with Collision Detection) method to determine whether a transmit collision has occurred. Upon sensing a jamming signal from a specific Ethernet switch (downstream), the Ethernet switch is considered to experience a transmit collision. Then, a back pressure, that is, a jamming signal is sent to the other Ethernet switches (upstream) within the same segment to stop packet transmission for a predetermined random back-off time.

On the other hand, the pause frame transfer scheme utilizes a pause frame which is one of MAC control frames, first defined under the IEEE 802.3x standard. If an Ethernet switch (downstream) suffers a congestion, it sends a specific pause frame to the other Ethernet switches (upstream) in the same segment, so that the other Ethernet switches stop packet transmission for a pause time period set in a pause frame.

As described above, the conventional back-pressure and pause frame transfer schemes performs the above flow control simply by determining whether a common memory is full or not and considering that a congestion has occurred if it is full. The jamming signal and the pause frame are transmitted to the plurality of Ethernet switches (upstream) through input ports connected to the Ethernet switches. Therefore, the conventional flow control method is likely to stop even packet transmission from an Ethernet switch (upstream) which is not a congestion source.

SUMMARY OF THE INVENTION

It is, therefore, an object of embodiments of the present invention to provide a method of equally sharing a buffer capacity among the input ports of an Ethernet switch.

It is another object of embodiments of the present invention to provide a method of minimizing packet loss at a congestion in an Ethernet switch.

It is a further object of embodiments of the present invention to provide a method of increasing a packet processing rate over an entire network.

To achieve the above objects, there is provided a flow control method in an Ethernet switch being a downstream device using a full duplex mode in a packet switched network. The Ethernet switch has a plurality of input ports connected to a plurality of Ethernet switches being upstream devices and a common memory for storing packet data received from each input port. In the flow control method, the buffer state of the common memory is first determined. If the buffer state is buffer-full, a pause frame including a predetermined pause time is transmitted to the plurality of Ethernet switches being upstream devices and an expected pause time of the upstream devices is counted. The buffer state of the common memory is determined again if the expected pause time is out. If the buffer state is buffer-full, the pause frame including the predetermined pause time is re-transmitted to the plurality of Ethernet switches being upstream devices and the expected pause time of the upstream devices is counted.

According to one aspect the invention provides a flow control method in a downstream Ethernet switch using a full duplex mode in a packet switched network, the downstream Ethernet switch having a plurality of input ports connected to a plurality of upstream Ethernet switches and a common memory for storing packet data received from each input port, the method comprising the steps of: determining a buffer state of the common memory; transmitting a pause frame including a predetermined pause time to the plurality of upstream Ethernet switches and counting an expected pause time of the upstream Ethernet switches, if the buffer state is buffer-full; determining the buffer state of the common memory again if the expected pause time has expired; and re-transmitting the pause frame including the predetermined pause time to the plurality of upstream Ethernet switches and counting the expected pause time of the upstream Ethernet switches, if the buffer state is buffer-full.

According to another aspect the invention provides a flow control method in a downstream Ethernet switch using a full duplex mode in a packet switched network, the Ethernet downstream switch having a plurality of input ports connected to a plurality of upstream Ethernet switches and a common memory for storing packet data received from each input port, the method comprising the steps of: determining a buffer state of the common memory for each input port; transmitting a pause frame including a predetermined pause time to an upstream Ethernet switch connected to a congested input port and counting an expected pause time of the upstream Ethernet switch, if the buffer state of the input port is buffer-full; determining the buffer state of the common memory again for each input port if the expected pause time has expired; and re-transmitting the pause frame including the predetermined pause time to the upstream

Ethernet switch and counting the expected pause time of the upstream Ethernet switch, if the buffer state of the congested input port is buffer-full. In a preferred embodiment, the common memory includes one packet counter for each input port to determine the buffer state of the common memory for each input port.

According to another aspect the invention provides a flow control method in a downstream Ethernet switch using a full duplex mode in a packet switched network, the downstream Ethernet switch having a plurality of input ports connected to a plurality of upstream Ethernet switches and a common memory for storing packet data received from each input port, and transmitting packet data read from the common memory to a destination upstream Ethernet switch, the method comprising the steps of: determining a buffer state of the common memory for each input port; and transmitting a jamming signal to an upstream Ethernet switch connected to a congested input port, if the buffer state of the input port is buffer-full.

According to another aspect the invention provides an Ethernet switch for transmitting/receiving data to/from other Ethernet switches using a full duplex mode in a packet switch network, comprising: a common buffer including a packet memory storing packet data input via a plurality of input ports, and packet counters provided for the plurality of input ports for counting an input packet for each corresponding port; a pause frame generator for generating a pause frame including pause time information for stopping transmission of packet data for a predetermined time period; and a host processor for determining whether a count value of at least one packet counter of the packet counters exceeds a predetermined threshold value and, if the

threshold value is exceeded, controlling the pause frame generator for transmitting the pause frame to an Ethernet switch corresponding to the input port for which the threshold value is exceeded.

According to another aspect the invention provides an Ethernet switch for transmitting/receiving data to/from other Ethernet switches using a full duplex mode in a packet switch network, comprising: a common buffer including a packet memory storing packet data input via a plurality of input ports, and packet counters being provided for the plurality of input ports for executing an up count if a packet data is input via each input port and executing a down count if the packet data is output; a pause frame generator for generating a pause frame including pause time information for stopping transmission of packet data for a predetermined time period; and a host processor for determining whether a count value of at least one packet counter of the packet counters exceeds a predetermined threshold value and, if the threshold value is exceeded, controlling the pause frame generator for transmitting the pause frame to an Ethernet switch corresponding to the input port for which the threshold value is exceeded.

According to another aspect the invention provides an Ethernet switch for transmitting/receiving data to/from other Ethernet switches using a half duplex mode in a packet switched network, comprising: a common buffer including a packet memory storing packet data input via a plurality of input ports, and packet counters being provided for the plurality of input port, for executing an up count if a packet data is input via each input port, and executing a down count if the packet data is output; a jamming signal generator for generating a jamming signal for stopping transmission of packet data; and a host processor for

determining whether a count value of at least one packet counter of the packet counters exceeds a predetermined threshold value and if the threshold value is exceeded, controlling the jamming signal generator for transmitting the jamming signal to an Ethernet switch corresponding to the input port for which the threshold value is exceeded.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present

invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings in which:

FIG. 1 is a schematic block diagram of a LAN according to the present invention;

FIG. 2 is a schematic block diagram of an Ethernet switch according to a first embodiment of the present invention;

FIG. 3 is a flowchart depicting a flow control operation of an Ethernet switch (downstream) using a full duplex mode according to the first embodiment of the present invention;

FIG. 4 is a flowchart depicting a flow control operation of an Ethernet switch (upstream) using the full duplex mode according to the first embodiment of the present invention;

FIG. 5 is a schematic block diagram of an Ethernet switch according to a second embodiment of the present invention;

FIG. 6 is a flowchart depicting a flow control operation of an Ethernet switch (downstream) using a full duplex mode according to the second embodiment of the present invention;

FIG. 7 is a flowchart depicting a flow control operation of an Ethernet (upstream) using the full duplex communication mode according to the second embodiment of the present invention; and

FIG. 8 is a flowchart depicting a flow control operation of the Ethernet switch (downstream) using a half duplex mode according to the second embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described hereinbelow with reference to the accompanying drawings. In the following description, well-known functions or constructions are not described in detail

since they would obscure the invention in unnecessary detail.

FIG. 1 is a schematic block diagram of a LAN according to the present invention. In FIG. 1, Ethernet switches 10, 12-1, ..., and 12-N are a kind of new LAN devices, that is, multi-port bridges. The plurality of Ethernet switches 12-1 to 12-N for transmitting packet data are termed upstream devices and the Ethernet switch 10 for transmitting a jamming signal in a half duplex mode or pause frame in a full duplex mode to the Ethernet switches 12-1 to 12-N is termed a downstream device in the embodiments of the present invention.

FIG. 2 is a block diagram of an Ethernet switch for a flow control in a full duplex mode according to a first embodiment of the present invention, and FIG. 3 is a flowchart depicting a flow control operation of an Ethernet (downstream) at a full duplex mode according to the first embodiment of the present invention.

Referring to FIG. 2, the Ethernet switch is comprised of a common buffer 20, a host processor 26, and a MAC unit 28. The common buffer 20 includes a packet memory 22 for storing all packet data received through a plurality of input ports of the Ethernet switch, and a packet memory interface 24 for interfacing between the packet memory 22 and the MAC unit 28. The packet memory interface 24 has an up/down counter according to the first embodiment of the present invention. The up/down counter counts up/down upon enqueueing/dequeueing packet data in/from the packet memory 22. If an up/down count value reaches a predetermined value indicating “buffer full”, the packet memory interface 24 feeds a signal indicating “buffer full” to the MAC unit 28.

The host processor 26 provides various operation and status controls to

the MAC unit 28. According to the first embodiment of the present invention, the host processor 26 transmits information about a pause time period, for which the Ethernet switches 12-1 to 12-N temporarily stop transmission of packet data, to the MAC unit 28 in an initialization state.

One MAC unit 28 is provided for each port of the Ethernet switch, for performing a MAC function. The MAC unit 28 includes a pause frame generator 30, a transmission block 32, a remote pause timer 34, a reception block 36, and a reception pause timer 38. The pause frame generator 30 constructs a pause frame based on the pause time information received from the host processor 26 upon reception of the signal indicating "buffer full" from the packet memory interface 24. The transmission block 32 transmits a MAC control frame including packet data read from the common buffer 20 or the pause frame to the Ethernet switches 12-1 to 12-N through a corresponding input port of the Ethernet switch. The transmission block 32 also activates the remote pause timer 34. The remote pause timer 34 counts an expected pause time period for which the Ethernet switches 12-1 to 12-N will stop data transmission temporarily. The remote pause timer 34 is activated based on the expected pause time and an activation command RPT_ACT of the transmission block 32 and outputs a time-out signal to the transmission block 32 if the expected pause time has elapsed. The expected pause time period is provided by the transmission block 32. The reception block 36 receives a MAC control frame from the Ethernet switch 10. If the received MAC control frame is a pause frame, the reception block 36 activates the reception pause timer 38 based on a pause time period included in the pause frame. The reception pause timer 38 is activated by the pause time period and an activation command RXT_ACT of the reception block 36 and sends a time-out signal RXT_CPL to the transmission block 32 if the pause time period has elapsed.

Now, a more detailed description of the Ethernet switch 10 will be given hereinbelow referring to FIGs. 1, 2, and 3.

The up/down counter of the packet memory interface 24 in the Ethernet switch 10, which is a downstream device operated at a full duplex mode, counts up/down upon enqueueing/dequeueing packet data in/from the packet memory 22. The packet memory interface 24 compares the count value with a predetermined threshold value indicating "buffer full" at every enqueueing/dequeueing and feeds a buffer status signal buf_full to the frame pause generator 30 of the MAC unit 28. If the count value is larger than the threshold value, the packet memory interface 24 transmits all MAC units 28 of the Ethernet switch 10 a buffer status signal set to 1, buf_full="1" indicating that the packet memory 22 is placed in a buffer-full state.

Referring to FIG. 3, the pause frame generator 30 in each MAC unit 28 receives the buffer status signal buf_full at every enqueueing/dequeueing in step 100 and determines whether the packet memory 22 is placed in a buffer-full state from the buffer status signal buf_full in step 102. The buffer full status signal set to 1 buf_full="1" implies that the packet memory 22 is placed in the buffer-full state, that is, the Ethernet switch 10 is congested. Then, the pause frame generator 30 constructs a pause frame based on the pause time information received from the host processor 26 in an initialization state and transmits the pause frame to the transmission block 32 in step 104. The pause frame includes a broadcast address, a pause operation code, and a pause time.

In step 106, the transmission block 32 in each MAC unit 28 transmits the pause frame to a corresponding Ethernet switch 12-1 to 12-N through an input port corresponding to the MAC unit 28 and activates the remote pause timer 34. The remote pause timer 34 counts an expected pause time period for which the

plurality of Ethernet switches 12-1 to 12-N stop data transmission temporarily. The remote pause timer 34 is activated by the expected pause time and the activation command RPT_ACT of the transmission block 32. The expected pause time is equal to or smaller than a pause time included in the pause frame. In step 108, it is determined whether the remote pause timer 34 has expired and the remote pause timer 34 transmits the time-out signal RPT_CPL to the transmission block 32 upon time-out of the expected pause time period.

Upon reception of the time-out signal RPT_CPL, the transmission block 32 notifies the pause frame generator 30 of the time-out of the expected pause time. Then, the pause frame generator 30 determines whether the packet memory 22 is placed in a buffer-full state in step 102.

Now there will be given a detailed description of a flow control operation in each Ethernet switch 12-1 to 12-N being an upstream device at a full duplex mode, shown in FIG. 4, referring to FIGs. 1, 2, and 4.

In step 200, it is determined whether the reception block 36 of a corresponding MAC unit 28 in each Ethernet switch 12-1 to 12-N has received the pause frame from the Ethernet switch 10. If the pause frame has been received, the reception block 36 activates the reception pause timer 38 based on the pause time included in the pause frame in step 202. The reception pause timer 38 is activated based on the pause time and the activation command RXT_ACT of the reception block 36. If the reception pause timer 38 has expired, it transmits the time-out signal RXT_CPL to the transmission block 32 through the reception block 36 in step 204. In step 208, a packet data transmissible state is entered. Thus, if there is packet data to be transmitted to the Ethernet switch 10, the packet data is transmitted.

If the reception block 36 in each Ethernet switch (upstream) has received a pause frame before the time-out in steps 204 and 206, the procedure returns to step 202 to stop transmission of packet data and activate the reception pause timer 38 based on a pause time included in the received pause frame.

In accordance with the first embodiment of the present invention, congestion-caused packet loss is minimized and a packet processing rate is increased over the entire network. Furthermore, a flow control is facilitated.

FIG. 5 is a block diagram of the Ethernet switch 10 in a full duplex mode according to a second embodiment of the present invention, and FIG. 6 is a flowchart depicting a flow control operation in the Ethernet switch 10 in the full duplex mode according to the second embodiment of the present invention.

In the second embodiment of the present invention, a specific input port causing a congestion in the Ethernet switch 10 is detected and subject to a flow control, so that transmission of packet data through the input port is limited and corresponding Ethernet switches being upstream devices can transmit packet data through other input ports of the Ethernet switch 10.

The input port causing a congestion (hereinafter referred to as 'congested input port') can be detected in the following way. The common buffer 20 of the Ethernet switch 10 maintains a logical queue for each output port because it is an output buffering structure. More specifically, if N is the number of ports, there are N logical queues for the output ports in the common buffer 20. Accordingly, the number of packets in the packet memory 22, received through each input port at the time point of a congestion cannot be known. That is, a congested input port is not known. To solve this problem, N packet counters are provided to count the numbers of packet data input and output to and from each input port in

the second embodiment of the present invention.

Referring to FIGs. 5 and 7, the packet memory interface 24 of the common buffer 20 has N packet counters 40 for N input ports for counting up upon storing data received through a corresponding input port in the packet memory 22 of the common buffer 20 and counts down upon reading packet data from the packet memory 22 and output through the corresponding input port. If a count value of a specific packet counter exceeds a predetermined threshold value THR, the Ethernet switch 10 considers that the corresponding input port is likely to incur a congestion and performs a flow control. The predetermined threshold value THR is provided from the host processor 26 and can be equal or different among the input ports. The threshold value THR may vary with traffic characteristics, for example, traffic burstness.

A more detailed description of a flow control according to the second embodiment of the present invention will be given hereinbelow. The packet counters 40 for the N input ports count up upon storing packet data received through corresponding input ports in the packet memory 22 and count down upon outputting packet data read from the packet memory 22 through the corresponding input ports. If a count value of a specific packet counter exceeds a predetermined threshold value THR, the packet memory interface 24 shown in FIGs. 5 and 7 sends the MAC unit 24 a signal indicating that the corresponding input port is congested. Then, the MAC unit 28 implements a flow control on the congested input port alone. The configuration and operation of the MAC unit 28 shown in FIG. 5 are the same as those of the MAC unit 28 of FIG. 2. Thus, its detailed description will be omitted.

In accordance with the second embodiment of the present invention, congestion is prevented and input ports can equally share a bandwidth.

FIG. 6 is a flowchart depicting a flow control in the Ethernet switch 10 at a full duplex mode according to the second embodiment of the present invention. Referring to FIG. 6, the Ethernet switch 10 receives a threshold value THR for each input port from the host processor 26 in an initialization state in step 300. Upon enqueueing/dequeueing packet data to/from the packet memory 22, a corresponding packet counter counts up/down in step 302. The count value of the packet counter is compared with the threshold value THR preset for the input port in step 304. If the former is larger than the latter, the input port is considered congested and only the MAC unit 28 of the input port constructs a pause frame in step 306. The pause frame is constructed by the pause frame generator 30 and transmitted to the transmission block 32. The Ethernet switch 10 transmits the pause frame to an Ethernet switch connected to the congested input port and activates the remote pause timer 34 to count an expected pause time in step 308. If the remote pause timer 34 has expired in step 310, it is determined whether there is any other congested input port back in step 302. In the presence of a congested input port, a flow control is performed on the congested input port.

A flow control operation of an upstream device using the full duplex mode according to the second embodiment of the present invention is the same as in the first embodiment of the present invention. Thus, its description is omitted.

FIG. 7 is a block diagram of an Ethernet switch at a half duplex mode according to the second embodiment of the present invention. The components of the Ethernet switch except for the MAC unit 48 are the same in configuration as those of FIG. 5. The MAC unit 48 of FIG. 7 includes a jamming signal generator 50 and a transmission/reception block 52.

FIG. 8 is a flowchart depicting a flow control operation in the Ethernet switch 10 at a half duplex communication mode according to the second embodiment of the present invention. Referring to FIG. 8, the Ethernet switch 10 receives a threshold value THR for each input port from the host processor 26 in an initialization state in step 400. Upon enqueueing/dequeueing packet data to/from the packet memory 22, a corresponding packet counter counts up/down in step 402. The count value of the packet counter is compared with the threshold value THR preset for the input port in step 404. If the former is larger than the latter, the input port is considered congested and only the MAC unit 28 of the input port generates a jamming signal in step 406. The jamming signal is generated by the jamming signal generator 50 and transmitted to the transmission/reception block 52. The Ethernet switch 10 transmits the jamming signal to an Ethernet switch connected to the congested input port in step 406.

In the second embodiment of the present invention, a specific input port causing a congestion in the Ethernet switch 10 is detected and subject to a flow control, so that transmission of packet data through the input port is limited and corresponding Ethernet switches being upstream devices can transmit packet data to the Ethernet switch 10 through other input ports of the Ethernet switch 10.

As described above, the present invention is advantageous in that packet loss caused by a congestion is minimized and a packet processing rate is increased over the entire network. Furthermore, a flow control is facilitated.

While the invention has been shown and described with reference to certain preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

CLAIMS:

1. A flow control method in a downstream Ethernet switch using a full duplex mode in a packet switched network, the downstream Ethernet switch having a plurality of input ports connected to a plurality of upstream Ethernet switches and a common memory for storing packet data received from each input port, the method comprising the steps of:

determining a buffer state of the common memory;

transmitting a pause frame including a predetermined pause time to the plurality of upstream Ethernet switches and counting an expected pause time of the upstream Ethernet switches, if the buffer state is buffer-full;

determining the buffer state of the common memory again if the expected pause time has expired; and

re-transmitting the pause frame including the predetermined pause time to the plurality of upstream Ethernet switches and counting the expected pause time of the upstream Ethernet switches, if the buffer state is buffer-full.

2. The method of claim 1, wherein the buffer state is determined every time packet data is written in or read from the common memory.

3. A flow control method in a downstream Ethernet switch using a full duplex mode in a packet switched network, the Ethernet downstream switch having a plurality of input ports connected to a plurality of upstream Ethernet switches and a common memory for storing packet data

received from each input port, the method comprising the steps of:

determining a buffer state of the common memory for each input port;

transmitting a pause frame including a predetermined pause time to an upstream Ethernet switch connected to a congested input port and counting an expected pause time of the upstream Ethernet switch, if the buffer state of the input port is buffer-full;

determining the buffer state of the common memory again for each input port if the expected pause time has expired; and

re-transmitting the pause frame including the predetermined pause time to the upstream Ethernet switch and counting the expected pause time of the upstream Ethernet switch, if the buffer state of the congested input port is buffer-full.

4. The method of claim 3, wherein the common memory includes one packet counter for each input port to determine the buffer state of the common memory for each input port.

5. The method of claim 3, wherein it is determined whether each input port is buffer-full by comparing the buffer state of the common memory for the input port with a threshold value predetermined for the input port.

6. The method of claim 5, wherein the threshold value is equal or different for each input port according to traffic characteristics.

7. A flow control method in a downstream Ethernet switch using a full duplex mode in a packet switched

network, the downstream Ethernet switch having a plurality of input ports connected to a plurality of upstream Ethernet switches and a common memory for storing packet data received from each input port, the method comprising the steps of:

determining a buffer state of the common memory for each input port; and

transmitting a jamming signal to an upstream Ethernet switch connected to a congested input port, if the buffer state of the input port is buffer-full,

wherein the common memory includes one packet counter for each input port to determine the buffer state of the common memory for each input port.

8. The method of claim 7, wherein it is determined whether each input port is buffer-full by comparing the buffer state of the common memory for each input port with a threshold value predetermined for each input port.

9. The method of claim 8, wherein the threshold value is equal or different for each input port according to traffic characteristics.

10. An Ethernet switch for transmitting/receiving data to/from other Ethernet switches using a full duplex mode in a packet switch network, comprising:

a common buffer including a packet memory storing packet data input via a plurality of input ports, and packet counters provided for the plurality of input ports for counting an input packet for each corresponding port;

a pause frame generator for generating a pause frame including pause time information for stopping

transmission of packet data for a predetermined time period; and

a host processor for determining whether a count value of at least one packet counter of the packet counters exceeds a predetermined threshold value and, if the threshold value is exceeded, controlling the pause frame generator for transmitting the pause frame to an Ethernet switch corresponding to the input port for which the threshold value is exceeded.

11. The Ethernet switch of claim 10 further comprising:

a remote pause timer for counting the pause time of the pause frame; and

if the pause time is exceeded by the timer after transmitting the pause frame, re-examining whether the threshold value is exceeded by the count value of the packet counter corresponding to at least one input port transmitting the pause frame in the host processor.

12. An Ethernet switch for transmitting/receiving data to/from other Ethernet switches using a full duplex mode in a packet switched network, comprising:

a common buffer including a packet memory storing packet data input via a plurality of input ports, and packet counters being provided for the plurality of input ports for executing an up count if a packet data is input via each input port and executing a down count if the packet data is output;

a pause frame generator for generating a pause frame including pause time information for stopping

transmission of packet data for a predetermined time period; and

a host processor for determining whether a count value of at least one packet counter of the packet counters exceeds a predetermined threshold value and, if the threshold value is exceeded, controlling the pause frame generator for transmitting the pause frame to an Ethernet switch corresponding to the input port for which the threshold value is exceeded.

13. The Ethernet switch of claim 12, further comprising:

a remote pause timer for counting the pause time of the pause frame; and

if the pause time is exceeded by the timer after transmitting the pause frame, re-examining whether the threshold value is exceeded by the count value of packet counter corresponding to at least one input port transmitting the pause frame in the host processor.

14. An Ethernet switch for transmitting/receiving data to/from other Ethernet switches using a half duplex mode in a packet switched network, comprising:

a common buffer including a packet memory storing packet data input via a plurality of input ports, and packet counters being provided for the plurality of input port, for executing an up count if a packet data is input via each input port, and executing a down count if the packet data is output;

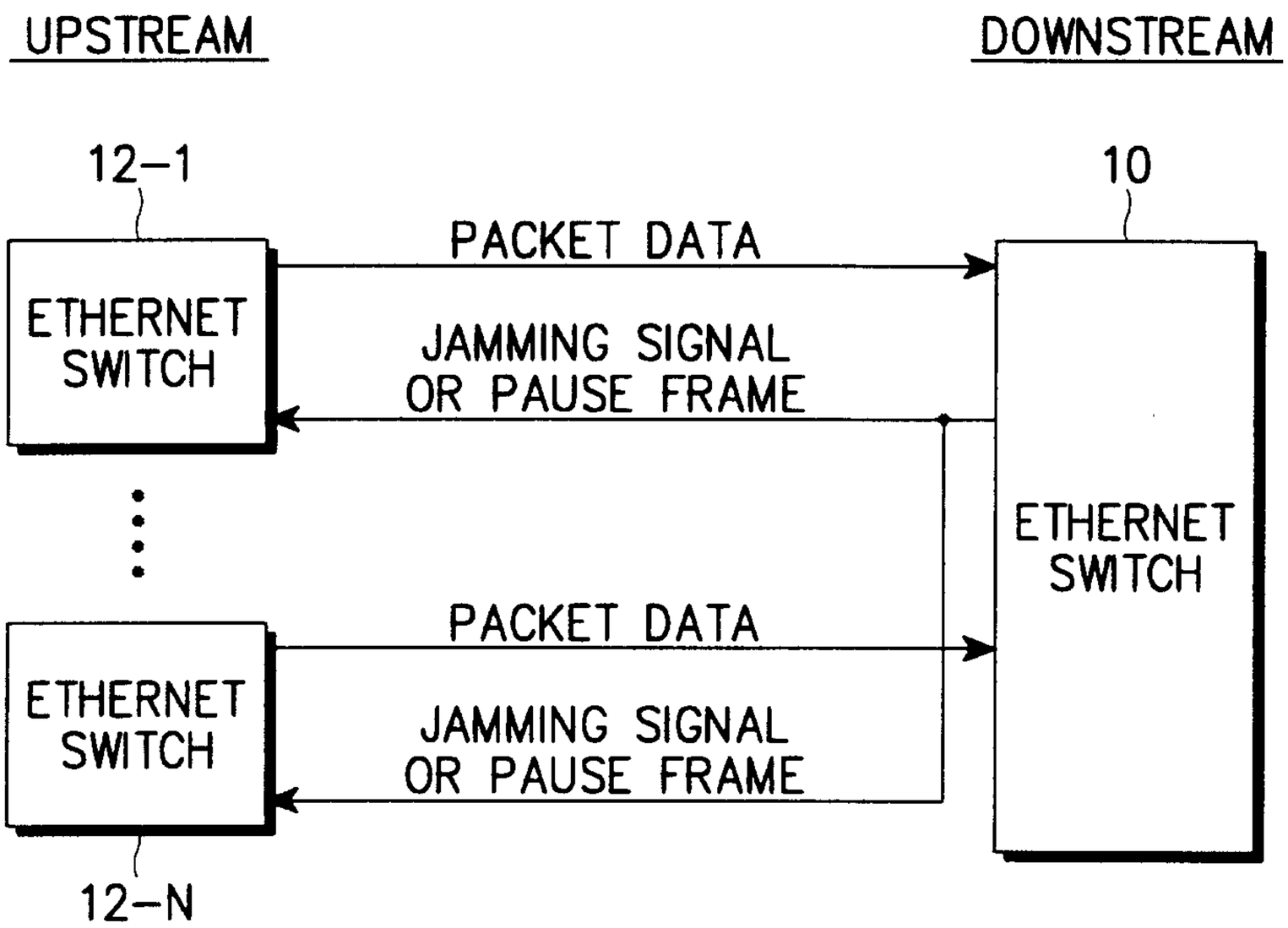
a jamming signal generator for generating a jamming signal for stopping transmission of packet data; and

a host processor for determining whether a count value of at least one packet counter of the packet counters exceeds a predetermined threshold value and if the threshold value is exceeded, controlling the jamming signal generator for transmitting the jamming signal to an Ethernet switch corresponding to the input port for which the threshold value is exceeded.

SMART & BIGGAR

OTTAWA, CANADA

PATENT AGENTS


UPSTREAM
DOWNSTREAM
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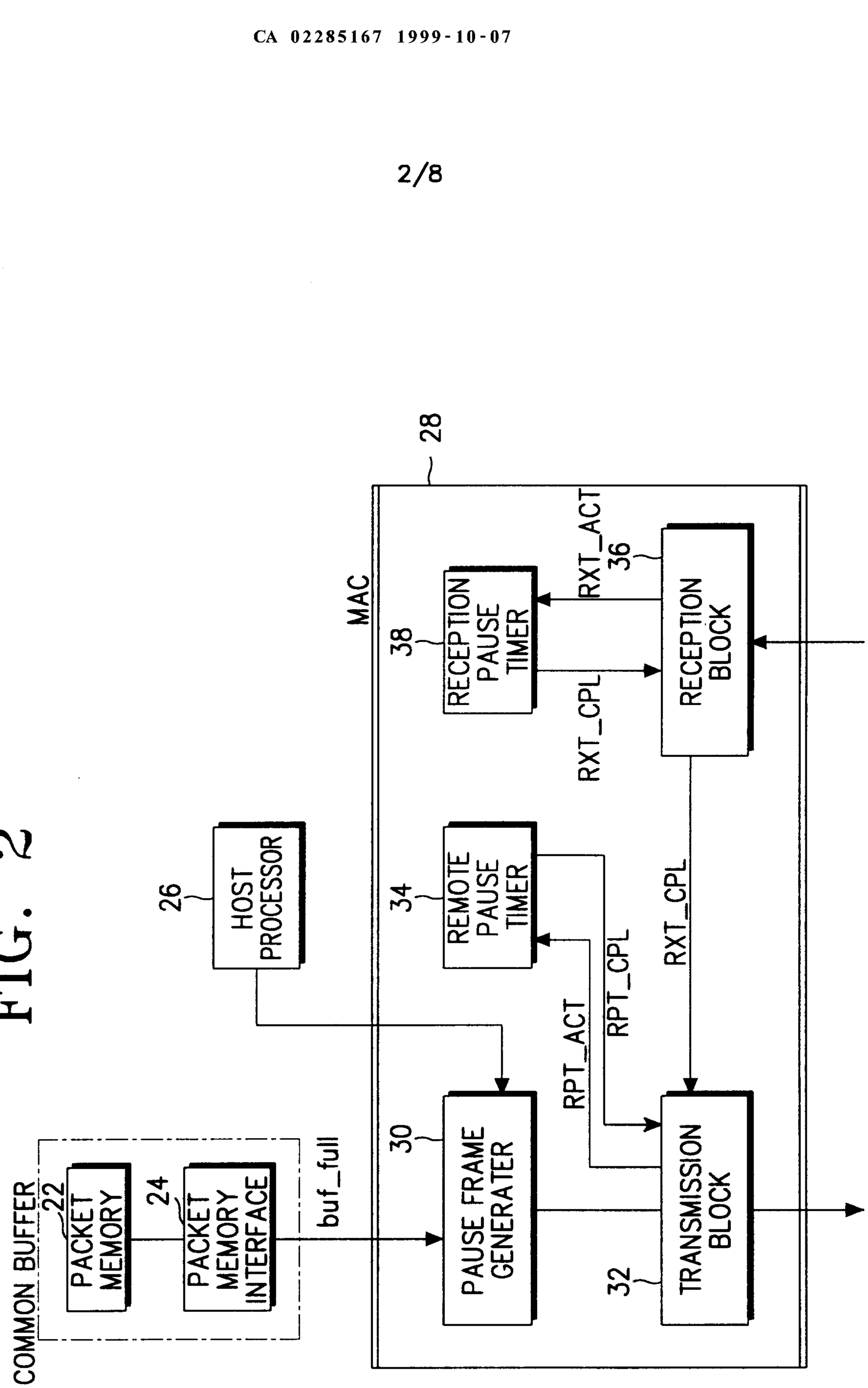
10
ETHERNET SWITCH
PACKET DATA
JAMMING SIGNAL OR PAUSE FRAME
ETHERNET SWITCH
PACKET DATA
JAMMING SIGNAL OR PAUSE FRAME
ETHERNET SWITCH
12-N

FIG. 1

FIG. 2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MAC
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RECEPTION PAUSE TIMER
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RXT_CPL
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HOST PROCESSOR
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REMOTE PAUSE TIMER
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PAUSE FRAME GENERATER
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TRANSMISSION BLOCK
COMMON BUFFER
22
PACKET MEMORY
24
PACKET MEMORY INTERFACE
buf_full

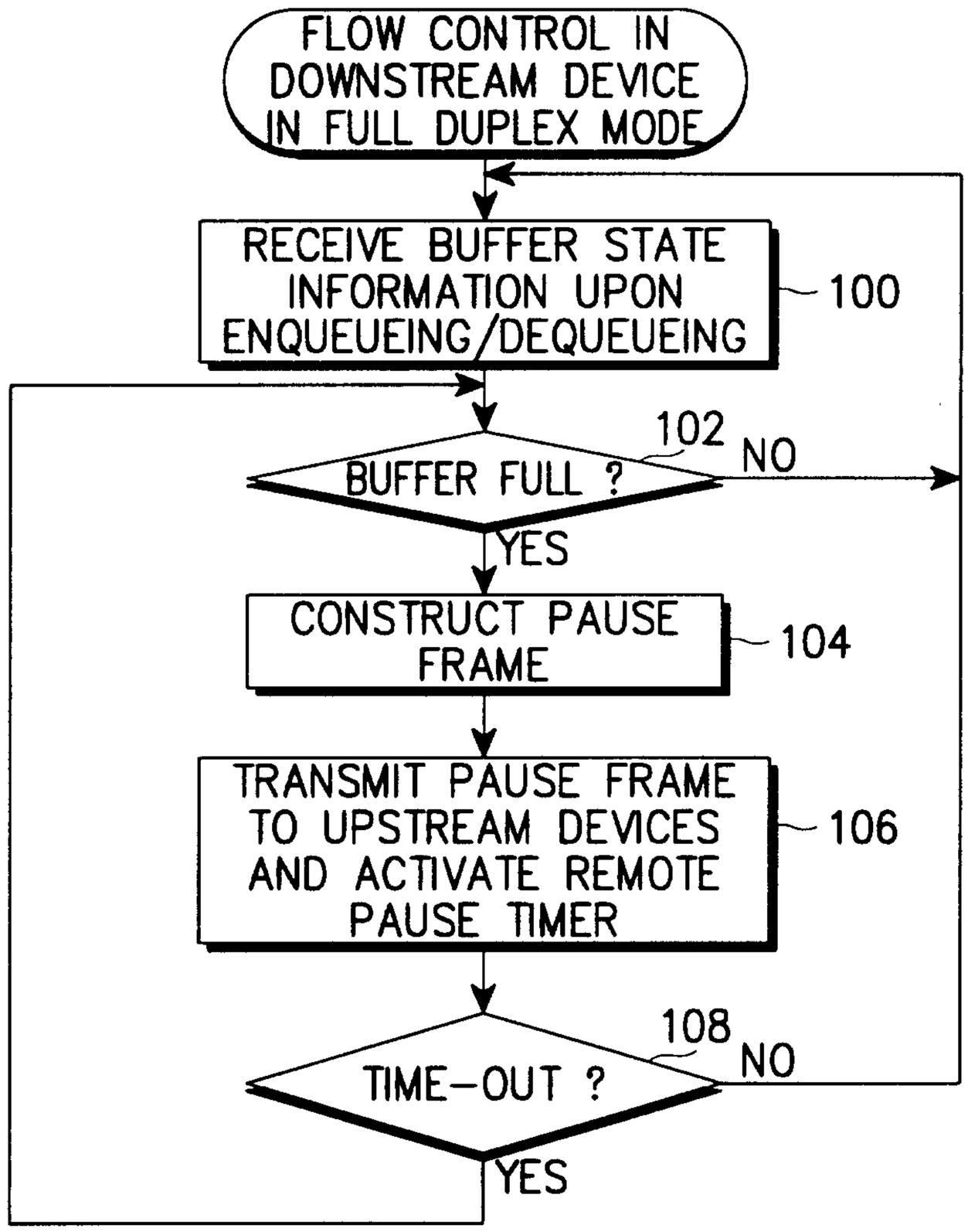

FLOW CONTROL IN DOWNSTREAM DEVICE IN FULL DUPLEX MODE
RECEIVE BUFFER STATE INFORMATION UPON ENQUEUEING/DEQUEUEING
100
102
BUFFER FULL ?
NO
YES
CONSTRUCT PAUSE FRAME
104
TRANSMIT PAUSE FRAME TO UPSTREAM DEVICES AND ACTIVATE REMOTE PAUSE TIMER
106
108
TIME-OUT ?
NO
YES

FIG. 3

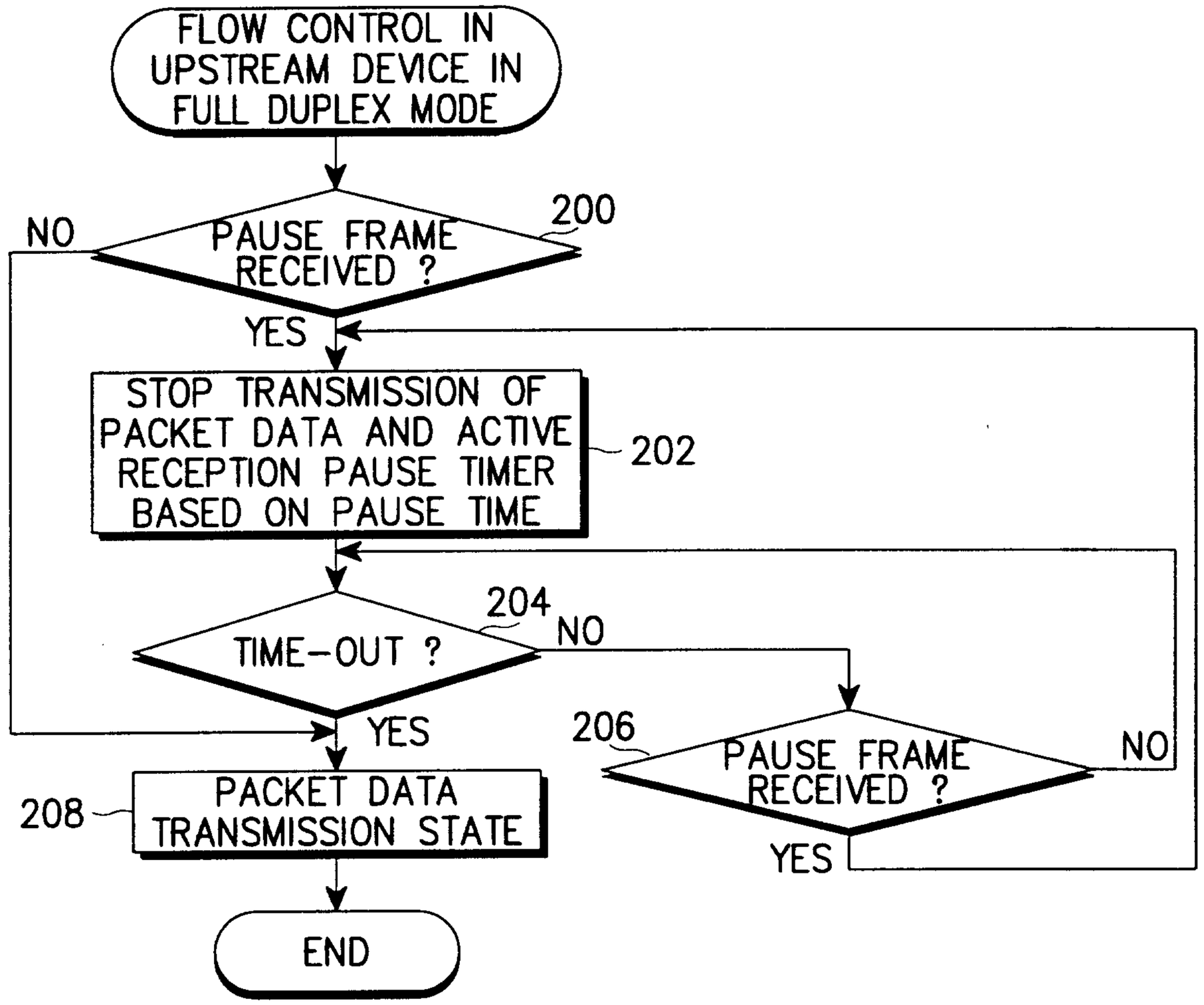
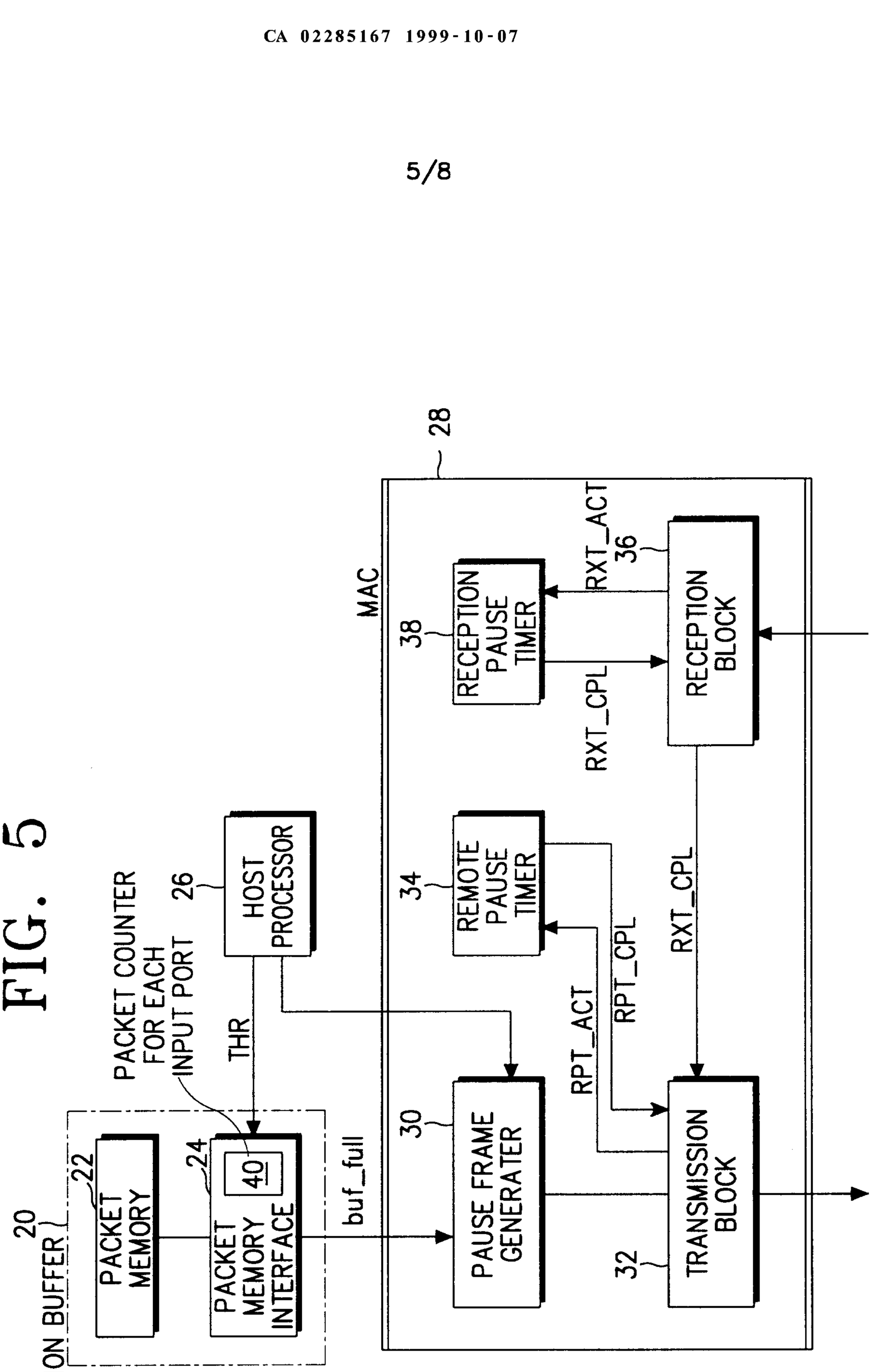

FLOW CONTROL IN UPSTREAM DEVICE IN FULL DUPLEX MODE
PAUSE FRAME RECEIVED ?
200
NO
YES
STOP TRANSMISSION OF PACKET DATA AND ACTIVE RECEPTION PAUSE TIMER BASED ON PAUSE TIME
202
TIME-OUT ?
204
NO
YES
PAUSE FRAME RECEIVED ?
206
NO
YES
PACKET DATA TRANSMISSION STATE
208
END

FIG. 4

FIG. 5


COMMON BUFFER
20
PACKET MEMORY
22
PACKET MEMORY INTERFACE
24
40
PACKET COUNTER FOR EACH INPUT PORT
buf_full
HOST PROCESSOR
26
THR
MAC
8
RECEPTION PAUSE TIMER
38
RXT_ACT
36
RXT_CPL
RECEPTION BLOCK
REMOTE PAUSE TIMER
34
PAUSE FRAME GENERATER
30
RPT_ACT
RPT_CPL
RXT_CPL
TRANSMISSION BLOCK
32

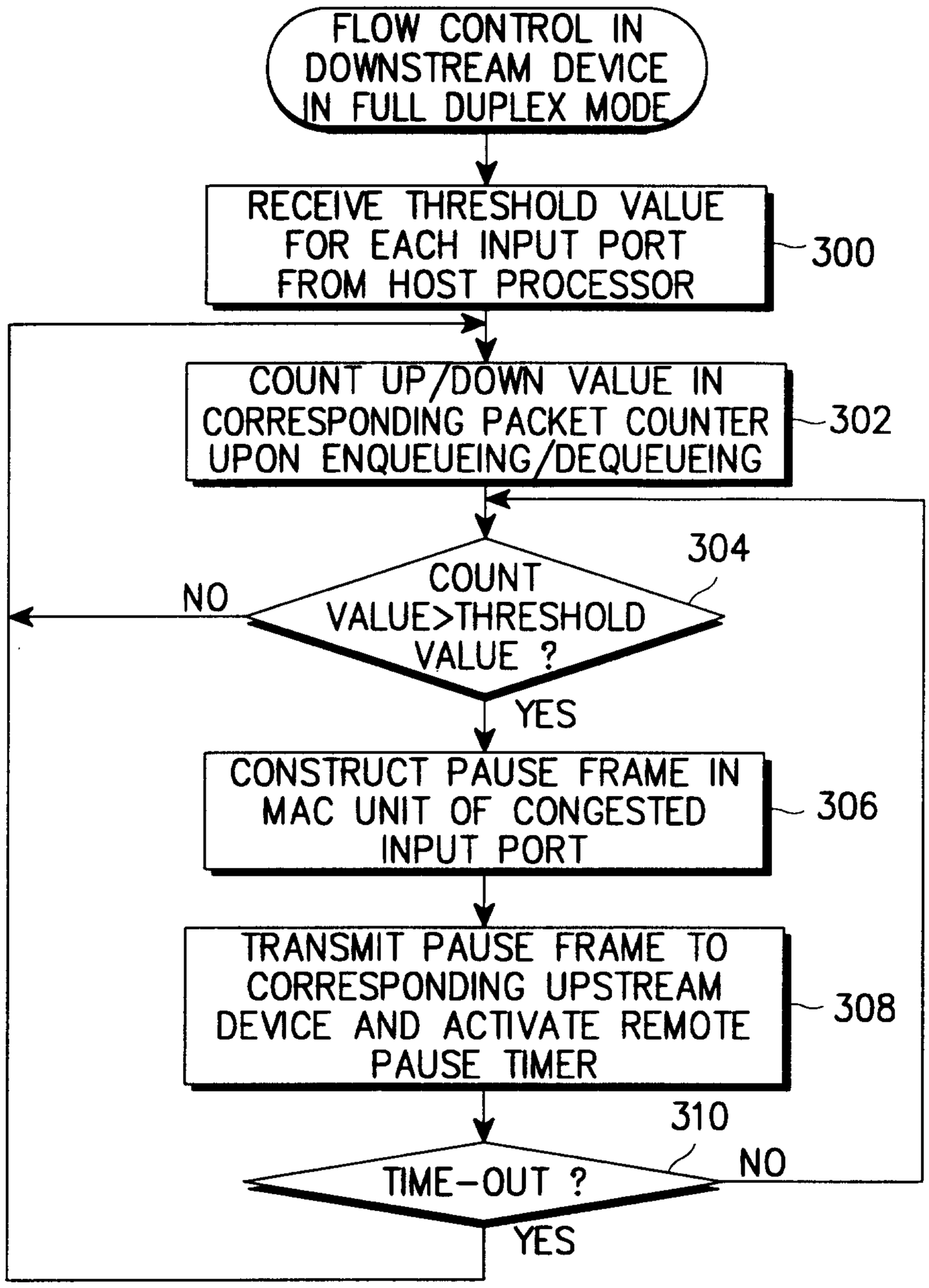

FLOW CONTROL IN DOWNSTREAM DEVICE IN FULL DUPLEX MODE
RECEIVE THRESHOLD VALUE FOR EACH INPUT PORT FROM HOST PROCESSOR
300
COUNT UP/DOWN VALUE IN CORRESPONDING PACKET COUNTER UPON ENQUEUEING/DEQUEUEING
302
304
COUNT VALUE>THRESHOLD VALUE ?
NO
YES
CONSTRUCT PAUSE FRAME IN MAC UNIT OF CONGESTED INPUT PORT
306
TRANSMIT PAUSE FRAME TO CORRESPONDING UPSTREAM DEVICE AND ACTIVATE REMOTE PAUSE TIMER
308
310
TIME-OUT ?
NO
YES

FIG. 6

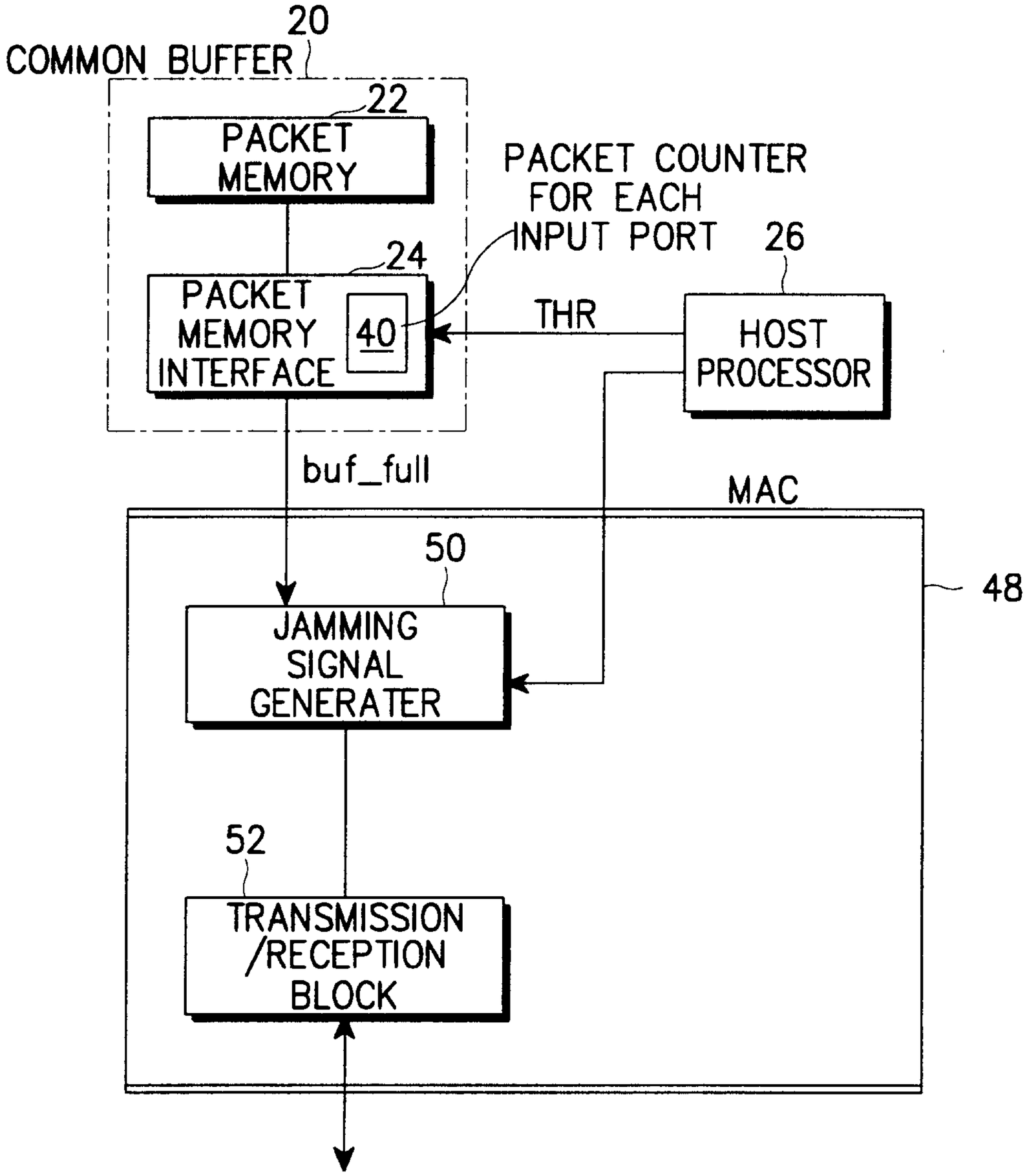

20
COMMON BUFFER
22
PACKET MEMORY
PACKET COUNTER FOR EACH INPUT PORT
26
24
PACKET MEMORY INTERFACE
40
THR
HOST PROCESSOR
buf_full
MAC
50
48
JAMMING SIGNAL GENERATER
52
TRANSMISSION /RECEPTION BLOCK

FIG. 7

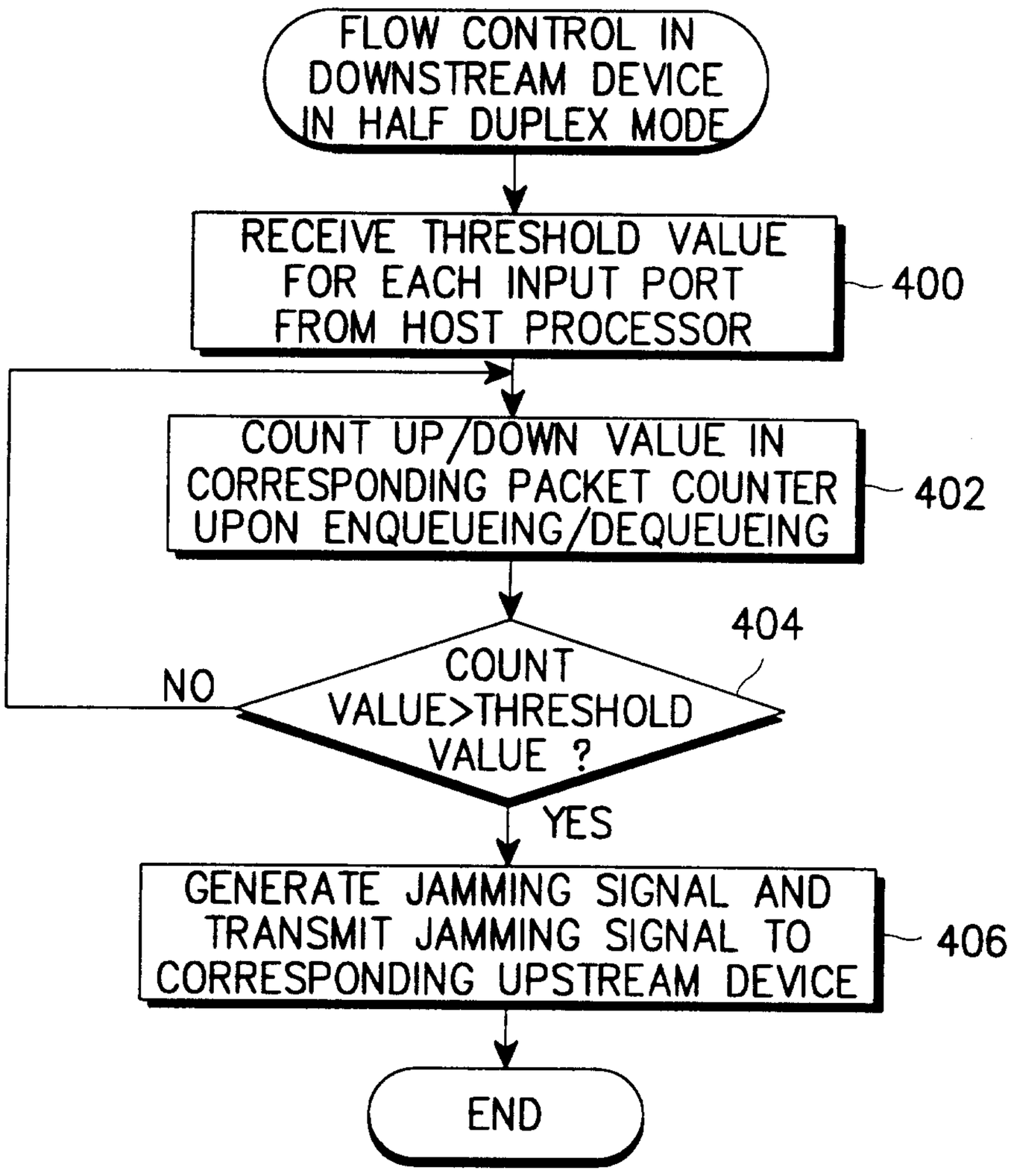
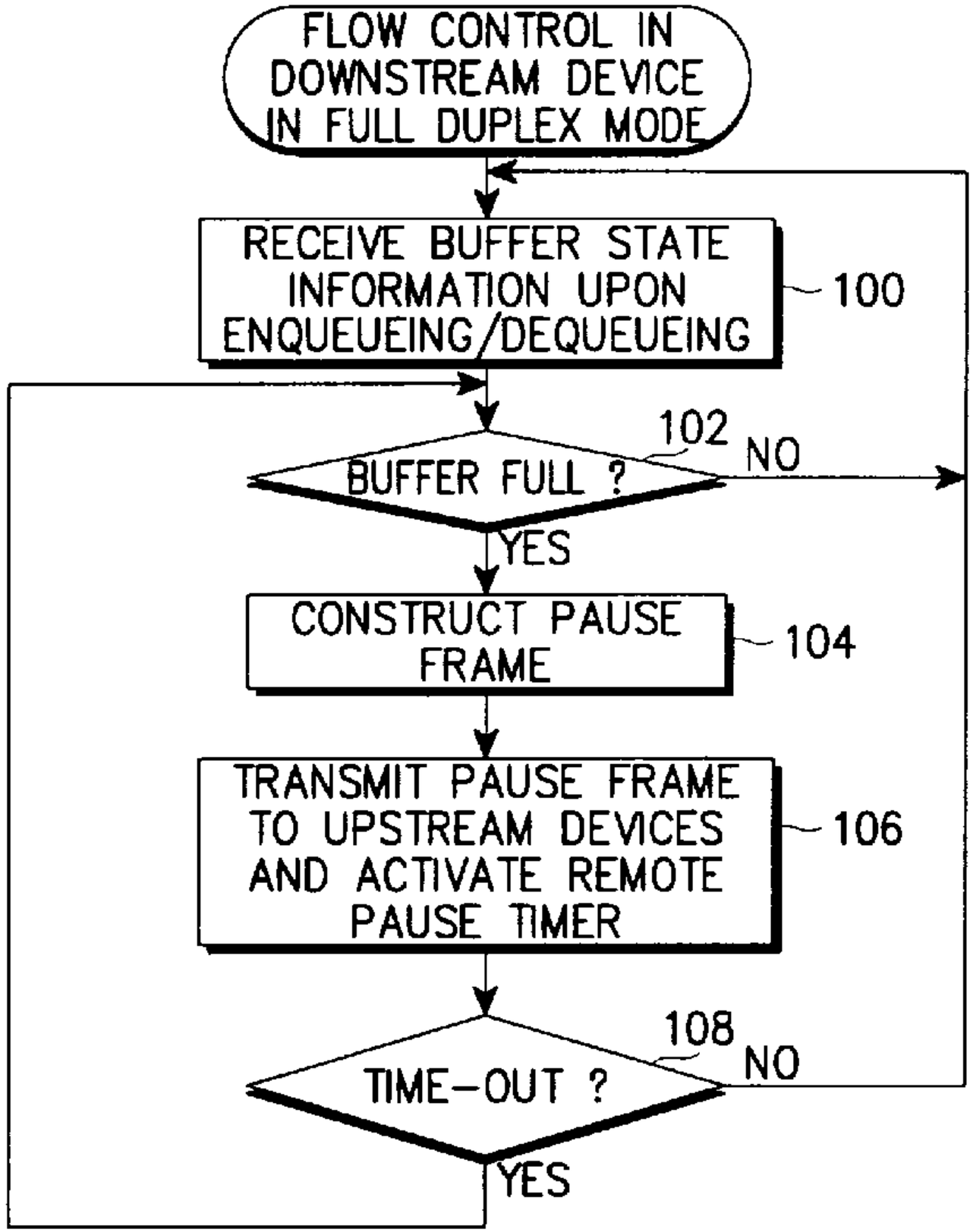

FLOW CONTROL IN DOWNSTREAM DEVICE IN HALF DUPLEX MODE
RECEIVE THRESHOLD VALUE FOR EACH INPUT PORT FROM HOST PROCESSOR
400
COUNT UP/DOWN VALUE IN CORRESPONDING PACKET COUNTER UPON ENQUEUEING/DEQUEUEING
402
404
COUNT VALUE>THRESHOLD VALUE ?
NO
YES
GENERATE JAMMING SIGNAL AND TRANSMIT JAMMING SIGNAL TO CORRESPONDING UPSTREAM DEVICE
406
END

FIG. 8


FLOW CONTROL IN DOWNSTREAM DEVICE IN FULL DUPLEX MODE
RECEIVE BUFFER STATE INFORMATION UPON ENQUEUEING/DEQUEUEING
100
BUFFER FULL ?
102
NO
YES
CONSTRUCT PAUSE FRAME
104
TRANSMIT PAUSE FRAME TO UPSTREAM DEVICES AND ACTIVATE REMOTE PAUSE TIMER
106
TIME-OUT ?
108
NO
YES