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(54) **TEST APPARATUS AND SEMICONDUCTOR CHIP**

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(57) **ABSTRACT**

A test apparatus may be provided. The test apparatus may include a delay compensator configured to generate delayed read data by delaying read data according to a difference between an external turnaround delay value provided externally from the test apparatus and a turnaround delay detection value detected within the test apparatus. The test apparatus may include a determination circuit configured to perform a test result determination operation by comparing the delayed read data with reference data. The turnaround delay detection value may be generated by detecting a time of from a point of time when write data including a read command as the reference data is output to a point of time when the read data is received.

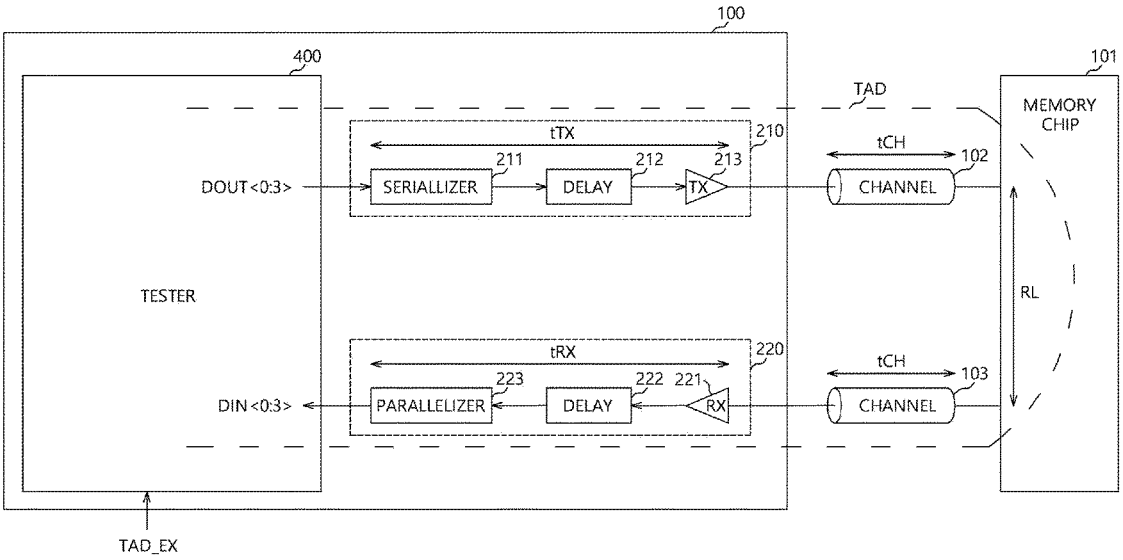


FIG.1

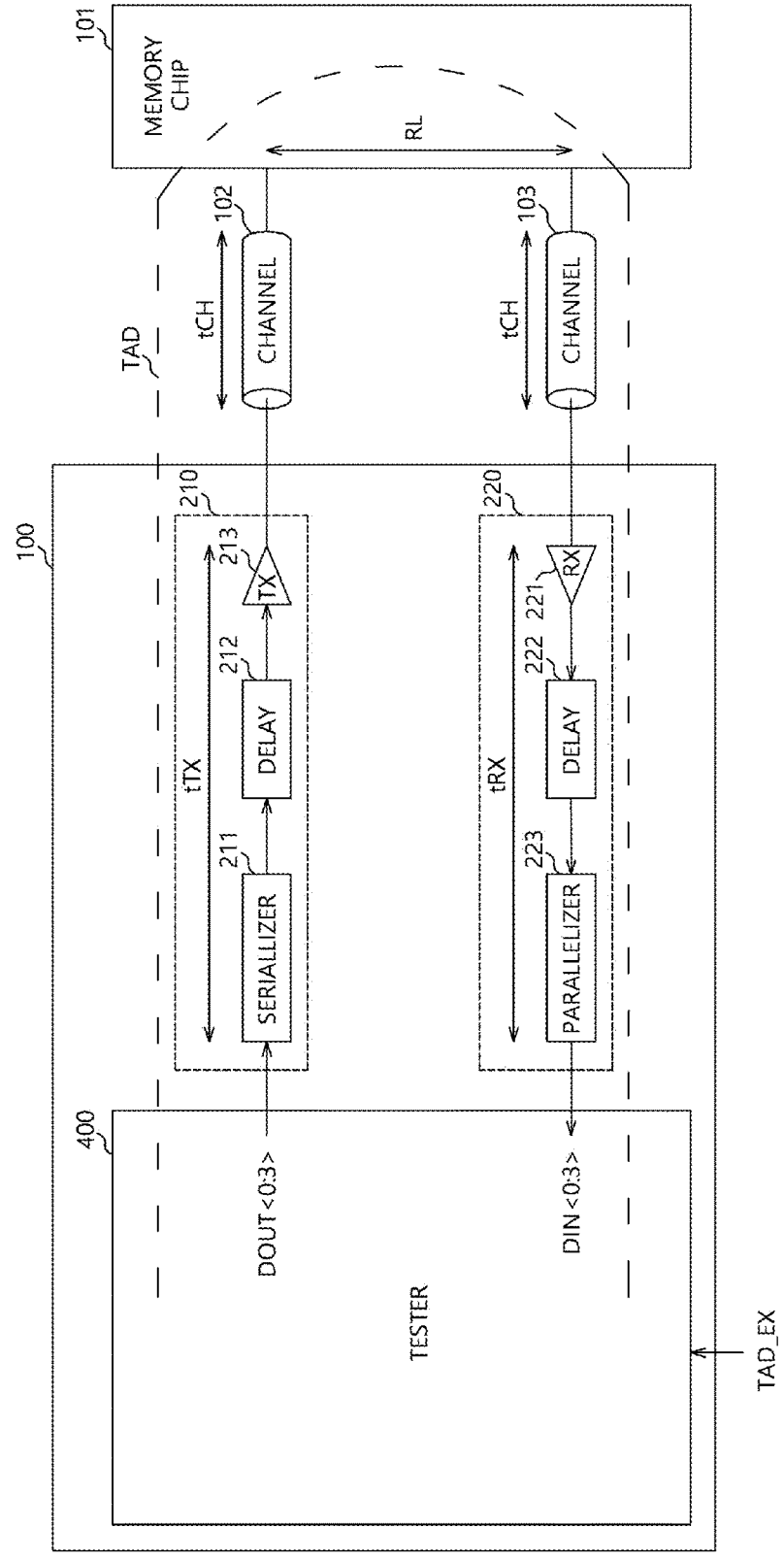

101
MEMORY CHIP
RL
102
103
tCH
CHANNEL
TAD
100
210
220
213
TX
212
DELAY
tTX
211
SERIALLIZER
221
RX
222
DELAY
tRX
223
PARALLELIZER
400
DOUT<0:3>
DIN<0:3>
TESTER
TAD_EX

FIG.2

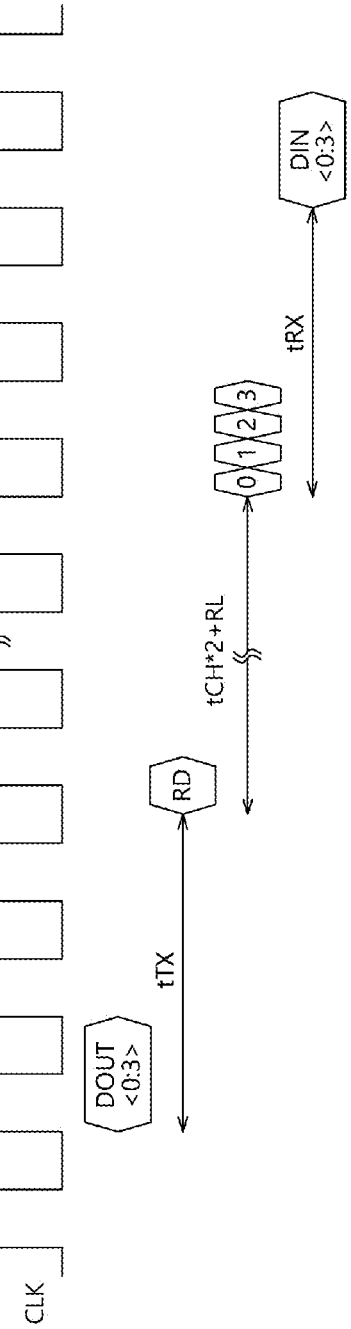


FIG.3

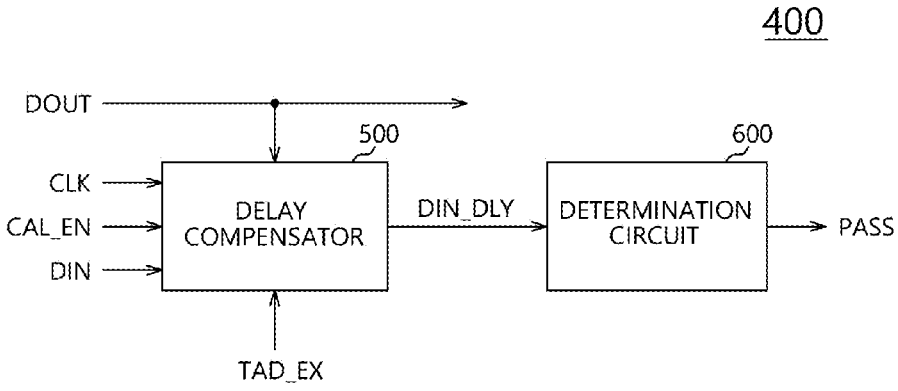

400
DOUT
500
600
CLK
CAL_EN
DIN
DELAY COMPENSATOR
DIN_DLY
DETERMINATION CIRCUIT
PASS
TAD_EX

FIG.4

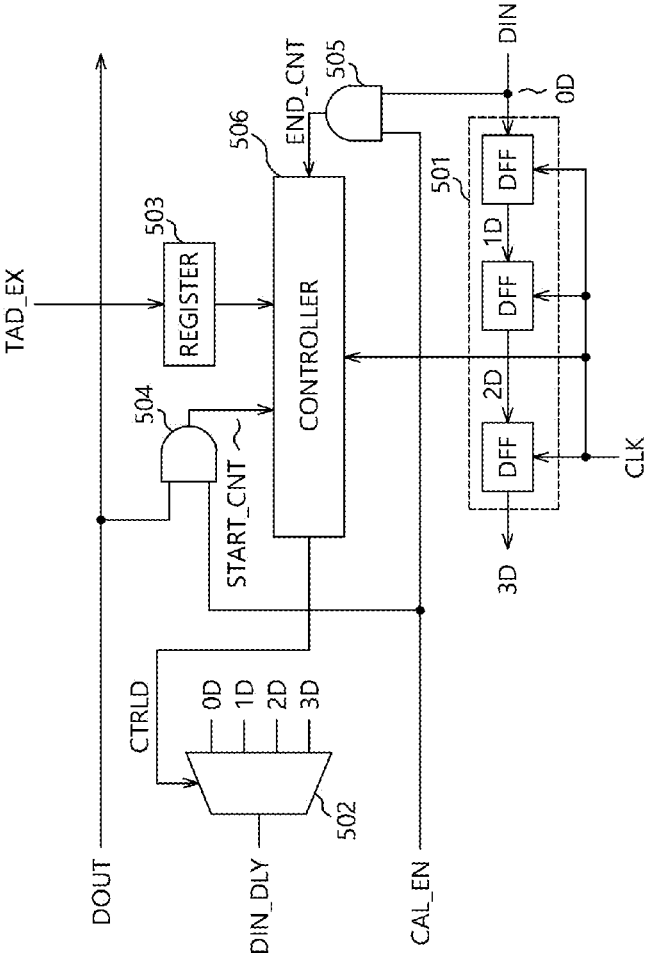
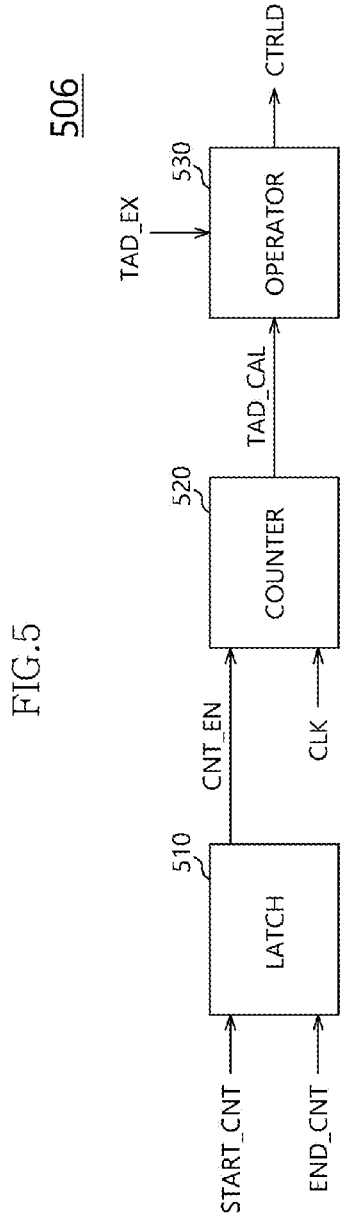

500
TAD_EX
REGISTER
503
CONTROLLER
506
END_CNT
505
DIN
0D
501
DFF
1D
DFF
2D
DFF
3D
CLK
504
START_CNT
CTRLD
0D
1D
2D
3D
502
DOUT
DIN_DLY
CAL_EN

FIG.5


506
510
LATCH
520
COUNTER
530
OPERATOR
START_CNT
END_CNT
CNT_EN
CLK
TAD_CAL
TAD_EX
CTRLD

TEST APPARATUS AND SEMICONDUCTOR CHIP

CROSS-REFERENCES TO RELATED APPLICATION

[0001] This application claims priority under 35 U.S.C. 119(a) to Korean application No. 10-2016-0024360, filed on Feb. 29, 2016, in the Korean intellectual property Office, which is incorporated by reference in its entirety as set forth in full.

BACKGROUND

[0002] 1. Technical Field

[0003] Various embodiments may generally relate to a semiconductor integrated circuit, and more particularly, to a test apparatus for testing a semiconductor chip.

[0004] 2. Related Art

[0005] Test apparatuses for testing a data input/output (I/O) operation of a semiconductor chip, for example, a memory chip may store write data in the memory chip. As such, a determination may be made on whether the memory chip has passed or failed by comparing read data output from the memory chip according to a read command with the write data stored therein.

[0006] A delay time of from a point of time when the read command is generate to a point of time when the read data is input may refer to a turnaround delay (TAD).

[0007] An asynchronous delay component is included in the turnaround delay. The asynchronous delay may be influenced by variation in power, voltage, and temperature, and thus the turnaround delay value may be changed. Since the test apparatus may have no information for the variation of the turnaround delay, the reliability of the test operation may be degraded.

SUMMARY

[0008] According to an embodiment, a test apparatus may be provided. The test apparatus may include a delay compensator configured to generate delayed read data by delaying read data according to a difference between an external turnaround delay value provided externally from the test apparatus and a turnaround delay detection value detected within the test apparatus. The test apparatus may include a determination circuit configured to perform a test result determination operation by comparing the delayed read data with reference data. The turnaround delay detection value may be generated by detecting a time of from a point of time when write data including a read command as the reference data is output to a point of time when the read data is received.

[0009] According to an embodiment, a test apparatus may be provided. The test apparatus may include a tester configured to set a delay compensation time of read data by detecting a turnaround delay of from a first point of time when write data including a read command is output in a turnaround delay compensation mode to a second point of time when the read data received exteriorly from the test apparatus is received, generate delayed read data by delaying the read data by the delay compensation time in a normal test mode, and perform a test result determination operation by comparing the delayed read data with the write data as reference data.

[0010] According to an embodiment, a test apparatus for a semiconductor chip may be provided. The test apparatus may include a delay compensator configured to generate delayed read data by delaying read data according to a difference between an external turnaround delay value provided externally from the test apparatus and a turnaround delay detection value detected within the test apparatus. The test apparatus may include a determination circuit configured to perform a test result determination operation by comparing the delayed read data with reference data. The turnaround delay detection value may be generated by detecting a time of from a point of time when write data including a read command as the reference data is output to the semiconductor chip to a point of time when the read data is input from the semiconductor chip.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIG. **1** is a view illustrating a representation of an example of a configuration of a test chip according to an embodiment.

[0012] FIG. **2** is a view for explaining an example of a turnaround delay according to the test chip of FIG. **1**.

[0013] FIG. **3** is a view illustrating a representation of an example of a configuration of a tester of FIG. **1**.

[0014] FIG. **4** is a view illustrating a representation of an example of a configuration of a delay compensator of FIG. **3**.

[0015] FIG. **5** is a view illustrating a representation of an example of a configuration of a controller of FIG. **4**.

DETAILED DESCRIPTION

[0016] Hereinafter, examples of embodiments will be described below with reference to the accompanying drawings. Examples of embodiments are described herein with reference to cross-sectional illustrations that are schematic illustrations of examples of embodiments (and intermediate structures). As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments should not be construed as limited to the particular shapes of regions illustrated herein but may be to include deviations in shapes that result, for example, from manufacturing. In the drawings, lengths and sizes of layers and regions may be exaggerated for clarity. Like reference numerals in the drawings denote like elements. It is also understood that when a layer is referred to as being "on" another layer or substrate, it can be directly on the other or substrate, or intervening layers may also be present.

[0017] The concepts are described herein may be discussed with reference to cross-section and/or plan illustrations that are schematic illustrations of various embodiments. However, the embodiments should not be construed as limiting. Although a few embodiments will be illustrated and described, it will be appreciated by those of ordinary skill in the art that changes may be made in these examples of embodiments without departing from the principles and spirit of the disclosure.

[0018] One or more examples of embodiments may be provided to a test apparatus capable of compensating a turnaround delay according to a chip to be tested.

[0019] Referring to FIG. **1**, a test chip **100** as a test apparatus according to an embodiment may be coupled to a

chip to be tested, for example, a memory chip **101** through a plurality of channels, for example, a first channel **102** and a second channel **103**.

[0020] The test chip **100** may include a plurality of path circuits (for example, a first path circuit **210** and a second path circuit **220**) and a tester **400**.

[0021] The first path circuit **210** may transmit write data DOUT<0:3> to the memory chip **101** through the first channel **102**.

[0022] An example of the write data DOUT<0:3> that a burst length is '4' is illustrated in FIG. **1**.

[0023] The write data DOUT<0:3> may include a command, for example, a read command or a write command.

[0024] A corresponding bit among bits constituting the write data DOUT<0:3> may be set to a predetermined value, and thus the memory chip **101** may recognize the write data DOUT<0:3> as the command, for example, the read command or the write command.

[0025] The first path circuit **210** may include a serializer **211**, a delay **212**, and a transmitter (TX) **213**.

[0026] The serializer **211** may serialize the write data DOUT<0:3> and output the serialized write data.

[0027] The delay **212** may delay an output of the serializer **211** by a preset time and output the delayed output of the serializer **211**.

[0028] The transmitter **213** may transmit an output of the delay **212** to the first channel **102**.

[0029] The second path circuit **220** may transmit the read data DIN<0:3> transmitted from the memory chip **101** to the tester **400** through the second channel **103**.

[0030] The second path circuit **220** may include a receiver (RX) **221**, a delay **222**, and a parallelizer **223**.

[0031] The receiver **221** may receive data transmitted through the second channel **103** and output the received data.

[0032] The delay **222** may delay an output of the receiver **221** by a preset time and output the delayed output of the receiver **221**.

[0033] The parallelizer **223** may parallelize an output of the delay **222** and input the parallelized output of the delay **222** as the read data DIN<0:3> to the tester **400**.

[0034] The tester **400** may include, for example, an algorithmic pattern generator (ALPG) (not illustrated).

[0035] The tester **400** may delay the read data DIN<0:3> according to a difference between an external turnaround delay value TAD_EX provided from the outside of the test apparatus **100** and a turnaround delay detection value generated by detecting a time of from a point of time when the write data DOUT<0:3> including the read command is output to the semiconductor chip **101** to a point of time when the read data DIN<0:3> output from the semiconductor chip **101** is input, and determine a pass or fail of the memory chip **101** by comparing the delayed read data with the write data. The semiconductor chip **101** may be realized with a memory chip **101** or include a memory chip **101**.

[0036] The time of from a point of time when the write data DOUT<0:3> is output from the tester **400** to a point of time when the write data DOUT<0:3> is input to the tester **400** via the first path circuit **210**, the first channel **102**, the memory chip **101**, the second channel **103**, and the second path circuit **220** may refer to the turnaround delay TAD.

[0037] The turnaround delay TAD may be divided into a delay time tTX according to the first path circuit **210**, a delay time tCH according to the first channel **102**, a delay time tCH according to the second channel **103**, a delay time tRX according to the second path circuit **220**, and a read latency RL, which is a delay time of from a point of time when the memory chip **101** recognizes a read command RD (RD not illustrated) from the write data DOUT<0:3> to a point of time when the memory chip **101** outputs actual data, according to a component.

[0038] Referring to FIG. **2**, the turnaround delay TAD according to an embodiment may be defined as TAD=tTX+2*tCH+RL+tRX.

[0039] The tester **400** according to an embodiment may autonomously detect the turnaround delay TAD, compensate the delay time of the read data DIN<0:3> using the detected turnaround delay value as the turnaround delay detection value, and determine a pass or fail of the memory chip **101** by comparing the delayed read data with the write data.

[0040] Referring to FIG. **3**, the tester **400** may include a delay compensator **500** and a determination circuit **600**.

[0041] The delay compensator **500** may generate delayed read data DIN_DLY by delaying read data DIN according to a difference between the external turnaround delay value TAD_EX and the turnaround delay detection value generated by detecting a time of from a point of time when write data DOUT including the read command RD is output to the memory chip **101** to a point of time when the read data DIN is input from the memory chip **101**.

[0042] The delay compensator **500** may generate the delayed read data DIN_DLY according to a calibration enable signal CAL_EN, the write data DOUT, the read data DIN, a clock signal CLK, and the external turnaround delay value TAD_EX.

[0043] The determination circuit **600** may generate a determination signal PASS which defines pass or fail of the memory chip **101** by comparing the delayed read data DIN_DLY with the write data DOUT.

[0044] Referring to FIG. **4**, the delay compensator **500** may include a delay circuit **501**, a multiplexer **502**, a register **503**, period signal generators **504** and **505**, and a controller **506**.

[0045] The delay circuit **501** may generate a plurality of delay signals **0**D to **3**D by delaying the read data DIN according to the clock signal CLK.

[0046] The read data DIN may be any one of DIN<0:3>.

[0047] The delay circuit **501** may include a plurality of flip flops DFF.

[0048] The plurality of flip flops DFF may generate the plurality of delay signals **0**D to **3**D by shifting the read data DIN or an output of a previous flip flop DFF according to the clock signal CLK.

[0049] The multiplexer **502** may select one among the plurality of delay signals **0**D to **3**D and output the selected delay signal as the delayed read data DIN_DLY according to a control signal CTRLD.

[0050] The register **503** may store the turnaround delay value provided from the outside of the test apparatus **100**, that is, the external turnaround delay value TAD_EX.

[0051] The period signal generators **504** and **505** may generate a first period signal START_CNT and a second period signal END_CNT according to the calibration enable signal CAL_EN, the write data DOUT, and the read data DIN.

[0052] The period signal generators **504** and **505** may include a first logic gate **504** and a second logic gate **505**.

[0053] The first logic gate **504** may output the first period signal START_CNT to a high level when the write data DOUT is transit to a high level in a state that the calibration enable signal CAL_EN has an activation level (that is, high level).

[0054] The second logic gate **505** may output the second period signal END_CNT to a high level when the read data DIN is transit to a high level in a state that the calibration enable signal CAL_EN has a high level.

[0055] The timing that an input terminal of the first logic gate **504** which receives the write data DOUT is transit to a high level may be an output timing of the write data DOUT.

[0056] The timing that an input terminal of the second logic gate **505** which receives the read data DIN is transit to a high level may be an input timing of the read data DIN.

[0057] The delay time of from a point of time when the first period signal START_CNT is transit to a high level to a point of time when the second period signal END_CNT is transit to a high level may refer to an actual turnaround delay TAD.

[0058] The controller **506** may detect the turnaround delay according to the first and second period signals START_CNT and END_CNT and the clock signal CLK, and generate the control signal CTRLD according to the difference between the external turnaround delay value TAD_EX and the detected turnaround delay value.

[0059] Referring to FIG. **5**, the controller **506** may include a latch **510**, a counter **520**, and an operator **530**.

[0060] The latch **510** may generate a counting enable signal CNT_EN according to the first and second period signals START_CNT and END_CNT.

[0061] The latch **510** may activate the counting enable signal CNT_EN according to activation of the first period signal START_CNT and inactivate the counting enable signal CNT_EN according to activation of the second period signal END_CNT.

[0062] The counter **520** may detect the turnaround delay by counting the clock signal CLK according to the counting enable signal CNT_EN.

[0063] The counter **520** may output a counting value of the clock signal CLK corresponding to an activation period of the counting enable signal CNT_EN as the turnaround delay detection value TAD_CAL.

[0064] The operator **530** may output an operation result value for a difference between the external turnaround delay value TAD_EX and the turnaround delay detection value TAD_CAL as the control signal CTRLD.

[0065] An operation of the test apparatus **100** having an above-described configuration according to an embodiment will be described.

[0066] Referring to FIG. **1**, the tester **400** may perform a write operation. That is, the tester **400** may perform data write on the memory chip **101** by outputting data having a predetermined pattern together with the write command.

[0067] Referring to FIG. **4**, after the write operation, the tester **400** may enter the turnaround delay compensation mode by activating the calibration enable signal CAL_EN to a high level.

[0068] The tester **400** may output the write data DOUT<0:3> including the read command RD to the memory chip **101** in the turnaround delay compensation mode.

[0069] As the write data DOUT<0:3> is output in a state that the calibration enable signal CAL_EN is a high level, that is, as a level of a predetermined bit among the bits constituting the write data DOUT<0:3> is transit to a high level, the first period signal START_CNT may be activated to a high level.

[0070] Referring to FIG. **5**, as the first period signal START_CNT is transit to a high level, the counting enable signal CNT_EN may be activated.

[0071] As the counting enable signal CNT_EN is activated, the counter **520** may start to count the clock signal CLK.

[0072] Referring to FIG. **1**, the memory chip **101** may output the read data DIN<0:3> by recognizing the read command RD included in the write data DOUT<0:3>.

[0073] Referring to FIG. **4**, as the read data DIN<0:3> is input to the tester **400**, that is, as a level of a predetermined bit among the bits constituting the read data DIN<0:3> is transit to a high level, the second period signal END_CNT may be activated to a high level.

[0074] Referring to FIG. **5**, as the second period signal END_CNT is transit to a high level, the counting enable signal CNT_EN may be inactivated.

[0075] The counter **520** may output a counting value of the clock signal CLK which is a value of from a point of time when the counting enable signal CNT_EN is activated to a point of time when the counting enable signal CNT_EN is inactivated as the turnaround delay detection value TAD_CAL.

[0076] The operator **530** may perform an operation on the difference between the external turnaround delay value TAD_EX and the turnaround delay detection value TAD_CAL and output an operation result value as the control signal CTRLD.

[0077] The delay compensation time of the read data DIN<0:3> may be determined according to the control signal CTRLD.

[0078] The tester **400** may enter the normal test mode by inactivating the calibration enable signal CAL_EN to a low level when a predetermined time elapsed after the second period signal END_CNT is activated.

[0079] When the read data DIN<0:3> according to the read command RD is input in the normal test mode, the delay compensator **500** may generate the delayed read data DIN_DLY by delaying the read data DIN<0:3> by a predetermined time through the delay circuit **501** and provide the delayed read data DIN_DLY to the determination circuit **600** according to the control signal CTRLD.

[0080] The determination circuit **600** may generate the pass signal PASS which defines pass or fail of the memory chip **101** by comparing the delayed read data DIN_DLY with the write data DOUT.

[0081] The above embodiments are illustrative and not limitative. Various alternatives and equivalents are possible. The disclosure is not limited by the embodiments described herein. Nor is the disclosure limited to any specific type of semiconductor device. Other additions, subtractions, or modifications are obvious in view of the present disclosure and are intended to fall within the scope of the appended claims.

What is claimed is:

1. A test apparatus comprising:

a delay compensator configured to generate delayed read data by delaying read data according to a difference between an external turnaround delay value provided

externally from the test apparatus and a turnaround delay detection value detected within the test apparatus; and

a determination circuit configured to perform a test result determination operation by comparing the delayed read data with reference data,

wherein the turnaround delay detection value is generated by detecting a time of from a point of time when write data including a read command as the reference data is output to a point of time when the read data is received.

2. The test apparatus of claim **1**, wherein the test apparatus is coupled to a first channel and a second channel,

the test apparatus further comprising:

a first path circuit configured to transmit the write data to the first channel; and

a second path circuit configured to transmit the read data transmitted through the second channel to the delay compensator.

3. The test apparatus of claim **2**, wherein the first path circuit includes:

a serializer configured to serialize the write data and output serialized write data; and

a transmitter configured to transmit an output of the serializer to the first channel.

4. The test apparatus of claim **2**, wherein the second path circuit includes:

a receiver configured to receive the read data; and

a parallelizer configured to parallelize an output of the receiver and transmit the parallelized output of the receiver to the delay compensator.

5. The test apparatus of claim **1**, wherein the delay compensator includes:

a delay circuit configured to generate a plurality of delay signals by delaying the read data;

a multiplexer configured to select one among the plurality of delay signals and output the selected delay signal as the delayed read data according to a control signal;

a period signal generator configured to generate a period signal according to a calibration enable signal, the write data, and the read data; and

a controller configured to generate the turnaround delay detection value according to the period signal and a clock signal and generate the control signal according to the external turnaround delay value and the turnaround delay detection value.

6. The test apparatus of claim **5**, wherein the period signal generator includes:

a first logic gate configured to generate a first period signal according to the calibration enable signal and the write data; and

a second logic gate configured to generate a second period signal according to the calibration enable signal and the read data.

7. The test apparatus of claim **5**, wherein the controller includes:

a latch configured to generate a counting enable signal according to the period signal;

a counter configured to output a counting value of the clock signal as the turnaround delay detection value according to the counting enable signal; and

an operator configured to output an operation result value for a difference between the external turnaround delay value and the turnaround delay detection value as the control signal.

8. The test apparatus of claim **5**, wherein the delay circuit includes a plurality of flip flops configured to shift the read data or an output of a previous flip flop according to the clock signal.

9. A test apparatus comprising:

a tester configured to set a delay compensation time of read data by detecting a turnaround delay of from a first point of time when write data including a read command is output in a turnaround delay compensation mode to a second point of time when the read data received exteriorly from the test apparatus is received, generate delayed read data by delaying the read data by the delay compensation time in a normal test mode, and perform a test result determination operation by comparing the delayed read data with the write data as reference data.

10. The test apparatus of claim **9**, wherein the tester enters the turnaround delay compensation mode by activating a calibration enable signal.

11. The test apparatus of claim **9**, wherein the tester enters the normal test mode by inactivating the calibration enable signal.

12. The test apparatus of claim **9**, wherein the tester includes:

a delay circuit configured to generate a plurality of delay signals by delaying the read data;

a multiplexer configured to select one of the plurality of delay signals and output the selected delay signal as the delayed read data according to a control signal;

a period signal generator configured to generate a period signal which defines a period of from the first point of time to the second point of time according to a calibration enable signal, the write data, and the read data; and

a controller configured to generate a turnaround delay detection value corresponding to the turnaround delay according to the period signal and a clock signal and generate the control signal according to an external turnaround delay value and the turnaround delay detection value.

13. The test apparatus of claim **12**, wherein the delay circuit includes a plurality of flip flops configured to shift the read data or an output of a previous flip flop according to the clock signal.

14. The test apparatus of claim **12**, wherein the period signal generator includes:

a first logic gate configured to generate a first period signal activated at the first point of time according to the calibration enable signal and the write data; and

a second logic gate configured to generate a second period signal activated at the second point of time according to the calibration enable signal and the read data.

15. The test apparatus of claim **12**, wherein the controller includes:

a latch configured to generate a counting enable signal according to the period signal;

a counter configured to output a counting value of the clock signal as the turnaround delay detection value according to the counting enable signal; and

an operator configured to output an operation result value for a difference between the external turnaround delay value and the turnaround delay detection value as the control signal.

16. The test apparatus of claim **9**, wherein the test apparatus is coupled to a first channel and a second channel, the test apparatus further comprising:

a first path circuit configured to transmit the write data to the first channel; and

a second path circuit configured to transmit the read data transmitted through the second channel to the tester.

17. The test apparatus of claim **16**, wherein the first path circuit includes:

a serializer configured to serialize the write data and output serialized write data; and

a transmitter configured to transmit an output of the serializer to the first channel.

18. The test apparatus of claim **16**, wherein the second path circuit includes:

a receiver configured to receive the read data; and

a parallelizer configured to parallelize an output of the receiver and transmit the parallelized output of the receiver to the tester.

19. A test apparatus for a semiconductor chip, the test apparatus comprising:

a delay compensator configured to generate delayed read data by delaying read data according to a difference between an external turnaround delay value provided externally from the test apparatus and a turnaround delay detection value detected within the test apparatus; and

a determination circuit configured to perform a test result determination operation by comparing the delayed read data with reference data,

wherein the turnaround delay detection value is generated by detecting a time of from a point of time when write data including a read command as the reference data is output to the semiconductor chip to a point of time when the read data is input from the semiconductor chip.

* * * * *