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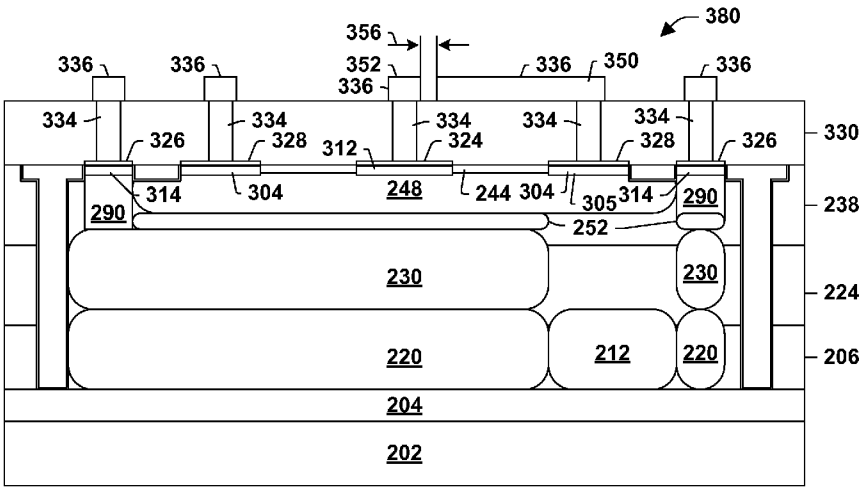
— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

[Continued on next page]

(54) **Title:** OPEN SOURCE/DRAIN JUNCTION FIELD EFFECT TRANSISTOR



(57) **Abstract:** An n channel junction field effect transistor (NJFET) and/or a p channel junction field effect transistor (PJFET) (370) are formed with an open drain, where the open drain allows the transistors to operate at higher voltages before experiencing gate leakage current. The open drain allows the voltage to be increased several fold without increasing the size of the transistors. Opening the drain essentially spreads equipotential lines of respective electric fields developed at the drains of the devices so that the local electric fields, and hence the impact ionization rates are reduced to redirect current below the surface of the transistors.

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OPEN SOURCE/DRAIN JUNCTION FIELD EFFECT TRANSISTOR

The invention relates generally to semiconductor processing, and more particularly to fashioning a junction field effect transistor (JFET) where a drain (and source for bi-directional operation) of the JFET is "opened" to direct current away from the surface of the transistor.

BACKGROUND

It can be appreciated that different electronic devices may have different requirements depending upon a particular device's application. For example, operational amplifiers used in precision analog applications have to be able to operate at relatively high voltages while experiencing little to no leakage due to the high voltages and correspondingly high drive currents. It is also desirable for such devices to experience very little low frequency noise and to be very stable such that offset voltages shift very little.

One basic building block of semiconductor circuitry and electronic devices, such as operational amplifiers, is a junction field effect transistor (JFET). It can thus be appreciated that it would be desirable to fashion a JFET that could be operated at high voltages and drive currents while experiencing little to no leakage, and that also experiences very little low frequency noise and has very stable offset voltages so that the device would be suitable for use in precision analog applications, for example.

SUMMARY

The disclosure herein pertains to fashioning an n channel junction field effect transistor (NJFET) and/or a p channel junction field effect transistor (PJFET) with an open drain, where the open drain allows the transistors to operate at higher voltages before experiencing gate leakage current. The open drain allows the voltage to be increased several fold without increasing the size of the transistors. Opening the drain essentially spreads equipotential lines of respective electric fields developed at the drains of the devices so that the local electric fields, and hence the impact ionization rates are reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A and 1B illustrate a flow diagram of an example methodology for fashioning a junction field effect transistor (JFET) as described herein.

FIGS. 2-37 are cross-sectional illustrations of a semiconductor substrate wherein an example JFET is fashioned as described herein.

FIG. 38 is a simulation developed representation of a conventional JFET wherein equipotential lines of an electric field developed at the drain of the device are illustrated as well as current flow within the device.

FIG. 39 is a simulation developed representation of an open drain JFET wherein equipotential lines of an electric field developed at the drain of the device are illustrated as well as current flow within the device.

FIG. 40 is a simulation developed representation of a conventional JFET similar to that of FIG. 38, but illustrating a zoomed in view of the drain.

FIG. 41 is a simulation developed representation of an open drain JFET similar to that of FIG. 39, but illustrating a zoomed in view of the drain.

FIG. 42 is a graph illustrating gate current developed at different voltages for different NJFET configurations.

FIG. 43 is a graph illustrating gate current developed at different voltages for NJFETs having different size open drains.

FIG. 44 is a cross sectional illustration of an example PJFET wherein the source is "opened" instead of the drain.

FIG. 45 is a cross sectional illustration of an example NJFET wherein the source is "opened" instead of the drain.

FIG. 46 is a cross sectional illustration of an example PJFET comprising a single epitaxial layer and a single p buried layer.

FIG. 47 is a cross sectional illustration of an example NJFET comprising a single epitaxial layer and a single p buried layer.

FIG. 48 is a graph illustrating noise reduction in a JFET when a silicide block is used in forming gate, source and drain regions.

FIGS. 49 and 50 graphically illustrate improvements in device stability when a surface shield is implemented in a JFET.

DETAILED DESCRIPTION OF THE EMBODIMENTS

An example methodology 100 for fashioning a junction field effect transistor (JFET) is illustrated in FIGS. 1A and 1B, and FIGS. 2-37 are cross sectional views of a semiconductor substrate 200 wherein such a method is implemented. As will be appreciated that the method 100 has application to both an n channel JFET or NJFET and a p channel

JFET or PJFET, where the electrical conductivity types are generally just reversed in NJFET and PJFET transistors. Additionally, while the method 100 is illustrated and described below as a series of acts or events, it will be appreciated that the invention is not limited by the illustrated ordering of such acts or events. For example, some acts may occur in different orders and/or concurrently with other acts or events apart from those illustrated and/or described herein. In addition, not all illustrated steps may be required to implement a methodology in accordance with one or more aspects or embodiments of the invention. Further, one or more of the acts depicted herein may be carried out in one or more separate acts and/or phases.

At the outset, a first resist 208 is formed and patterned over the substrate 200 or workpiece and a first implantation 210 of one or more n type dopants is performed at 102 to form a first n type buried layer (NBL1) 212 in a (lightly doped n or p type) top silicon portion 206 of workpiece 200 above a buried oxide (BOX) portion 204 of the workpiece (FIG. 2). As will be appreciated, the leftmost NBL1 212 region in the illustrated example will reside under the subsequently formed "open" drain of an n type junction field effect transistor (NJFET).

It will be appreciated that while the illustrated substrate 200 comprises a support portion 202, the BOX 204 and the top 206, that substrate as referred to herein may comprise any type of semiconductor body (e.g., silicon, SiGe) such as a semiconductor wafer or one or more die on a wafer, as well as any other type of semiconductor and/or epitaxial layers grown thereon and/or otherwise associated therewith. It will also be appreciated that the patterning of the first resist 208 (as with all masking and/or patterning mentioned herein) can be performed in any suitable manner, such as with lithographic techniques, for example, where lithography broadly refers to processes for transferring one or more patterns between various media. Additionally, while many implantations are described herein to dope or add dopant atoms and/or other agents/impurities to treated regions, it will be appreciated that regions can be doped by different techniques, such at diffusion, for example, and that such other doping operations are not intended to be excluded merely because "implantations" are referred to herein.

The first resist 208 is then stripped and a second resist 216 is formed and patterned over the substrate 200 or workpiece and a second implantation 218 of one or more p type

dopants is performed at 104 to form a first p type buried layer (PBL1) 220 in the top silicon portion 206 of workpiece 200 (FIG. 3). As will be appreciated the rightmost PBL1 220 in the illustrated example, will reside under the subsequently formed "open" drain of a p type junction field effect transistor (PJFET). The second resist 216 is then stripped and a first layer of n type material is epitaxially grown (NEPI1) 224 over the top silicon portion 206 of the workpiece 200 at 106 (FIG. 4). It will be appreciated that the NBL1 212 and the PBL1 220 migrate up a little into NEPI 1 224 as a result of the growth process, such as from increased temperatures, for example.

At 108, a third resist 226 is formed and patterned over the NEPI1 layer 224 and a third implantation 228 of one or more p type dopants is performed to form a second p type buried layer (PBL2) 230 (FIG. 5). The PBL2 230 is formed substantially in the NEPI1 layer 224 and over the PBL1 220. While the PBL1 220 and the PBL2 230 may merge slightly (e.g., at their interface), the PBL2 230 is generally formed such that it has a concentration of p type dopants that is typically less than the concentration of p type dopants in the PBL1 220. As with all dopant concentrations recited herein, the concentration of dopants in the PBL2 230 is nevertheless consistent with the high-voltage and/or breakdown voltage requirements of the structure(s). Additionally, the PBL2 230 may be formed by multiple (e.g., four) implants carried out at various energies and/or doses.

The third resist 226 is then stripped and a fourth resist 232 is formed and patterned over the NEPI1 layer 224 and a fourth implantation 234 of one or more n type dopants is performed at 110 to form one or more DEEPNX 236 regions in the NEPI1 layer 224 over the NBL1 212 (FIG. 6). As will be appreciated, these doped regions 236 comprise an abundance of n type dopant carriers, and thus serve to reduce a down contact resistance. Like the PBL2 230, these regions 236 may be formed by multiple (e.g., four) implants carried out at various energies and/or doses. Additionally, these implants are merely performed on the right half of the substrate in the illustrated example, which corresponds to the PJFET.

The fourth resist 232 is stripped and a second layer of n type material is epitaxially grown (NEPI2) 238 over the NEPI1 224 at 112 (FIG. 7). The NEPI2 layer 238 is formed such that it has a concentration of n type dopants that is substantially the same as the concentration of n type dopants in the NEPI1 layer 224. Similar to when the NEPI1 224 layer

is formed, the PBL2 230 and DEEPNX 236 regions migrate up a little when the NEPI2 238 is formed.

At 114, a fifth resist 240 is formed and patterned over the NEPI2 layer 238 and a fifth implantation 242 of one or more p type dopants is performed to form a p type surface shield or thin skin 244 across the surface of the NEPI2 layer 238 and over most of the PBL2 230 on the left half, or NJFET portion, of the substrate 200 in the illustrated example (FIG. 8). The surface shield 244 is formed to have a concentration of p type dopants that is typically less than the concentration of dopants in subsequently formed source and drain regions. Additionally, the shield 244 is formed so that it is shallower than the subsequently formed source and drain regions. More generally, the shield 244 is formed to a concentration and depth that facilitates adequate shielding while keeping impact ionization current below a specified maximum level.

At 116, a sixth implantation 246 of one or more n type dopants is performed to form an n type channel 248 in the NEPI2 layer 238 substantially under the p skin 244 (FIG. 9). Accordingly, like the p skin 244, the n channel 248 is formed primarily over the PBL2 230 on the left half, or NJFET portion, of the substrate 200 in the illustrated example. The channel 248 is formed to have a concentration of n type dopants that is typically greater than the concentration of n type dopants in the first NEPI1 layer 224. The impurity profile of the channel 248 is tailored to facilitate current drive and transconductance while maintaining impact ionization current below a specified maximum level. The channel 248 may, for example, be established by three n type implants, where each subsequent implant is performed at a decreased energy level than the previous implant, but where the dose remains substantially the same in each of the implants. Such a triple channel implant facilitates desired drive current, impact ionization current, and also improves the transconductance (gm) of the transistor. Alternatively, the channel may be formed by a single implant, a single implant with subsequent thermal treatment, and/or by multiple implants with increasing (rather than decreasing) energy levels, with or without thermal treatments, for example. It will be appreciated that the same mask 240 can be used to form the p type skin 244 and the n type channel 248, where the mask keeps dopants out of other devices (not shown) formed on the same workpiece. Utilizing the same mask streamlines the fabrication process and reduces costs – which is an ongoing desire in the semiconductor industry.

At 118, the fifth resist 240 is stripped and a sixth resist 249 is formed and patterned over the NEPI2 layer 238 and a seventh implantation 250 of one or more p type dopants is performed to form a p type back gate (BG) extension 252 substantially in a lower portion of the NEPI2 layer 238 and below the n channel 248 (FIG. 10). Although the extension region 252 may merge slightly with the underlying PBL2 230 (e.g., at their interface), the BG 252 is generally formed to have a concentration of p type dopants that is typically less than the concentration of p type dopants in the PBL2 230. Additionally, the sixth resist 249 is patterned such that the BG extension region 252 is blocked from entering a region located under the (subsequently formed) drain. Stated another way, the extension region 252 is formed to be discontinuous so as to comprise a gap 253, which facilitates the open drain in the NJFET, as will be appreciated.

The sixth resist 249 is then stripped and a seventh resist 254 is formed and patterned over the NEPI2 layer 238 and an eighth implantation 256 of one or more n type dopants is performed at 120 to form an n type surface shield or thin skin 258 across the surface of the NEPI2 layer 238 substantially between the DEEPNX regions 236 (FIG. 11). Like shield 244, the surface shield 258 is formed to have a concentration of n type dopants that is typically less than the concentration of dopants in subsequently formed source and drain regions. Additionally, the shield 258 is formed so that it is shallower than the subsequently formed source and drain regions. More generally, the shield 258 is formed to a concentration and depth that facilitates adequate shielding while keeping impact ionization current below a specified maximum level.

At 122, a ninth implantation 260 of one or more p type dopants is performed to form a p type channel 262 in the NEPI2 layer 238 substantially under the n skin 258 (FIG. 12). The channel 262 is formed to have a concentration of p type dopants that is typically less than the concentration of n type dopants in the NBL 212. The impurity profile of the channel 262 is tailored to facilitate current drive and transconductance while maintaining impact ionization current below a specified maximum level. Like channel 248, channel 262 may, for example, be established by three p type implants, where each subsequent implant is performed at a decreased energy level than the previous implant, but where the dose remains substantially the same in each of the implants. Such a triple channel implant facilitates desired drive current, impact ionization current, and also improves the transconductance (gm)

of the transistor. Alternatively, the channel may be formed by a single implant, a single implant with subsequent thermal treatment, and/or by multiple implants with increasing (rather than decreasing) energy levels, with or without thermal treatments, for example. Like mask 240, mask 254 can be used to form the n type skin 258 and the p type channel 262, where the mask keeps dopants out of other devices (not shown) formed on the same workpiece. Utilizing the same mask streamlines the fabrication process and reduces costs – which is an ongoing desire in the semiconductor industry.

At 124, the seventh resist 254 is stripped and an eighth resist 263 is optionally formed and patterned over the NEPI2 layer 238 and an optional tenth implantation 264 of one or more n type dopants is performed to form an n type back gate (BG) extension 266 substantially in a lower portion of the NEPI2 layer 238 and below the p channel 262 (FIG. 13). It will be appreciated that this implantation is optional since the NEPI2 layer 238 already possesses an n type doping. Similar to sixth resist 249, eighth resist 263 is patterned such that the BG extension region 266 is blocked from entering a region located under the (subsequently formed) drain. Stated another way, the extension region 266 is formed to be discontinuous so as to comprise a gap 267, which facilitates the open drain in the PJFET, as will be appreciated.

At 126, the eighth patterned resist 263 (or seventh 254 if the eighth 263 was not implemented) is stripped and shallow isolation areas 270 are formed in the workpiece 200. Turning to FIGS. 14 and 15, where FIG. 14 is a zoomed in view of the PJFET and FIG. 15 is a zoomed in view of the NJFET illustrated in the preceding FIGS., the shallow isolation areas 270 are formed in an upper part of the NEPI2 layer 238. The shallow isolation areas 270 can, for example, be formed with a mask (not shown) that facilitates etching trenches or apertures into the NEPI2 layer 238, where the trenches are then filled with a dielectric material. Additionally, a thin liner oxide 272 can be grown in the shallow trenches before the trenches are filled with the dielectric material. It will be appreciated that the shallow isolation areas 270 generally mitigate vertical and lateral parasitic capacitances and laterally isolate junctions from one another.

Turning to FIGS. 16 and 17, deep isolation areas 274 are then formed in the workpiece 200 at 128, where FIG. 16 illustrates a zoomed in view of the PJFET and FIG. 17 illustrates a zoomed in view of the NJFET. Similar to the shallow isolation areas 270, the

deep isolation areas 274 can, for example, be formed with a mask (not shown) that facilitates etching trenches or apertures down to the BOX 204, where the trenches are then filled with a dielectric material (e.g., sub-atmospheric chemical vapor deposition (SACVD) TEOS oxide). Further, a deep liner oxide 276 can be grown in the deep trenches before the dielectric filler is added. Although not illustrated, it will be appreciated that the liner oxide 276 may exist predominately on the sidewalls of the deep isolation areas 274 as little to no oxide forms on the BOX 204. It will be appreciated that the deep isolation areas 274 isolate the respective transistors from surrounding devices, such as other transistors, for example. It will also be appreciated that the deep isolation areas 274 can be formed before the shallow isolation areas 270 are formed.

After the shallow 270 and deep 274 isolation areas are formed, a ninth resist 280 is formed and patterned over the NEPI2 layer 238 and an eleventh implantation 282 of one or more n type dopants is performed to form n type deep back gate (BG) contact regions 284 in the PJFET at 130 (FIG. 18). It will be appreciated that these contact regions 284 may be formed with multiple implants (e.g., four) carried out at various energies and/or doses to reduce down contact resistance. The implantation 282 is nevertheless performed so that there is a continuous low resistance vertical n type pathway. The dopant profiles are thus chosen to reduce vertical resistance while meeting specifications on impact-ionization current. Note that resist 280 covers all of the NJFET during implantation 282 so that the n type dopants from implantation 282 do not affect the NJFET (FIG. 19).

At 132, the ninth resist 280 is stripped and a tenth resist 286 is formed and patterned over the NEPI2 layer 238 and a twelfth implantation 288 of one or more p type dopants is performed to form a deep p type region 289 in the PJFET (FIG. 20) and p type deep back gate (BG) contact regions 290 in the NJFET (FIG. 21). As with regions 284, regions 289 and 290 may be formed with multiple implants (e.g., four) carried out at various energies and/or doses to reduce down contact resistance.

The tenth patterned resist 286 is stripped and a silicide block layer 292 is formed and patterned (e.g., with a mask – not shown) over the NEPI2 layer 238 at 134 (FIGS. 22 and 23). The silicide block 292 generally comprises insulating material, such as oxide and/or nitride, for example. It will be appreciated that the silicide block (SBLK) 292 serves to isolate conductive areas, such as subsequently formed gate, source and drain regions, for

example, from one another. The SBLK 292 can be implemented instead of other isolation techniques without increasing the dimensions of the transistor so that valuable semiconductor real estate is conserved.

An eleventh resist 296 is formed and patterned over the NEPI2 layer 238 and a thirteenth implantation 298 of one or more n type dopants is performed at 136 to form n type gate 300 and n type top back gate (BG) contact 302 regions in the PJFET (FIG. 24) and to form n type source and drain regions 304 in the NJFET (FIG. 25). It will be appreciated that the SBLK 292 is sufficiently thick so as to block implantation/penetration of the n type dopants into underlying areas. Similarly, the dielectric material of the shallow 270 and deep 274 isolation areas is sufficiently thick to halt dopants from penetrating into underlying areas given the implantation energies.

The eleventh resist 296 is stripped and a twelfth resist 306 is formed and patterned over the NEPI2 layer 238 and a fourteenth implantation 308 of one or more p type dopants is performed at 138 to form p type source and drain regions 310 regions in the PJFET (FIG. 26) and to form p type gate 312 and p type top back gate (BG) contact 314 regions in the NJFET (FIG. 27). Again, the SBLK 292 and the dielectric material of the shallow 270 and deep 274 isolation areas blocks implantation/penetration of the dopants into underlying areas. It can thus be appreciated that the SBLK 292 serves to self align the source, drain and gate regions within the NEPI2 layer 238.

The twelfth resist 306 is stripped and a layer of refractory metal 316 (e.g., cobalt based material) is formed (e.g., deposited) over the entire surface at 140 (Figs 28 and 29). The layer of refractory metal 316 is then processed (e.g., heated) at 142 so that it reacts with the silicon that it is in contact with to form silicides. In particular, silicides 318, 320 and 322 are formed over the gate 300, back gate 302 and source and drain 310 regions, respectively, of the PJFET (FIG. 30), while silicides 324, 326 and 328 are formed over the gate 312, back gate 314 and source and drain 304 regions, respectively, of the NJFET (FIG. 31). Excess un-reacted refractory metal is then removed (not shown).

At 144, a layer of dielectric material (e.g., Inter-Level Dielectric (ILD), Boro-Phospho-Silicate Glass (BPSG)) 330 is formed over the NEPI2 layer 238 and the silicides (FIGS. 32 and 33). The ILD 330 is patterned (e.g., with a mask – not shown) down to the silicides, where the apertures in the patterned ILD 330 are then filled with a conductive

material to form contacts 332 down to the silicides 318, 320, 322 in the PJFET (FIG. 32) and to form contacts 334 down to the silicides 324, 326, 328 in the NJFET (FIG. 33), and the contacts and ILD 330 are planarized to be uniform and smooth.

A layer of first metal (e.g., metal-1) conductive material (e.g., aluminum, copper) 336 is formed (e.g., deposited) and patterned (e.g., with a mask – not shown) over the ILD 330 and contacts 332, 334 at 146. In particular, the metal 336 is patterned to so that some of it remains over the respective contacts 332, 334 in the PJFET and NJFET (FIGS. 34-37). In one example, the metal 336 is patterned so that a portion 340 of it remains over the respective gates 300, 312 of the PJFET and NJFET and extends so as to overlap at least some of the source and drain regions 310, 304 of the PJFET and NJFET (FIGS. 34 and 35). Portion 340 nevertheless is distanced from the portions 342, 344 of metal 336 by a distance 346 that is on the order of about a fraction of a micrometer. In another example, a portion 350 of the metal 336 that extends over the drain regions 310, 304 of the PJFET and NJFET also overlaps at least some of the gates 300, 312 of the PJFET and NJFET (FIGS. 36 and 37). Portion 350 nevertheless is distanced from portion 352 by a distance 356 that is on the order of about a fraction of a micrometer. It will be appreciated that these distances 346 and 356 are merely example, though, since the minimum metal to metal spacing is dependent on applicable design rules. Additionally, portions 340, 350 may be referred to as field plates, and such field plates mitigate drift in electrical parameters that can be caused by field induced migration of charge and/or impurities in the semiconductor surface, for example. The field plates may, for example, be tied to the potential applied to the gates 300, 312 to mitigate depletion of the respective surface shields 258, 244 of the PJFET and the NJFET, for example. After the field plates are formed, the method 100 advances to 148 where further back end processing is performed, such as forming one or more conductive or insulative layers (not illustrated) over the NJFET and/or PJFET, for example.

As will be appreciated the NJFET 370 can be said to have an "open" drain since the PBL2 230 and the BG extension 252 do not extend under the drain 305 (FIGS. 35, 37). More particularly, n type material exits from the drain 305 down to the NBL 212, with the drain 305 and the NBL 212 having a higher concentration of n type dopant atoms than the intervening channel 248 and the NEPI1 224. Similarly, the PJFET 370 can also be said to have an open drain since the NBL1 212 does not extend under the drain 307 (FIGS. 34, 36).

In the illustrated example, a continuous p type pathway in the PJFET 370 comprises the drain 307, deep p type region 289, PBL2 230 and the PBL1 220.

Turning to FIGS. 38-41, the effect of the open drain can be appreciated. FIGS. 38 and 40 illustrate a conventional NJFET with an un-opened drain, where FIG. 40 is a zoomed in view of the drain illustrated in FIG. 38. By contrast, FIGS. 39 and 41 illustrate an NJFET with the drain opened as described herein, where FIG. 41 is a magnified view of the drain illustrated in FIG. 39. It can be seen that equipotential lines 406 are more concentrated in FIGS. 38 and 40 (where the drain is not open) than in FIGS. 39 and 41 (where the drain is open). The equipotential lines 406 are indicative of an electric field developed around the drain, where the electric field is a function of voltage applied to the gate, drain and source (or rather just to the drain where zero volts are applied to the gate and source) and the distance between the source and drain. It can thus be seen that the field is stronger where the drain is not open (FIGS. 38, 40). A strong electric field accelerates electrons to a high velocity and instills substantial kinetic energy in them. Electrons with sufficient kinetic energy may collide with the lattice structure of the substrate, and ionize the lattice site creating an electron hole pair. Some of the holes can get swept back into the channel and out of the gate terminal as gate current, which is highly undesirable. Excess gate current can begin to materialize in this manner when the drain voltage is around 3 or 4 volts, for example.

Opening the drain as described herein thus helps to mitigate gate leakage current by reducing the magnitude of an electric field generated at the drain, which in turn mitigates the generation of electron-hole pairs by impact ionization. It will be appreciated that opening the drain as described herein allows the operating voltage of the transistor to be increased several fold before appreciable gate leakage current occurs. Turning to FIG. 42, for example, a graph 500 illustrates gate leakage current versus applied voltage. The right hand y axis in the graph 500 corresponds to gate current in amps. per. micron, while the x axis corresponds to voltage applied to the drain (Vd). The three solid curves 502, 504, 506 (as opposed to those drawn with repeated squares) illustrate when gate current develops for differently configured transistors. Curve 502 corresponds to an NJFET without an open drain and with a surface shield. In this transistor gate leakage current occurs when the drain voltage is about 7 volts. Curve 504 corresponds to an NJFET without an open drain and also without a surface shield. Gate leakage current appears when about 13 volts are applied to the drain of this device. It

will be appreciated that while a surface shield mitigates low frequency noise, it also increases leakage current (curve 502) because it comprises dopant atoms that cause the equipotential lines to be closer together. The resulting higher electric field thus accelerates electrons and produces ionized electron hole pairs that lead to increase gate leakage current. Finally, curve 506 corresponds to an open drain NJFET with a surface shield as described herein. It can be seen that appreciable gate leakage current doesn't appear in this device until Vd is about 20 volts.

Accordingly, opening the drain as described herein makes the NJFET more tolerant, and thus suitable for higher voltage applications, by increasing the voltage that can be applied to the drain before appreciable leakage current appears at the gate. Moreover, this is accomplished without increasing the dimensions of the transistor so that valuable semiconductor real estate is conserved. Nevertheless, opening the drain further can increase the voltage that can be applied to the drain before gate leakage occurs. By way of example, FIG. 43 illustrates a graph 600 wherein curve 506 from FIG. 42 is compared to a curve 602 for an NJFET where the drain is open about twice as much as the drain for curve 506 (and where the NJFET similarly has a surface shield). For example, if the drain for curve 506 is said to be opened to about 2.5 microns, then the drain in the NJFET giving rise to curve 602 can be said to be opened to about 5.0 microns. In this manner, the drain voltage can be increased from about 20 volts to about 30 volts before gate leakage occurs.

It will be appreciated that while opening the drain has been described herein, the source could be opened as well (or opened instead of the drain) to allow operating voltages to be increased before appreciable gate leakage current occurs. FIG. 44, for example, is a mirror image of FIG. 36 and thus illustrates a PJFET where the source 309 is open rather than the drain 307. Similarly, FIG. 45 is a mirror image of FIG. 37 and thus illustrates an NJFET where the source 311 is open rather than the drain 305.

Additionally, while first and second epitaxial layers NEPI1 224 and NEPI2 238 are disclosed herein, as well as first and second p buried layers PBL1 220 and PBL2 230, an NJFET and/or a PJFET having an open drain and/or an open source can be formed with a single epitaxial layer and/or a single p buried layer. Turning to FIGS. 46 and 47, for example, an example open source PJFET and NJFET are respectively illustrated where the transistors are formed with merely a single epitaxial layer NEPI 1 224 and a single p buried layer PBL1

220. The devices would be fashioned as described herein except that the second epitaxial layer NEPI2 238 would not be grown, the second p buried layer PBL2 230 would not be formed and the features previously formed in the second epitaxial layer NEP2 238 would instead be formed in the first epitaxial layer NEPI1 224.

As alluded to above, it will be appreciated that the silicide block 292, surface shields 244, 258 and the field plates 340, 350 implemented herein substantially reduce noise while increasing device stability. Turning to FIG. 48, for example, a graph 2000 illustrates how noise is improved (or rather reduced) by an order of magnitude through fabrication as described herein. In the graph 2000, frequency, as measured in Hertz (Hz), is plotted logarithmically on the x axis, while a noise metric known as noise density (Sld) is plotted on the y axis, where the Sld is measured in amps squared per Hz. A first curve 2002 corresponds to noise in a JFET where STI is used to separate the gate, source and drain regions, while a second curve 2004 depicts noise in a JFET where SBLK is used to separate the gate, source and drain regions, and a third curve 2006 corresponds to noise in a JFET where SBLK and a surface shield are implemented in the JFET. With the silicide block alone, at around 100 Hz, it can be seen that noise is reduced to around 1E-23 down from around 1E-22 when STI is used. The noise is further reduced to around 1E-24 at around 100 Hz when the surface shield is implemented along with the SBLK. It will be appreciated that the noise (SId) begins to decrease abruptly as the frequency goes above 10000 Hz. This is due to limited high frequency response of the device(s) used to generate data for FIG. 20. Additionally, although not as dramatic, it will be appreciated that implementing field plates as described herein further reduces noise in the JFET by mitigating charge trapping that can occur in and around non uniform regions of the device.

FIGS. 49 and 50 illustrate improvement in device stability when a surface shield is implemented in a JFET. In FIG. 49, for example, a graph 2100 includes multiple instances or samples of input offset voltages plotted over time. It will be appreciated that input offset voltage is a metric that is indicative of device stability, where less change in input offset voltage implies a more stable device. Accordingly, the group 2102 of plots toward the bottom of the graph 2100 corresponds to more stable devices, while the other group 2104 of plots corresponds to less stable devices. It will be appreciated that the plots in the lower group

2102 were derived from devices that included a surface shield, while the other plots 2104 were generated from devices that did not include a surface shield.

To generate the plots illustrated in FIG. 49, two like JFETS (e.g., two NJFETS or two PJFETS with a surface shield or two NJFETS or two PJFETS without a surface shield) were coupled together in a differential amplifier input configuration, where the respective sources of the devices were tied together and a differential voltage was applied across the gates of the devices to stress the devices. The devices were stressed for just under an hour (x axis) and the change in input offset voltage (dVos) was plotted on the y axis (in millivolts (mV)), where input offset voltage is the difference in the respective gate voltages of the JFETS being stressed/tested.

FIG. 50 is a graph 2200 that illustrates the change in input offset voltage (dVos) (y axis) for the respective samples/curves (x axis) from FIG. 49, where the end point of each plot in FIG. 49 is plotted as a single point in FIG. 50. It can be seen that nine samples were obtained from JFETS having surface shields and that six samples were obtained from JFETS not having surface shields. The samples derived from JFETS having surface shields are substantially more stable than those generated from JFETS that do not have surface shields since they experience a much lower change in input offset voltage. Generally speaking, the JFETS that have surface shields are approximately ten times more stable than the JFETS that lack surface shields. Accordingly, fashioning a JFET as described herein allows the device to be substantially more stable and produce substantially less noise while not requiring the size of the device to be increased.

It will be appreciated that while reference is made throughout this document to example structures in discussing aspects of one or more methodologies described herein (e.g., those structures presented in FIGS. 2-37 while discussing the methodology set forth in FIG. 1), that those methodologies are not to be limited by the corresponding structures presented. Rather, the methodologies (and structures) are to be considered independent of one another and able to stand alone and be practiced without regard to any of the particular aspects depicted in the FIGS. Additionally, the structures and/or layers described herein can be formed in any number of suitable ways, such as with spin-on techniques, sputtering techniques (e.g., magnetron or ion beam sputtering), (thermal) growth techniques and/or deposition techniques such as chemical vapor deposition (CVD), for example.

Those skilled in the art to which the invention relates will appreciate that the foregoing are just some examples of the many ways to implement the invention within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. A method of forming a p type junction field effect transistor (PJFET) and an n type junction field effect transistor (NJFET) in a semiconductor substrate, comprising:

forming a first n type buried layer (NBL1) in the substrate;

forming a first p type buried layer (PBL1) in the substrate,;

forming a first n type epitaxial layer (NEPI1) over the substrate;

forming a second p type buried layer (PBL2) over the PBL1 in the NEPI1;

forming one or more DEEPNX regions over at least some of the NBL1 in the NEPI1;

forming a second n type epitaxial layer (NEPI2) over the NEPI1;

forming a p type surface shield near an upper surface of the NEPI2, where the p type surface shield resides over at least some of the PBL2;

forming an n type channel in the NEPI2, where the n type channel resides over at least some of the PBL2;

forming a p type back gate (BG) extension near a lower surface of the NEPI2, where the p type BG extension resides over at least some of the PBL2 and over less than all of the NBL1;

forming an n type surface shield near an upper surface of the NEPI2, where the n type surface shield resides over at least some of the NBL1;

forming a p type channel in the NEPI2, where the p type channel resides over at least some of the NBL1;

forming one or more isolation areas that isolate the PNFET from the NJFET;

forming one or more n type deep back gate contact regions in the NEPI2 down to the DEEPNX regions in the PJFET;

forming one or more p type deep back gate contact regions in the NEPI2 down to the PBL2 in the NJFET;

forming a deep p type region in the NEPI2 down to the PBL2 in the PJFET:

forming a layer of silicide block material (SBLK) over the NEPI2;

patterning the SBLK to expose areas of the NEPI2 where gate, source and drain regions are to be formed;

forming an n type gate region in the p type channel of the PJFET, and n type source and drain regions in the n type channel of the NJFET;

forming p type source and drain regions in the p type channel of the PJFET, and a p type gate region in the n type channel of the NJFET;

siliciding the gate, source and drain regions in the p type channel of the PJFET and the n type channel of the NJFET;

forming a layer of dielectric material over the silicides and NEPI2;

forming conductive contacts down through the layer of dielectric material to the silicided gate, source and drain regions in the p type channel of the PJFET and the n type channel of the NJFET; and

forming a field plate over at least one of the conductive contacts extending down to the gate regions of the PJFET and the NJFET, where the field plates also extend over at least some of at least one of the source and drain regions of the PJFET and the source and drain regions of the NJFET.

2. The method of Claim 1, further comprising:

forming an n type back gate (BG) extension near a lower surface of the NEPI2, where the n type BG extension resides over at least some of the NBL1 and over less than all of the PBL1.

3. The method of Claim 1, where the field plate is formed over at least one of the conductive contacts extending down to the drain regions of the PJFET and the NJFET, where the field plates also extend over at least some of the gate region of the PJFET and the gate region in the NJFET.

4. The method of Claim 2, where the field plate is formed over at least one of the conductive contacts extending down to the drain regions of the PJFET and the NJFET, where the field plates also extend over at least some of the gate region of the PJFET and the gate region in the NJFET.

5. The method of Claim 1, where the drain of the NJFET is formed over at least some of the NBL1.

6. A method of forming a p type junction field effect transistor (PJFET) in a semiconductor substrate, comprising:

forming a first n type buried layer (NBL1) in the substrate;

forming a first p type buried layer (PBL1) in the substrate between NBL1 regions;

forming a first n type epitaxial layer (NEPI1) over the substrate;

forming a second p type buried layer (PBL2) in the NEPI1 over at least some of the PBL1;

forming one or more DEEPNX regions over the NBL1 in the NEPI1;

forming a second n type epitaxial layer (NEPI2) over the NEPI1;

forming an n type surface shield near an upper surface of the NEPI2, where the n type surface shield resides over at least some of the NBL1;

forming a p type channel in the NEPI2, where the p type channel resides over at least some of the NBL1;

forming one or more n type deep back gate contact regions in the NEPI2 down to the DEEPNX regions;

forming a deep p type region in the NEPI2 down to the PBL2;

forming a layer of silicide block material (SBLK) over the NEPI2;

patterning the SBLK to expose areas of the NEPI2 where gate, source and drain regions are to be formed;

forming an n type gate region in the p type channel of the PJFET;

forming p type source and drain regions in the p type channel of the PJFET;

siliciding the gate, source and drain regions in the p type channel of the PJFET;

forming a layer of dielectric material over the silicides and NEPI2;

forming conductive contacts down through the layer of dielectric material to the silicided gate, source and drain regions in the p type channel of the PJFET; and

forming a field plate over the conductive contact extending down to the gate region of the PJFET, where the field plate also extends over at least some of the source and drain regions of the PJFET.

7. A method of forming an n type junction field effect transistor (NJFET) in a semiconductor substrate, comprising:

forming a first n type buried layer (NBL1) in the substrate;

forming a first p type buried layer (PBL1) in the substrate along both sides of the NBL1;

forming a first n type epitaxial layer (NEPI1) over the substrate;

forming a second p type buried layer (PBL2) over the PBL1 in the NEPI1;

forming a second n type epitaxial layer (NEPI2) over the NEPI1;

forming a p type surface shield near an upper surface of the NEPI2, where the p type surface shield resides over at least some of the PBL2;

forming an n type channel in the NEPI2, where the n type channel resides over at least some of the PBL2;

forming a p type back gate (BG) extension near a lower surface of the NEPI2, where the p type BG extension resides over at least some of the PBL2 and over less than all of the NBL1;

forming one or more p type deep back gate (BG) contact regions in the NEPI2 down to the PBL2;

forming a layer of silicide block material (SBLK) over the NEPI2;

patterning the SBLK to expose areas of the NEPI2 where gate, source and drain regions are to be formed;

forming n type source and drain regions in the n type channel of the NJFET;

forming a p type gate region in the n type channel of the NJFET;

siliciding the gate, source and drain regions in the n type channel of the NJFET;

forming a layer of dielectric material over the silicides and NEPI2;

forming conductive contacts down through the layer of dielectric material to the silicided gate, source and drain regions in the n type channel of the NJFET; and

forming a field plate over the conductive contact extending down to the gate region of the NJFET, where the field plate also extends over at least some of the source and drain regions of the NJFET.

8. A p type junction field effect transistor (PJFET) in a semiconductor substrate, comprising:

a first n type buried layer (NBL1) in the substrate;

a first p type buried layer (PBL1) in the substrate between NBL1 regions;

a first n type epitaxial layer (NEPI1) over the substrate;

a second p type buried layer (PBL2) I the NEPI1 and over at least some of the PBL1;

one or more DEEPNX regions over the NBL1 in the NEPI1;

a second n type epitaxial layer (NEPI2) over the NEPI1;

an n type surface shield near an upper surface of the NEPI2, where the n type surface shield resides over at least some of the NBL1;

a p type channel in the NEPI2, where the p type channel resides over at least some of the NBL1;

one or more n type deep back gate contact regions in the NEPI2 extending down to the DEEPNX regions;

a silicided n type gate region in the p type channel;

silicided p type source and drain regions in the p type channel;

a layer of dielectric material over the silicides and NEPI2;

conductive contacts extending down through the layer of dielectric material to the silicided gate, source and drain regions; and

a field plate over the conductive contact extending down to the gate region, where the field plate also extends over at least some of the source and drain regions.

9. An n type junction field effect transistor (NJFET) in a semiconductor substrate, comprising:

a first n type buried layer (NBL1) in the substrate;

a first p type buried layer (PBL1) in the substrate along both sides of the NBL1;

a first n type epitaxial layer (NEPI1) over the substrate;

a second p type buried layer (PBL2) over the PBL1 in the NEPI1;

a second n type epitaxial layer (NEPI2) over the NEPI1;

a p type surface shield near an upper surface of the NEPI2, where the p type surface shield resides over at least some of the PBL2;

an n type channel in the NEPI2, where the n type channel resides over at least some of the PBL2;

a p type back gate (BG) extension near a lower surface of the NEPI2, where the p type BG resides over at least some of the PBL2 and over less than all of the NBL1;

one or more p type deep back gate contact regions in the NEPI2 extending down to the PBL2;

silicided n type source and drain regions in the n type channel;

a silicided p type gate region in the n type channel;

a layer of dielectric material over the silicides and NEPI2;

conductive contacts extending down through the layer of dielectric material to the silicided gate, source and drain regions; and

a field plate over the conductive contact extending down to the gate region, where the field plate also extends over at least some of the source and drain regions.

10. A method of forming a p type junction field effect transistor (PJFET) and an n type junction field effect transistor (NJFET) in a semiconductor substrate, comprising:

forming a first n type buried layer (NBL1) in the substrate;

forming a first p type buried layer (PBL1) in the substrate,;

forming a first n type epitaxial layer (NEPI1) over the substrate;

forming one or more DEEPNX regions over the NBL1 in the NEPI1;

forming a p type surface shield near an upper surface of the NEPI, where the p type surface shield resides over at least some of the PBL1;

forming an n type channel in the NEPI1, where the n type channel resides over at least some of the PBL1;

forming a p type back gate (BG) extension near a lower surface of the NEPI1, where the p type BG extension resides over at least some of the PBL1 and over less than all of the NBL1;

forming an n type surface shield near an upper surface of the NEPI1, where the n type surface shield resides over at least some of the NBL1;

forming a p type channel in the NEPI1, where the p type channel resides over at least some of the NBL1;

forming one or more isolation areas that isolate the PNFET from the NJFET;

forming one or more n type deep back gate contact regions in the NEPI1 down to the DEEPNX regions in the PJFET;

forming one or more p type deep back gate contact regions in the NEPI1 down to the PBL1 in the NJFET;

forming a deep p type region in the NEPI1 down to the PBL1 in the PJFET:

forming a layer of silicide block material (SBLK) over the NEPI1;

patterning the SBLK to expose areas of the NEPI1 where gate, source and drain regions are to be formed;

forming an n type gate region in the p type channel of the PJFET, and n type source and drain regions in the n type channel of the NJFET;

forming p type source and drain regions in the p type channel of the PJFET, and a p type gate region in the n type channel of the NJFET;

siliciding the gate, source and drain regions in the p type channel of the PJFET and the n type channel of the NJFET;

forming a layer of dielectric material over the silicides and NEPI1;

forming conductive contacts down through the layer of dielectric material to the silicided gate, source and drain regions in the p type channel of the PJFET and the n type channel of the NJFET; and

forming a field plate over at least one of the conductive contacts extending down to the gate regions of the PJFET and the NJFET, where the field plates also extend over at least some of at least one of the source and drain regions of the PJFET and the source and drain regions of the NJFET.

11. A method of forming a p type junction field effect transistor (PJFET) in a semiconductor substrate, comprising:

forming a first n type buried layer (NBL1) in the substrate;

forming a first p type buried layer (PBL1) in the substrate between NBL1 regions;

forming a first n type epitaxial layer (NEPI1) over the substrate;

forming one or more DEEPNX regions over the NBL1 in the NEPI1;

forming an n type surface shield near an upper surface of the NEPI1, where the n type surface shield resides over at least some of the NBL1;

forming a p type channel in the NEPI1, where the p type channel resides over at least some of the NBL1;

forming one or more n type deep back gate contact regions in the NEPI1 down to the DEEPNX regions;

forming a deep p type region in the NEPI1 down to the PBL1;

forming a layer of silicide block material (SBLK) over the NEPI1;

patterning the SBLK to expose areas of the NEPI1 where gate, source and drain regions are to be formed;

forming an n type gate region in the p type channel of the PJFET;

forming p type source and drain regions in the p type channel of the PJFET;

siliciding the gate, source and drain regions in the p type channel of the PJFET;

forming a layer of dielectric material over the silicides and NEPI1;

forming conductive contacts down through the layer of dielectric material to the silicided gate, source and drain regions in the p type channel of the PJFET; and

forming a field plate over the conductive contact extending down to the gate region of the PJFET, where the field plate also extends over at least some of the source and drain regions of the PJFET.

12. A method of forming an n type junction field effect transistor (NJFET) in a semiconductor substrate, comprising:

forming a first n type buried layer (NBL1) in the substrate;

forming a first p type buried layer (PBL1) in the substrate along both sides of the NBL1;

forming a first n type epitaxial layer (NEPI1) over the substrate;

forming a p type surface shield near an upper surface of the NEPI1, where the p type surface shield resides over at least some of the PBL1;

forming an n type channel in the NEPI1, where the n type channel resides over at least some of the PBL1;

forming a p type back gate (BG) extension near a lower surface of the NEPI1, where the p type BG extension resides over at least some of the PBL1 and over less than all of the NBL1;

forming one or more p type deep back gate (BG) contact regions in the NEPI1 down to the PBL1;

forming a layer of silicide block material (SBLK) over the NEPI1;

patterning the SBLK to expose areas of the NEPI1 where gate, source and drain regions are to be formed;

forming n type source and drain regions in the n type channel of the NJFET;

forming a p type gate region in the n type channel of the NJFET;

siliciding the gate, source and drain regions in the n type channel of the NJFET;

forming a layer of dielectric material over the silicides and NEPI1;

forming conductive contacts down through the layer of dielectric material to the silicided gate, source and drain regions in the n type channel of the NJFET; and

forming a field plate over the conductive contact extending down to the gate region of the NJFET, where the field plate also extends over at least some of the source and drain regions of the NJFET.

13. A p type junction field effect transistor (PJFET) in a semiconductor substrate, comprising:

a first n type buried layer (NBL1) in the substrate;

a first p type buried layer (PBL1) in the substrate between NBL1 regions;

a first n type epitaxial layer (NEPI1) over the substrate;

one or more DEEPNX regions over the NBL1 in the NEPI1;

an n type surface shield near an upper surface of the NEPI1, where the n type surface shield resides over at least some of the NBL1;

a p type channel in the NEPI1, where the p type channel resides over at least some of the NBL1;

one or more n type deep back gate contact regions in the NEPI1 extending down to the DEEPNX regions;

a silicided n type gate region in the p type channel;

silicided p type source and drain regions in the p type channel;

a layer of dielectric material over the silicides and NEPI1;

conductive contacts extending down through the layer of dielectric material to the silicided gate, source and drain regions; and

a field plate over the conductive contact extending down to the gate region, where the field plate also extends over at least some of the source and drain regions.

14. An n type junction field effect transistor (NJFET) in a semiconductor substrate, comprising:

a first n type buried layer (NBL1) in the substrate;

a first p type buried layer (PBL1) in the substrate along both sides of the NBL1;

a first n type epitaxial layer (NEPI1) over the substrate;

a p type surface shield near an upper surface of the NEPI1, where the p type surface shield resides over at least some of the PBL1;

an n type channel in the NEPI1, where the n type channel resides over at least some of the PBL1;

a p type back gate (BG) extension near a lower surface of the NEPI1, where the p type BG resides over at least some of the PBL2 and over less than all of the NBL1;

one or more p type deep back gate contact regions in the NEPI1 extending down to the PBL1;

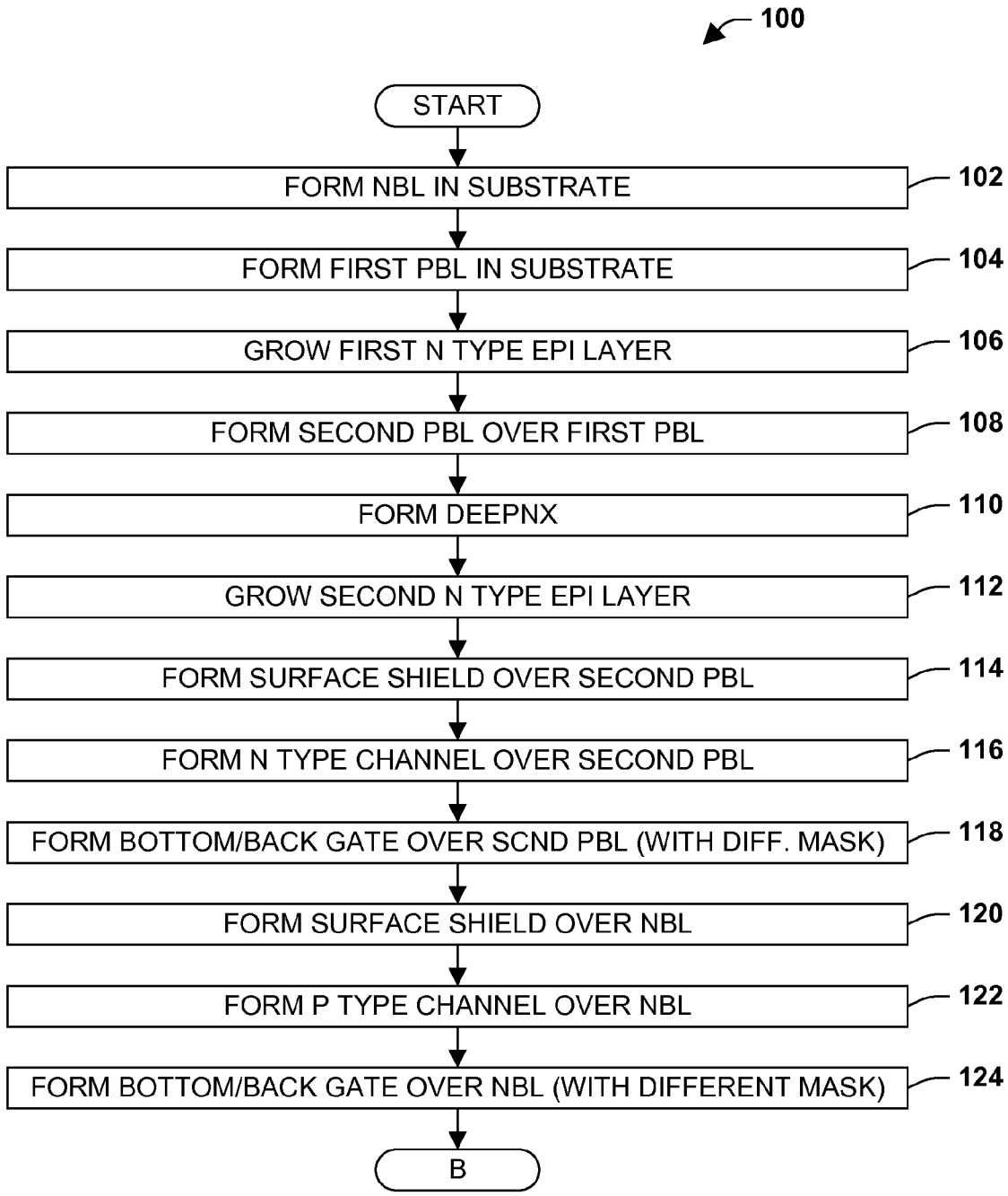
silicided n type source and drain regions in the n type channel;

a silicided p type gate region in the n type channel;

a layer of dielectric material over the silicides and NEPI1;

conductive contacts extending down through the layer of dielectric material to the silicided gate, source and drain regions; and

a field plate over the conductive contact extending down to the gate region, where the field plate also extends over at least some of the source and drain regions.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FORM FIRST PBL IN SUBSTRATE
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GROW FIRST N TYPE EPI LAYER
106
FORM SECOND PBL OVER FIRST PBL
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FORM DEEPNX
110
GROW SECOND N TYPE EPI LAYER
112
FORM SURFACE SHIELD OVER SECOND PBL
114
FORM N TYPE CHANNEL OVER SECOND PBL
116
FORM BOTTOM/BACK GATE OVER SCND PBL (WITH DIFF. MASK)
118
FORM SURFACE SHIELD OVER NBL
120
FORM P TYPE CHANNEL OVER NBL
122
FORM BOTTOM/BACK GATE OVER NBL (WITH DIFFERENT MASK)
124
B

Fig. 1A

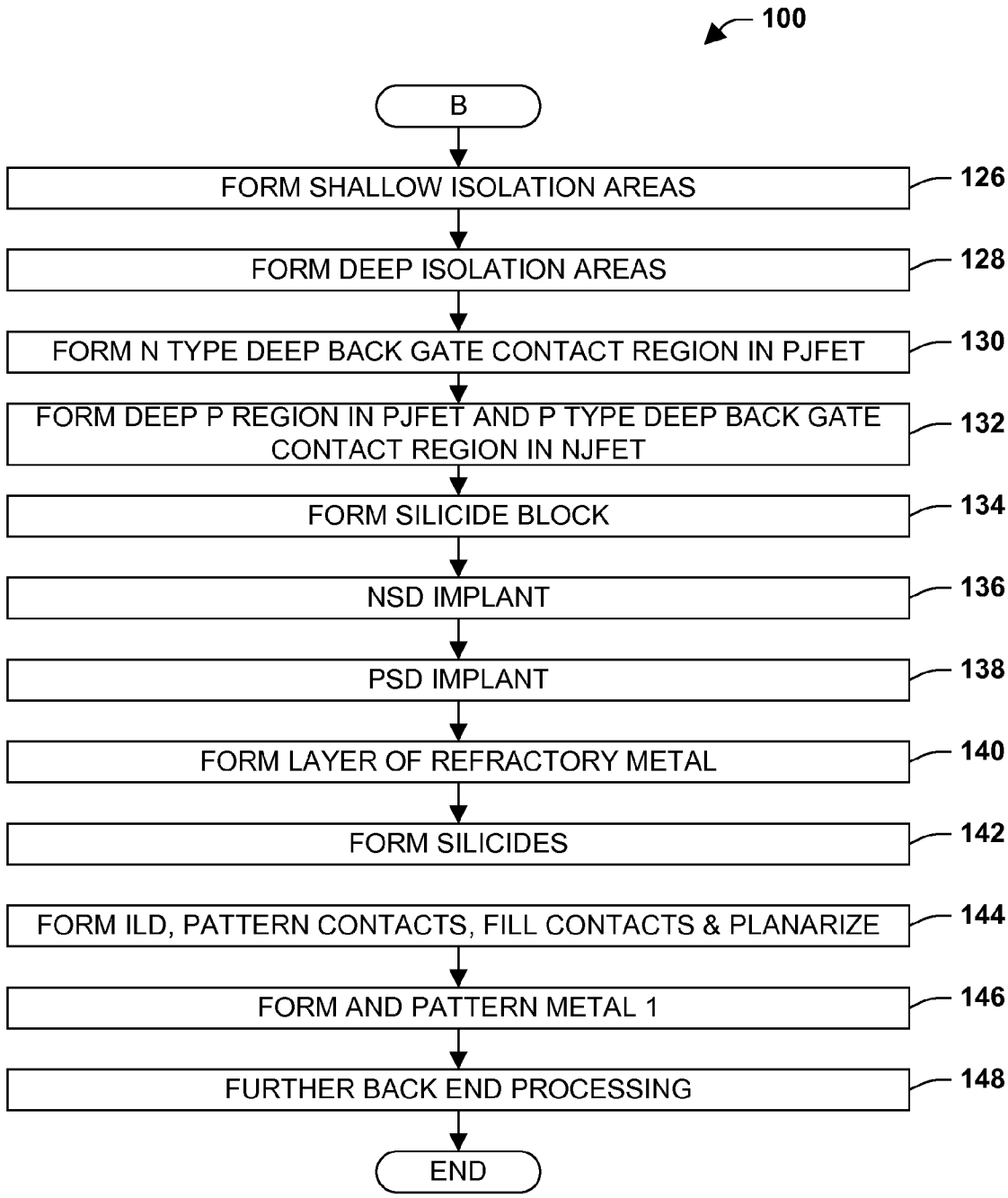
100
B
FORM SHALLOW ISOLATION AREAS
126
FORM DEEP ISOLATION AREAS
128
FORM N TYPE DEEP BACK GATE CONTACT REGION IN PJFET
130
FORM DEEP P REGION IN PJFET AND P TYPE DEEP BACK GATE CONTACT REGION IN NJFET
132
FORM SILICIDE BLOCK
134
NSD IMPLANT
136
PSD IMPLANT
138
FORM LAYER OF REFRACTORY METAL
140
FORM SILICIDES
142
FORM ILD, PATTERN CONTACTS, FILL CONTACTS & PLANARIZE
144
FORM AND PATTERN METAL 1
146
FURTHER BACK END PROCESSING
148
END

Fig. 1B

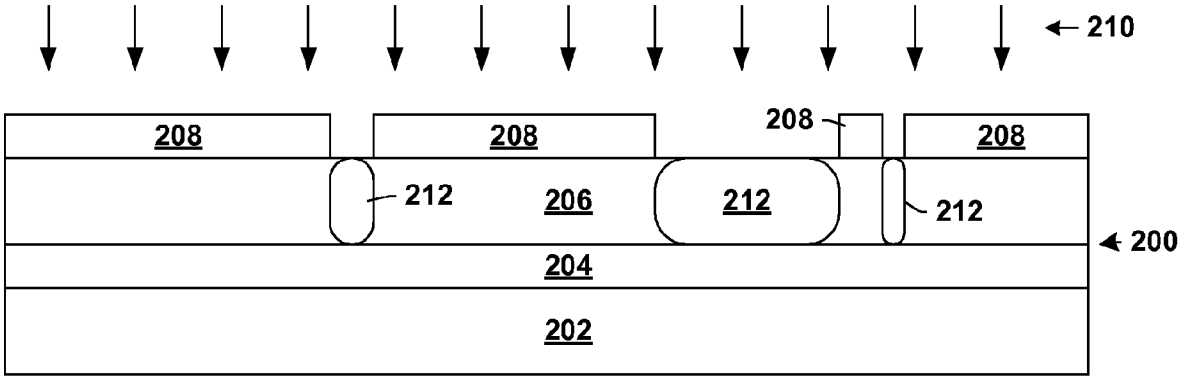
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Fig. 2

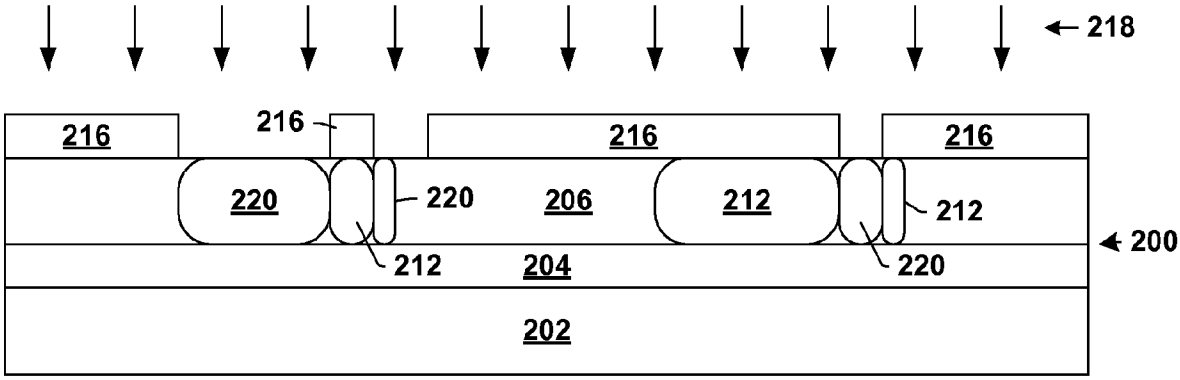
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Fig. 3

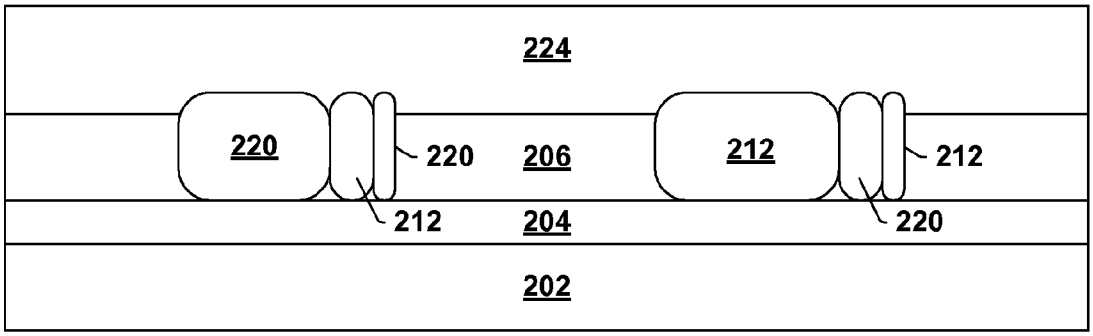
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Fig. 4

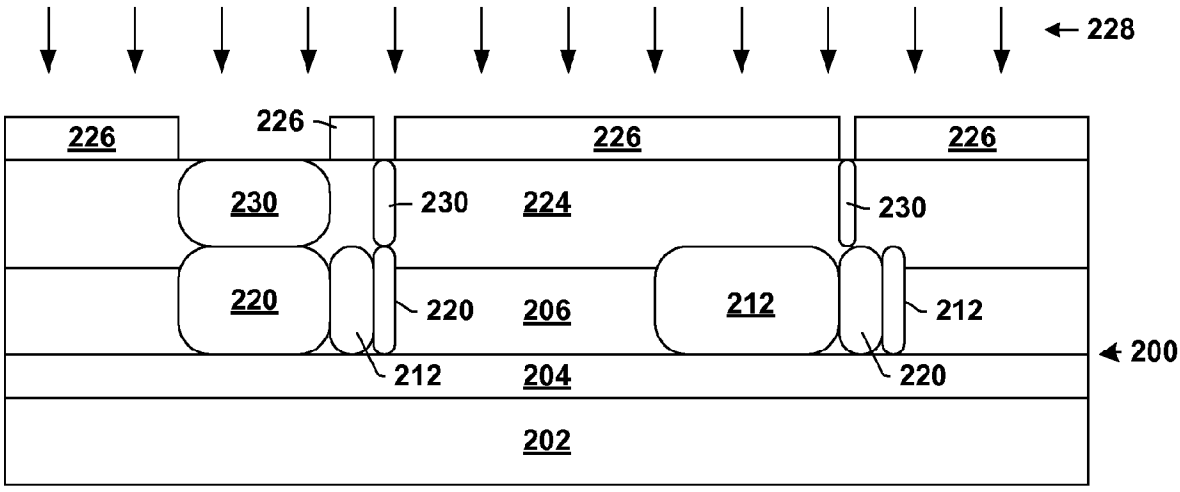
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Fig. 5

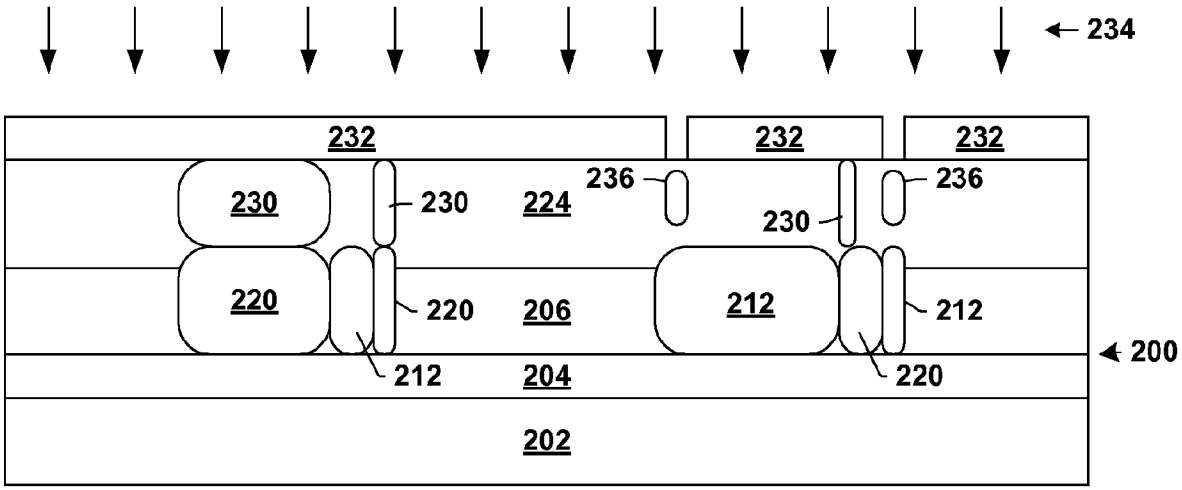
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Fig. 6

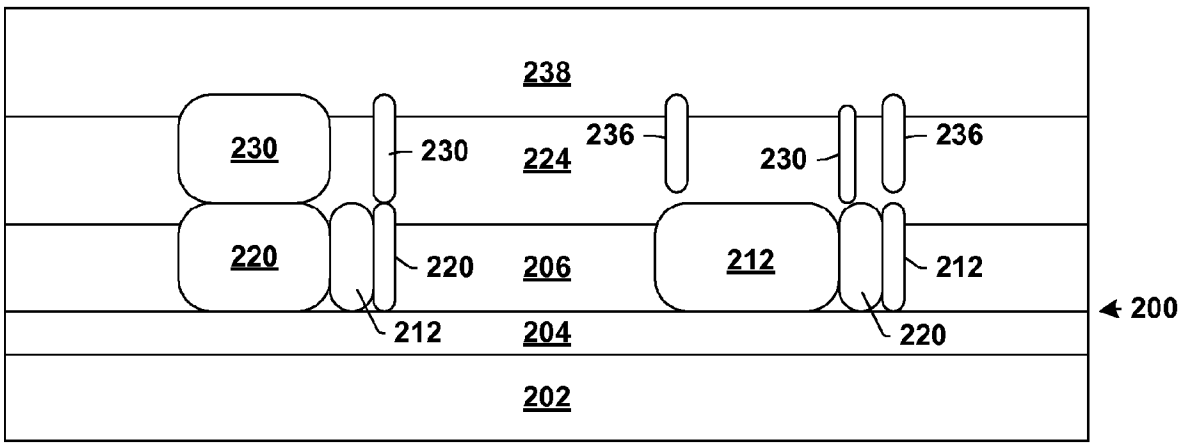
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Fig. 7

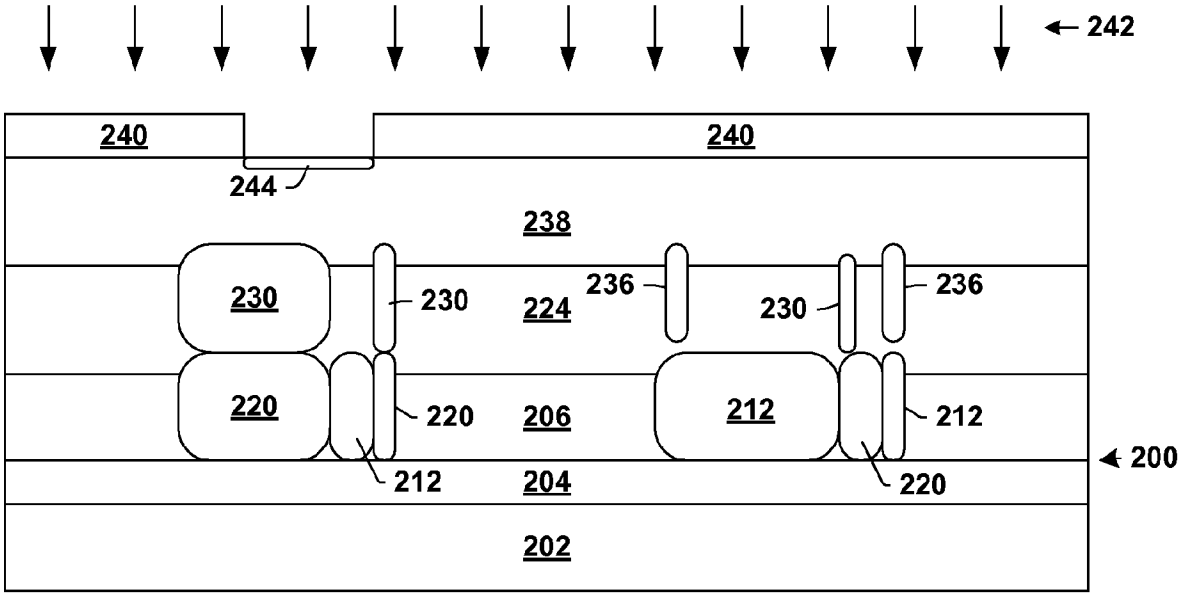
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Fig. 8

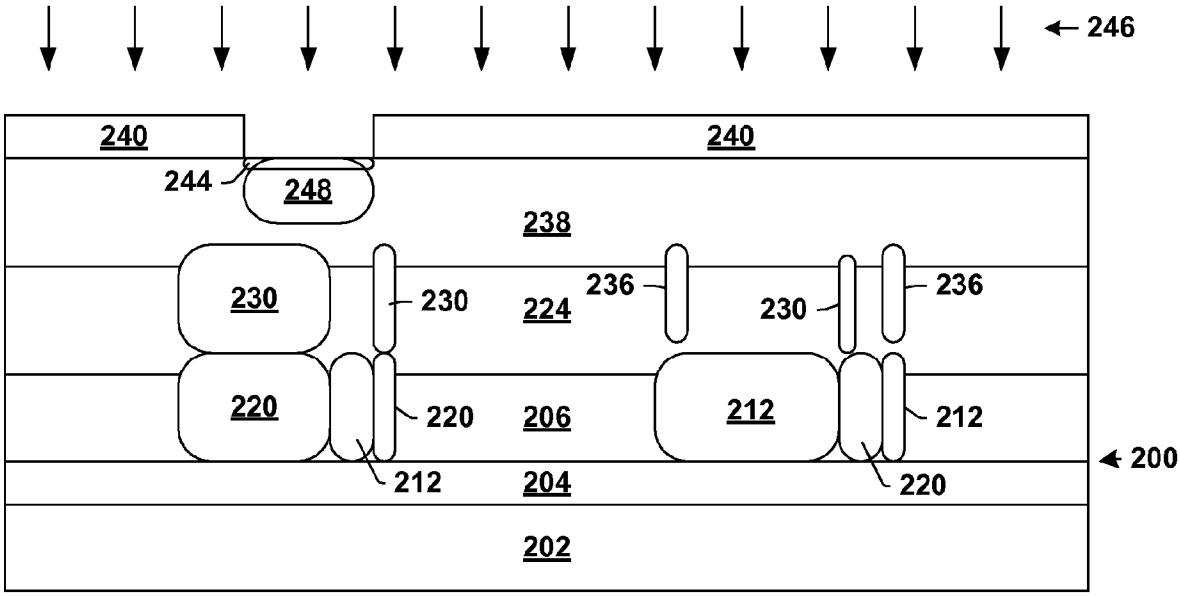
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Fig. 9

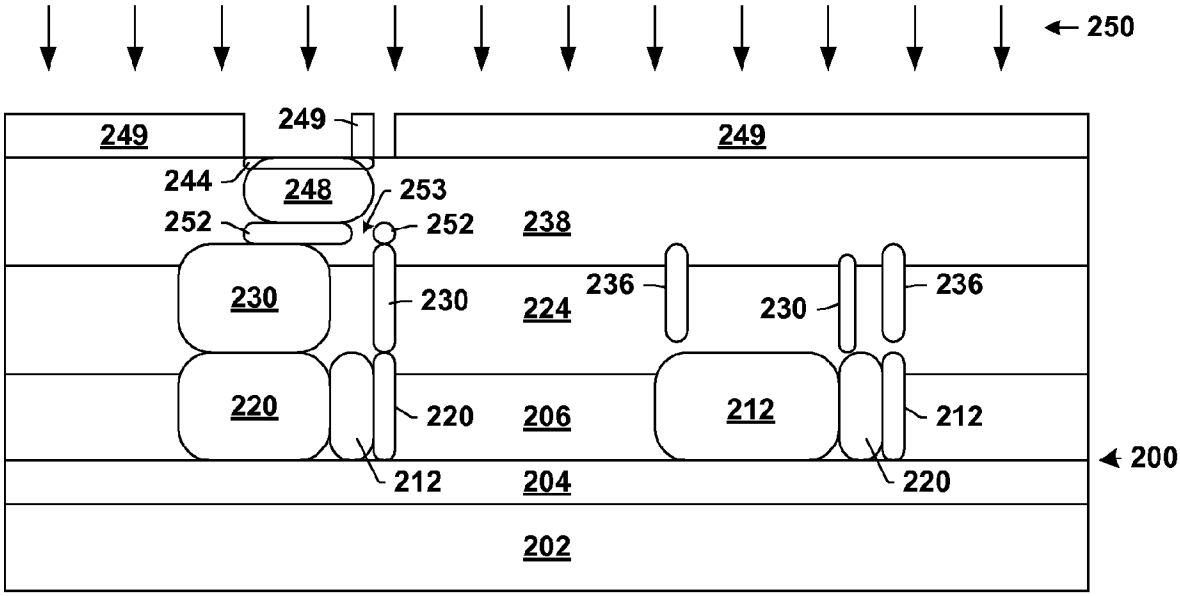
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Fig. 10

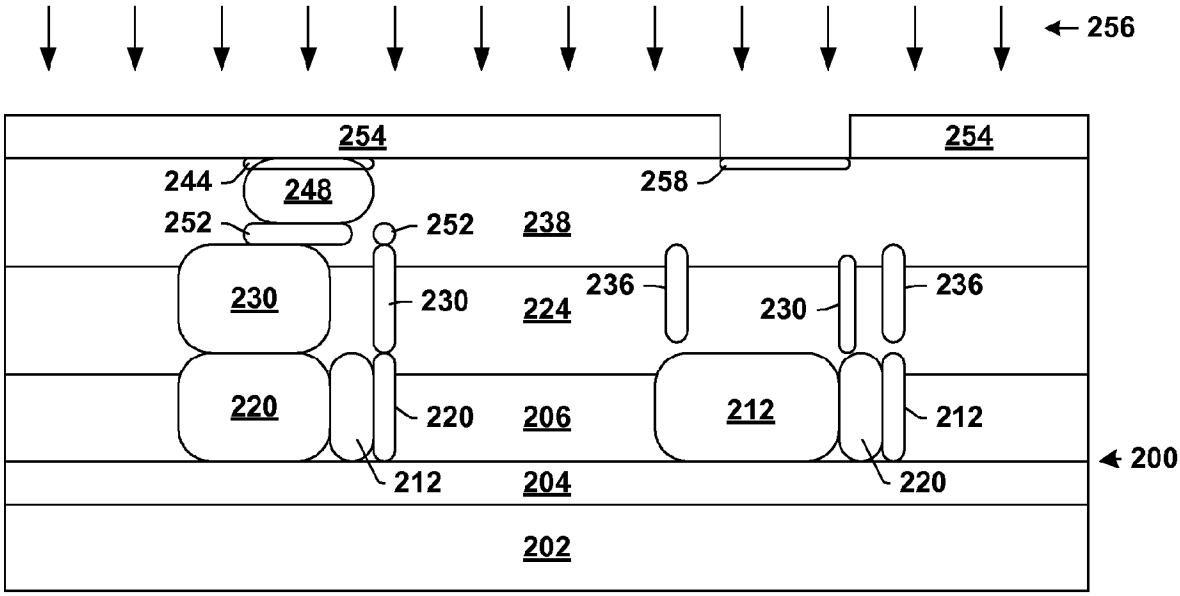
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Fig. 11

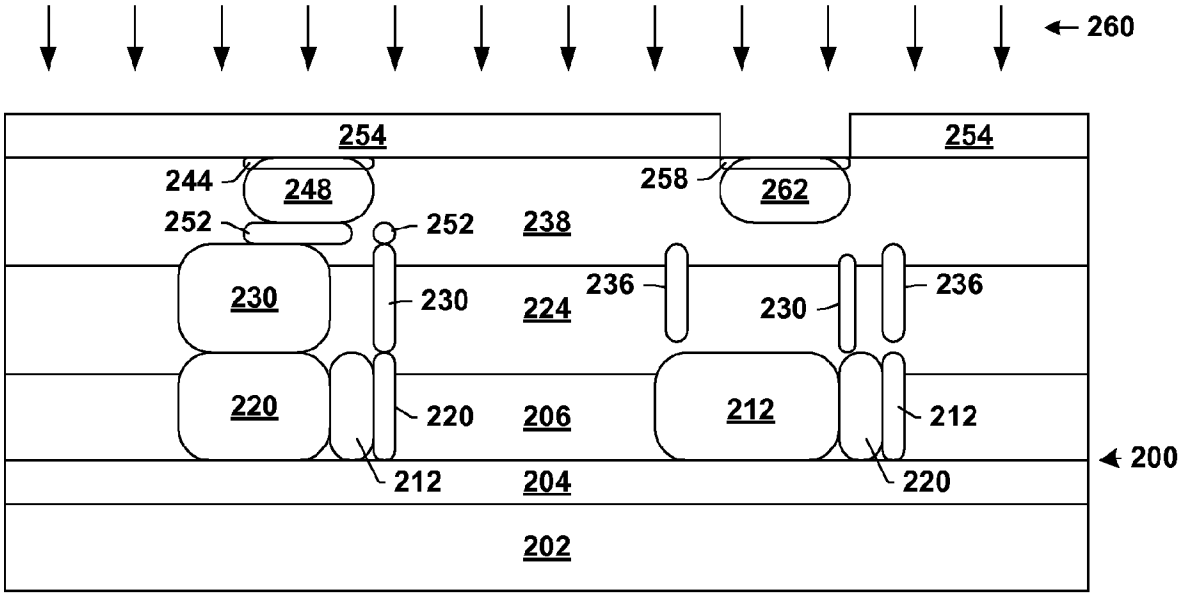
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Fig. 12

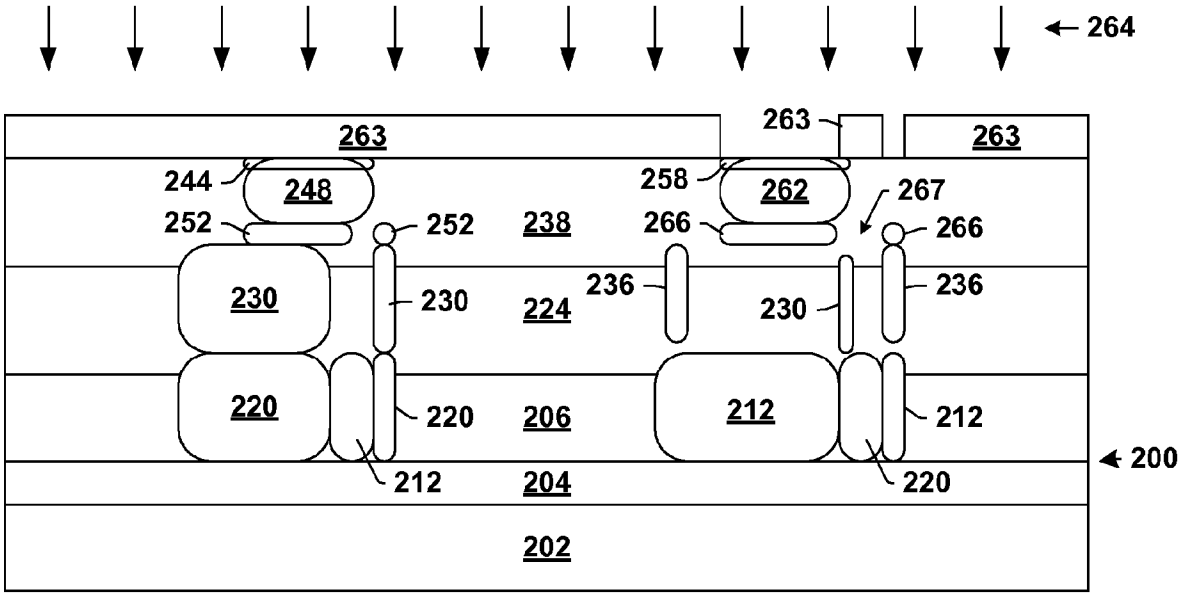
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Fig. 13

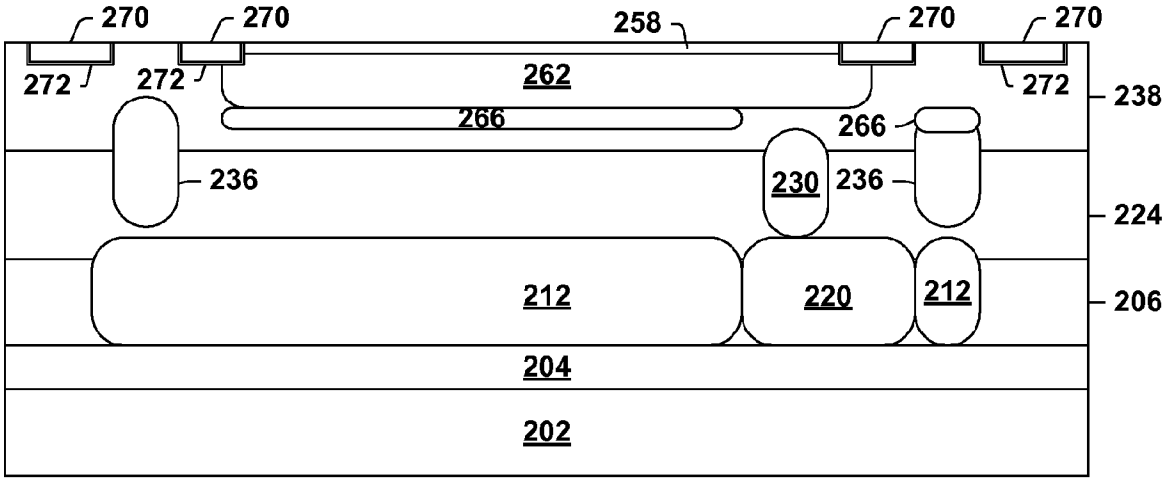
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Fig. 14

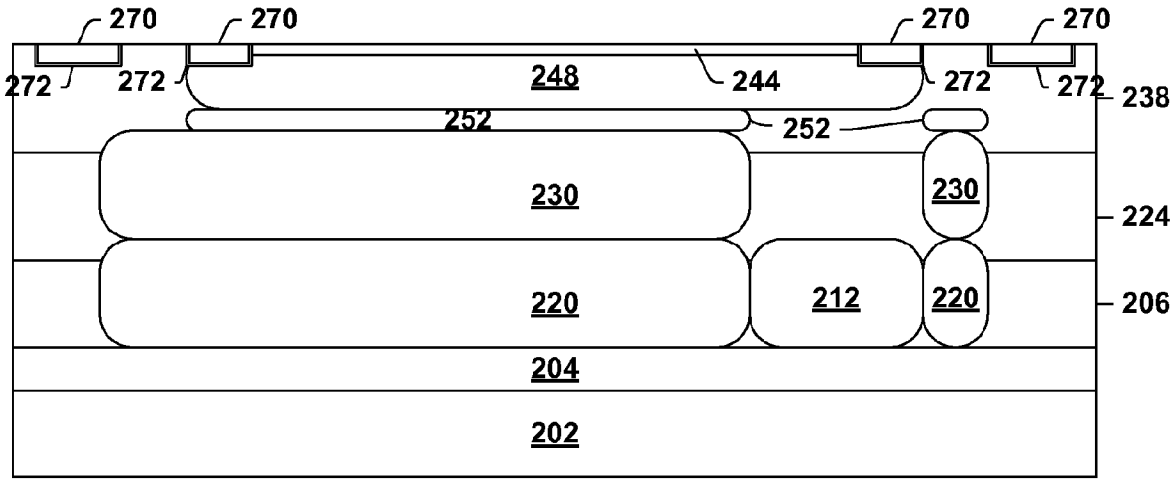
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Fig. 15

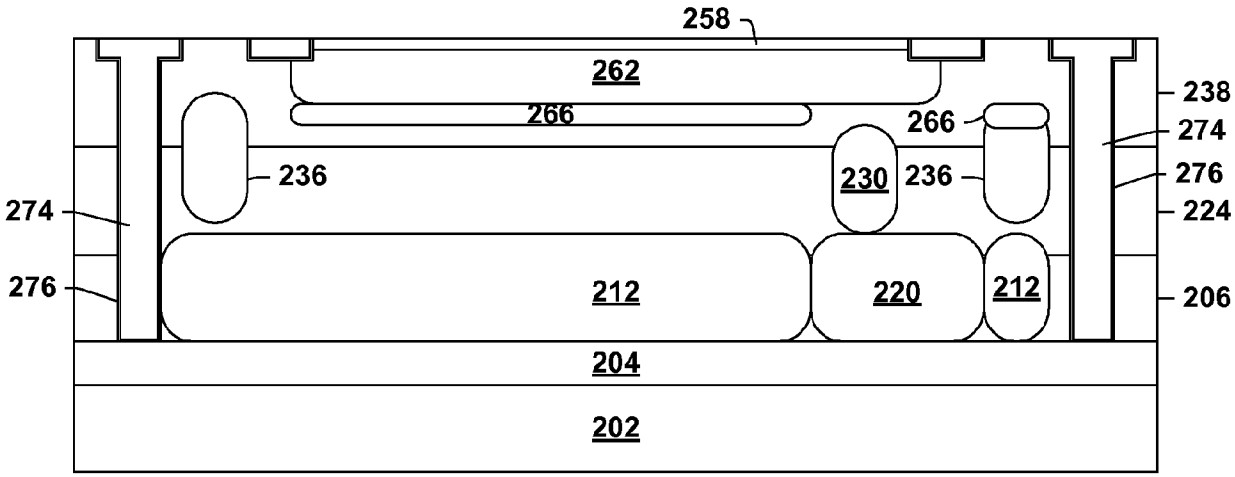
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Fig. 16

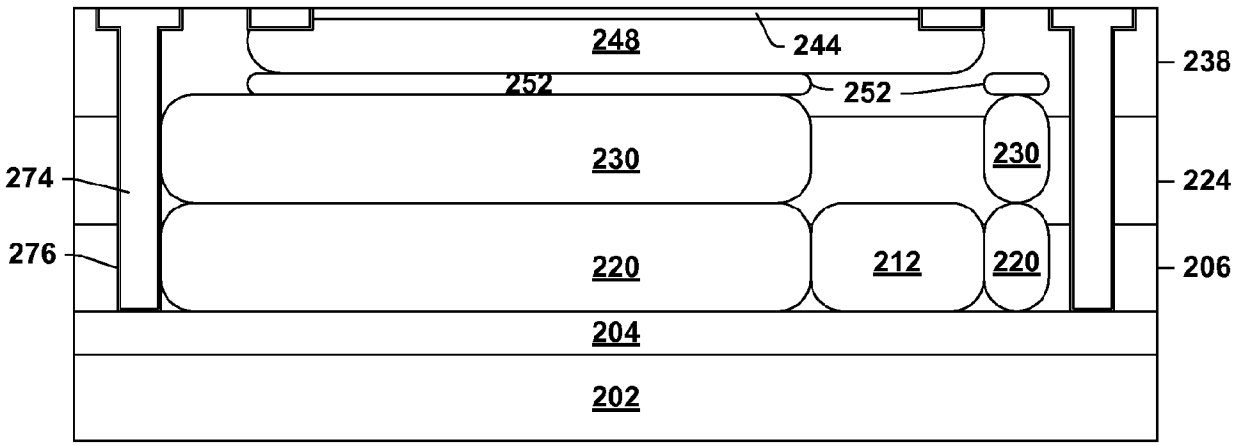
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Fig. 17

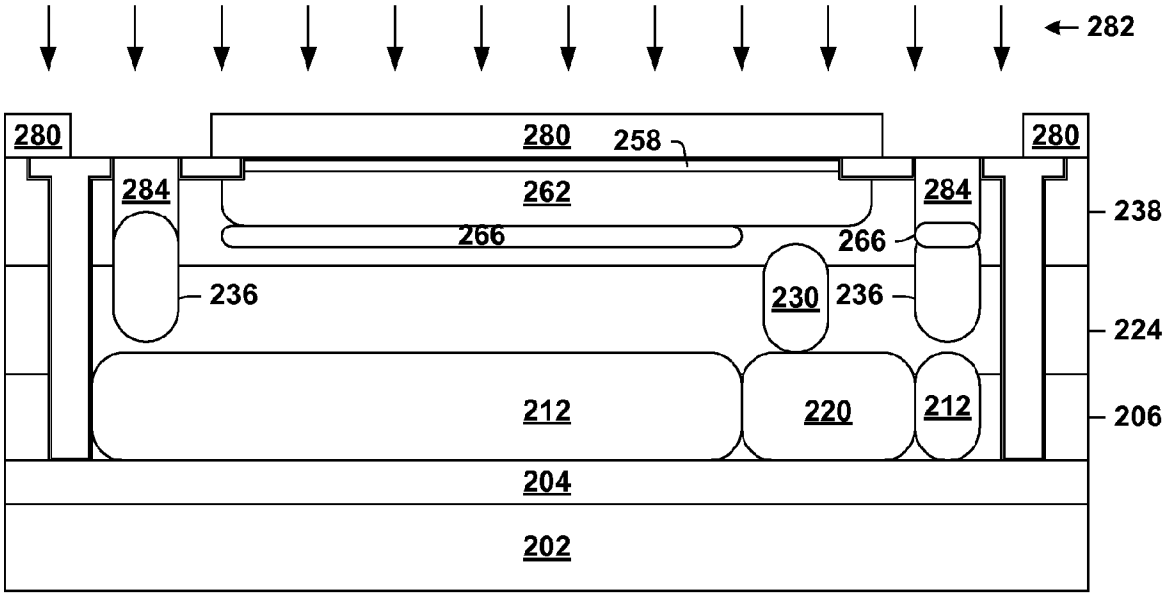
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Fig. 18

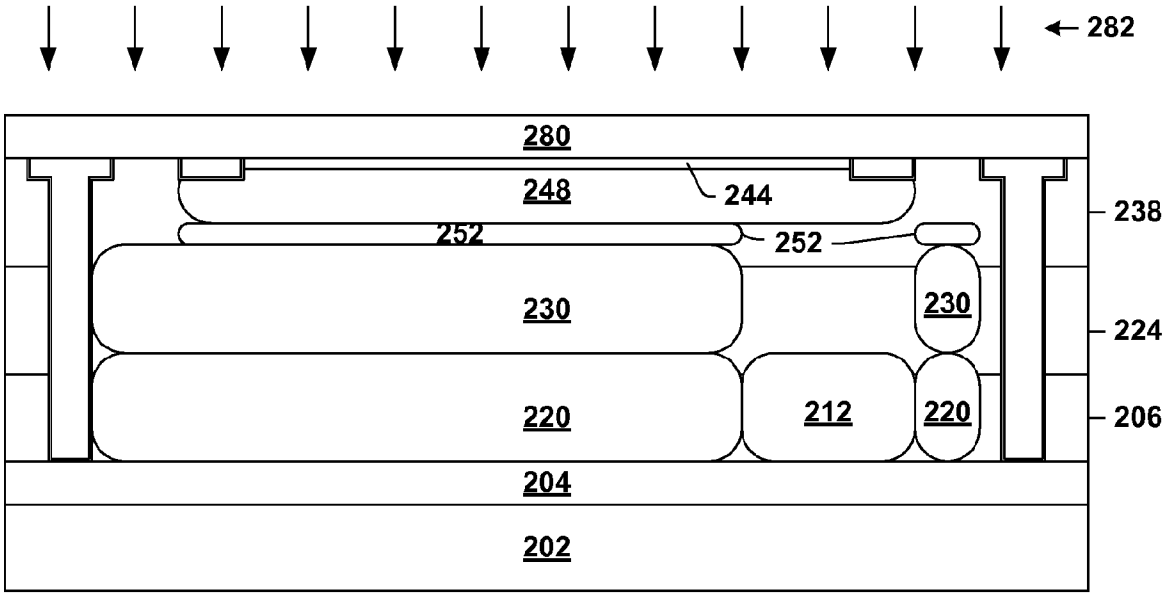
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Fig. 19

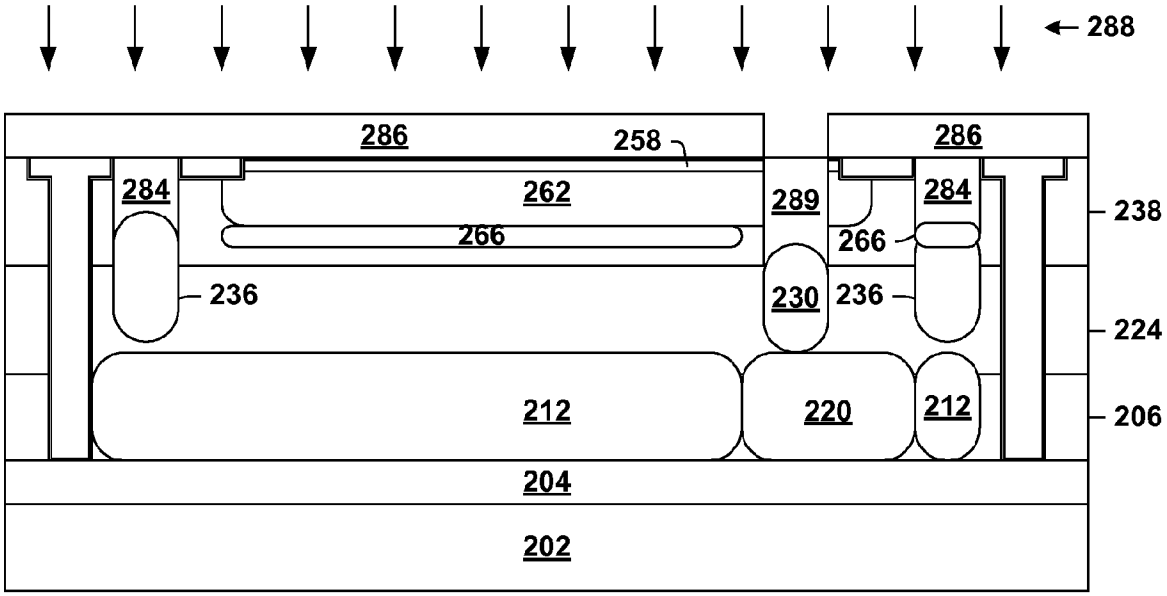
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Fig. 20

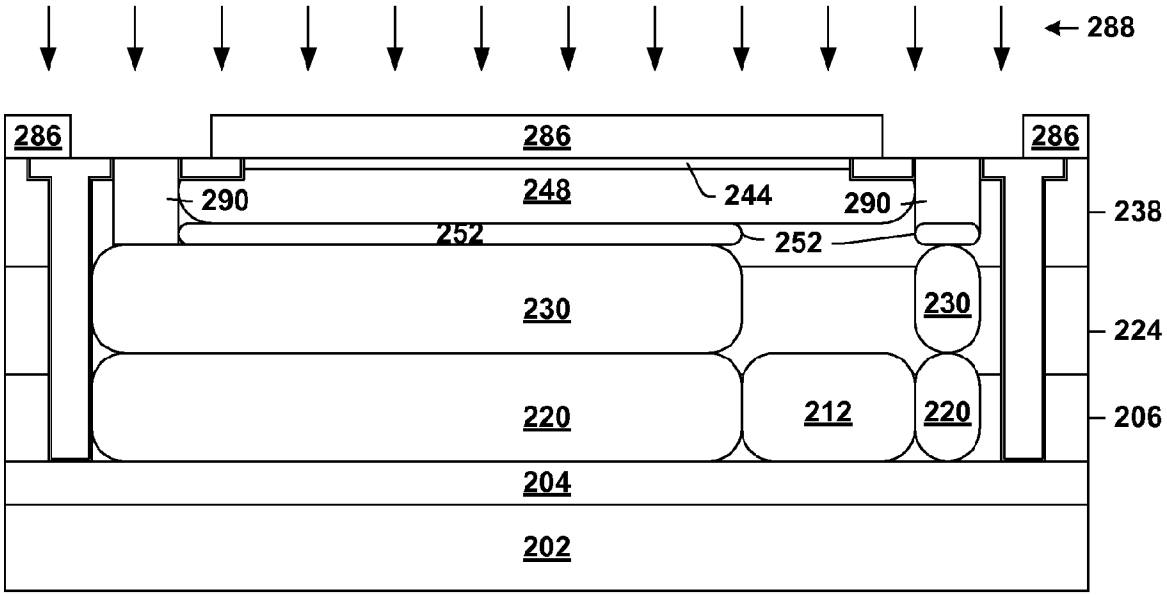
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Fig. 21

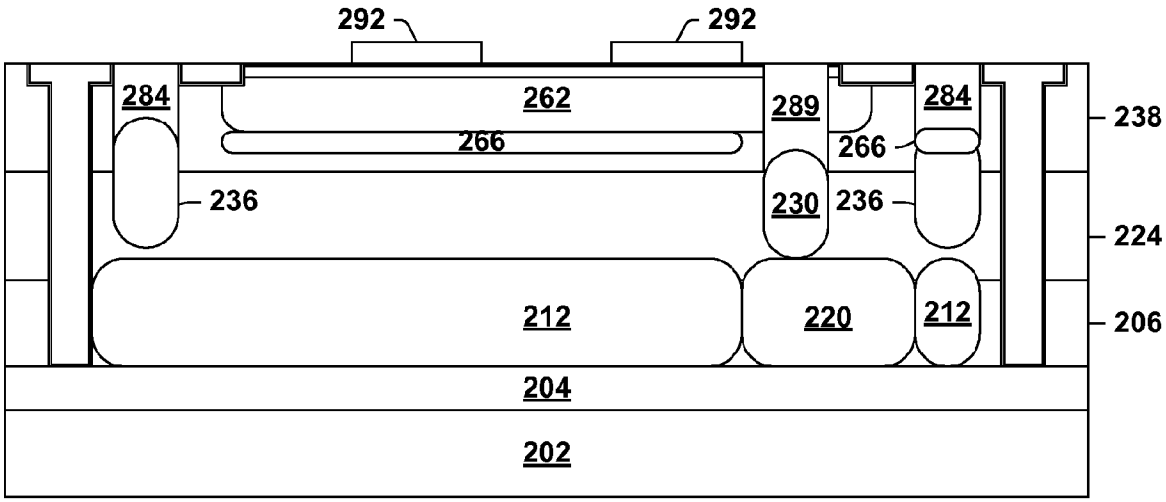
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Fig. 22

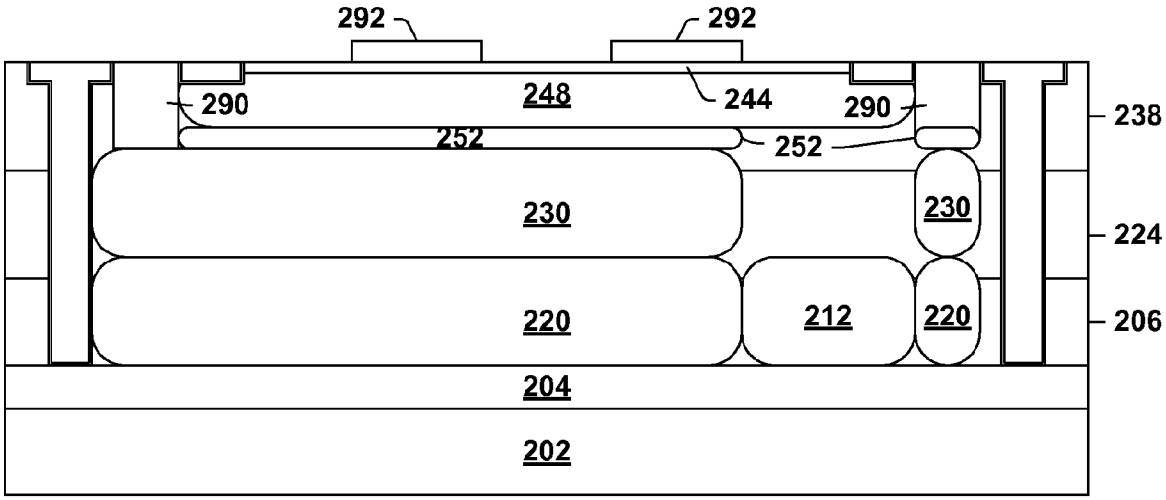
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Fig. 23

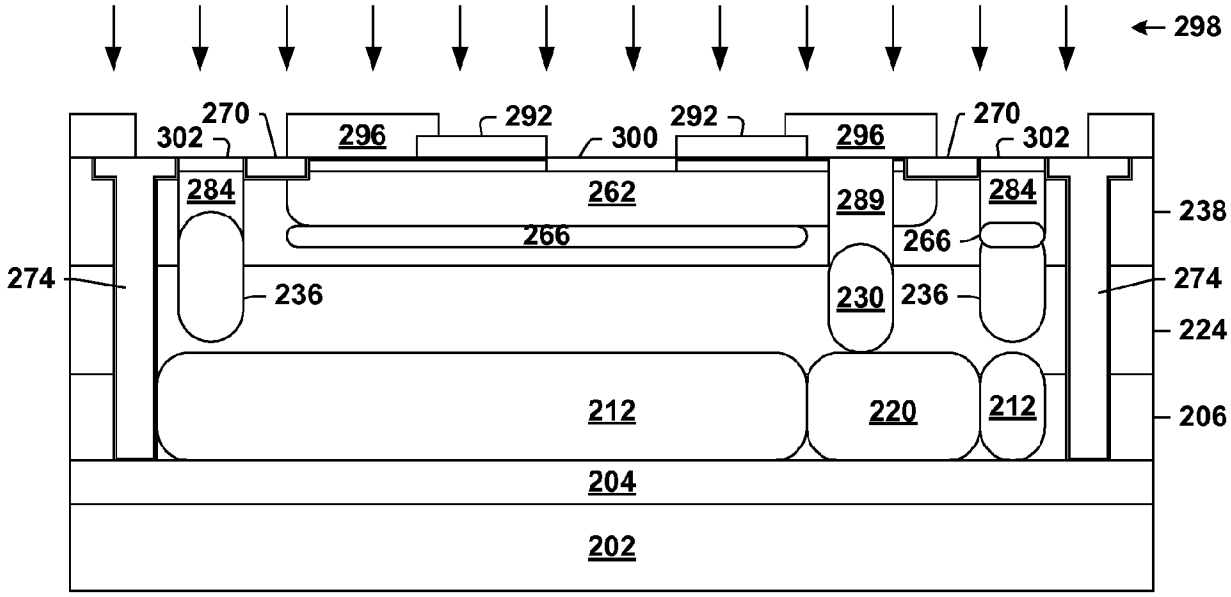
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Fig. 24

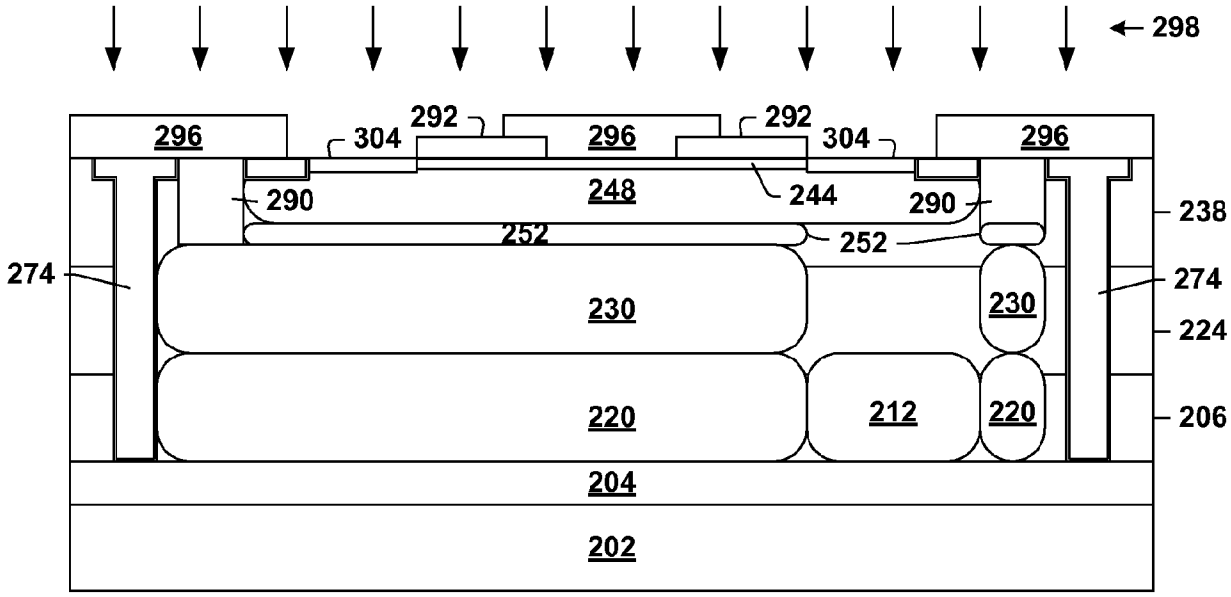
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Fig. 25

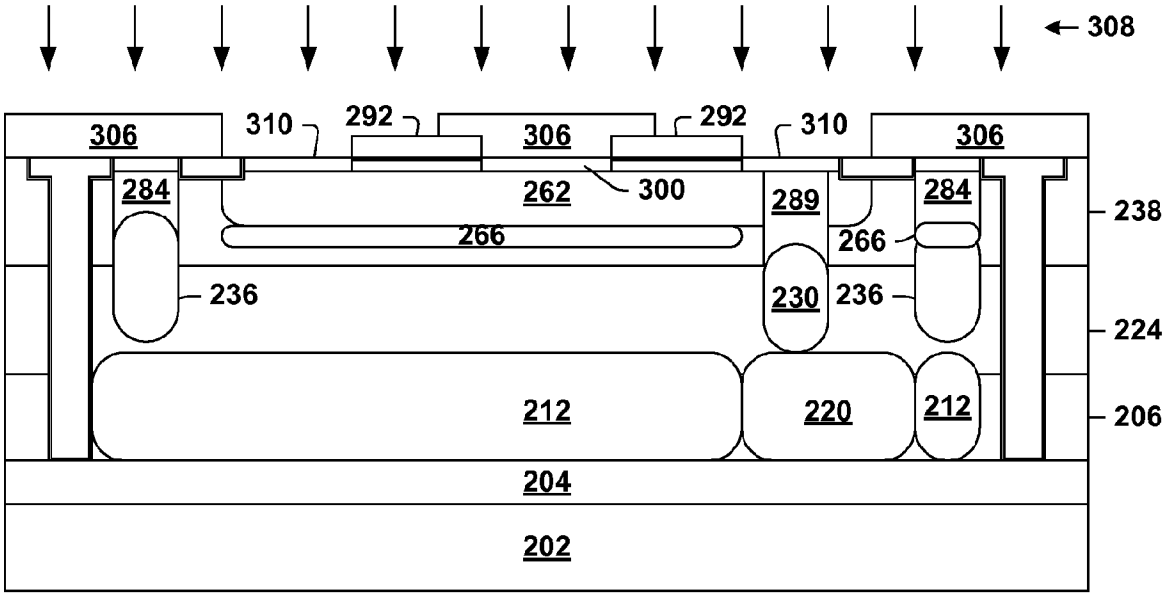
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Fig. 26

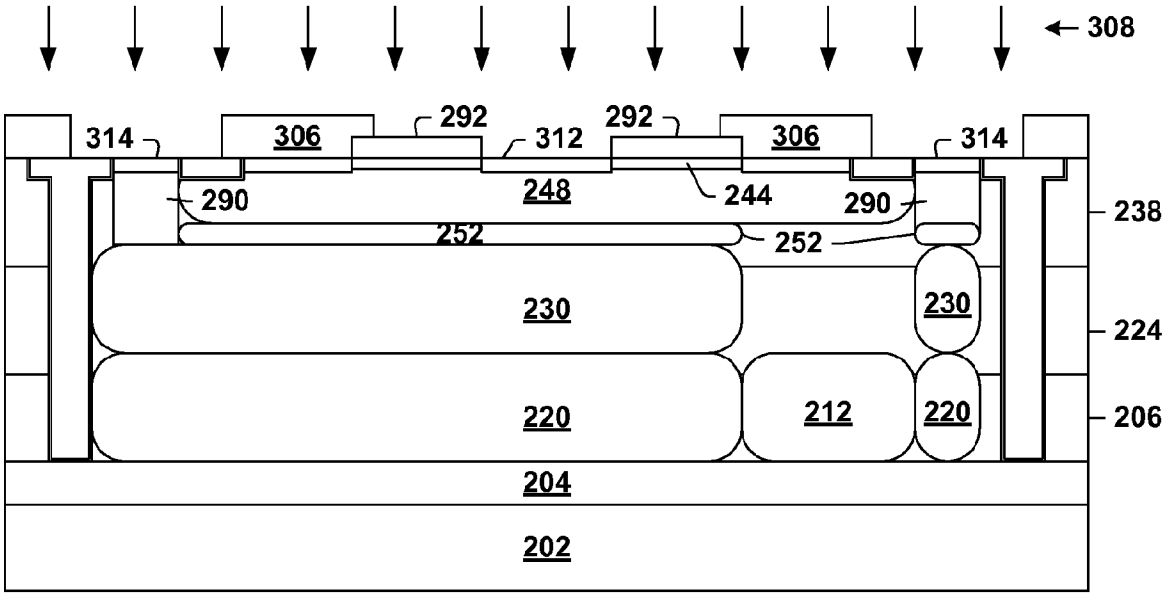
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Fig. 27

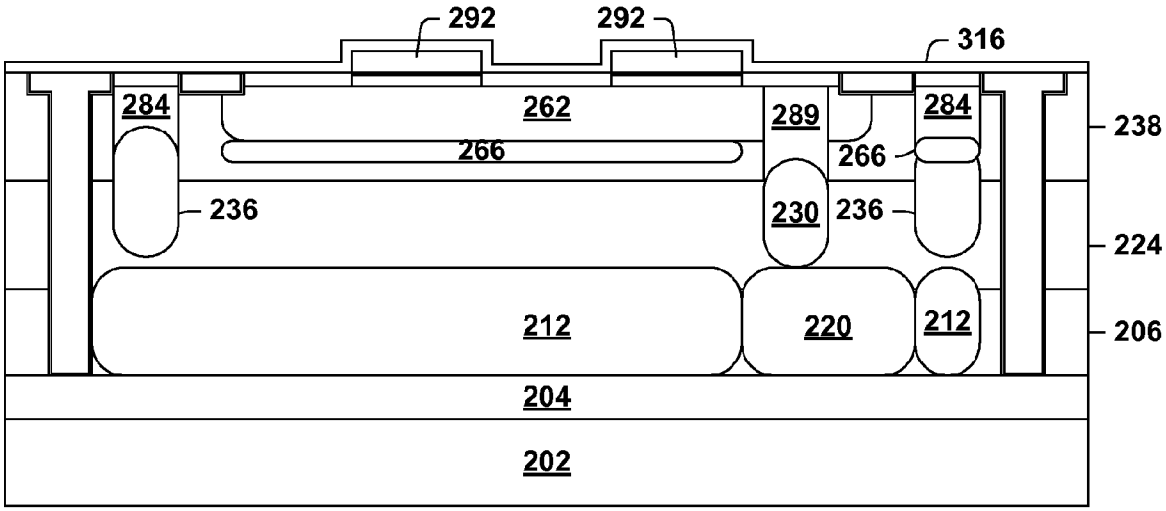
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Fig. 28

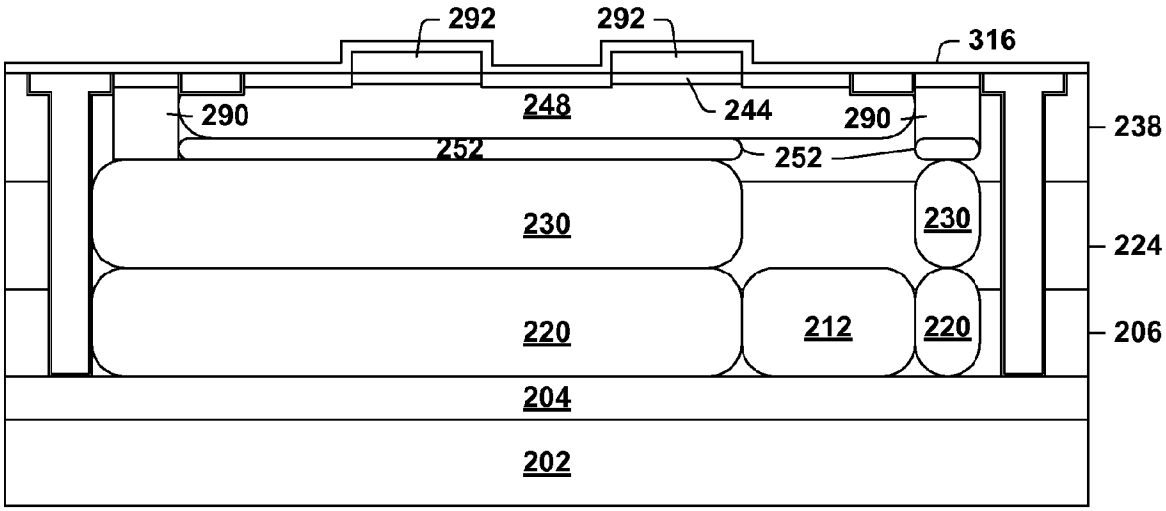
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Fig. 29

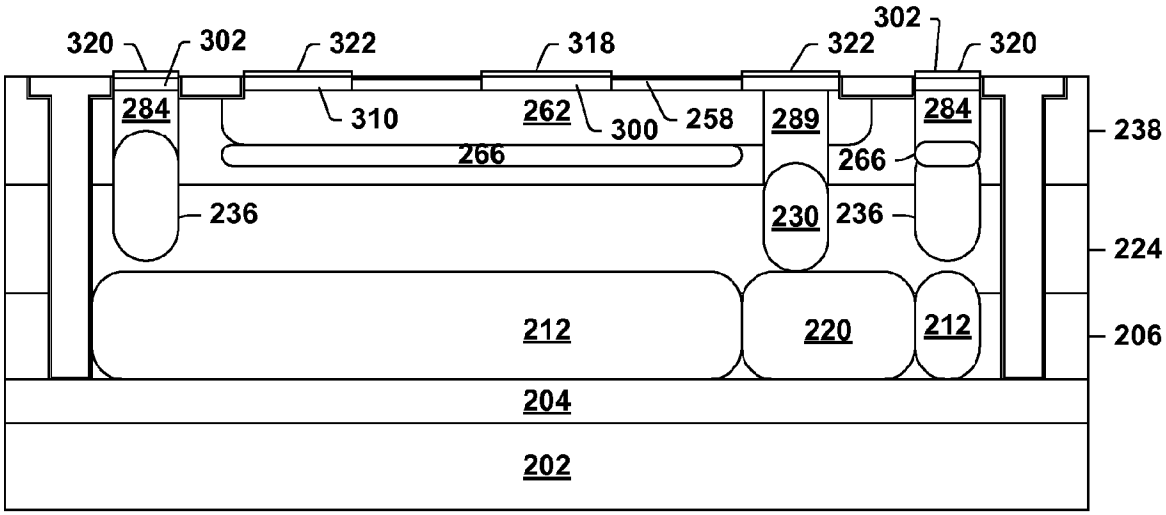
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Fig. 30

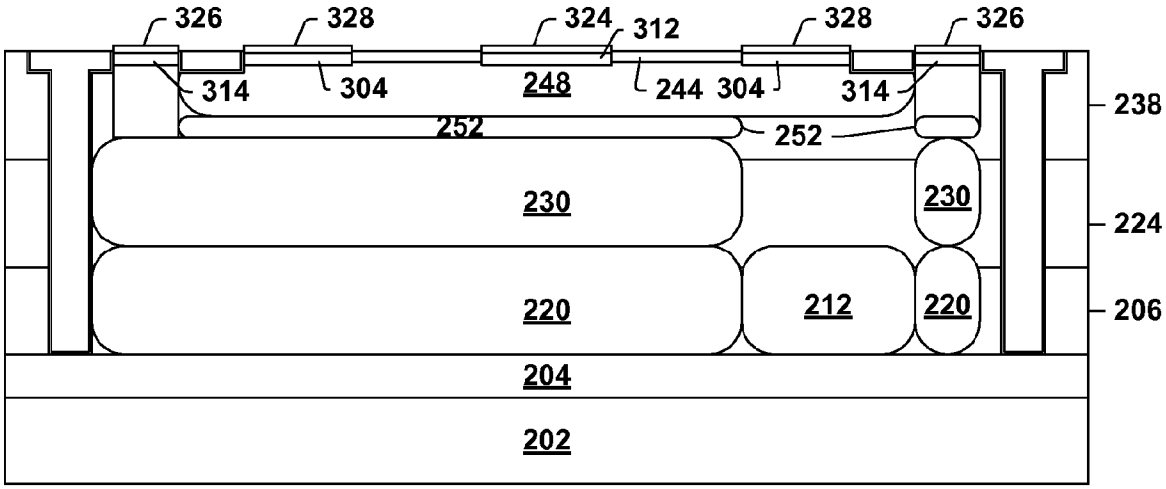
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Fig. 31

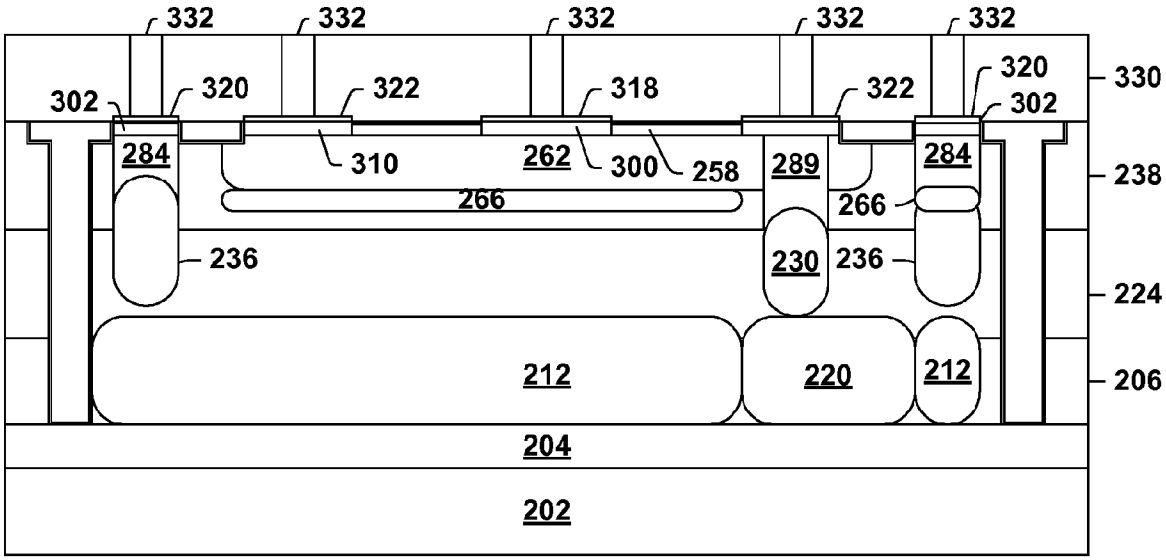
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Fig. 32

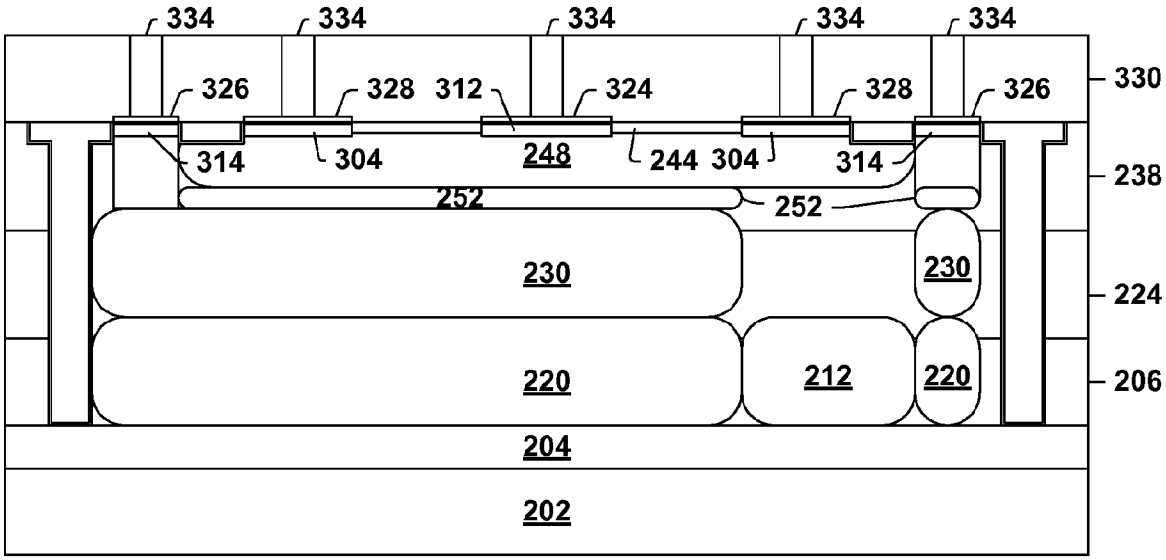
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Fig. 33

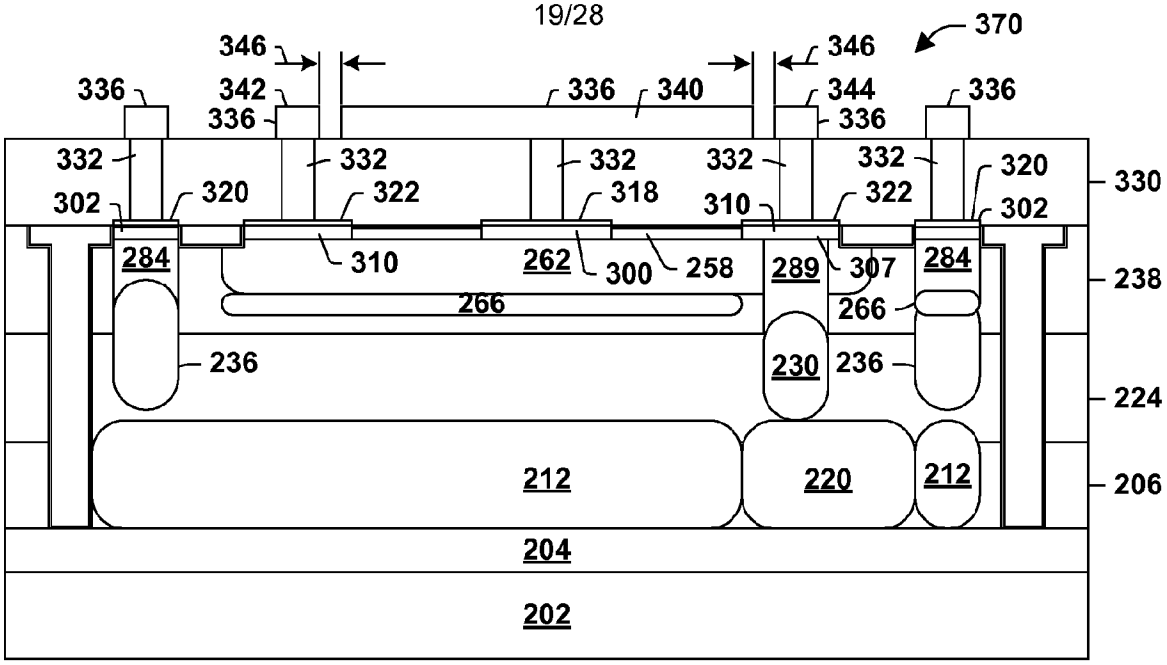
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Fig. 34

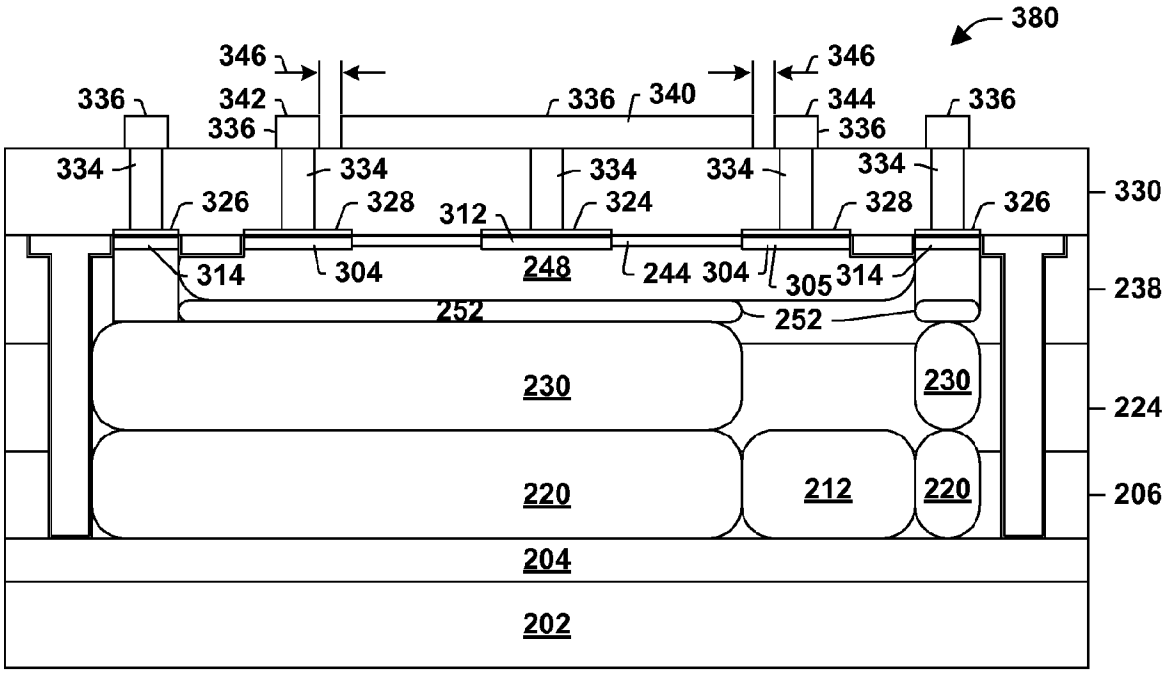
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Fig. 35

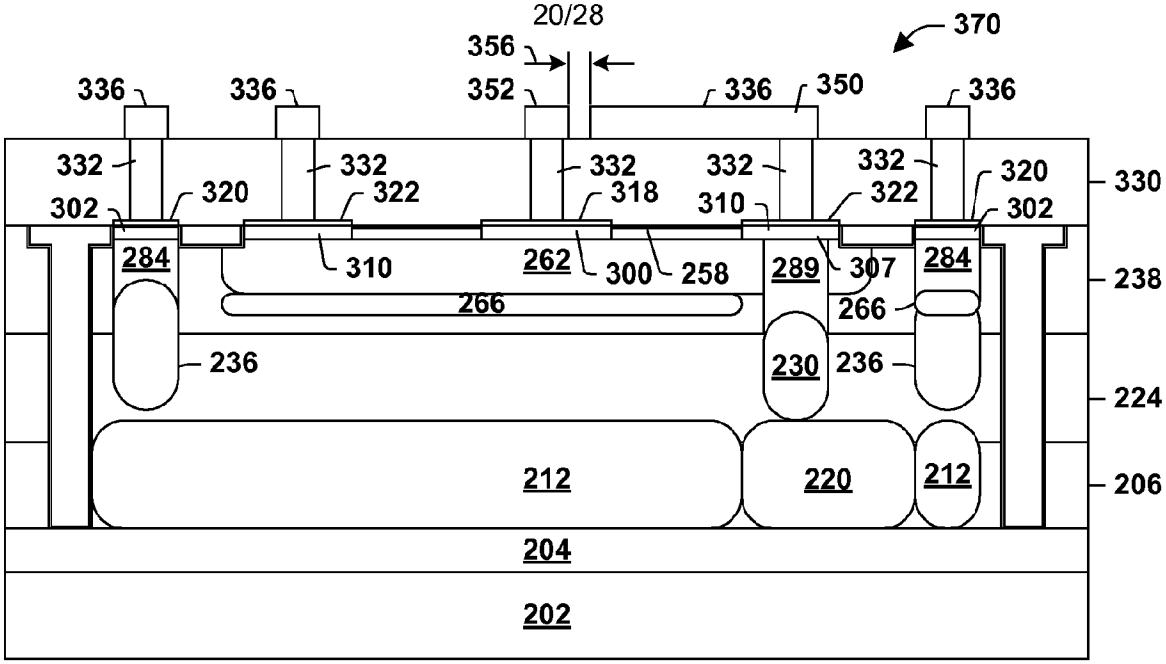
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Fig. 36

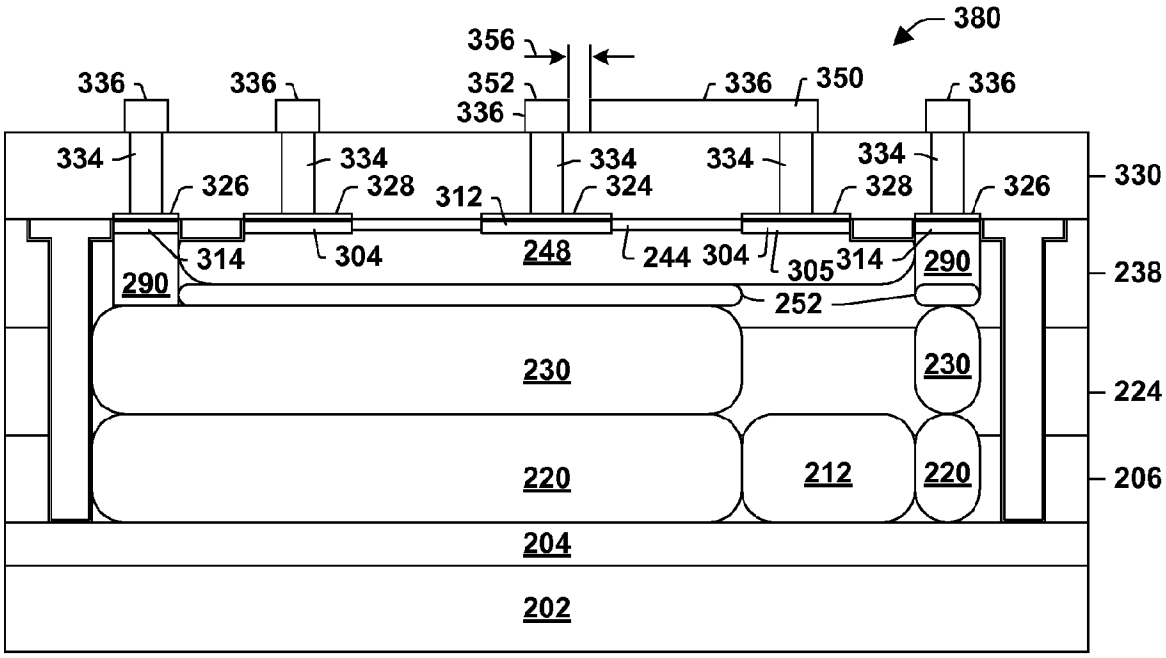
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Fig. 37

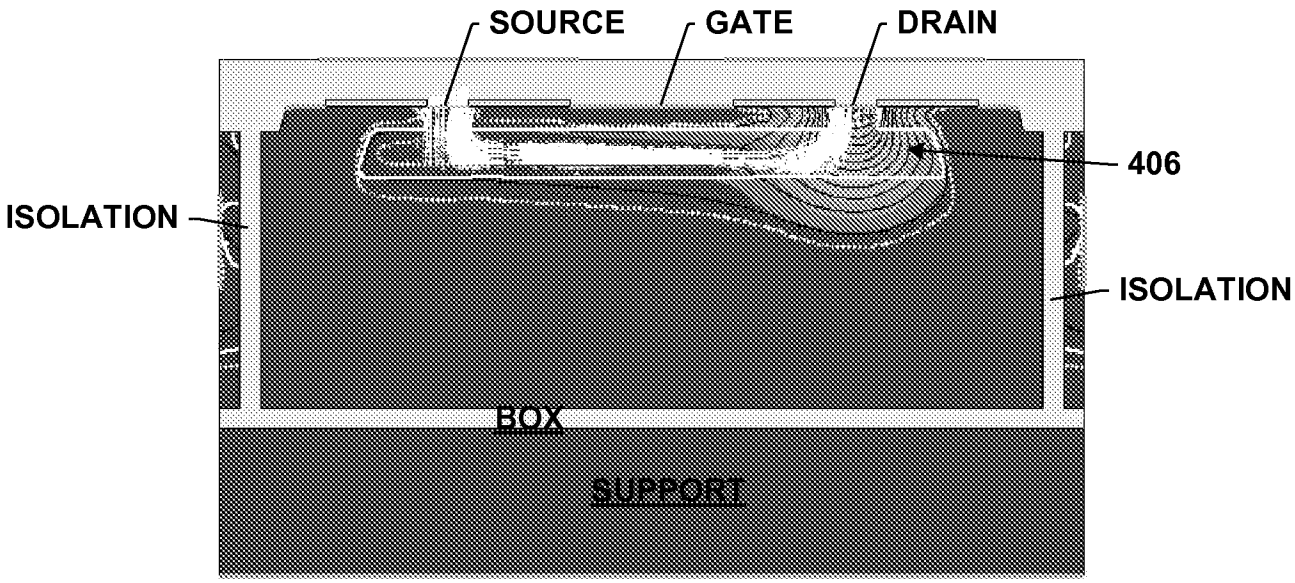
SOURCE
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Fig. 38

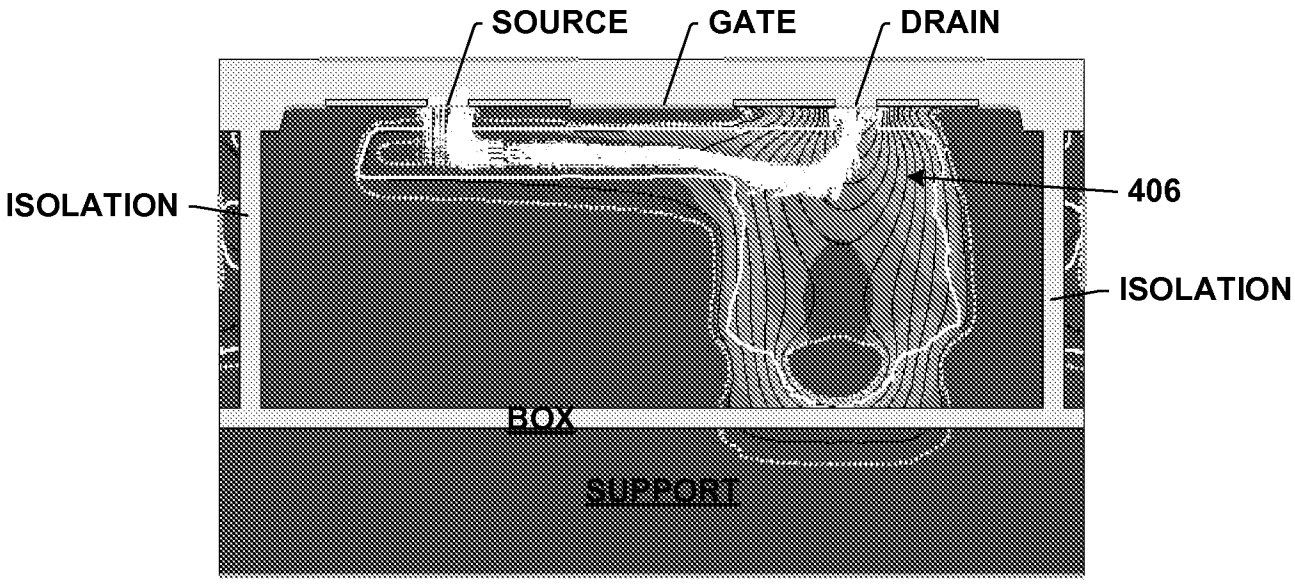
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Fig. 39

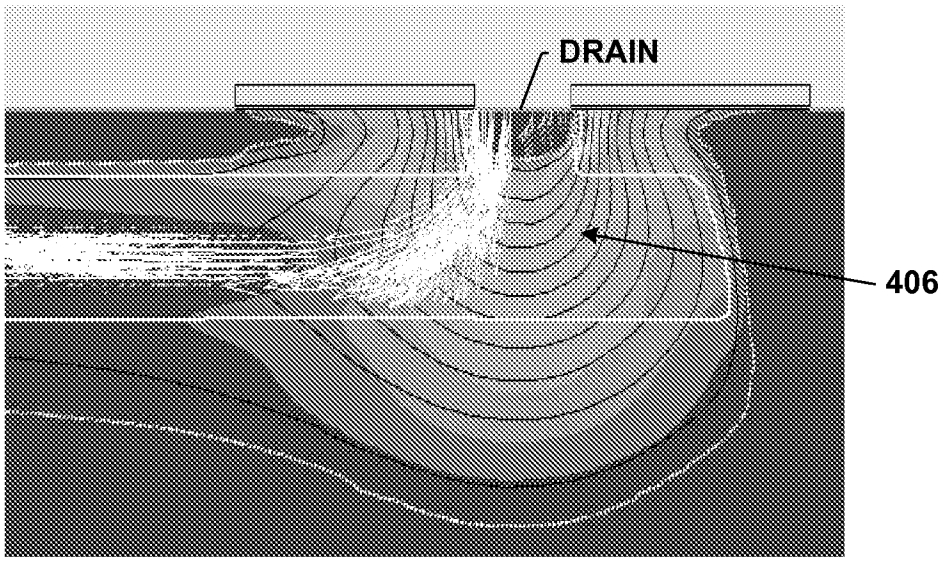


Fig. 40

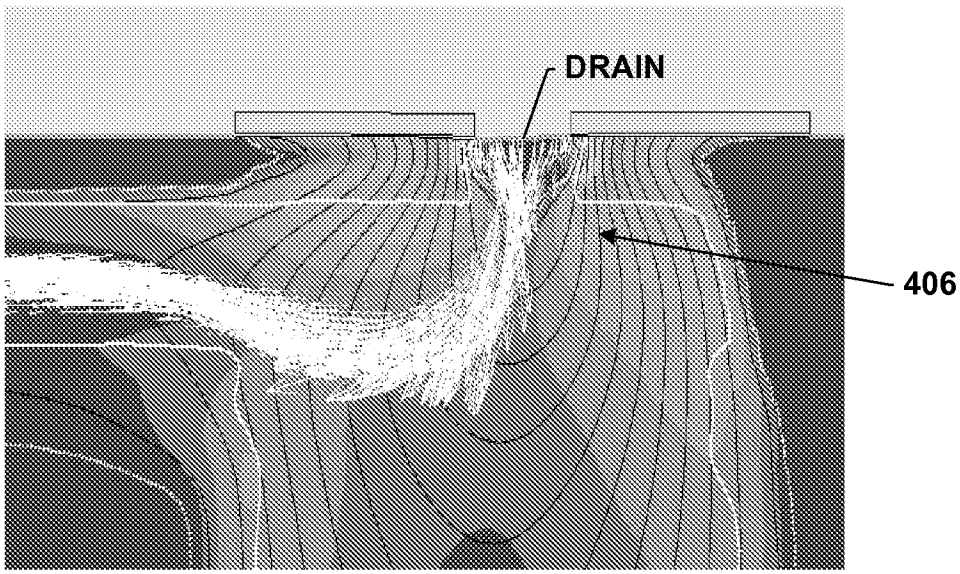
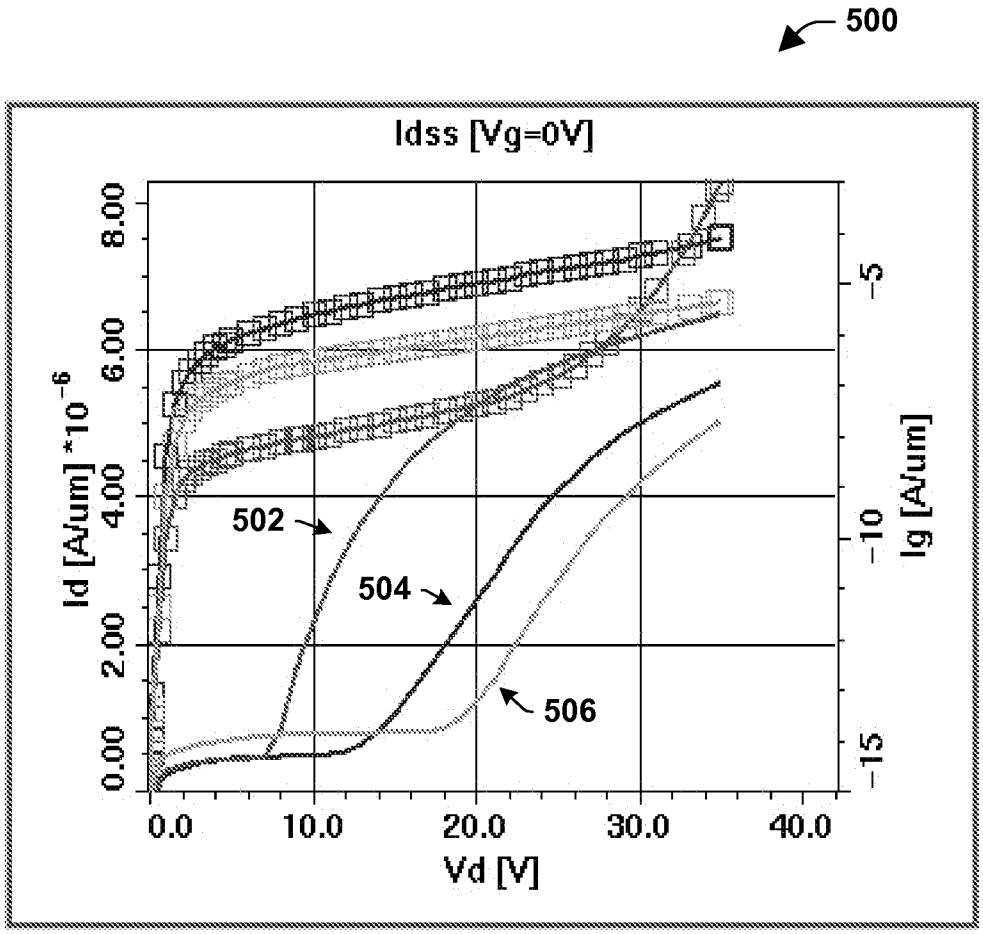


Fig. 41


500
Idss [Vg=0V]
Id [A/um] *10^-6
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6.00
4.00
2.00
0.00
-5
-10
-15
Ig [A/um]
502
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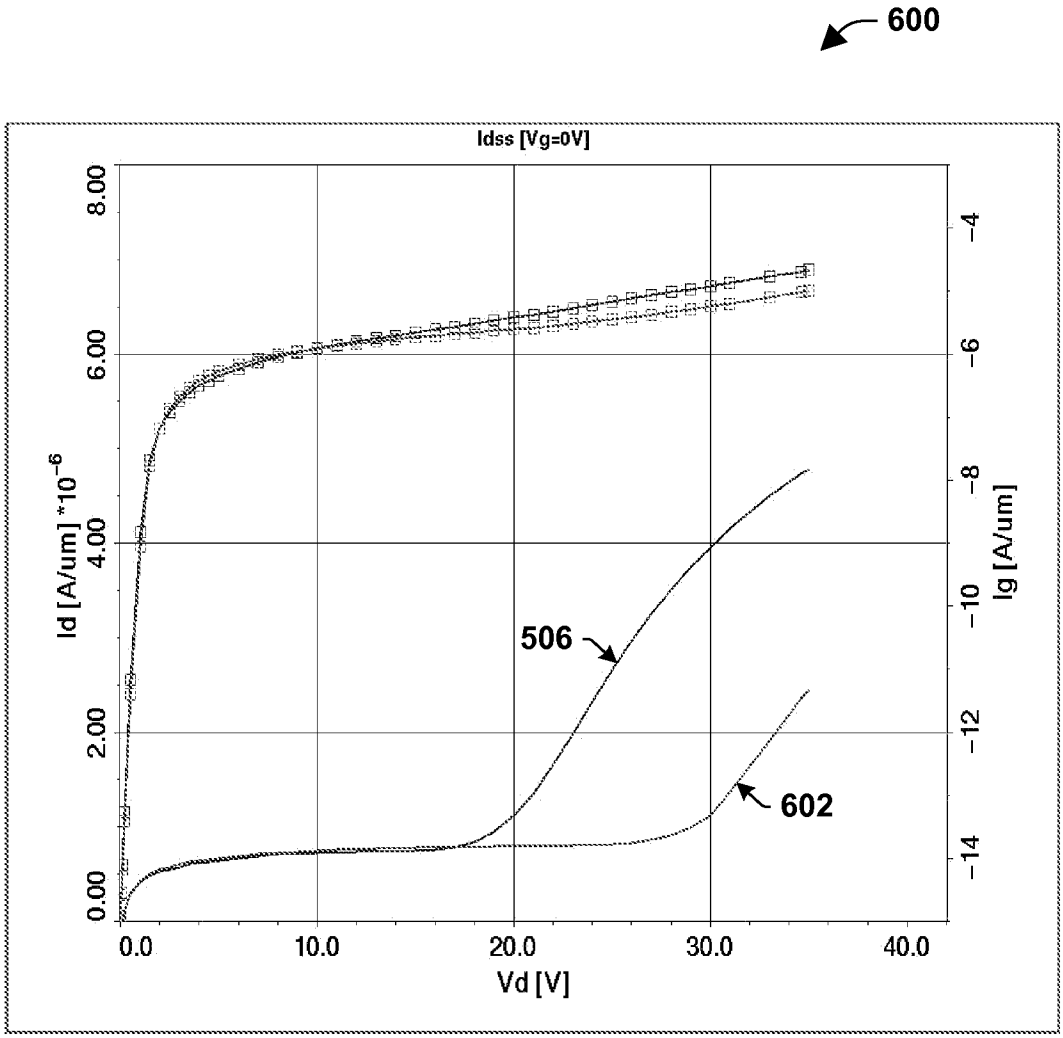
506
0.0
10.0
20.0
30.0
40.0
Vd [V]

Fig. 42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Idss [Vg=0V]
Id [A/um] *10^-6
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10.0
20.0
30.0
40.0
Vd [V]
-4
-6
-8
-10
-12
-14
Ig [A/um]
506
602

Fig. 43

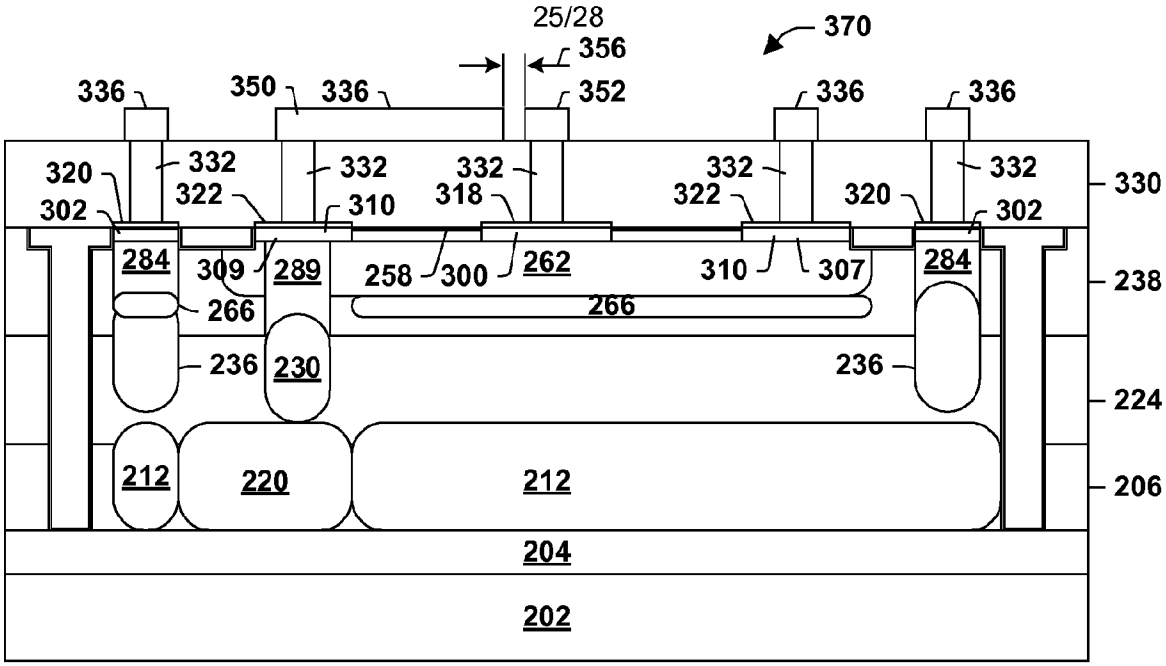
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Fig. 44

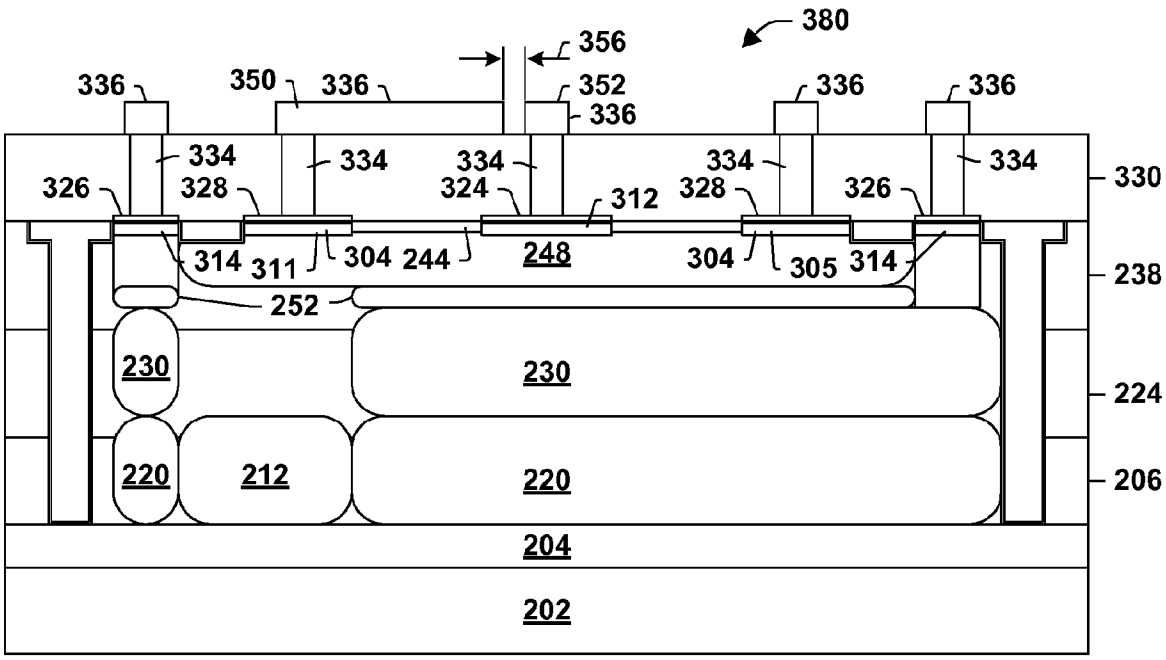
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Fig. 45

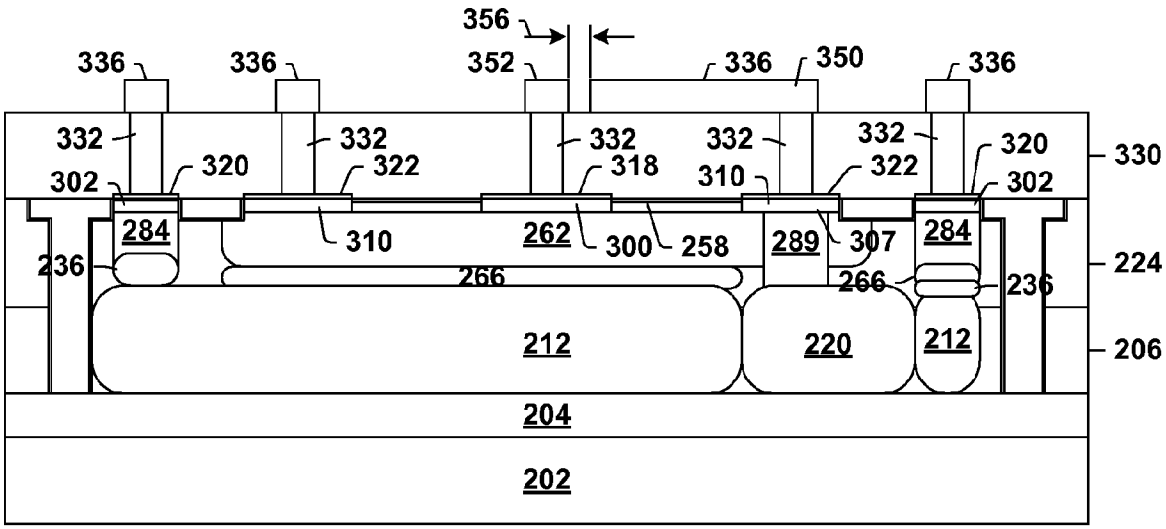
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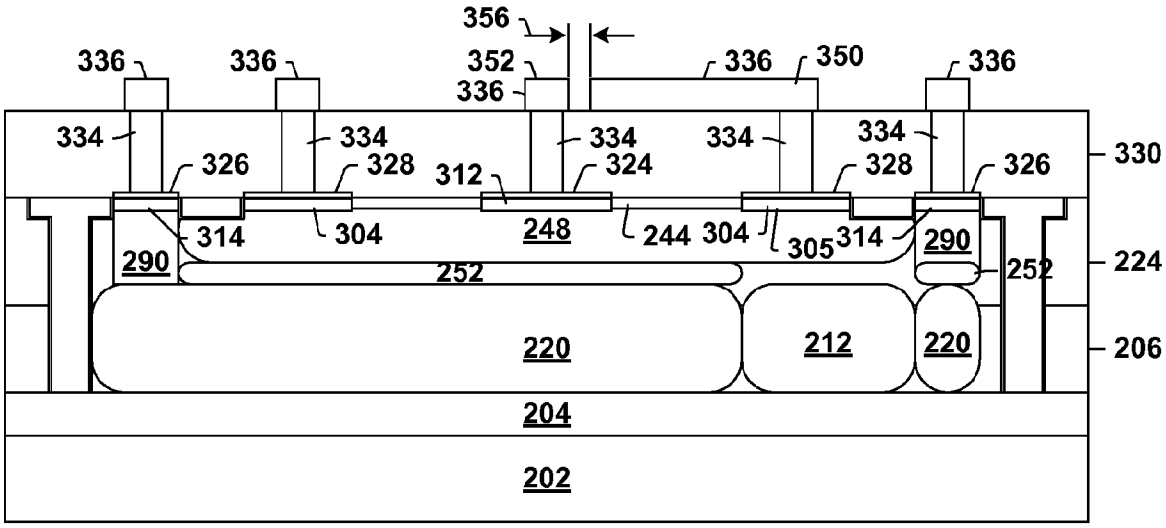
Fig. 46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202

Fig. 47

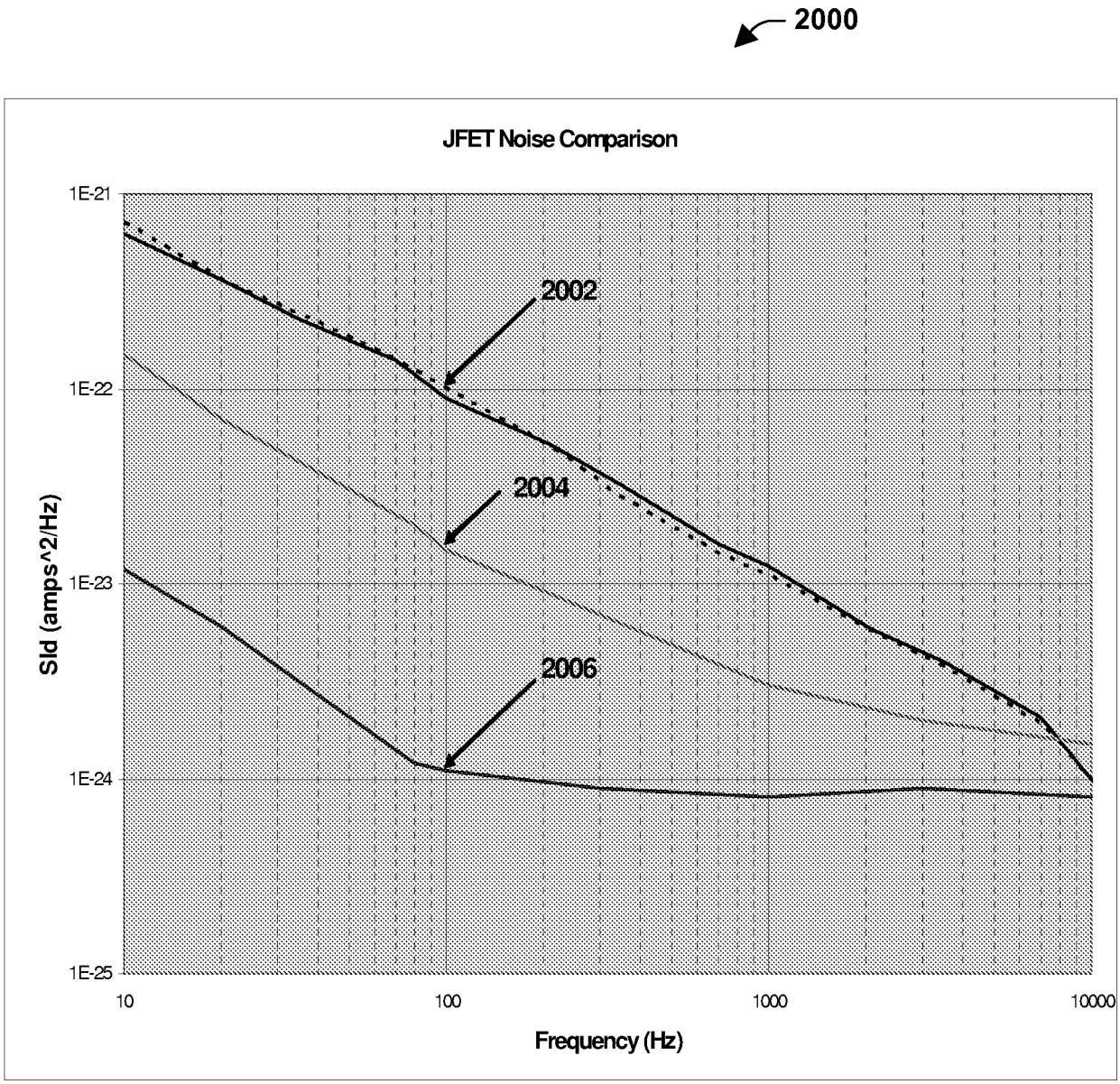
2000
JFET Noise Comparison
1E-21
1E-22
1E-23
1E-24
1E-25
Sld (amps^2/Hz)
2002
2004
2006
10
100
1000
10000
Frequency (Hz)

Fig. 48

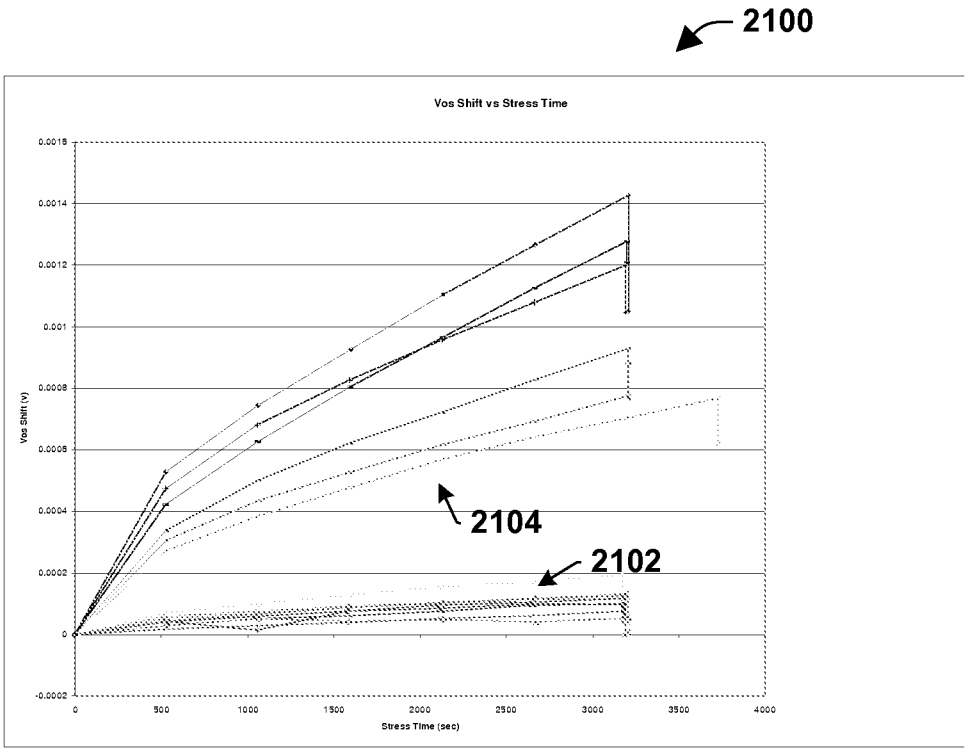
2100
Vos Shift vs Stress Time
Vos Shift (v)
Stress Time (sec)
2104
2102

Fig. 49

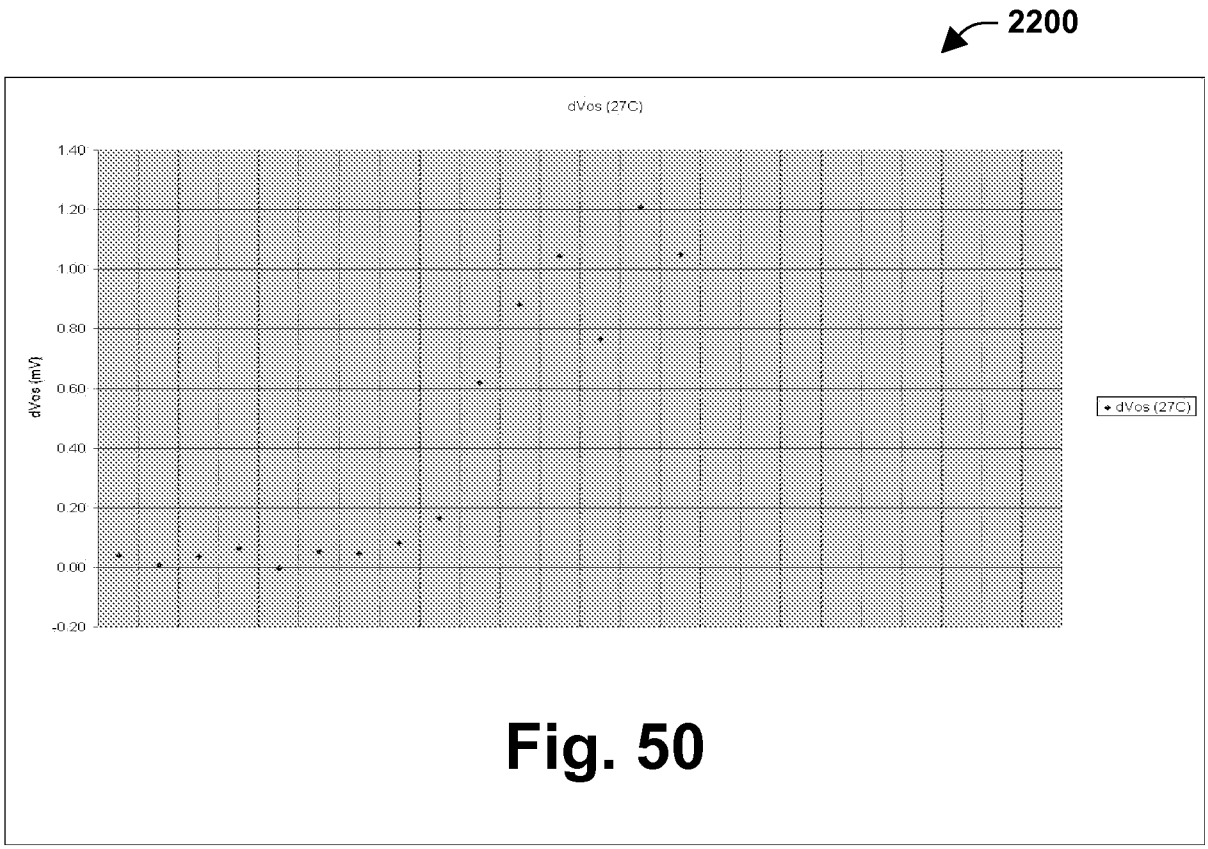
2200
dVos (27C)
dVos (mV)
dVos (27C)

Fig. 50